

SW Test Workshop

Semiconductor Wafer Test Workshop

TECHNICAL TUTORIAL

Get Your Tutor On !

June 3 - 6, 2018

Rancho Bernardo Inn,
San Diego, CA

www.swtest.org

Chairman's Welcome to SW Test 2018

Wafer Test Technology Conference and EXPO

On behalf of the SW Test Executive Team, Program Committee, and Committee Members, it is my great pleasure to welcome you to the 28th Annual SW Test Conference and EXPO.

I would like to thank all our sponsors (9-platinum, 9-gold, and 7-silver), 64 exhibitors, committee members, and the volunteers who help make the SW Test Conference and EXPO such a valuable event for the wafer test industry.

For the SW Test 2018 program, we received many outstanding submissions for podium and poster presentations. Rey Rincon, Technical Program Chair, and the Program Committee implemented a new review process for building the program. All submissions were reviewed by a 9-member Selection Committee, ranked using a criteria algorithm, and then organized into themed technical sessions. Using this new selection process, we have built a technical program with thirty-one podium and nine poster presentations. It was an extremely competitive selection process and the SW Test Team thanks all of the authors and their companies.

Our goal is to provide all attendees with an informative and diverse technical program that addresses real-world challenges faced by test professionals. Leading technologists will discuss device testing challenges under the most demanding electrical, and environmental conditions.

We encourage and support student participation. This year the William R. Mann Travel Grant with awarded to three student attendees (Alex Poles from The University of Nevada, Reno; Gaurav Rajavendra Reddy from The University of Texas at Dallas; and Mehmet Tas from the University of Surrey, UK).

During the SW Test EXPO, top suppliers will have an opportunity to showcase their latest product offerings and technical services. This year, our available exhibit space has increased from 42 booths to 64 booths. Our goal for the EXPO is to provide attendees unprecedented, focused access to key technologies and services, while not competing with the technical program.

Throughout the year, SW Test Executive Team also works on co-marketing activities with various organizations and other conferences that touch thousands of technical professionals. Our co-marketing relationships have been developed with BiTS Workshop, IS-Test Workshop, IEEE Holm Conference, IEEE NATW, SEMI.org, TEST VISION 2020, and VLSI Research.

The SW Test Team is also proud to announce our 1st Annual SW Test Asia conference to be held in Hsinchu, Taiwan, October 18 to 19, 2018, at the Sheraton in Zhubei City. This one and one-half day conference will be organized in the spirit of SW Test San Diego and will consist of a Technical Program, EXPO, and Technology Showcase. The SW Test Asia Technical Chair is Clark Liu and we are happy to announce that Joey Wu (STAr Technology) and Nobuhiro Kawamata (Formfactor K.K.) have joined the Steering Committee for this conference.

Once again, thank you for being a part of the 28th SW Test and I hope you enjoy San Diego!



Jerry Broz, Ph.D.
General Chair
SW Test
SW Test Asia

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PROGRAM SCHEDULE

SW Test 2018 Platinum Sponsors

(alphabetically)

CHPT

FormFactor™

international TEST SOLUTIONS

JEM

MJC®

MPI

TECHNOPROBE
Wafer Probing Technologies

TERADYNE

Xcerra
measured by your success

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PROGRAM SCHEDULE

SW Test 2018 Gold Sponsors

(alphabetically)

Melexis
INSPIRED ENGINEERING

Nidec SV TCL

PacTech
member of nagase group

RUDOLPH TECHNOLOGIES

STAr Technologies

T.I.P.S.
Technical Innovation - Physical Solutions

TEL
TOKYO ELECTRON

TRANSLARITY

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PROGRAM SCHEDULE

SW Test 2018 Silver Sponsors

(alphabetically)

APS

cmrsummit TECHNOLOGIES

ERS

FEINMETALL Contact Technologies

Johnstech

SEMICS

SCS SPECIALTY COATING SYSTEMS™ A KISCO Company

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PROGRAM SCHEDULE

Sunday, June 3

8 a.m. – 12 Noonish	7th Annual SW Test William Mann Golf Tournament
2:00 PM - 4:00 PM	Tutorials – Challenges for Stable Probing (Santiago Ballroom)
4:00 PM - 6:00 PM	REGISTRATION (Aragon South Foyer)
6:00 PM - 7:00 PM	RECEPTION (Aragon Lawn)
7:00 PM - 8:15 PM	Dinner in the Aragon II/III Ballroom
8:15 PM - 8:30 PM	Welcome SW Test 2018
8:30 PM - 9:45 PM	Keynote Presentation by Brett Debenham, Senior Director of Test Probe Central Engineering, Micron Technology, Inc., Boise, ID

Monday, June 4

7:00 AM - 5:00 PM	REGISTRATION / EXHIBITOR CHECK IN (Aragon South Foyer)
7:00 AM - 8:00 AM	CONTINENTAL BREAKFAST (Aragon Lawn)
8:00 AM - 10:00 AM	Wafer Test Trends and Complications (Aragon I/II)
10:00 AM - 10:30 AM	BREAK (Aragon Lawn)
10:30 AM - 12:00 PM	Advanced Probing Processes
12:00 PM - 1:00 PM	LUNCH (Aragon Lawn)
1:00 PM - 3:00 PM	All About The Probe !
2:30 PM - 3:00 PM	BREAK and POSTER SESSION (Aragon Foyer and Lawn)
3:00 PM - 5:00 PM	Dial Up the Frequency
5:00 PM - 8:00 PM	EXHIBITS OPEN w/ Dinner Served at RECEPTION STATIONS

Tuesday, June 5

7:00 AM - 3:00 PM	REGISTRATION (Aragon South Foyer)
7:00 AM - 8:00 AM	CONTINENTAL BREAKFAST (Aragon Lawn)
8:00 AM - 10:00 AM	Extreme Wafer Probing (Aragon I/II)
10:00 AM - 10:30 AM	BREAK and POSTER SESSION (Aragon Foyer and Lawn)
10:30 AM - 12:00 PM	More … Extreme Wafer Probing (Aragon I/II)
12:00 PM - 1:00 PM	LUNCH (Aragon Lawn)
1:30 PM - 3:00 PM	Probe Cleaning and Wafer Inspection
3:00 PM - 5:00 PM	EXHIBITS OPEN (Refreshments will be served)
6:00 PM - 9:00 PM	WORKSHOP SOCIAL – Drinks, Networking, Dinner and Entertainment in the Aragon Ballroom

Wednesday, June 6

7:30 AM - 10:00 AM	REGISTRATION (Aragon South Foyer)
7:00 AM - 8:00 AM	CONTINENTAL BREAKFAST (Aragon Lawn)
8:00 AM - 10:00 AM	Probe Potpourri (Aragon I/II)
10:00 AM - 10:30 AM	BREAK (Aragon Lawn)
10:30 AM - 11:30 PM	High Performance Space Transformers & PCB's (Aragon I/II)
11:30 AM to 12:00 PM	AWARDS (Aragon I/II)
12:00 PM	ADJOURNMENT (Aragon Lawn) … see you 2018 !

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PROGRAM SCHEDULE

Program Overview

The 28th Annual SW Test Workshop will be held at the Rancho Bernardo Inn in San Diego, California, from June 3-6, 2018. The conference will begin on Sunday morning with a golf tournament and Sunday afternoon with a topical tutorial, followed by a welcome reception, dinner, and a Keynote Speaker. The Technical Program will start Monday morning with 30-minute presentations in theme-oriented sessions. SW Test EXPO 2018 will showcase many of the key suppliers to the wafer probe industry and, as always, there will be ample opportunities for networking. This year, we will also feature two poster sessions during which attendees can meet with authors face-to-face. The conference will conclude on Wednesday at Noon after an awards presentation. Conference registration includes all meals, refreshments, social activities, and technical program and exhibit attendance, as well as the eProceedings.

last revised: 5/30/18

June 3, 2018 (Sunday)

7:00 AM - 1:00 PM	**7th Annual SW Test William Mann Golf Tournament**
7:00 - 8:00	Box Breakfast
8:00AM	Tee Off: Scramble, Reverse Shotgun Format

2:00 PM - 4:00 PM	**Tutorials Chair: Clark Liu (PTI – Taiwan)** **Santiago Ballroom**
	Probe Card Stability during High Temperature Testing Yan Chen (Nidec SV TCL – USA) and Trung Ngoc (Nidec SV TCL – Vietnam)
	A Novel Measurement Method for Measuring CCC and MAC At Once Dr. Matthias Schnaithmann, Achim Weiland, and Gunther Boehm (FEINMETALL GmbH – Germany)
	Advances in MEMS Spring Probe Technology for Wafer Test Applications Koji Ogiwara and Norihiro Ohta (Nidec SV TCL – Japan)
	Data Driven Comparison and Qualification of WLCSP Probe Technologies Bert Brost (Xcerra Corporation – USA)

4:00 PM - 6:00 PM	**REGISTRATION OPEN**
6:00 PM - 7:00 PM	**WELCOME RECEPTION (Aragon Lawn)**
7:00 PM - 8:15 PM	**BUFFET DINNER (Aragon Ballroom)**

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PROGRAM SCHEDULE

Keynote Presentation

8:15 PM - 9:45 PM	Evening Session in Aragon Ballroom
8:15 - 8:30	**Opening Remarks for SW Test 2018** Jerry Broz, Ph.D., SW Test General Chair
8:30 - 9:45	**KEYNOTE** **Leveraging Advanced Manufacturing to Address Challenges in the Automotive Memory Market** **Brett Debenham** *Senior Director of Test Probe Central Engineering* Micron Technology, Inc. Boise, ID **Abstract** Advanced manufacturing is enabling Industry 4.0. We will review key concepts and solutions enabled at Micron. This talk will review industry trends in the automotive market and the resulting memory test challenges needed to support these requirements. Additionally, we will touch on how Big Data can help move manufacturing environments toward the goal of zero-defects.



Mr. Brett Debenham is the Senior Director of Test Probe Central Engineering at Micron Technology, Inc., in Boise, Idaho. Since joining Micron in 1992, he has held various key technical and managerial positions for DRAM Probe and Test Engineering. Currently, he is responsible for managing Micron's global engineering for NVM and DRAM Probe, package test, module test, and SSD. Mr. Debenham earned a B.S. degree in Electrical Engineering from the University of Utah and holds multiple US

9:45 PM NETWORKING / HOSPITALITY SUITES

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PROGRAM SCHEDULE

June 4, 2018 (Monday)	
7:00 AM - 8:00 AM CONTINENTAL BREAKFAST **7:00 AM - 5:00 PM REGISTRATION**	
8:00 AM - 8:30 AM	**Welcome in Aragon Ballroom**
8:00 - 8:30	**Welcome to SWTW-2018** Jerry Broz, Ph.D., General Chair
8:30 AM - 10:00 AM	**SESSION 1: Wafer Test Trends and Complications** **Session Chair: Jerry Broz, Ph.D., SW Test General Chair**
8:30 - 9:00	**Probe Card Market Update** Lin Fu (VLSI Research – United Kingdom)
9:00 - 9:30	**Device interface complexity challenges of the next decade** Steve Ledford (Teradyne – USA)
9:30 - 10:00	**5G: The Next Disruptive Technology in Production Test** Daniel Bock, Ph.D., Mike Bishop, and Jeff Damm (FormFactor – Beaverton) Balbir Singh, Bob Murphy, Michael Hemena, and Michael Engelhardt (Intel – Folsom)
10:00 AM - 10:30 AM COFFEE BREAK	
10:30 AM - 12:00	**SESSION 2: Advanced Probing Processes** **Session Chair: Geert Gouwy (Melexis – Belgium)**
10:30 - 11:00	**Effects of Aluminum Pad Stack Thickness On the AOT/POT of a 1-TD Probing Process** Aaron Woodard and Alistair Laing (Micron Technology, USA) Miho Kitayama and Yuma Tanaka (Micronics Japan Corp. – Japan) Dick Duncan (MJC Electronics –USA)
11:00 - 11:30	**Probing solutions and inherent customization to enable advanced copper-based 3D integration schemes** Dong-pill Yang, and Jung-woo Sung (Samsung Electronics Co., Korea) Daniele Acconcia, Dr. Andrea Calaon, and Raffaele Vallauri (Technoprobe Spa – Italy)
11:30 - 12:00	**Leading-Edge Wide-I/O2 Memory Probing Challenges: TPEG™ MEMS Solution** Ferenc Fodor, and Erik Jan Marinissen (IMEC – Belgium) Raffaele Vallauri and Daniele Acconcia (Technoprobe – Italy)
12:00 NOON - 1:00 PM LUNCH ON THE LAWN	

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PROGRAM SCHEDULE

1:00 PM - 3:00 PM	SESSION 3: All About The Probe ! Session Chair: Darren James (Rudolph Technologies – USA)
1:00 - 1:30	**TPEG Mantis: a new solution for multiple advanced applications** Davide Sangiorgio, and Marco Sciurba (STMicroelectronics SPA – Italy) Tommaso Masi, and Riccardo Vettori (Technoprobe SpA – Italy)
1:30 - 2:00	**New probe design and development for high current capacity using bi-furcated structure** Joonyeon Kim (Samsung Electronics – Korea)
2:00 - 2:30	**Advanced cantilever probes showing similar advantages as their vertical opponent** Franz Steger (Texas Instruments Deuschland GmbH – Germany)
2:30 PM - 3:00 PM COFFEE BREAK	

Poster Session 1: 2:30 PM - 3:00 PM

Session Chair: John Caldwell (Micron Technology – Boise, USA)

- **Optimizing Probe Tip Cleaning and Shaping using Advanced Polymers**
  Alex Poles (International Test Solutions – USA)
- **Tri-Temperature Probing: -55C to >125C**
  Chris Buckholtz and Roger Sinsheimer (Teradyne, Inc – USA)
- **A second study on chuck automatic tilting and chuck force sensing for minimizing probe pin damage and optimization of overdrive**
  Byung-Hyun Shin (Semics – Korea)
- **Modern Probe Card Analysis… Addressing Emerging Needs Cost-Effectively**
  Kjell Lundberg, Greg Olmstead, Audria Hurst, and John Strom (Rudolph Technologies – USA)
- **Temperature Test on Wafer Level – History and Outlook in the Days of Advanced Packaging in Semiconductor**
  Harald Ibele (ERS electronic GmbH - Germany)

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PROGRAM SCHEDULE

3:00 PM - 5:00 PM	SESSION 4: Dial Up the Frequency! Session Chair: Joey Wu (STAr Technologies – Hsinchu, Taiwan)
3:00 - 3:30	**PCB Test Solution for 5th Generation Mobile Communications Presenter** Ching Fang Tseng and Norman Hsu (Chunghwa Precision Test Tech. Co. - Taiwan)
3:30 - 4:00	**WLCSP xWave for high frequency wafer probe applications** Jason Mroczkowski (Multitest – USA)
4:00 - 4:30	**TPEG™ MEMS RF+ Technology for Vertical Probe Heads** Tommaso Masi, Alberto Berizzi, Raffaele Vallauri, Andrea Calaon,and Daniele Acconcia (Technoprobe – Italy)
4:30 - 5:00	**Enabling High Parallelism in Production RF Test** Patrick Rhodes (FormFactor – Livermore)
EXHIBITS OPEN	

5:00 PM - 8:00 PM	SESSION 4: Exhibits Open in Expo Tent and Bernardo Expo Hall
5:00	**Expo Scavenger Hunt Begins** – Scan all participating exhibitors' bar codes for a chance to win fabulous prizes!
5:00 - 8:00	**Reception & Carving Station Dinner in Bernardo Hall Expo and Expo Tent**
EXHIBITS OPEN	

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PROGRAM SCHEDULE

SW Test 2018 EXPO

2018 EXHIBITORS

Accretech
Aehr Test Systems
Afore
Celadon Systems
Chunghwa Precision Test Tech.Co.,Ltd.
CMR Summit Technologies
Complete Probe Solutions Inc.
Delta V Instruments, Inc
Deringer-Ney Inc.
ERS electronic GmbH
Feinmetall GmbH
Ferrotec (USA) Corp.
FormFactor, Inc.
Harbor Electronics
Heraeus Deutschland GmbH & Co. KG
Hitachi Chemical Co., Ltd.
INNO Global
Instec, Inc.
Integrated Technology Corporation
Integrated Test Corporation
International Test Solutions
InTEST Corporation
IWIN CO.,Ltd.
JEM America Corp.
Johnstech International
K-Jet Laser Tek Inc.
Kanematsu USA Inc.
Kita USA Inc
Kyocera International, Inc.
LEENO Industrial Inc.
Leica Microsystems, Inc.
LeoLSI Co., Ltd.
MarTek, Inc
Melexis
Microfriend Inc.
Micronics Japan Co., Ltd.
MPI Corporation
Nextwave 360
Nidec SV TCL
NTK Technologies
Optec Laser Systems
OpTek Systems Inc.
Oxford Lasers
PacTech USA Inc.
Plastronics
Posalux SA
Prober.com
R&D Altanova
Reid-Ashman Mfg., Inc.
Rika Denshi America Inc.
Rudolph Technologies
Specialty Coating Systems
STAr Technologies, Inc.
T.I.P.S. Messtechnik Gmbh
Tanaka Precious Metals
Technoprobe America Inc.
Teradyne
Tokyo Electron Limited (TEL)
Translarity
Veco USA
Vermont Microtechnologies
WinWay Technology
Wooam Semitech
Xcerra Corporation

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2018 Exhibitors

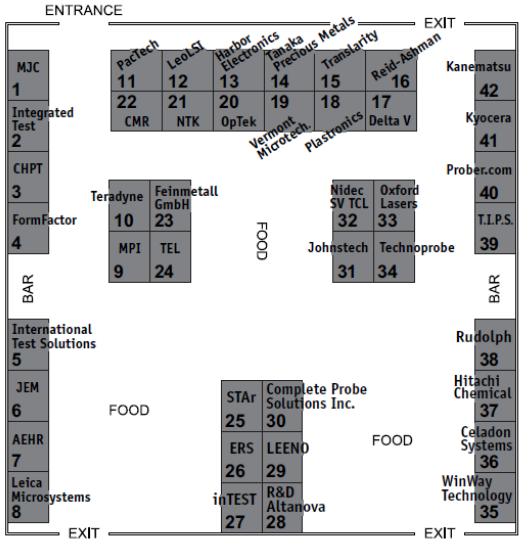
Bernardo Foyer/Ballroom Map



Booth	Company
B1	Heraeus Deutschland GmbH & Co. KG
B2	Nextwave 360
B3	Specialty Coating Systems
B4	INNO Global
101	IWIN Co., Ltd.
102	Posalux SA
103	Microfriend Inc.
104	Instec, Inc.
105	Wooam Semitech
106	Accretech
107	K-Jet Laser Tek Inc.
109	Ferrotec (USA) Corp.
110	Integrated Technology Corporation
200	Melexis
202	Optec Laser Systems
203	Xcerra Corporation
204	Afore
205	Kita USA Inc.
206	Deringer-Ney Inc.
207	MarTek, Inc.
209	Rika Denshi America Inc.
210	Veco USA

2018 Exhibitors

EXPO Tent Map



Booth	Company
1	Micronics Japan Co., Ltd.
2	Integrated Test Corporation
3	Chunghwa Precision Test Tech. Co., Ltd. (CHPT)
4	FormFactor, Inc.
5	International Test Solutions
6	JEM America Corp.
7	Aehr Test Systems
8	Leica Microsystems, Inc.
9	MPI Corporation
10	Teradyne
11	PacTech USA Inc.
12	LeoLSI Co., Ltd.
13	Harbor Electronics
14	Tanaka Precious Metals
15	Translarity
16	Reid-Ashman Mfg., Inc.
17	Delta V Instruments, Inc.
18	Plastronics
19	Vermont Microtechnologies
20	OpTek Systems Inc.
21	NTK Technologies
22	CMR Summit Technologies
23	Feinmetall GmbH
24	Tokyo Electron Limited (TEL)
25	STAr Technologies
26	ERS electronic GmbH
27	inTEST Corporation
28	R&D Altanova
29	LEENO Industrial Inc.
30	Complete Probe Solutions Inc.
31	Johnstech International
32	Nidec SV TCL
33	Oxford Lasers
34	Technoprobe America Inc.
35	WinWay Technology Co., Ltd.
36	Celadon Systems
37	Hitachi Chemical Co., Ltd.
38	Rudolph Technologies
39	T.I.P.S. Messtechnik Gmbh
40	Prober.com
41	Kyocera International Inc.
42	Kanematsu USA Inc.

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PROGRAM SCHEDULE

June 5, 2018 (Tuesday)	
7:00 AM - 8:00 AM CONTINENTAL BREAKFAST	
7:00 AM - 3:00 PM REGISTRATION OPEN	
8:00 AM - 10:00 AM	**SESSION 5: Extreme Wafer Probing (ONE)!** **Session Chair: Karen Armendariz (Celadon Systems – USA)**
8:00 - 8:30	**Break the Myth of Wafer Probing On Cu for Fan-out Wafer Level Packaging (FOWLP)** Amy Leong and Ashish Bhardwaj (FormFactor Inc. – Livermore) Chang-Hoon Hyun (Samsung Electronics/S.LSI Division – Korea) KH Kim (FormFactor Inc – Korea)
8:30 - 9:00	**Micro burn-in techniques at wafer-level test to implement cost effective solutions** Geert Gouwy and Arnaud Devos (Melexis – Ieper, Belgium) Dr. Alessandro Antonioli and Raffaele Vallauri (Technoprobe Spa – Italy)
9:00 - 9:30	**Carbon Nanotube Based Microprobe Design for Electromechanical Probing Applications at Wafer Level Chip Scale and Wafer Level Packaging** Mehmet Tas, Dr. Vlad Stolojan,and Mark Baker (University of Surrey –UK) Jedidiah Bentz (Smiths Interconnect – USA) Dr. Keir Boxshall (Smiths Group – UK)
9:30 - 10:00	**Test Cell Co-Planarity Optimization** Troy Harnisch (Teradyne, Inc. – USA)
10:00 AM - 10:30 AM COFFEE BREAK	

Poster Session 2: 10:00 AM - 10:30 AM

Session Chair: Mark Ojeda (Cypress Semiconductor – San Jose, USA)

- **Improvements in Laser Drilled Hole Geometries for Probe Card Applications**
  Andrew Webb (OpTek Systems Inc. – Greenville, USA)
  Dr. Mike Osborne (OpTek Systems Ltd. – UK)

- **Improvements in small pitch capability**
  Dr. Alan Ferguson (Oxford Lasers – UK)

- **Effect of Ceramic on Laser**
  Man-Seob Lee (Dawon Nexview – South Korea)

- **Innovative Laser Micro-Machining Improves Probe Card Fabrication in Many Ways**
  Hung-Lung Chen (KJet Laser Tek Inc. – HsinChu City, Taiwan)

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PROGRAM SCHEDULE

10:30 AM - 12:00	**SESSION 6: Extreme Wafer Probing (TWO)!** **Session Chair: Patrick Mui (JEM America – USA)**
10:30 - 11:00	**Known Good "Power" Die: Diced Wafer Test at 7 kV and 1000 A** Dr. Rainer Gaggl (T.I.P.S. Messtechnik GmbH – Austria), Mauro Serra (CREA s.r.l. – Italy) Ernest Fischer (INFOTECH AG – Switzerland)
11:00 - 11:30	**Vertical MEMS Probe Card Applied to High Speed Loopback Test of Network Communication IC** Haiyong Song, and Zheng Li (Hisilicon Technologies Co., A Huawei Company – China) Adolph Cheng, Fred Chou, Alex Wei, Jessie Deng, Zach Hsieh, and Bobby Chen (MPI Corporation – Chu-Pei, Taiwan)
11:30 - 12:00	**A Real-Life Pad Crack Study** Gunther Boehm (FEINMETALL GmbH – Germany) Jory Twitchell (NXP Semiconductor, USA)
12:00 NOON - 1:00 PM	**LUNCH ON THE LAWN**
1:00 PM - 3:00 PM	**SESSION 7: Probe Cleaning and Wafer Inspection** **Session Chair: Suz Ramsbottom (Texas Instruments – Dallas)**
1:00 - 1:30	**Fast Probe Mark Inspection (PMI)** Imran Ahmed (Texas Instruments Inc – Dallas)
1:30 - 2:00	**Cleaning Material Evaluations on Advanced MEMS and Vertical Technologies** Vincent Ellis (Texas Instruments, Inc. – Dallas)
2:00 - 2:30	**OCR Automation** Hector Moreno (Texas Instruments Inc. – Dallas)
2:30 - 3:00	**New Approach in Pogo Pin Socket Design to Improve Total Cost of Ownership** Richard Incognito (Texas Instruments – Philippines)
3:00 PM - 5:00 PM	**EXHIBITS OPEN**
3:00 - 5:00	**PM Break – Refreshments Served in both Expo Tent and Bernardo Expo Hall** **Expo Scavenger Hunt Continues** – Scan all participating exhibitors' bar codes for a chance to win fabulous prizes!

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PROGRAM SCHEDULE

Tuesday Evening Social Event	
6:00 PM - 7:00 PM	**Cocktails and Networking on the Patio and Lawn**
7:00 PM - 9:00 PM	**Dinner and Entertainment in the Aragon Ballroom with Kim Michael Polote, the "Southern Songstress" and Tony Guerrero, an award winning West Coast jazz entertainer.**



Traveling and hailing from the East Coast, Kim is a world renowned, vocal powerhouse who has performed all over the world. Sharing the stage with several greats including Al Green, Harry Connick Jr, and Charlie Daniels, this award-winning songbird will join forces with the West Coast critically acclaimed entertainer Mr. Tony Guerrero, for a one-night only, first-time appearance together.



Tony is a songwriter, producer and an incredible jazz trumpeter with a career spanning nearly 30 years. He's played on over 200 albums by other artists as diverse as Paul McCartney, Nancy Wilson, Joe Sample and recently Dick Van Dyke and Jane Lynch of the TV series Glee to name a few.

Accompanied by an amazing quartet of stellar musicians, this dynamic duo will take you on an exciting, fun journey celebrating an array of musical selections and genres. The dazzling collaboration of these East/West coast fireball performers is sure to spark an evening of unforgettable musical fireworks!

Join us for an evening of great food and fabulous music and entertainment, as well as the announcement of all the winners of our 1st annual Expo Scavenger Hunt.

9:00 PM	**NETWORKING / HOSPITALITY SUITES**

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June 6, 2018 (Wednesday)

7:00 AM - 8:00 AM CONTINENTAL BREAKFAST	
7:30 AM - 10:00 AM REGISTRATION OPEN	
8:00 AM - 10:00 AM	**SESSION 8: Probe Potpourri!** **Session Chair: Dr. Michael Huebner (FormFactor – Livermore)**
8:00 - 8:30	**Design and Analysis of Space Transformer with Hybrid Circuit Design on Probe Card** Tae Kyun Kim, and Yong Ho Cho (Microfriend Inc. – Korea) SangKyu Yoo (Samsung Electronics – Korea) Jong Gwan Yook (Yonsei Univ. – Korea)
8:30 - 9:00	**Automated Probe-Mark Analysis** Yu-Rong Jian and Prof. Cheng-Wen Wu (National Tsing Hua University – Taiwan) Ferenc Fodor and Erik Jan Marinissen (IMEC – Belgium), Prof. Cheng-Wen Wu (National Tsing Hua University – Taiwan)
9:00 - 9:30	**New Probe Testing Methodology-Over Current Analysis of Probe** Ching Fang Tseng and Norma Hsu (Chunghwa Precision Test Tech. Co.,Ltd. – Taiwan)
9:30 - 10:00	**Advances in metrology for guide plate analysis** Dr. Alan Ferguson (Oxford Lasers – UK)
10:00 AM - 10:30 AM COFFEE BREAK	
10:30 AM - 12:00	**SESSION 9: High Performance Space Transformers & PCB's** **Session Chair: Rey Rincon (SWTest – Austin, USA)**
10:30 - 11:00	**Sub-milliOhm impedances on a thick probe card? No problem!** Sandeep Sankararaman (R&D Altanova – USA)
11:00 - 11:30	**An introduction for novel multi-layer thin film substrates applied in space transformers** Dr. Chih-Kuang Yang (Princotest Co. Ltd. – Taiwan)
11:30 - 12:00	***Awards Presentations*** Jerry Broz and Rey Rincon (SW Test General Chair and Program Chair) Presenter: Jerry Broz (SW Test General Chair)
12:00 NOON – ADJOURNMENT … See you next year in San Diego or at SW Test Asia in Taiwan.	

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PROGRAM SCHEDULE

SWTEST ASIA 2018

Join us for the world premiere of the 1st annual SW Test Asia

October 18-19, 2018
Sheraton Hsinchu Hotel, Zhubei City, Taiwan (R.O.C.)

SW Test Asia is a one and a half day conference located at the beautiful Sheraton Hsinchu Hotel in Hsinchu, Taiwan featuring a perfect mixture of manufacturer and vendor technical presentations highlighting the "Best of SW Test 2018" in San Diego, as well as new regional presentations. SW Test Asia is a probe technology forum where attendees come to learn about recent developments in the industry and exchange ideas and solutions in a relaxed atmosphere.

The conference will also feature an Expo with over 30 exhibiting companies. The Expo will be enhanced with tea breaks, lunch buffets and cocktail receptions in the Expo Hall, providing excellent opportunities to visit with exhibitors and network with friends and colleagues. Also featured will be a Tech Showcase in the Expo Hall with 15-minute presentations from our Platinum Corporate Sponsors.

Join us at SW Test Asia in Hsinchu, Taiwan, October 18-19, 2018 for the semiconductor industry's premiere event!





Check out the SW Test Asia website for more information, to register and to add your name to the mailing list.
www.swtestasia.org

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PROGRAM SCHEDULE



Save The Dates

SW Test Workshop 2019

Rancho Bernardo Inn,
San Diego, CA

June 2 - 5, 2019

Abstract Submission Date
March 5, 2019

Golf Tournament
June 2, 2019

See You Next Year!

TERMS of SERVICE

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SW Test Workshop

Semiconductor Wafer Test Workshop

Sunday Afternoon Technical Tutorials

Welcome to the 28th Annual SW Test Workshop

June 3-6, 2018

SW Test 2018 eProceedings ?



Password for Sunday = mockingbird

- SW Test has a green initiative for reduced printing.
- Each day of the conference will be available in an e-Version for download in a password protected file.
  - Go to … http://www.swtest.org
  - Ballroom WiFi Password = santiago2018
- Free WiFi access will be available during the entire conference to allow attendee access to the downloads.
- Daily passwords to the download files will be announced through each day, respectively.
- The non-password locked files will be made available in the SW Test Archives after the conference adjourns.

Sunday, June 3, 2018

2:00 to 3:00 PM – Get Your Tutor On !

Probe Card Stability during High Temperature Testing

Yan Chen (Nidec SV TCL – USA) and Trung Ngoc (Nidec SV TCL – Vietnam)

A Novel Measurement Method for Measuring CCC and MAC At Once

Dr. Matthias Schnaithmann, Achim Weiland,
and Gunther Boehm (FEINMETALL GmbH – Germany)

Sunday, June 3, 2018

3:00 to 4:00 PM – Get Your Tutor On !

Advances in MEMS Spring Probe Technology for Wafer Test Applications

Koji Ogiwara and Norihiro Ohta (Nidec SV TCL – Japan)

Data Driven Comparison and Qualification of WLCSP Probe Technologies

Bert Brost (Xcerra Corporation – USA)

The Rest of Sunday …

- **4:00 to 6:00 PM – REGISTRATION**
  - Aragon South Foyer
- **6:00 to 7:00 PM – RECEPTION**
  - Aragon Lawn
- **7:00 to 8:15 PM – DINNER**
  - Aragon Ballroom
- **8:15 to 8:30 PM – Welcome to SW Test 2017**
- **8:30 to 9:45 PM – Keynote Presentation**

Come visit SW Test Asia …



See you Next Year in San Diego …



Thanks for your Support !

- **Contact the SW Test Team with any questions …**

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Tutorial Program
SW Test 2018

Sunday, June 3, 2018

SW Test Workshop

Semiconductor Wafer Test Workshop

2-0-1-8

Probe Card Stability during High Temperature Testing

Yan Chen, Nidec SV TCL (US)

Trung Hong Ngoc, Nidec SV TCL (Vietnam)

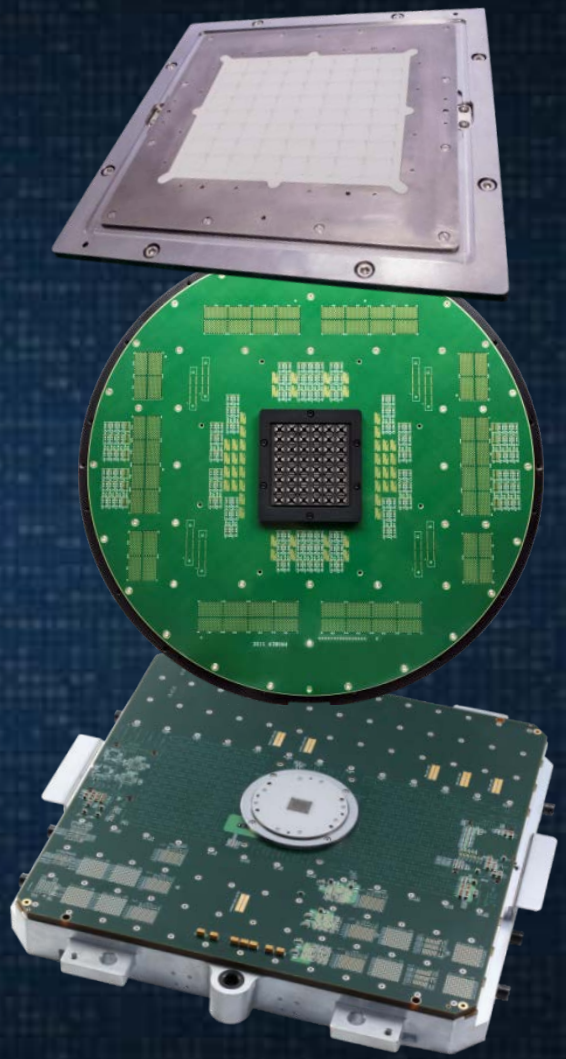
June 3-6, 2018

Overview

- Overview of Nidec SV TCL
- Introduction on High Temp Probing Challenges
- Motivation
- Approaches for Experiment & Simulation
- Experimental & Simulation Results
- Conclusions
- Future Work

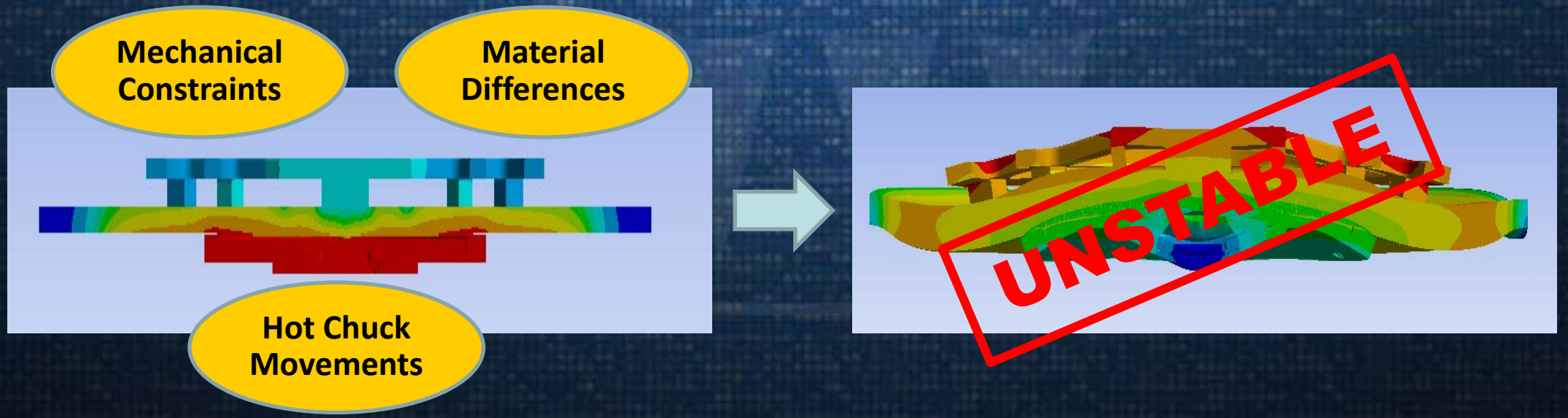
Overview of Nidec SV TCL

- Established in 1994 as a US-based probe card supplier offering cantilever product.
- Acquired by Nidec-Read Corp. October 31, 2017
- Products to enable technology roadmaps in the high growth Mobile, Networking/Data, Automotive & Internet of Things “IoT” markets
- Strength through diverse product portfolio, turnkey solutions, global presence with manufacturing, sales & service centers worldwide



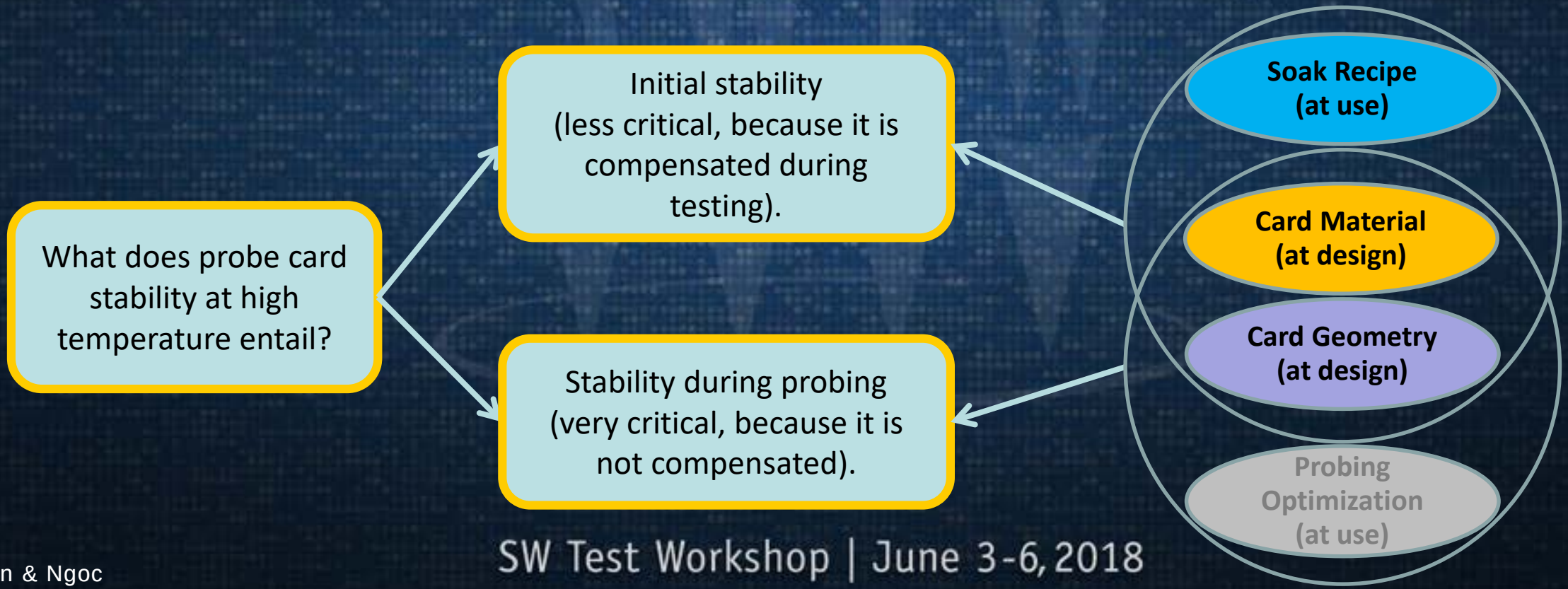
Introduction

- High temperature probing introduces extra failure modes that are not present at room temperature.
- Probe card stability at high temperature is a major issue & causes various failures.



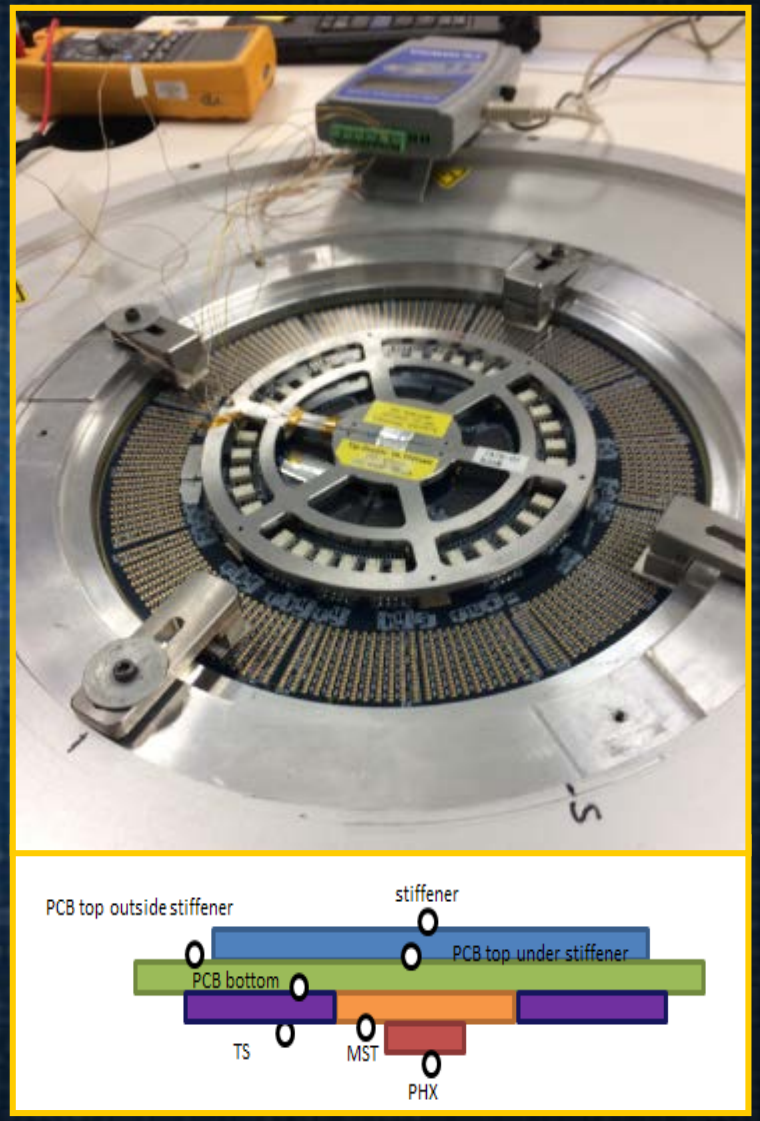
Motivation

- **Establish high temperature stability evaluation method.**
- **Develop FEA models to capture high temperature behavior.**
- **Counter measures to minimize stability issues.**



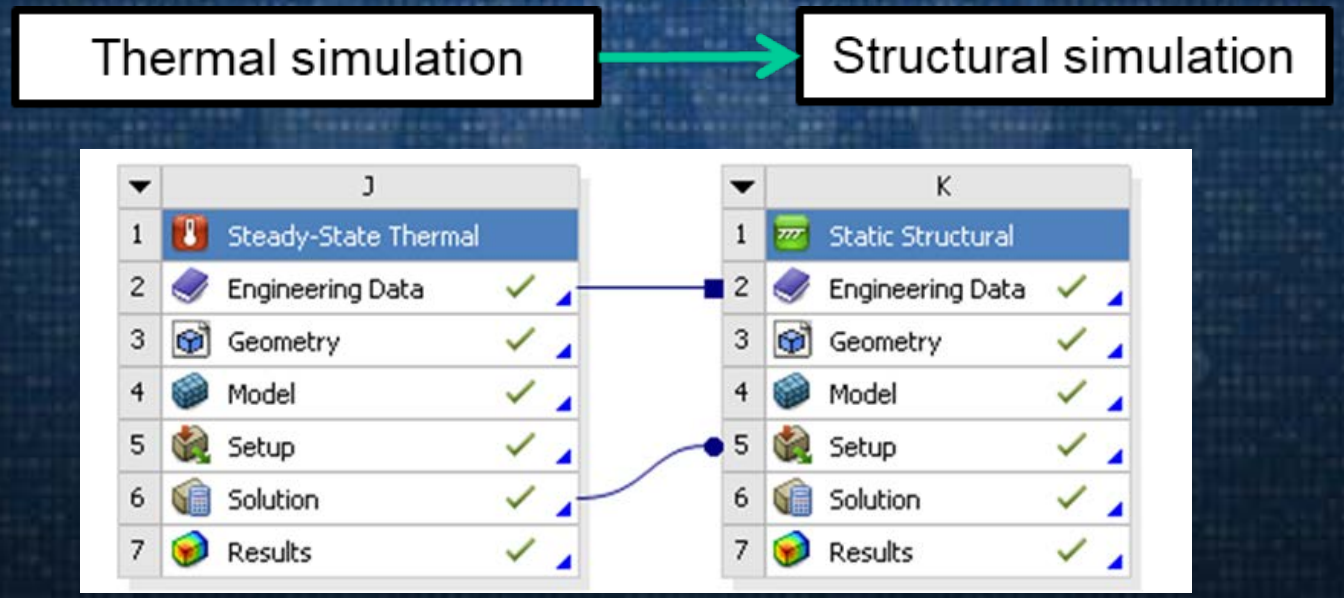
Approaches – Experiment

- **Setup**
  - J750 Platform Sample Card
  - Test Floor Operations
  - Simultaneous Deflection Measurement & Temperature Mapping
- **Experiments**
  - Soak Study
  - Component Level Study
  - Improvement Concept Study

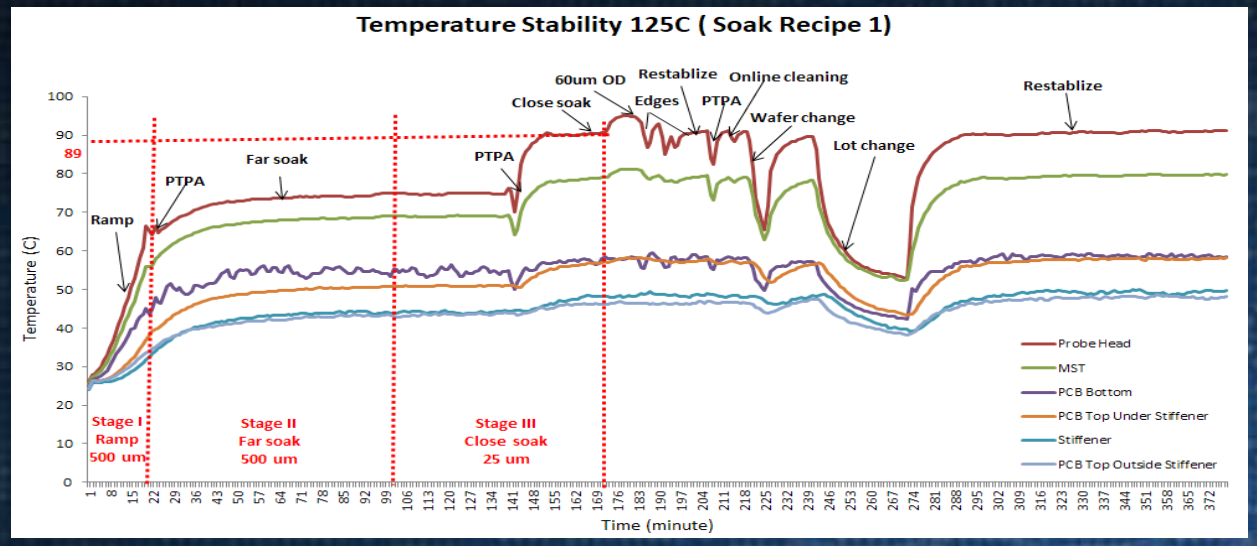


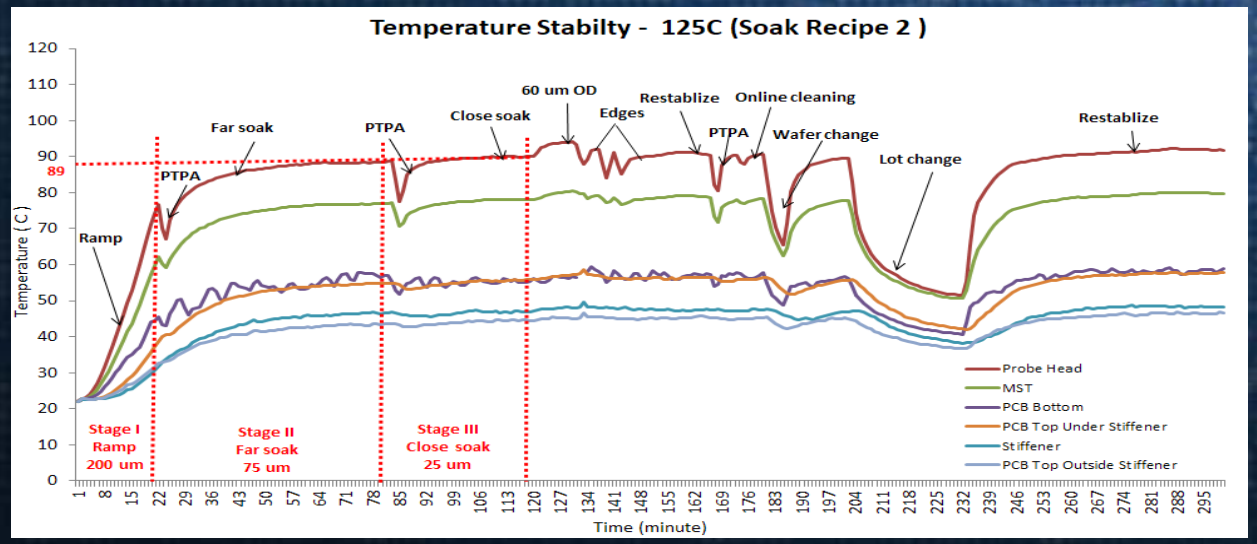
Approaches – Simulation

- **Setup**
  - Thermal Simulation Module
  - Input Thermal Results to Structural Module
  - Predict Deflection from Structural Module

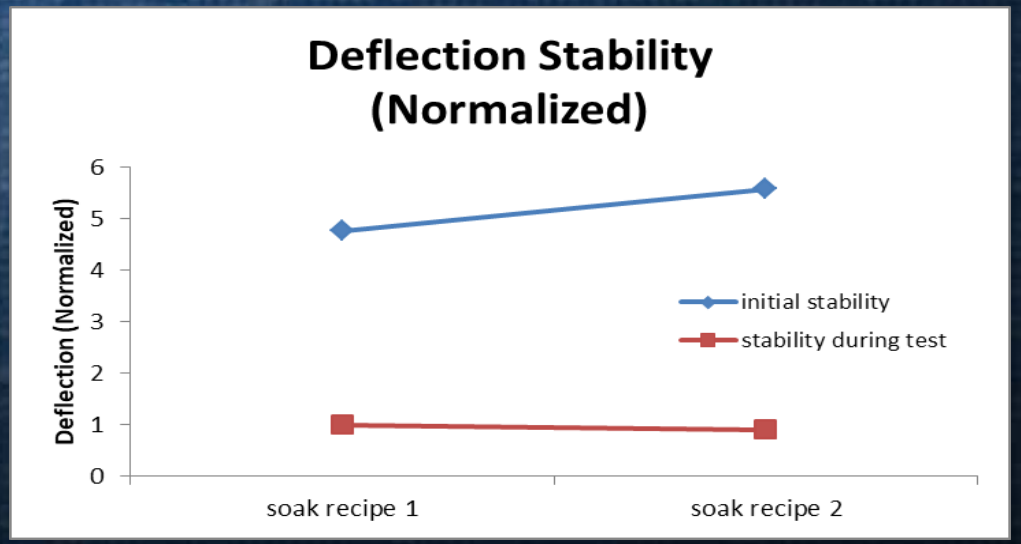


Results – Soak Study



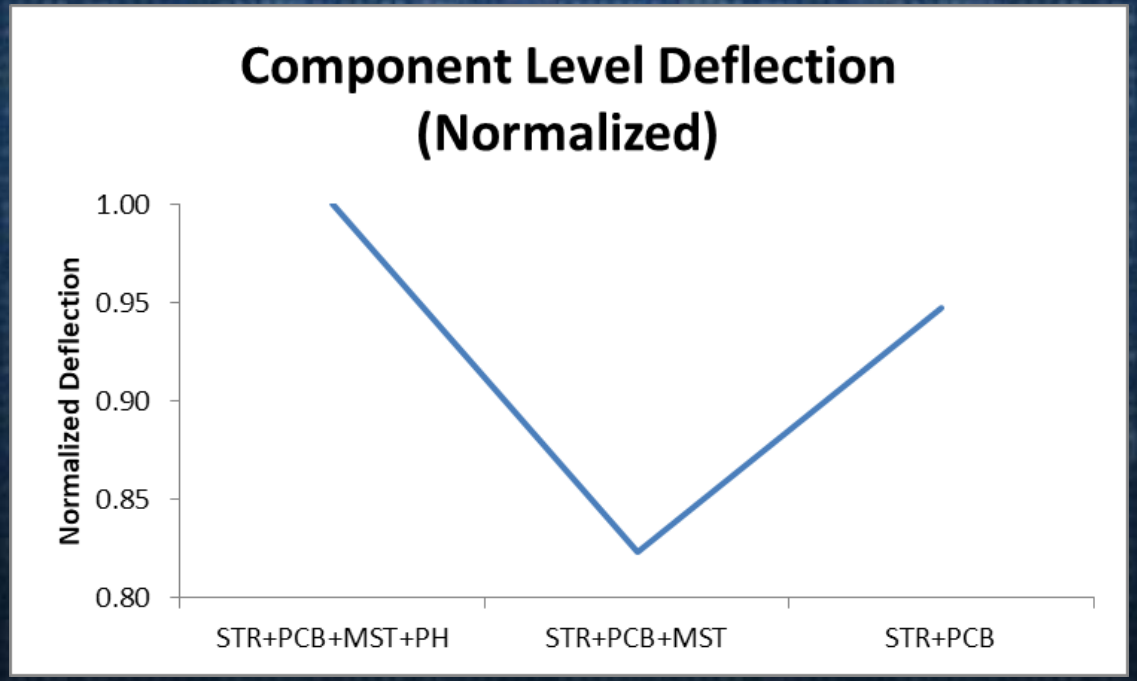


- Every probe card has one unique stability state.
- There are different paths to reach the stability state & some take less time.



Results – Component Level Study

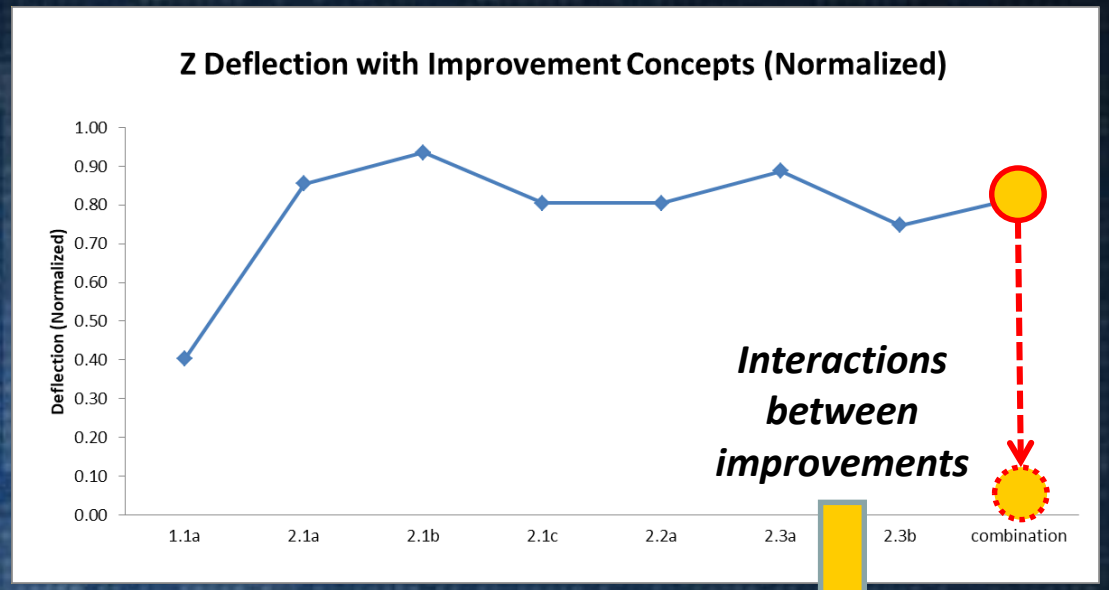
- PCB is the most unstable component in the probe card assembly, making up for 80% to 90% of total deflection.
- Improvement concepts should focus on isolating PCB from the assembly.



Results – Improvement Concept Study

- **Material Change**
- **Design Change to Isolate PCB**
- Soak Recipe Optimization

#	Category	Concept
1	1.1a	Change component material
2	2.1a	Add thermal control component design 1
3	2.1b	Add thermal control component design 2
4	2.1c	Add thermal control component design 3
5	2.2a	Isolate PCB from system design 1
6	2.2b	Isolate PCB from system design 2
7	2.3a	Modify stiffener design 1
8	2.3b	Change mounting mechanism within components



Interaction Map				
	1.1a	2.1c	2.2b	2.3b
1.1a				
2.1c				
2.2b				
2.3b				

Interaction Count			
	No Interaction	Weak Interaction	Strong Interaction
1.1a	1	1	1
2.1c	0	0	3
2.2b	2	1	0
2.3b	1	0	2

Results – Improvements Combination

Improvement Concept Combination DOE								
					Initial stability	Stability during probing		Overall stability
Run#	2.3b	1.1a	2.1c	2.2b	Normalized Z due to ramp	Normalized Z due to soak	Normalized Z due to close soak	Normalized total Z
1	+	+	+	+	0.80	0.78	0.98	0.82
2	+	+	+	-	0.80	0.36	0.67	0.72
3	+	+	-	+	0.64	0.16	0.31	0.53
4	+	+	-	-	0.70	0.02	0.40	0.58
5	+	-	+	+	1.07	1.00	1.14	1.07
6	+	-	+	-	1.08	0.78	0.95	1.03
7	+	-	-	+	0.80	0.07	0.31	0.64
8	+	-	-	-	0.86	0.40	0.45	0.75
9	-	+	+	+	1.01	0.84	0.76	0.96
10	-	+	+	-	1.02	0.60	0.98	0.96
11	-	+	-	+	0.55	0.07	0.26	0.45
12	-	+	-	-	0.58	0.27	0.05	0.40
13	-	-	+	+	1.04	1.22	1.12	1.10
14	-	-	+	-	0.80	0.71	0.93	0.80
15	-	-	-	+	0.79	0.76	0.93	0.80
default	-	-	-	-	1.00	1.00	1.00	1.00

High Pin & High Temperature Solution

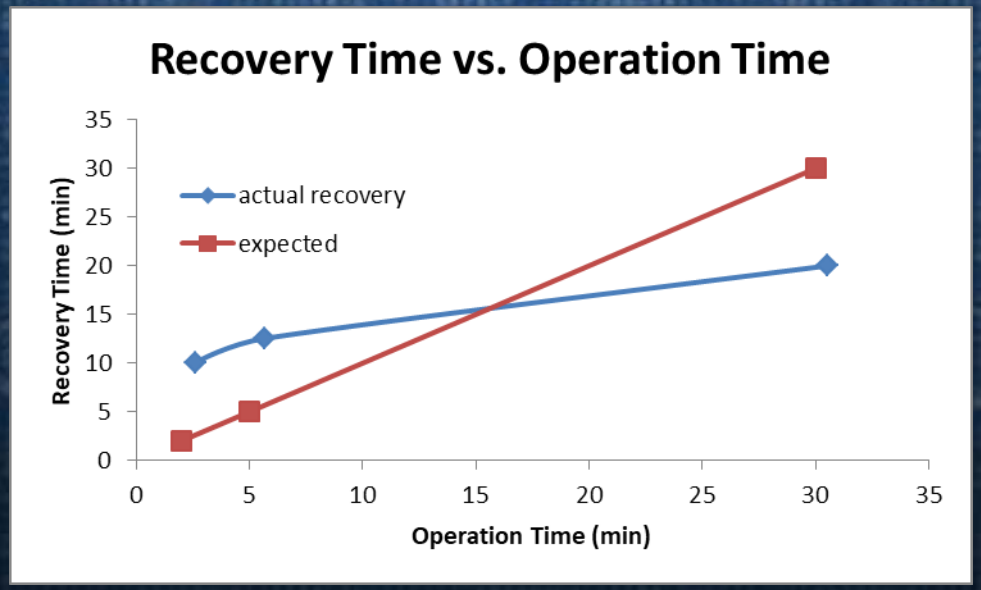
- 20% initial stability improvement.
- 81% stability during probing improvement.
- Stable within Stage I soak, approximately 30 minutes.

Low Pin & High Temperature Solution

- 42% initial stability improvement.
- 84% stability during probing improvement.
- Stable within Stage I soak, approximately 30 minutes.

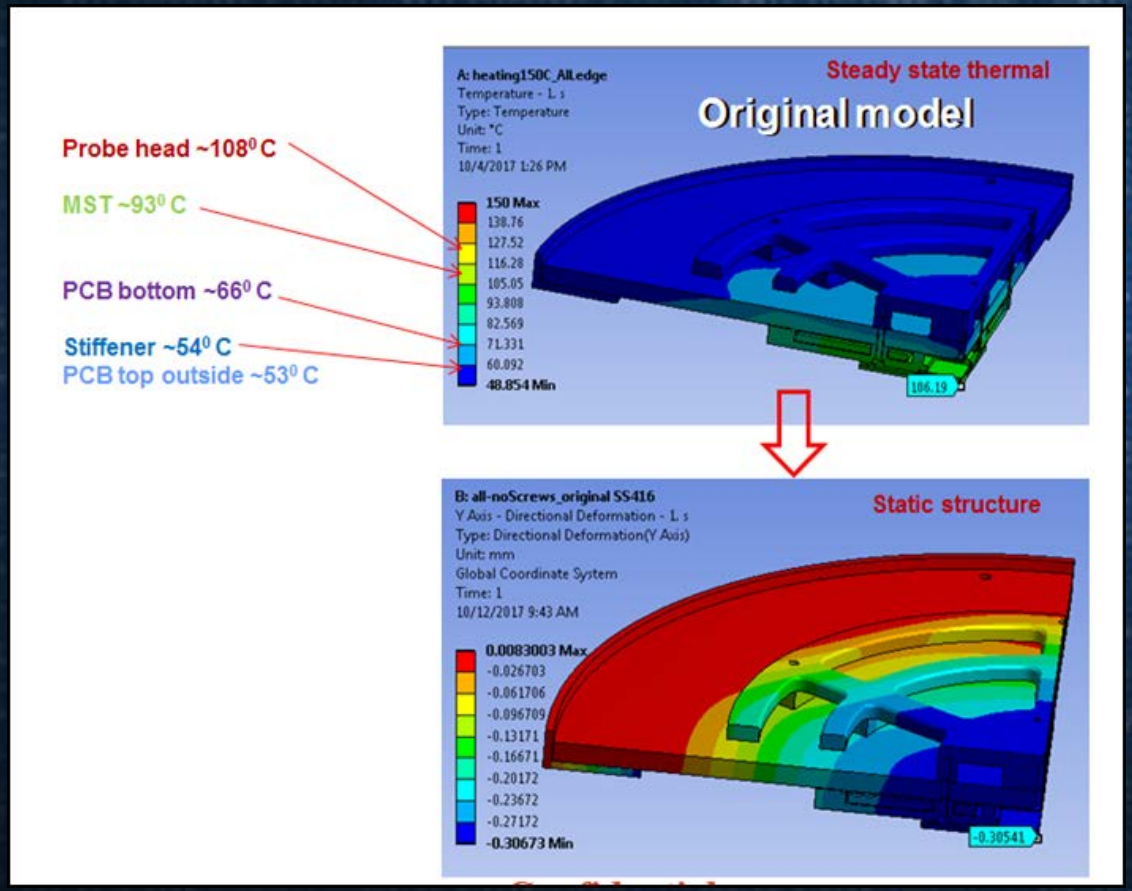
Results – the Unexpected

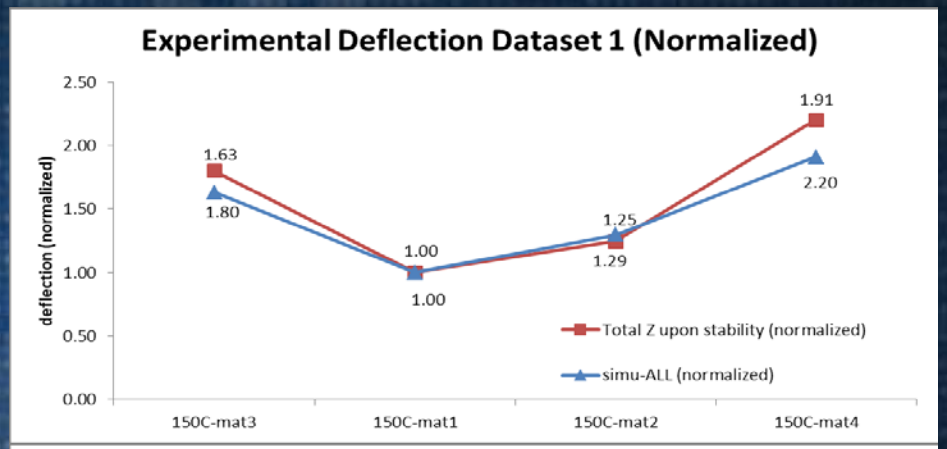
1. Typical soak recipes assume equal operation time & recovery time, but on the sample card, it is found that short operations take a long time to recover.
2. Recovery vs. operation time is very likely platform dependent.

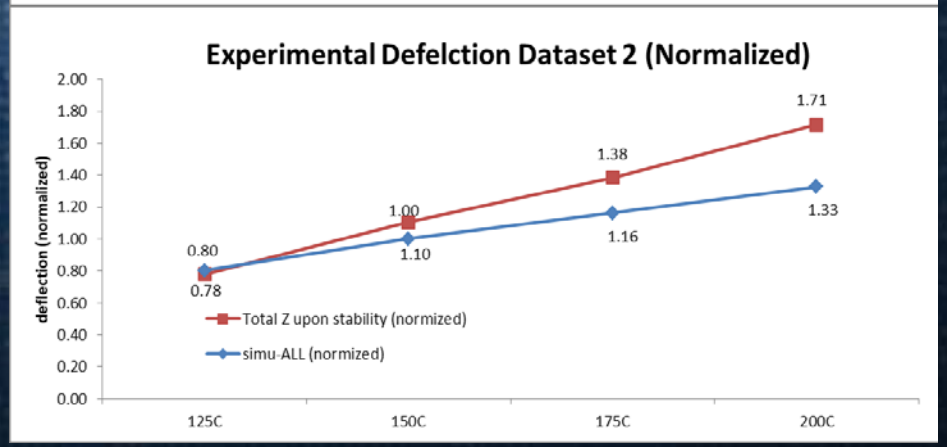


Simulation – Correlation to Experimental Data

- **FEA model showed good temperature & deflection correlation to experimental data.**

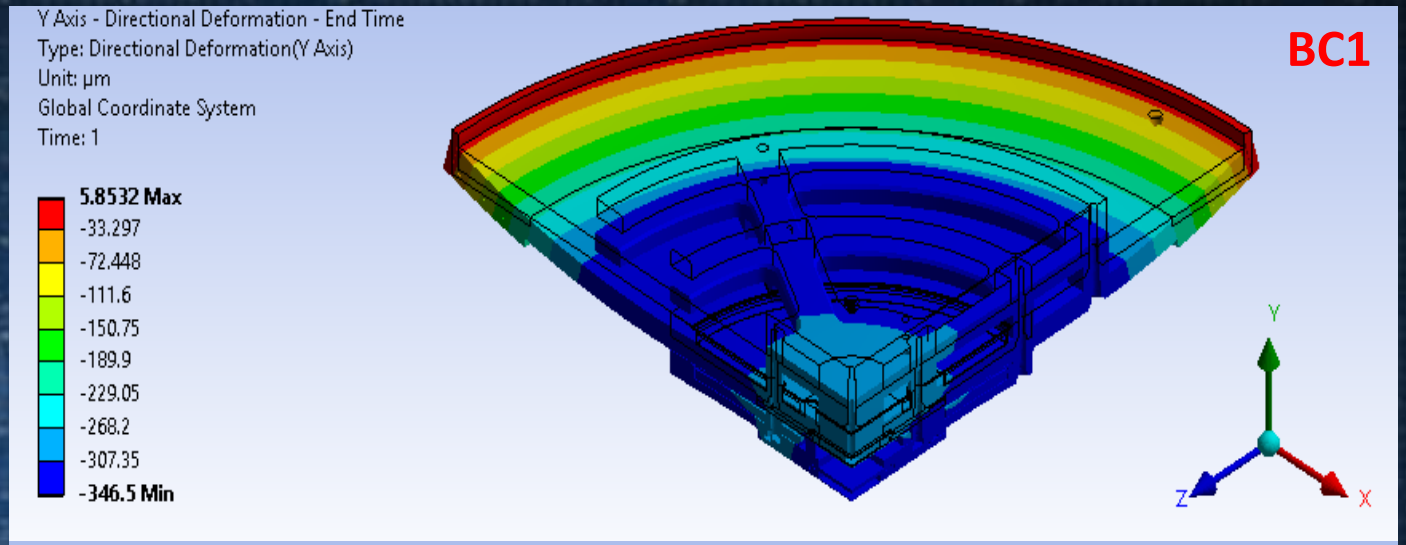


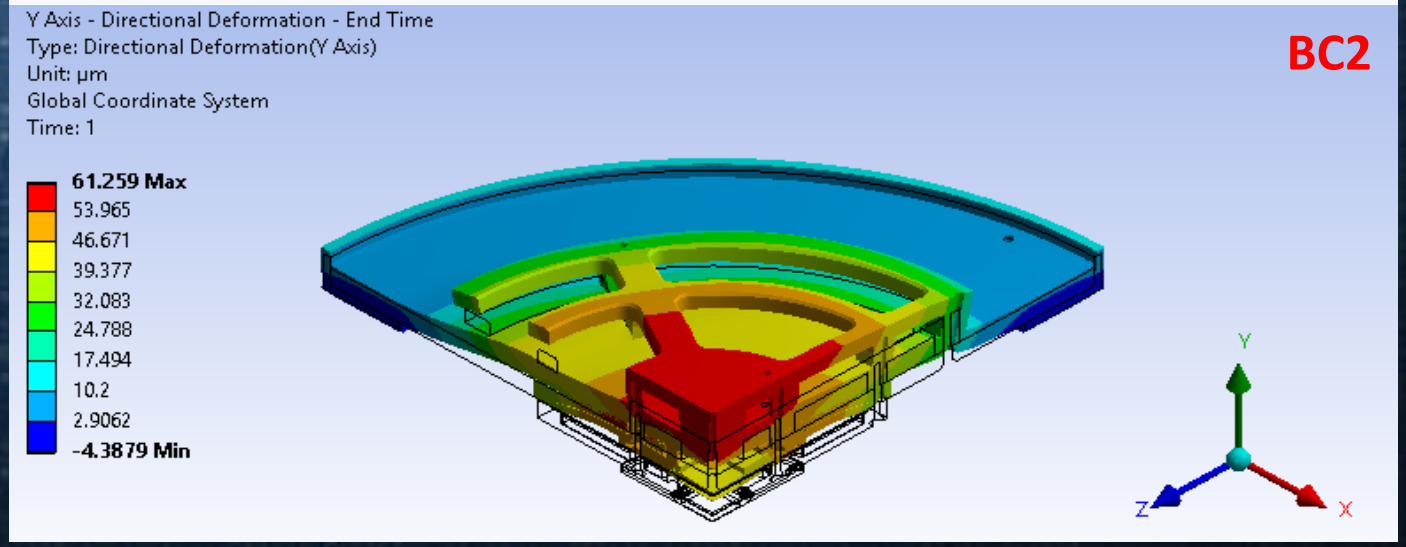




Simulation – Boundary & Contact Effects

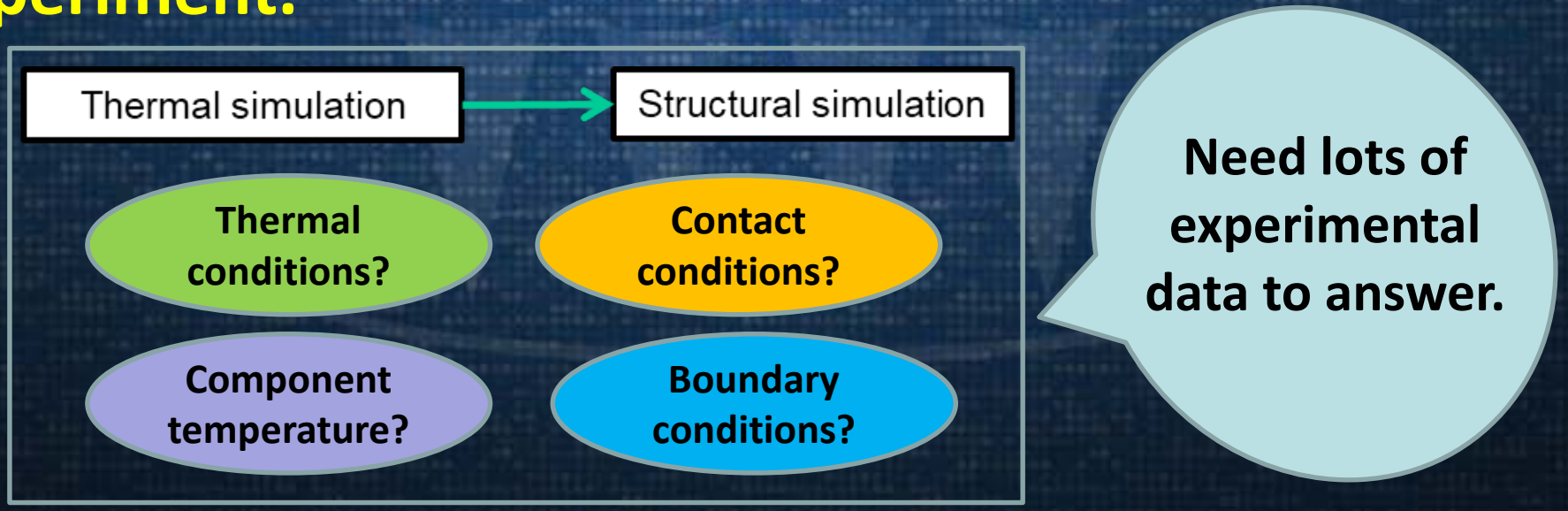
- High temperature simulations are much more sensitive to boundary & contact conditions than room temperature setups.
- Great care must be taken in modeling & results interpretation.





Simulation – Capabilities & Limitations

- Although capable of predicting general probe card high temperature behavior, the demonstrated model also has limitations in capturing subtle contact changes in real life cases.
- This type of model requires large amount of calibration data from experiment.



Conclusions – In General

- Probe card high temperature stability includes initial stability & stability during probing.
- Every probe card has one unique stability state, as a function of card construction & material composition.
- By adjusting soak procedures, the path to reach stability state can change & certain paths require shorter time.
- Improvements made to change card construction or material composition may interact & their application needs to be determined case by case.
- Every card has as its own recovery time vs. operation time characteristics, likely dependent of platform.
- High temperature simulation models are highly sensitive to BC & contact setups.

Conclusions – J750 Type Specific

- The PCB is the most unstable component in the probe card assembly.
- Short operations such as cleaning and wafer change take a long time to recover.
- Our high temperature solutions are applicable to other platforms similar to J750 with stiffeners only in contact with PCB.

High Temperature Solutions for J750 & Similar Platforms	
Time to Initial Stability	**Stability during Probing**
< 30 minutes	< 20 µm

Future Work

- Platform variation study
- Low temperature study, which is suspected to be a close reverse of high temperature, but not exact.

Acknowledgements

- **Special thanks to the high temperature project team at Nidec SV TCL for their hard work & dedication in preparing data used in this paper:**
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  - Phu Cong Phan
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  - Pete Rogan
  - Kyle Cotner
  - Robert Stampahar
  - JB Hollstein

Thank you!

Questions?

SW Test Workshop
Semiconductor Wafer Test Workshop

A Novel Measurement Method for Measuring CCC and MAC at once

Matthias Schnaithmann

Achim Weiland

Gunther Böhm

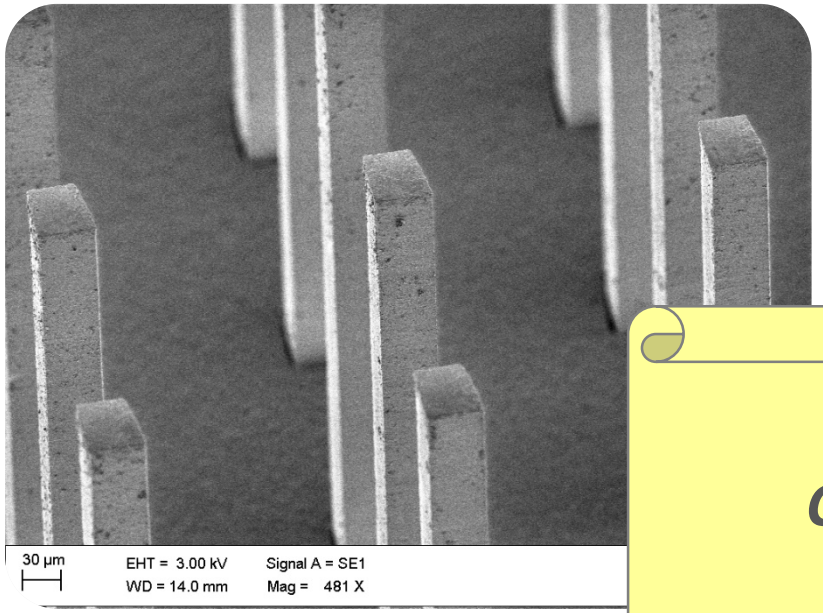
FEINMETALL GmbH

FEINMETALL
Contact Technologies

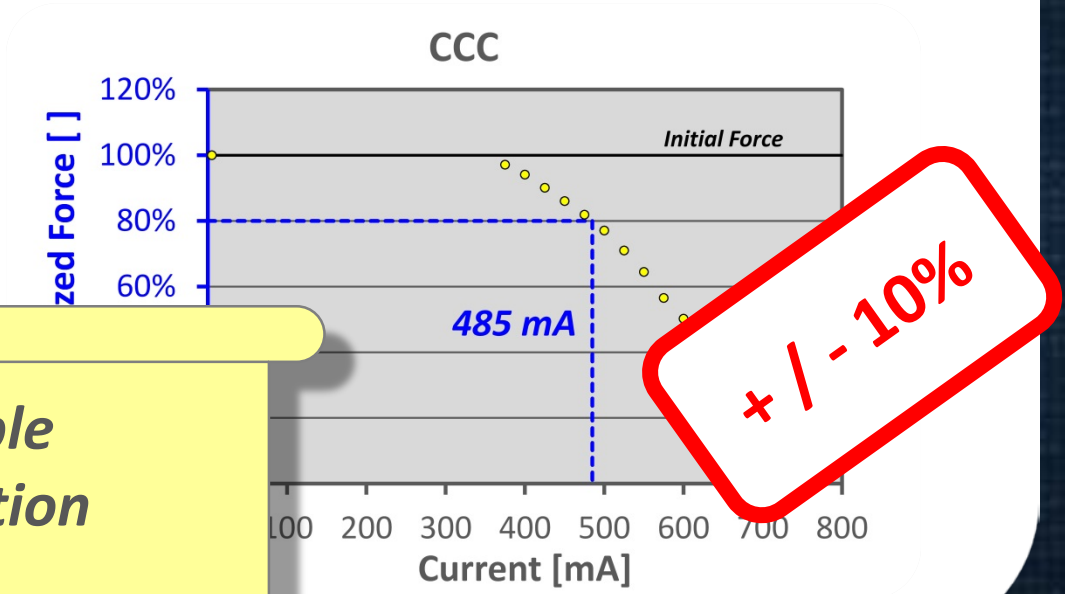
June 3-6, 2018

Objectives

New MEMS Product



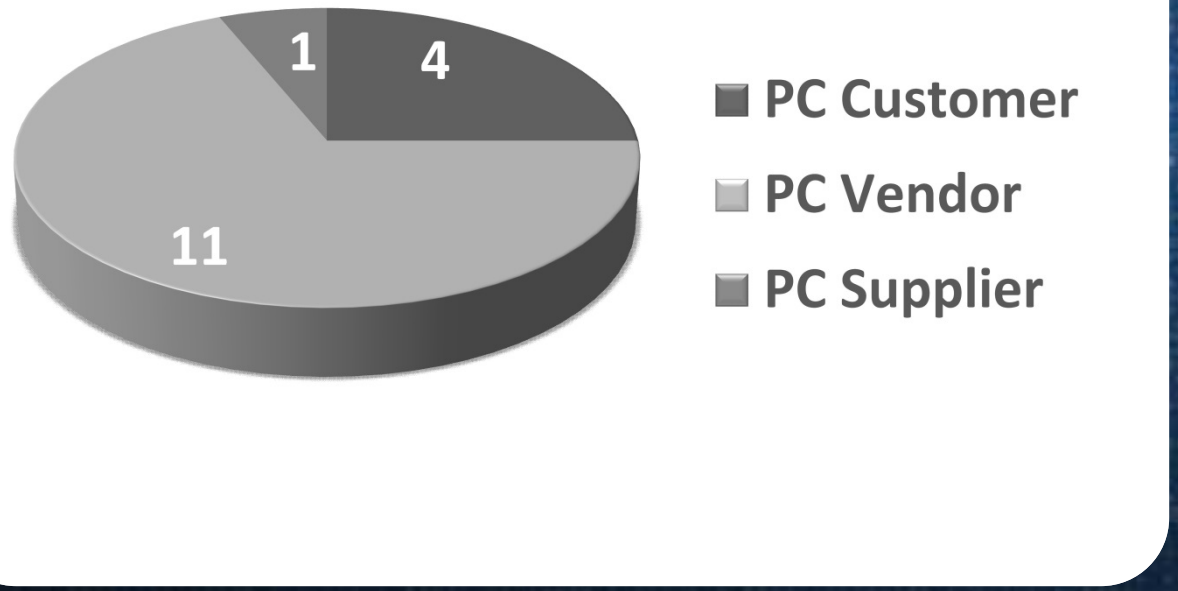
Large Scatter of Measurement Results

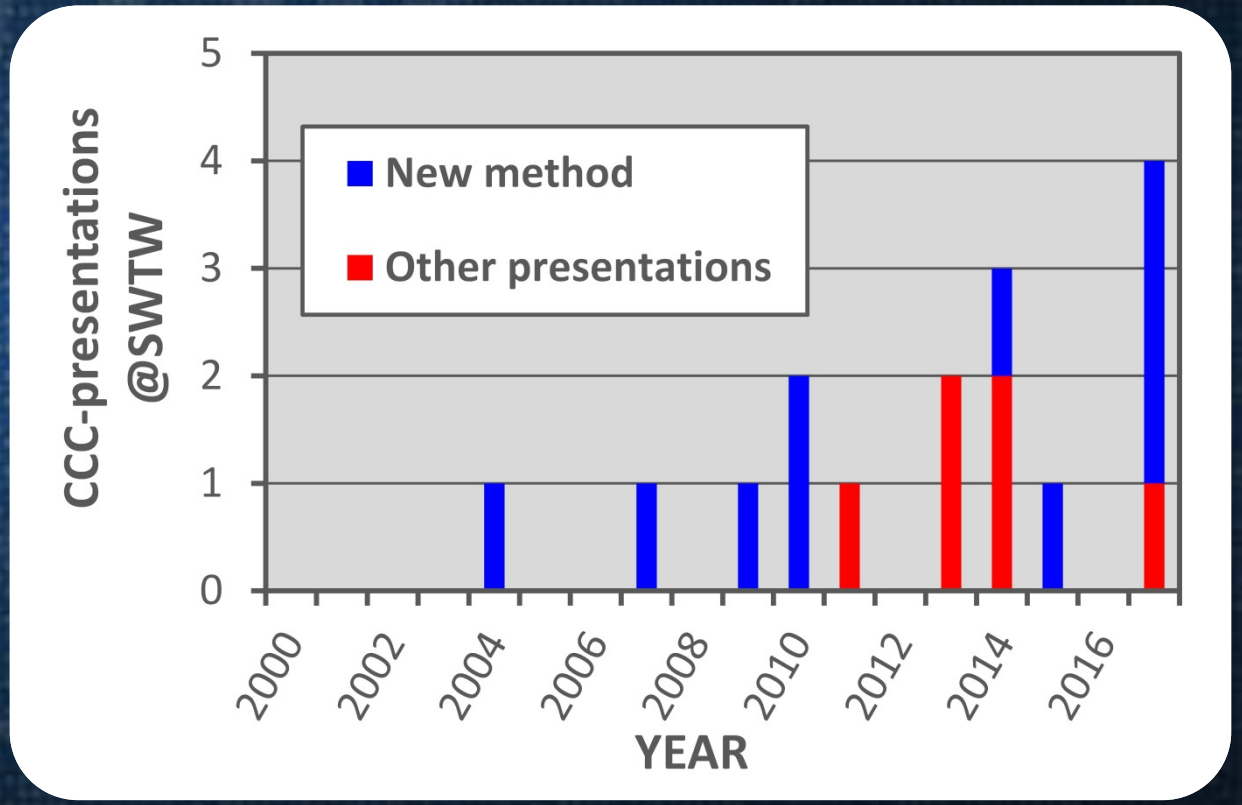


Reproducable Characterization of Current Carrying Capability

Methods

- CCC a Topic Often Presented at the SWTW



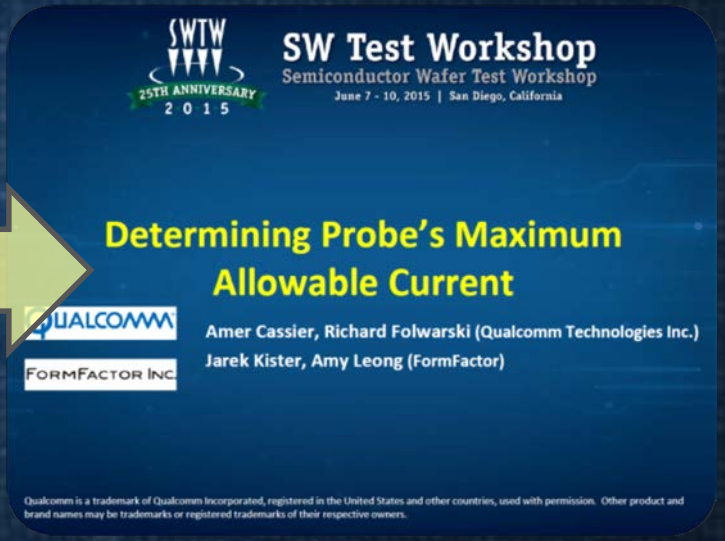


Methods

- **Current Carrying Capability – Main Presentations**

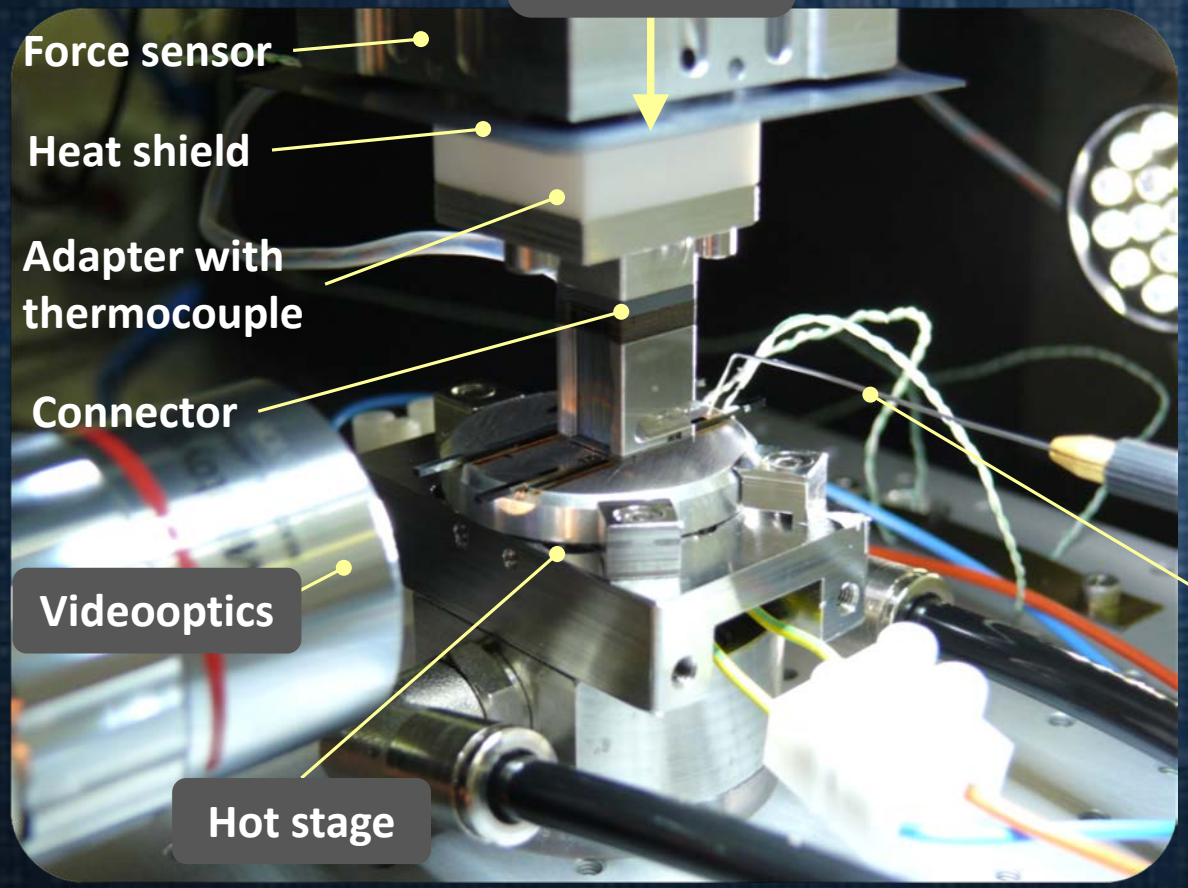


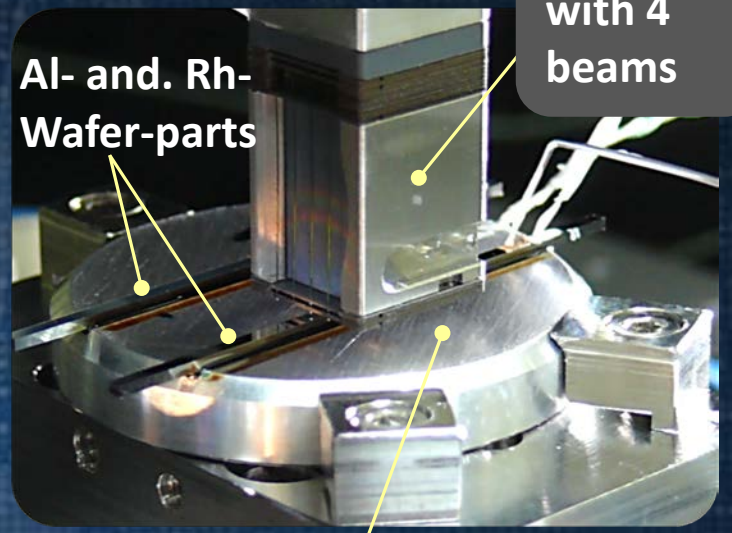




Methods

- **Test Setup**



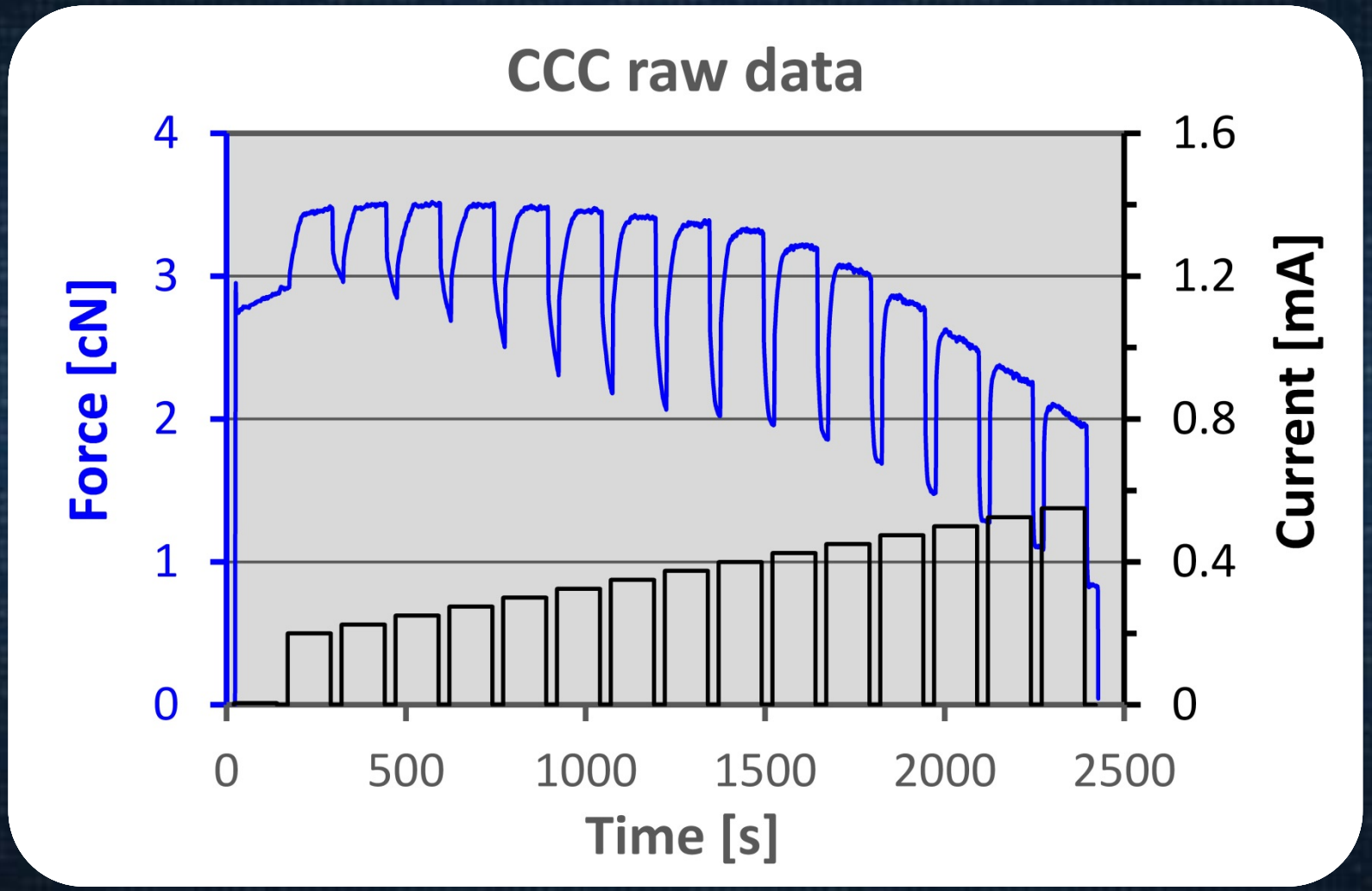


Specimen holder with attached Al- and Rh-Wafer-parts

Contacting (Tungsten needle)

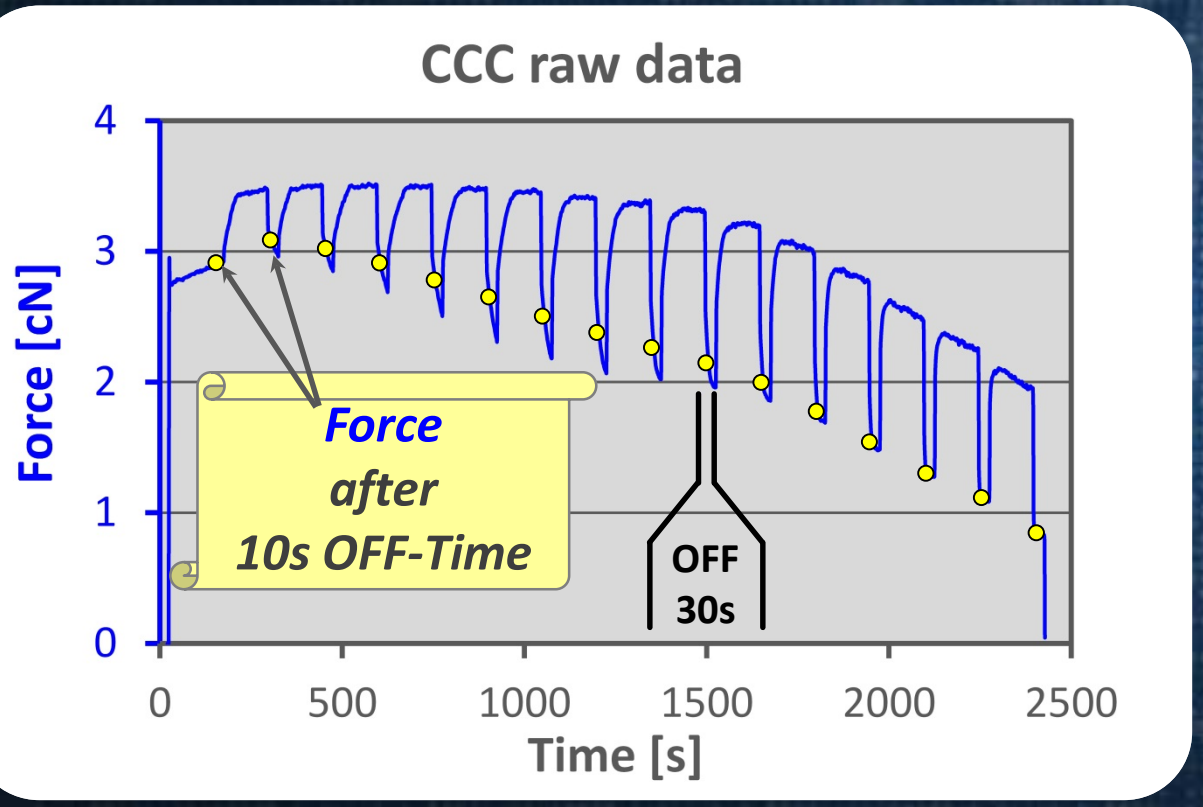
Thermocouple on the wafer surface

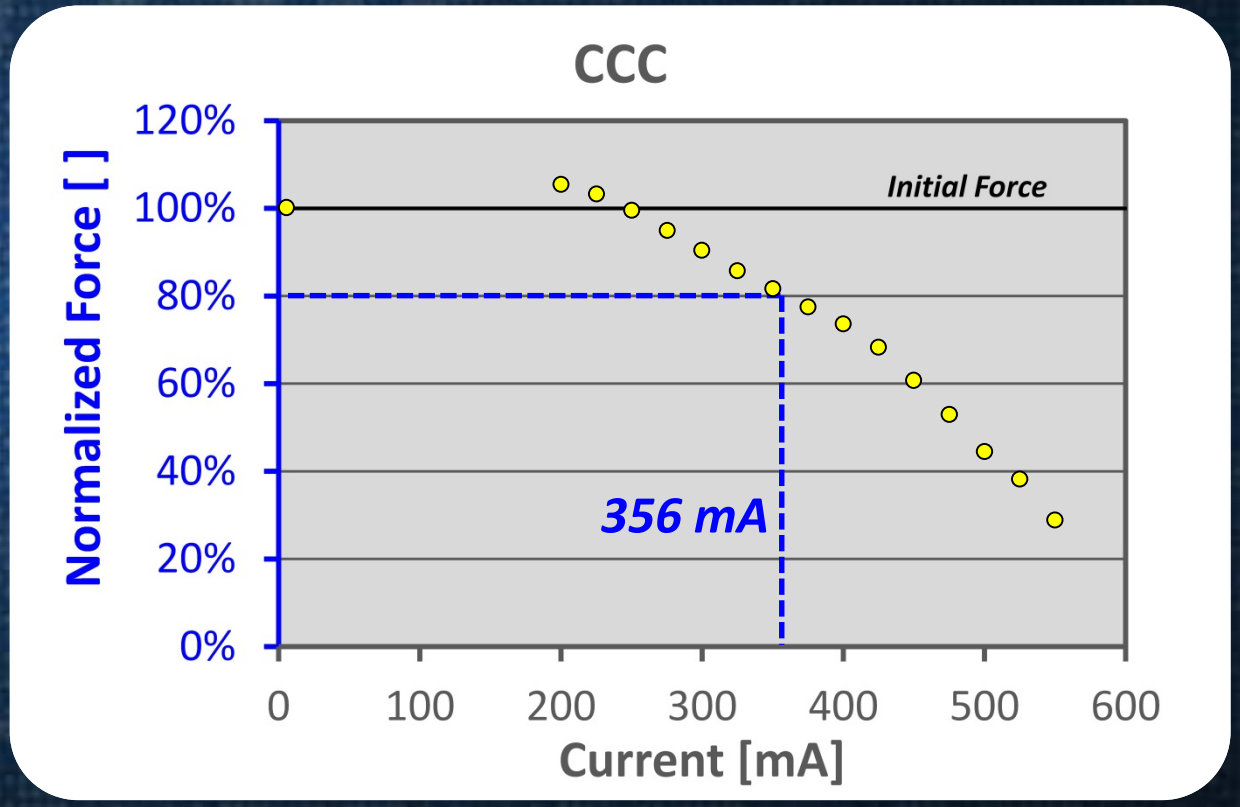
Methods


CCC raw data
Force [cN]
Current [mA]
Time [s]
0
1
2
3
4
0
0.4
0.8
1.2
1.6
0
500
1000
1500
2000
2500

Methods

- Standard CCC (ISMI 2009)





Methods

- **Influence on the CCC Result**

CCC according to ISMI 2009

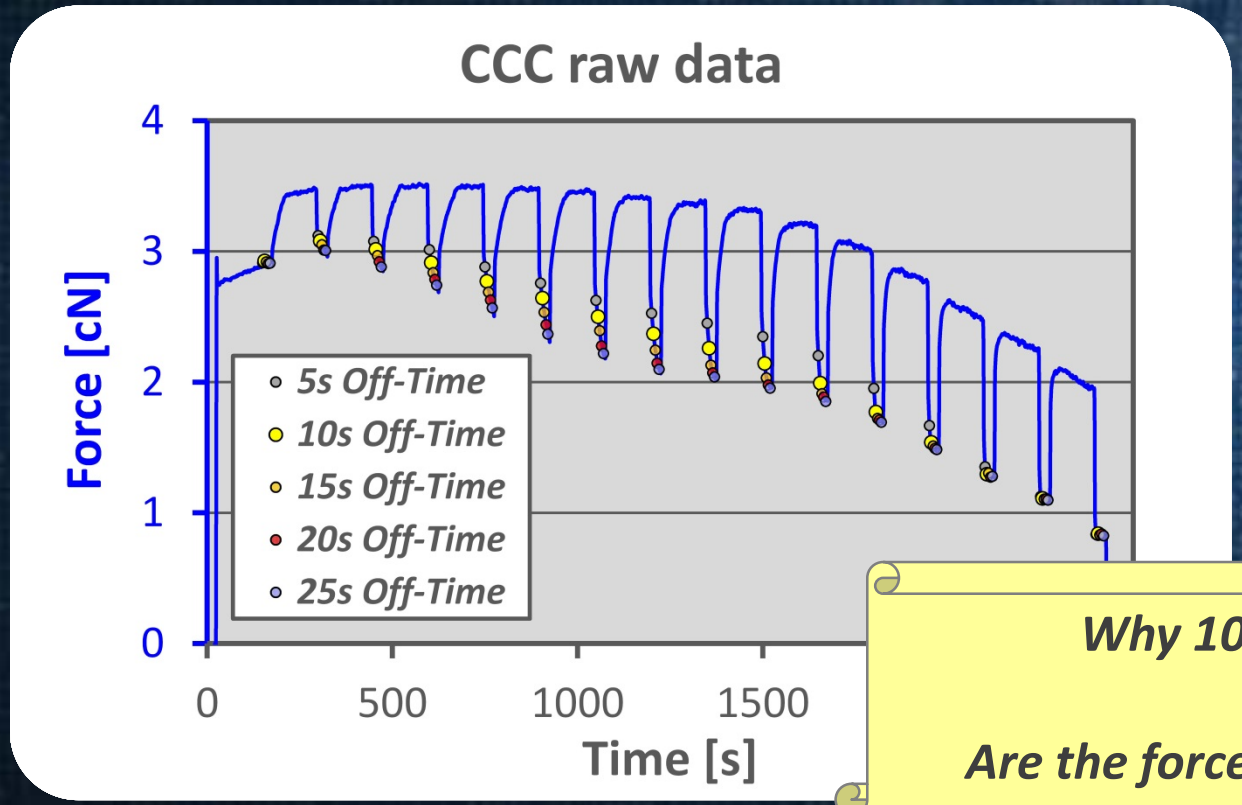
Vertical probe card technology

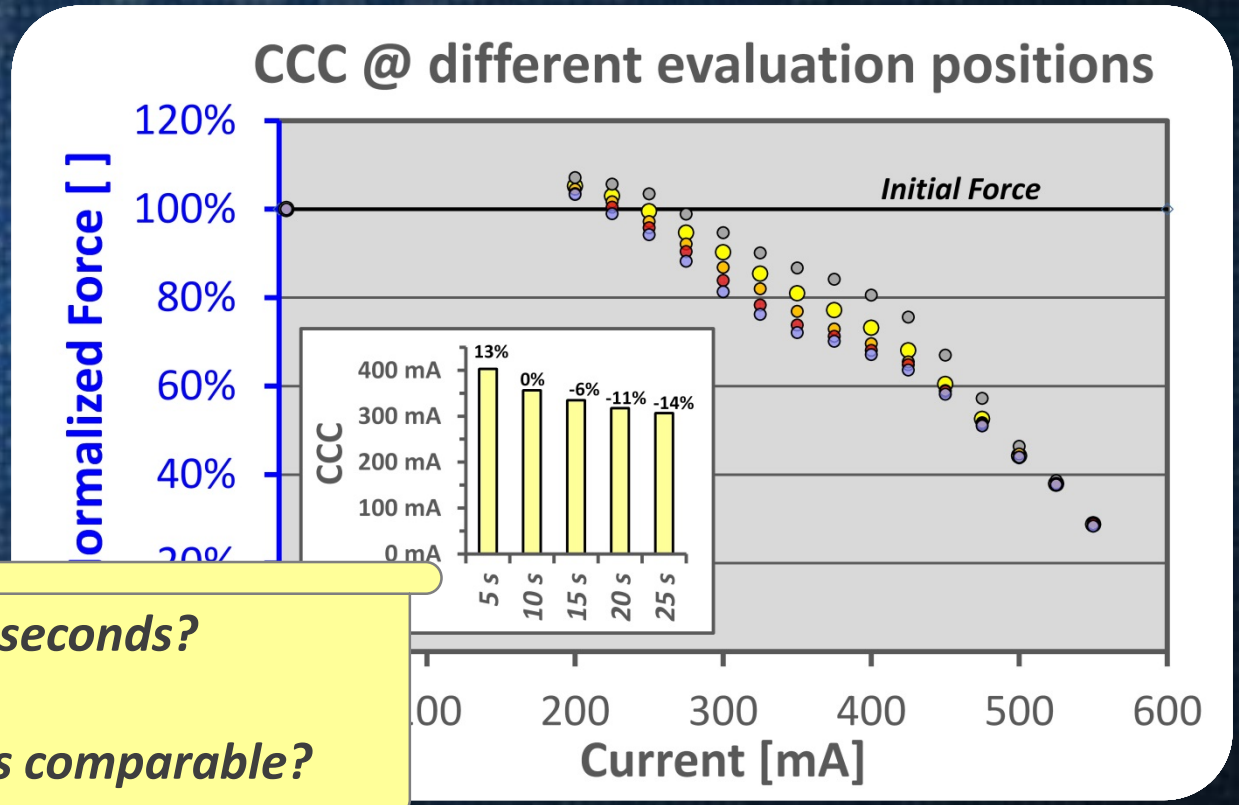
➔ DO WE COMPARE COMPARABLE FORCES?

  - Evaluation position of the force
  - Initial force

Methods

- **Evaluation Position of the Force**





Why 10 seconds?

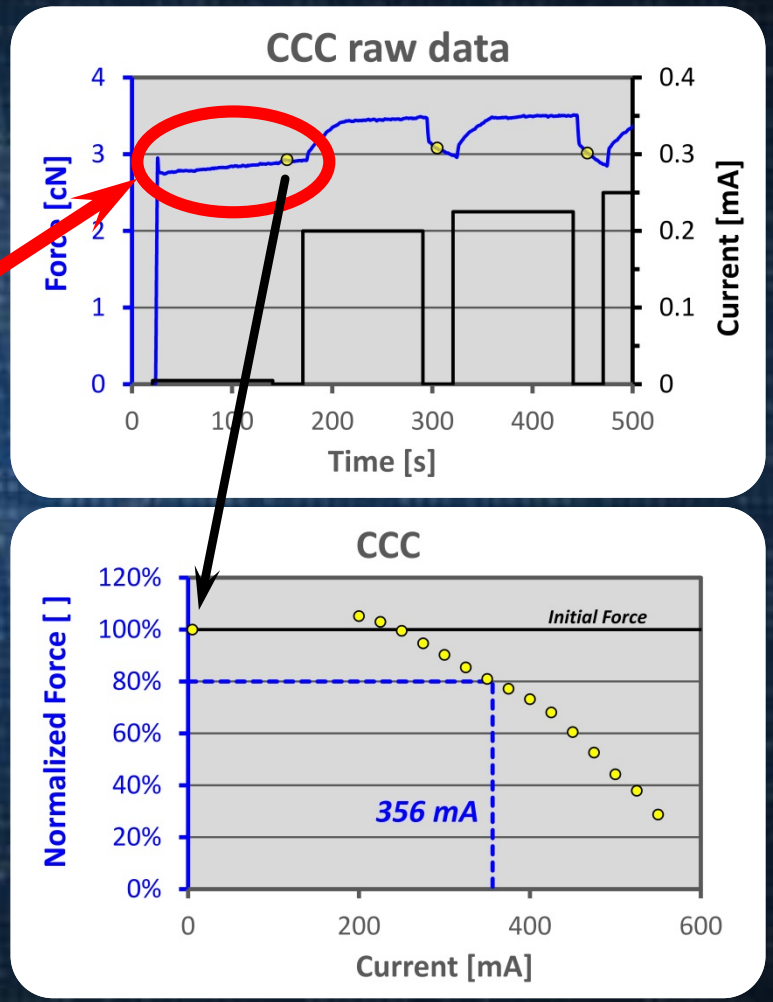
Are the forces comparable?

Methods

- **Initial Force**

The initial force has a large impact on the CCC result!

➔ *IS THE **INITIAL FORCE** WELL DEFINED?*

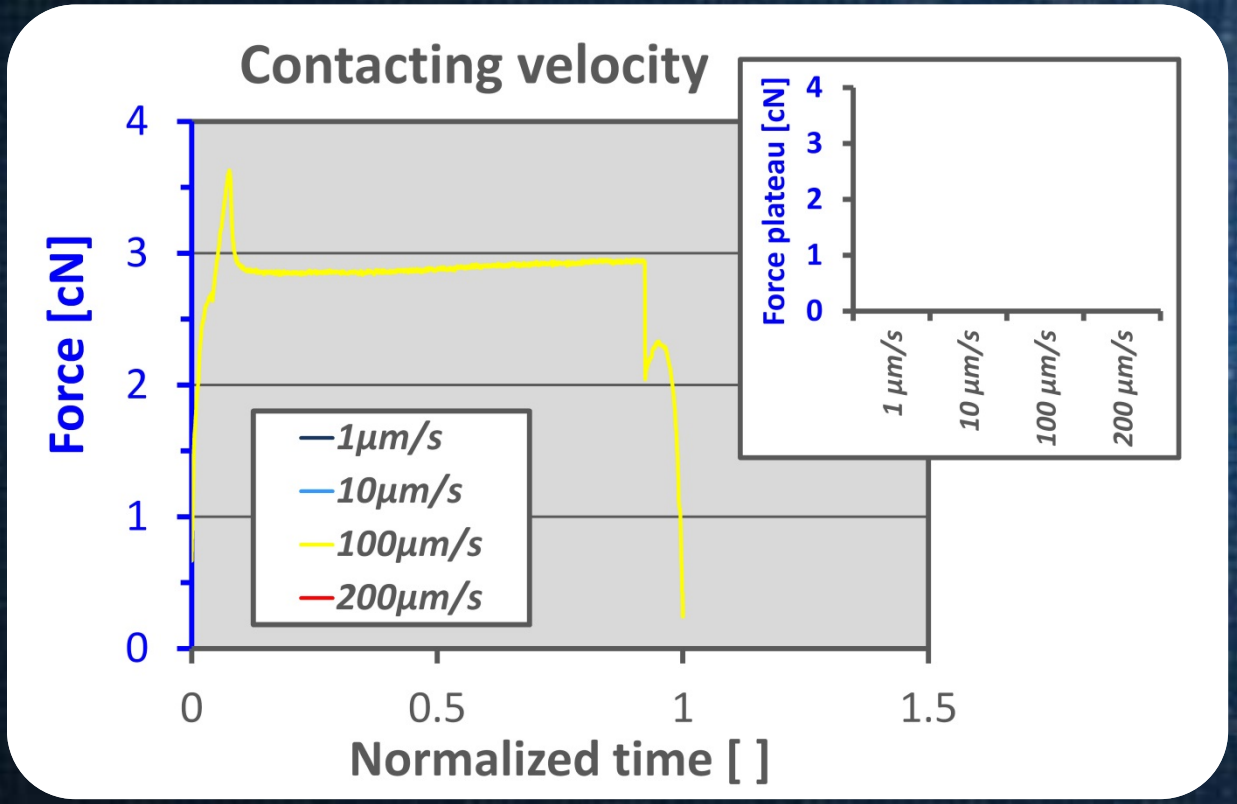


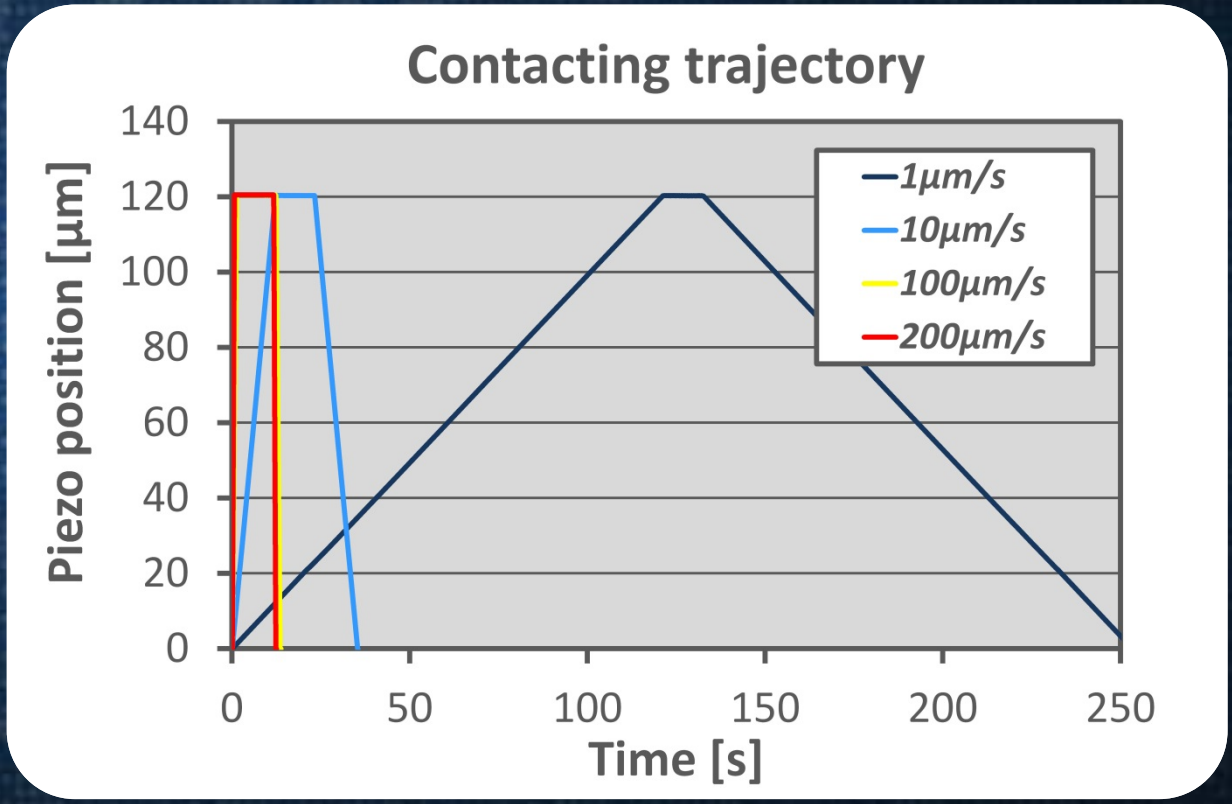
Influence?

- Velocity at Touch Down
- Relative movements

Methods

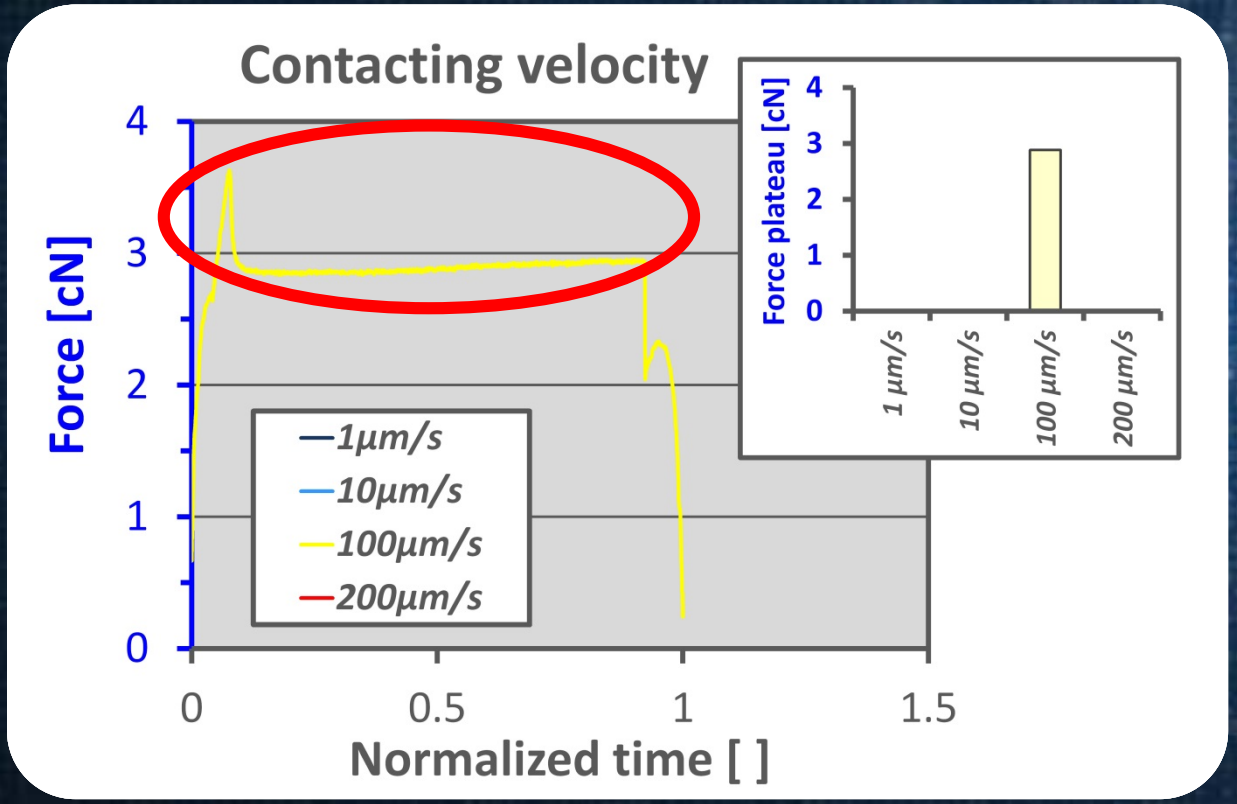
- Velocity at Touch Down

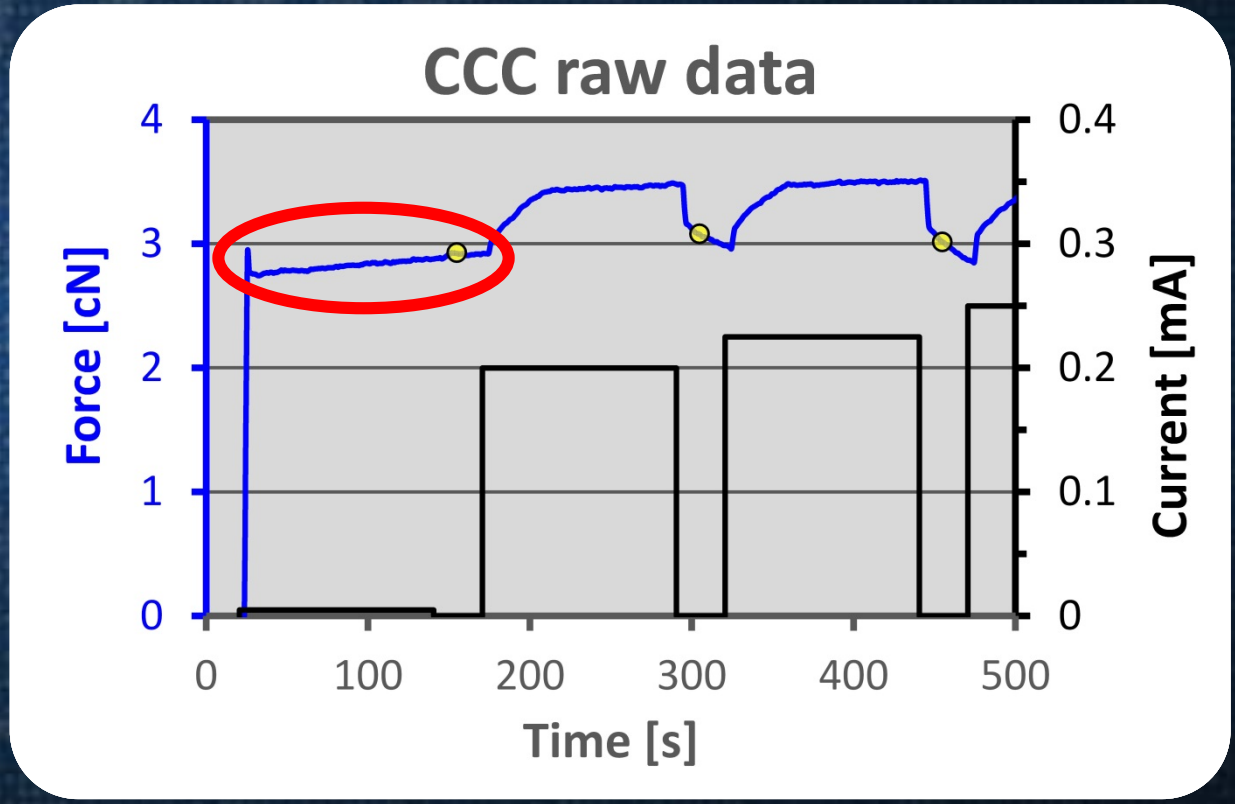




Methods

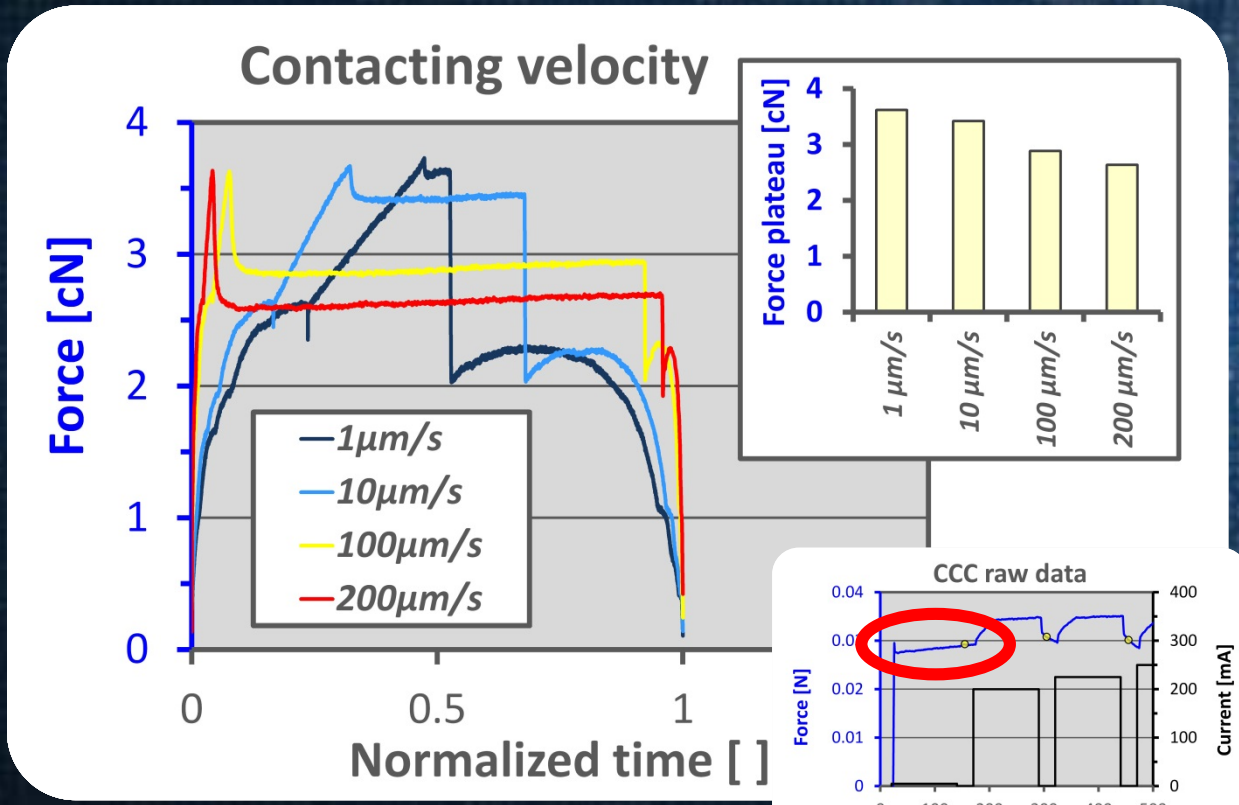
- Velocity at Touch Down

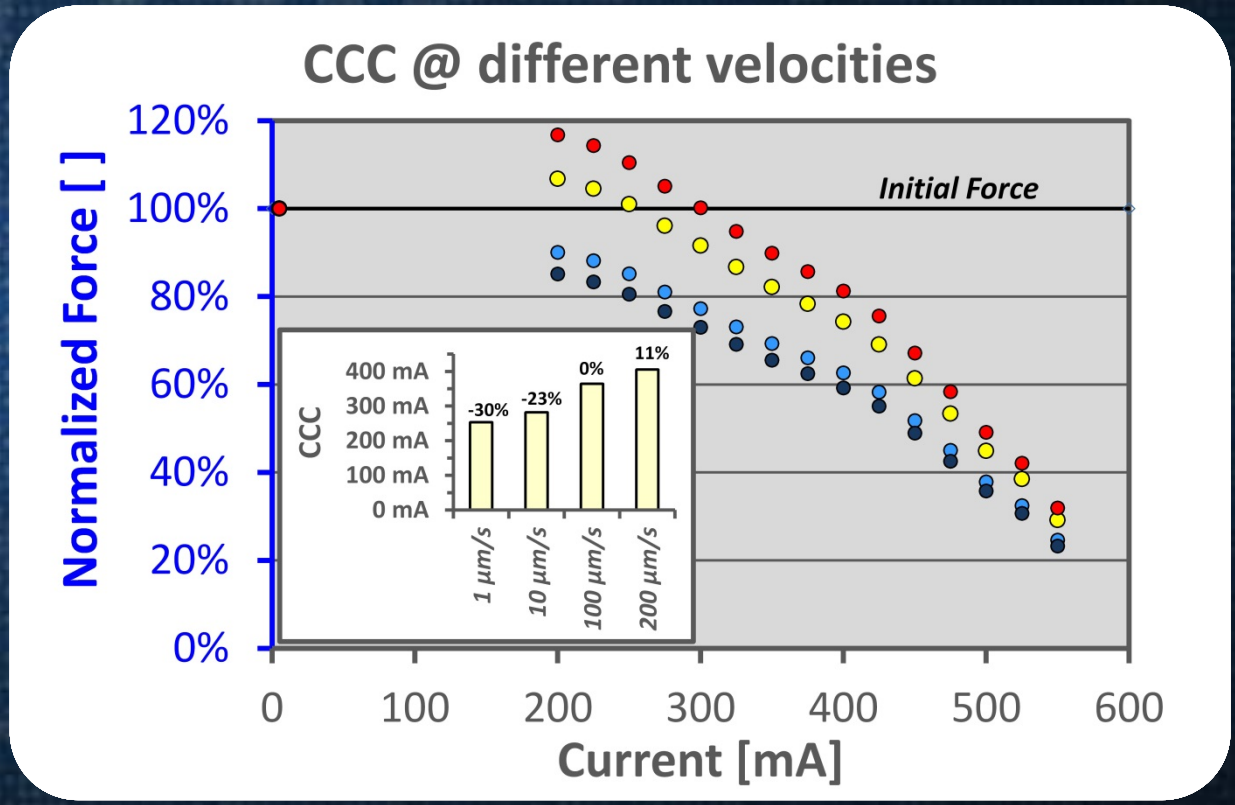




Methods

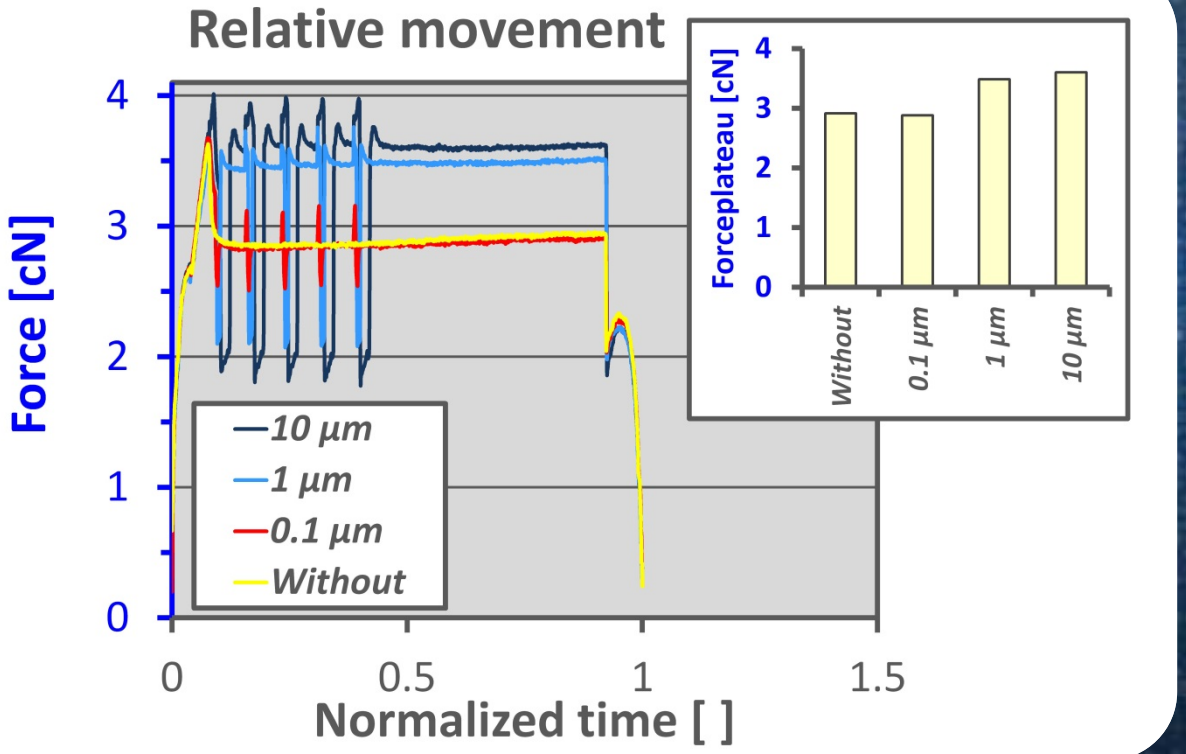
- Velocity at Touch Down

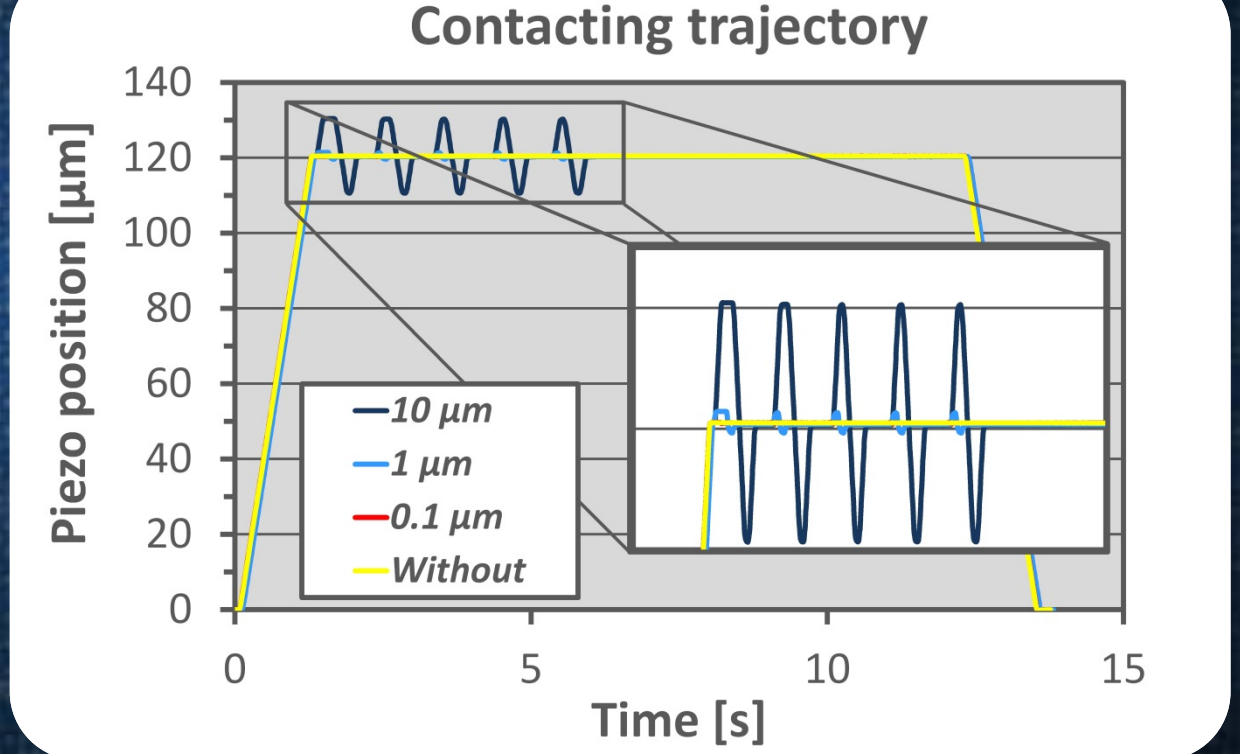




Methods

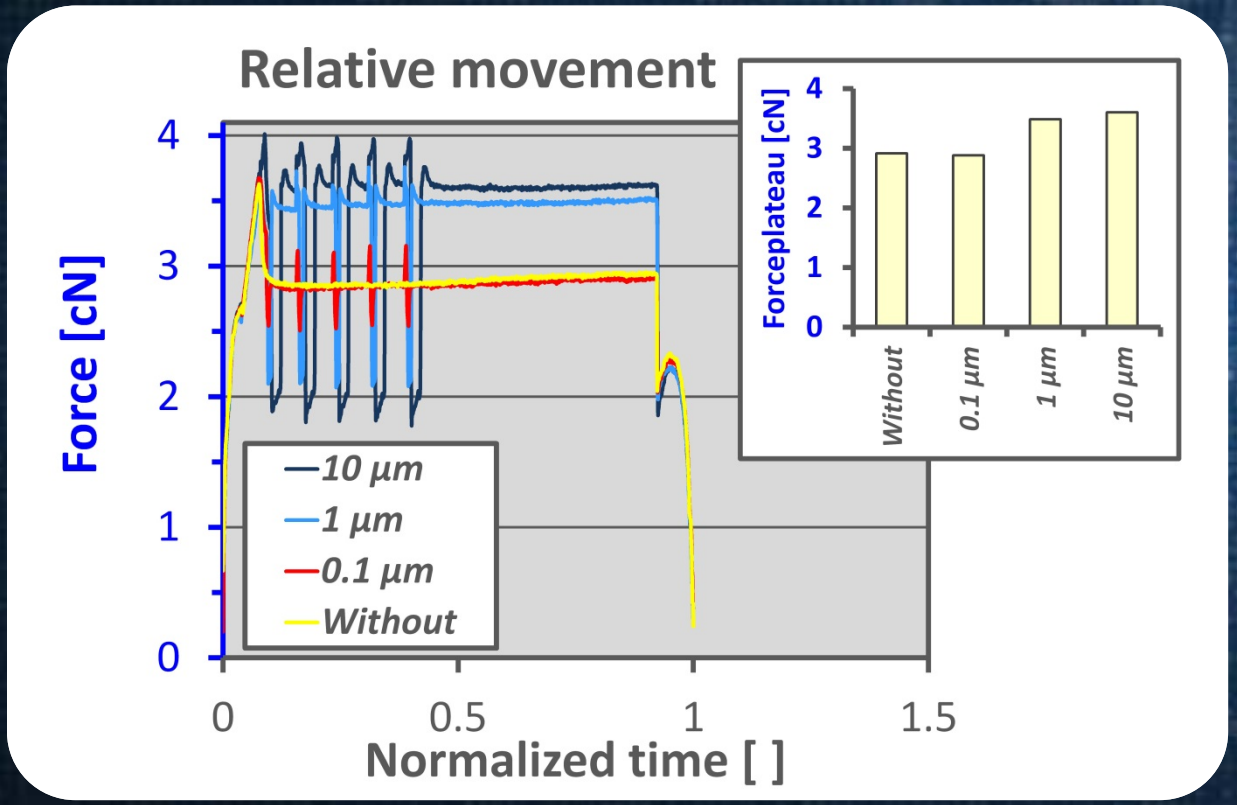
- **Relative Movements**

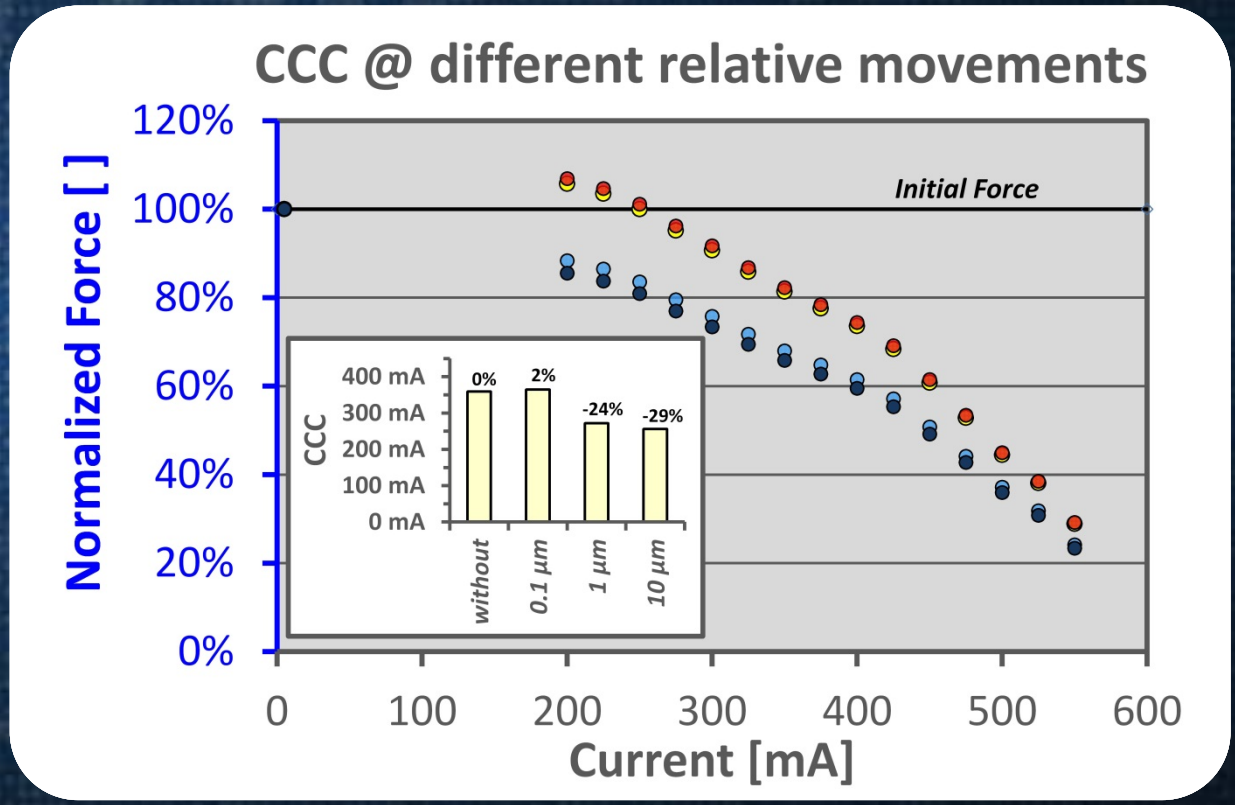




Methods

- **Relative Movements**





Methods

- **Influence on the CCC Result**

Better understanding of CCC-data needed

CCC according to ISMI 2009

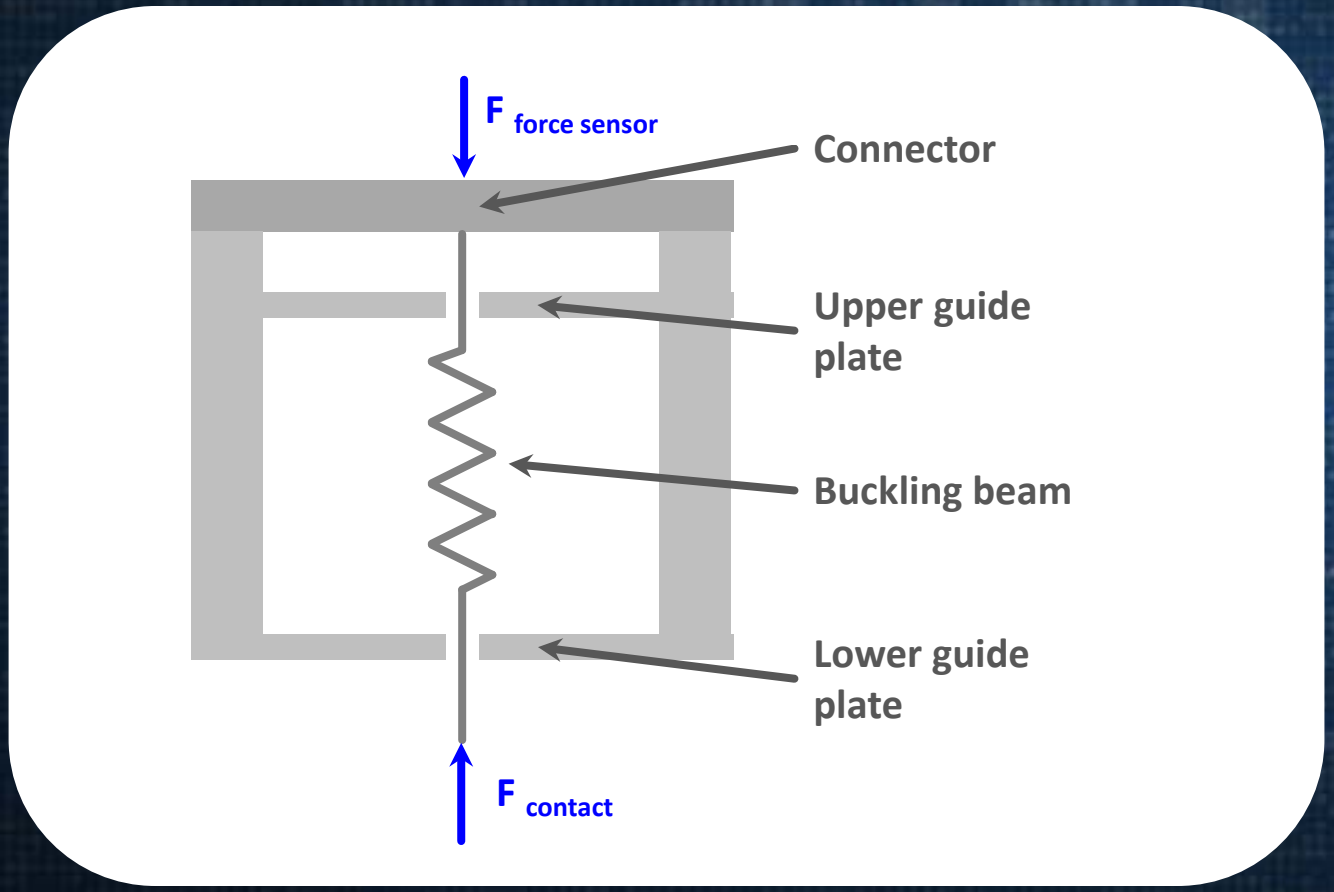
Vertical probe card technology

➔ *DO WE COMPARE **COMPARABLE FORCES**?*

  - Evaluation position of the force
  - Initial force

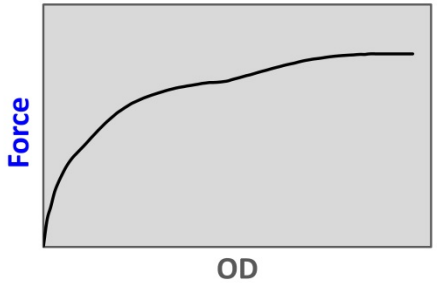
Methods

- **Understanding the CCC-Raw-Data**



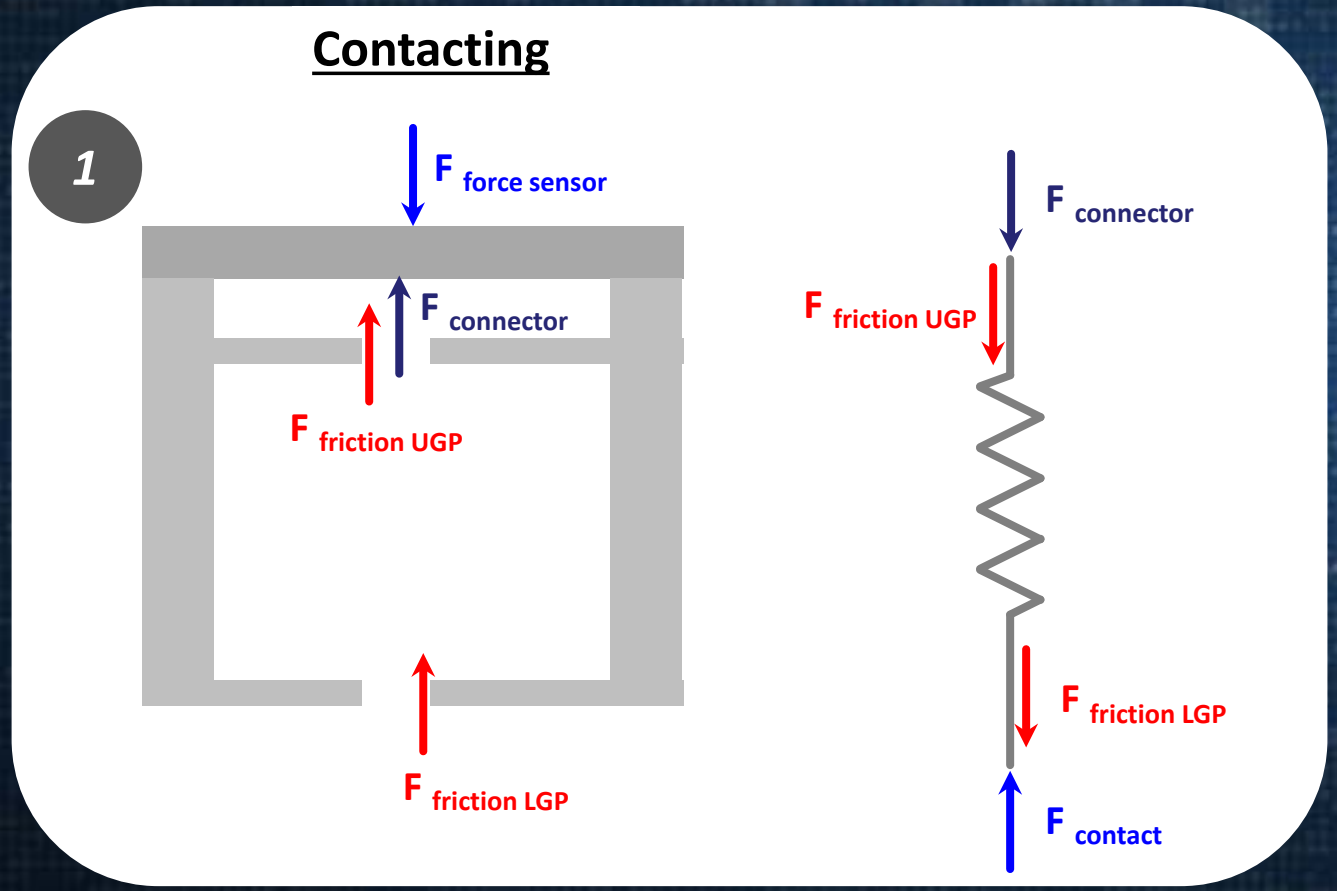
Simplified model

Buckling beam = Spring with a nonlinear spring constant



Methods

- Understanding the CCC-Raw-Data

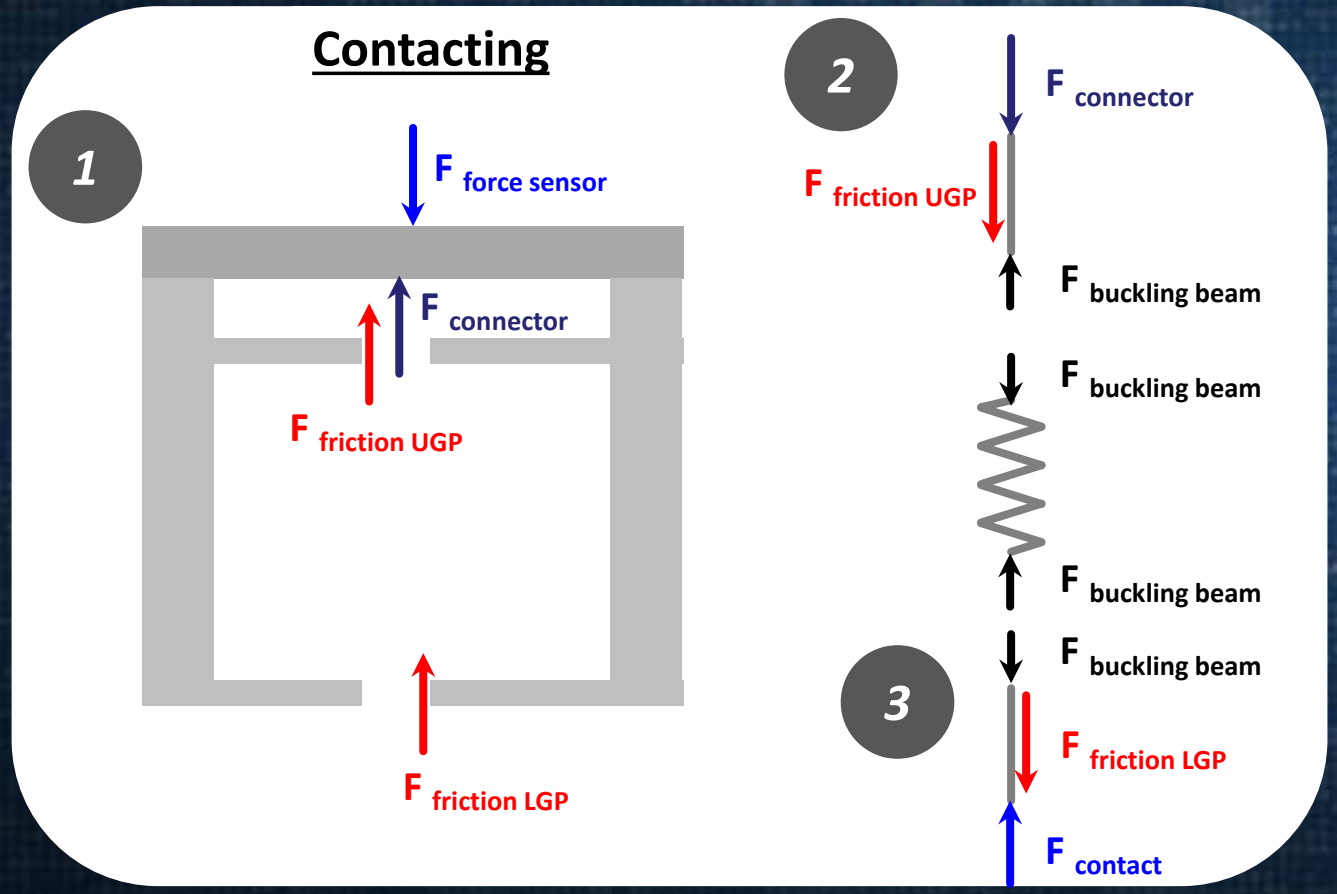


Free cutting and equilibrium of forces

$1: F_{force\ sensor} = F_{connector} + F_{friction\ UGP} + F_{friction\ LGP}$

Methods

- Understanding the CCC-Raw-Data



Free cutting and equilibrium of forces

$1: F_{force\ sensor} = F_{connector} + F_{friction\ UGP} + F_{friction\ LGP}$

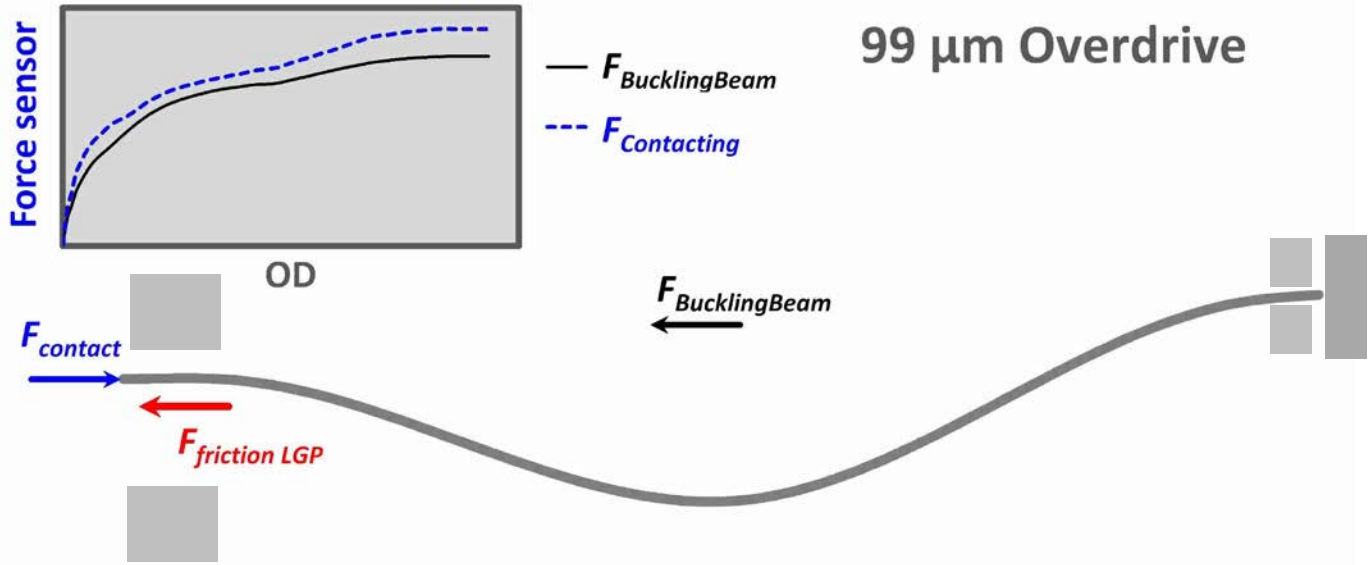
$2: F_{connector} = F_{buckling\ beam} - F_{friction\ UGP}$

$3: F_{contact} = F_{buckling\ beam} + F_{friction\ LGP}$

$\rightarrow F_{force\ sensor} = F_{contact} = F_{BucklingBeam} + F_{friction\ LGP}$

Methods

- **Understanding the CCC-Raw-Data**

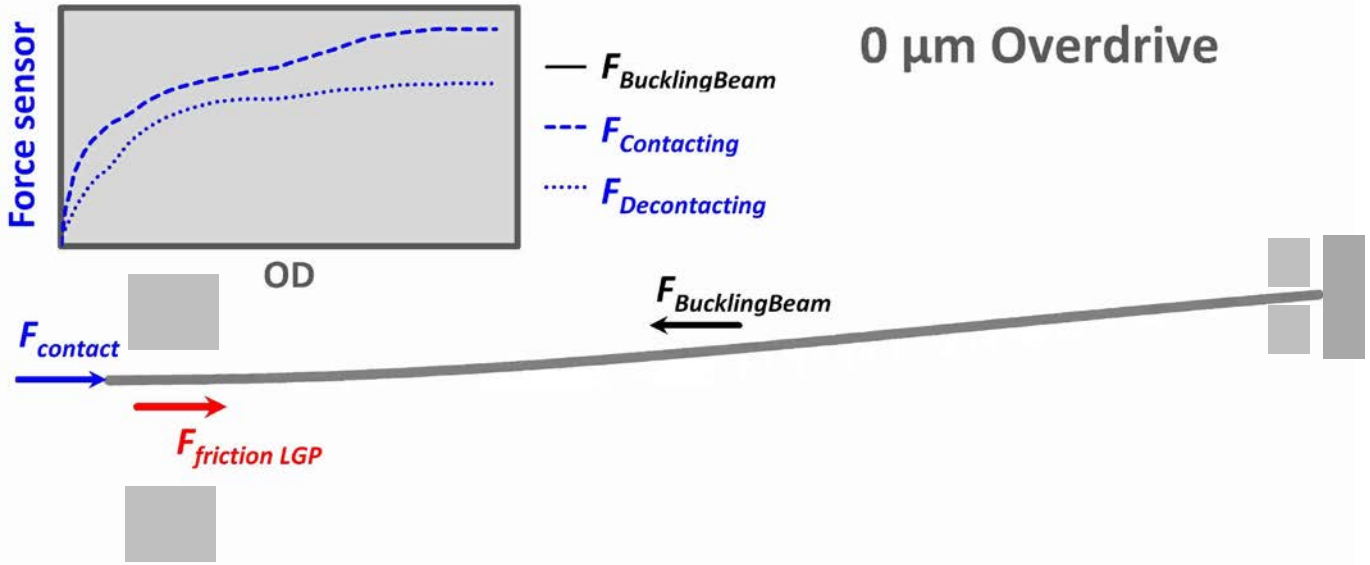


Contacting

➔ $F_{force\ sensor} = F_{BucklingBeam} + F_{friction\ LGP}$

Methods

- **Understanding the CCC-Raw-Data**



Contacting

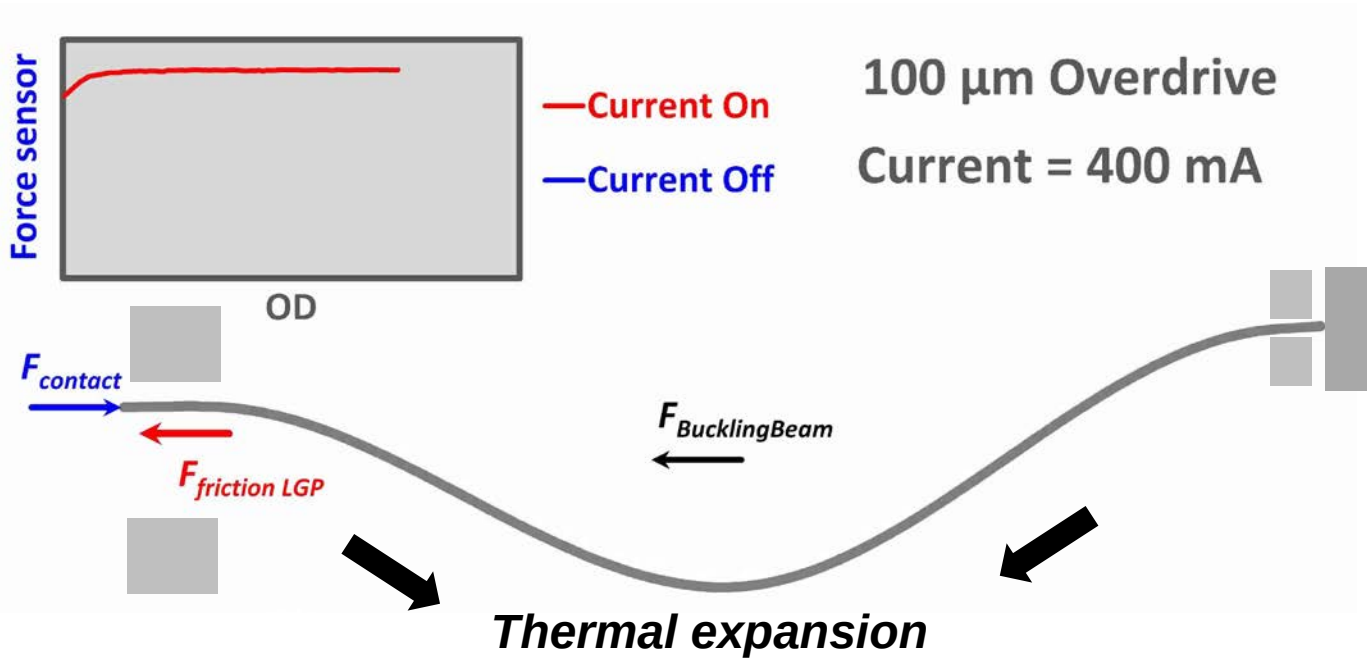
➔ $F_{force\ sensor} = F_{BucklingBeam} + F_{friction\ LGP}$

Decontacting

➔ $F_{force\ sensor} = F_{BucklingBeam} - F_{friction\ LGP}$

Methods

- **Understanding the CCC-Raw-Data**

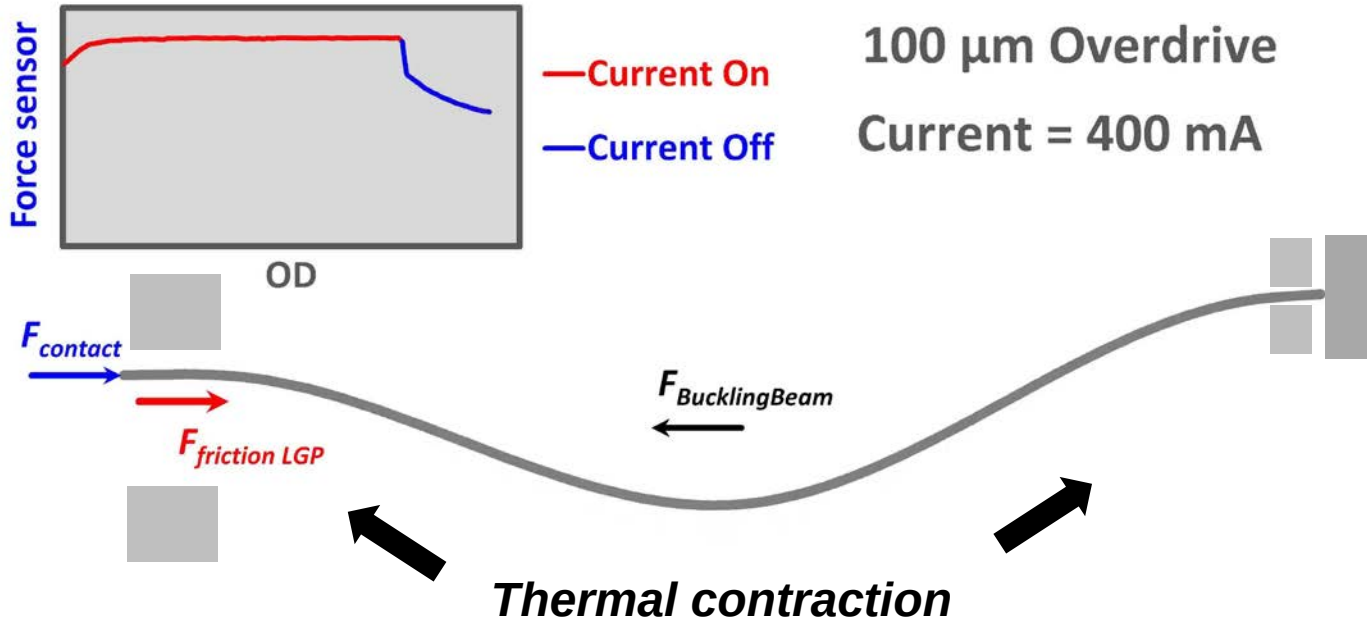


Current On

➔ $F_{force\ sensor} = F_{BucklingBeam} + F_{friction\ LGP}$

Methods

- **Understanding the CCC-Raw-Data**



Current On

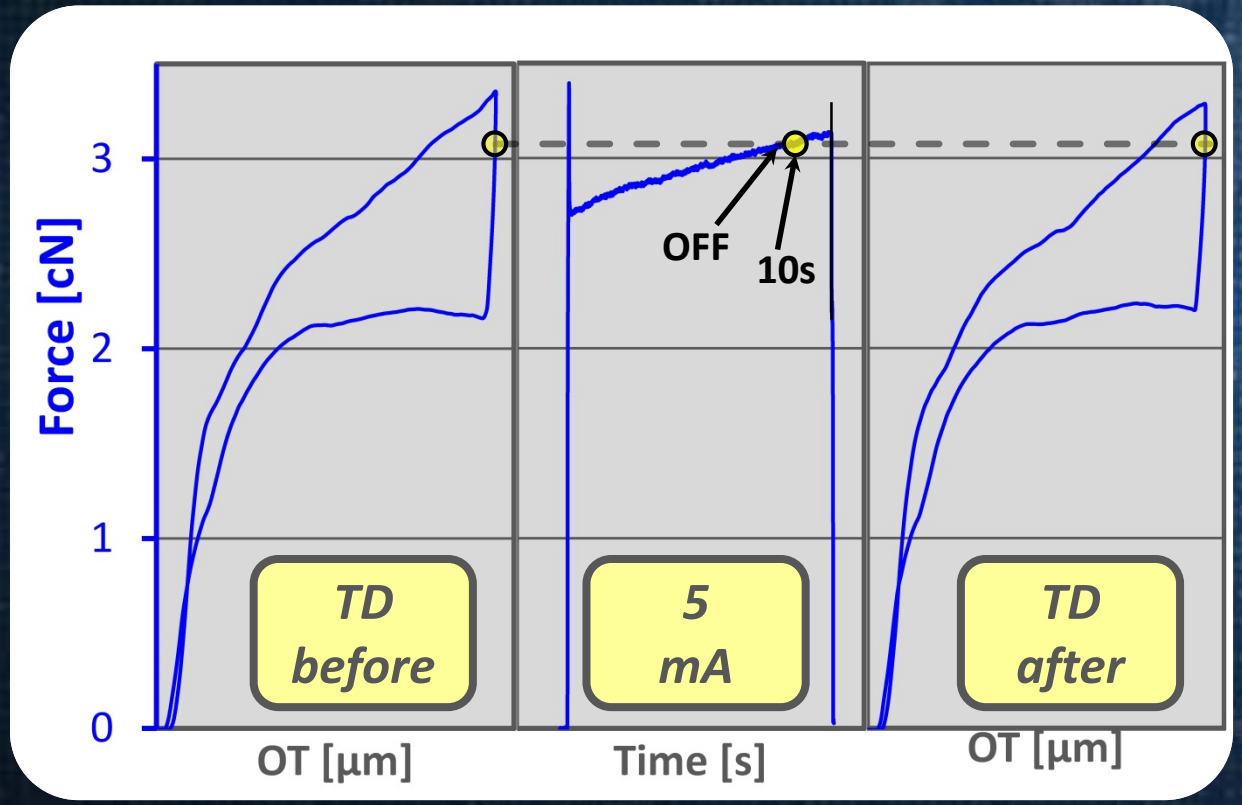
➔ $F_{force\ sensor} = F_{BucklingBeam} + F_{friction\ LGP}$

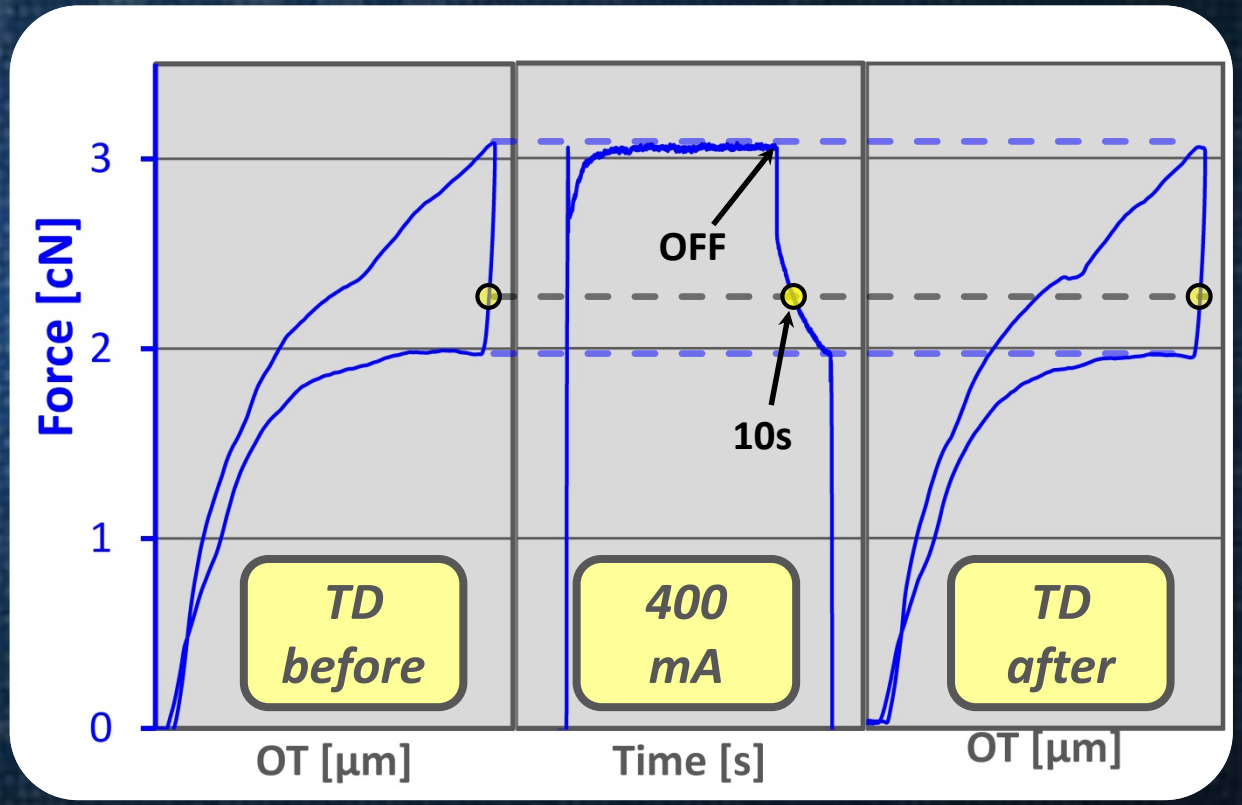
Current Off

➔ $F_{force\ sensor} = F_{BucklingBeam} - F_{friction\ LGP}$

Methods

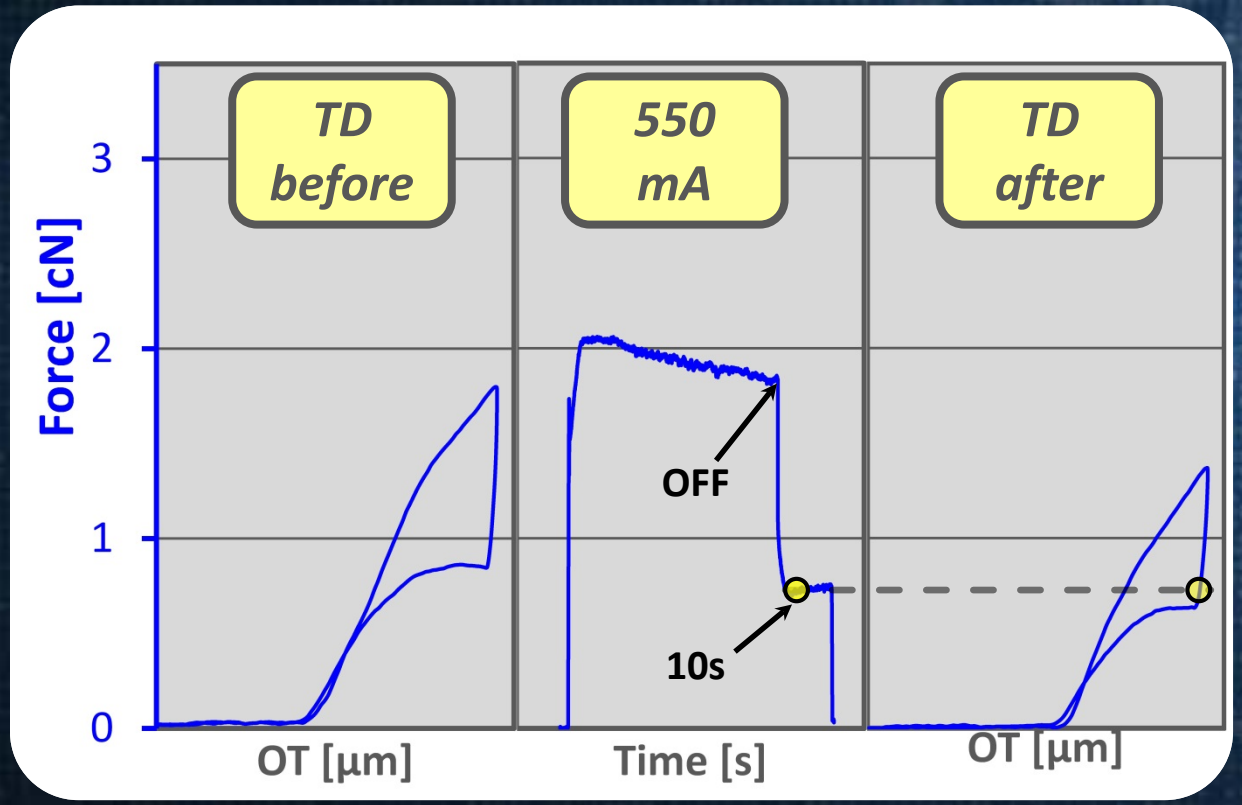
- Force vs. Overdrive Plots Before and After Current Load





Methods

- **Force vs. Overdrive Plots Before and After Current Load**



CCC according to ISMI 2009

Vertical probe card technology

➔ *The **FORCES** are not comparable*

Methods

- **More Comparable Method**

FORCE measurements
@ nominal overdrive
between
the different current steps

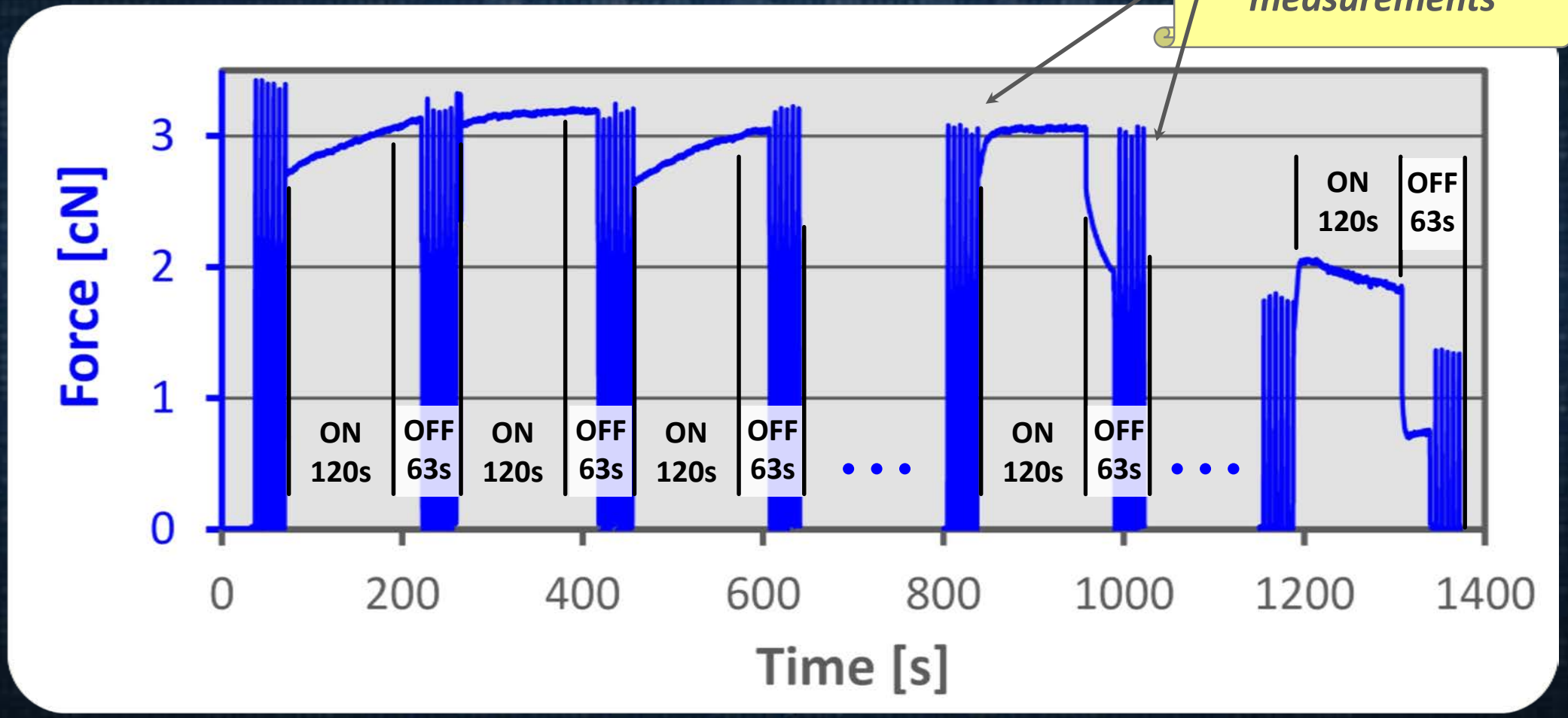
Comparable forces!

1. *5 FORCE measurements @ nominal Overdrive*
2. *Next CURRENT step applied 120 s CURRENT ON*
3. *30 s CURRENT OFF*
- *x. Restart again with 1.*

End with 5 FORCE measurements @ nominal Overdrive

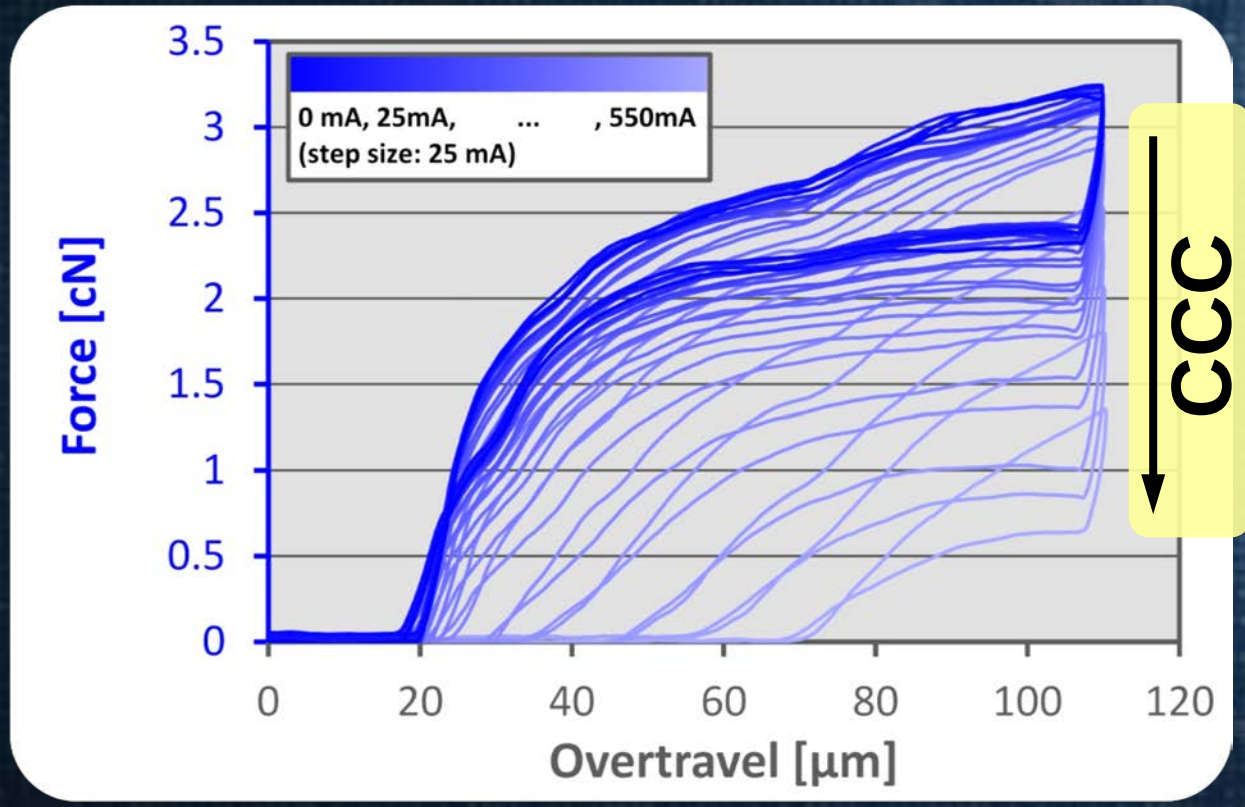
Methods

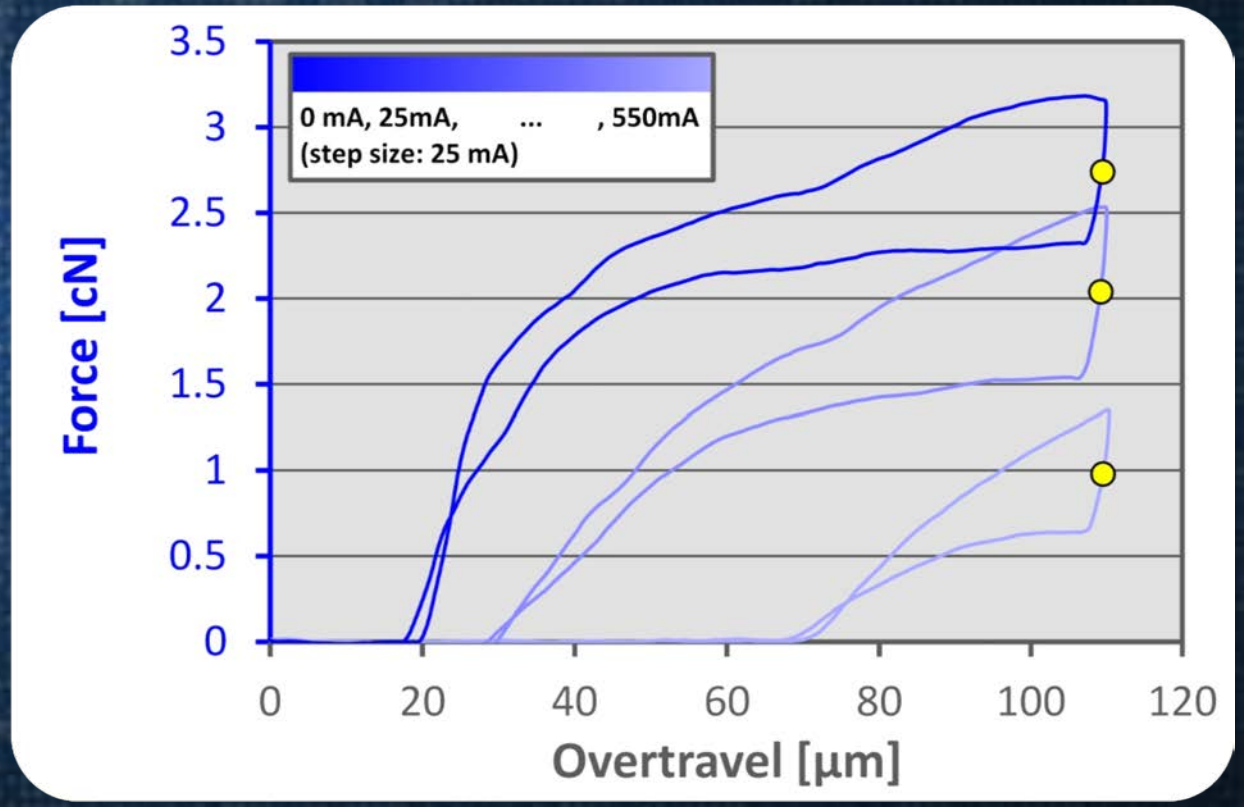
- **Better and More Comparable Method**



Methods

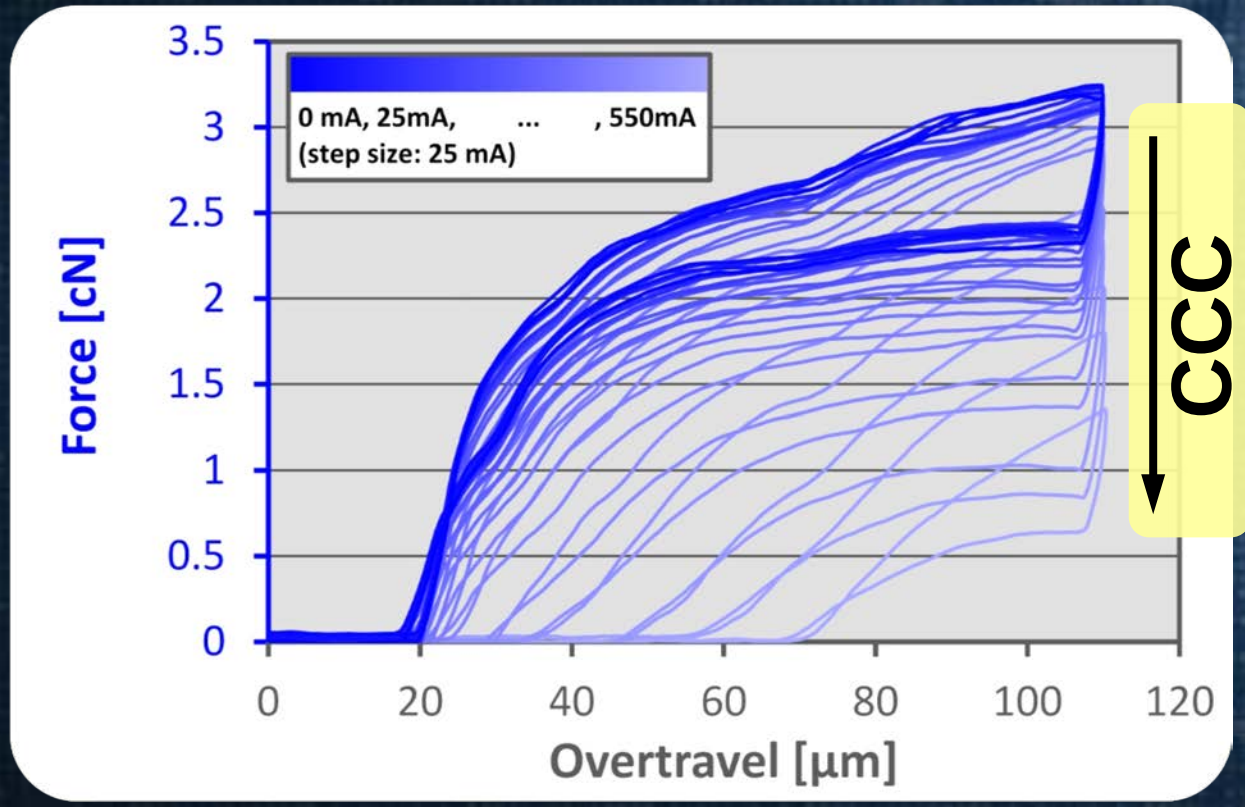
- **Better and More Comparable Method**

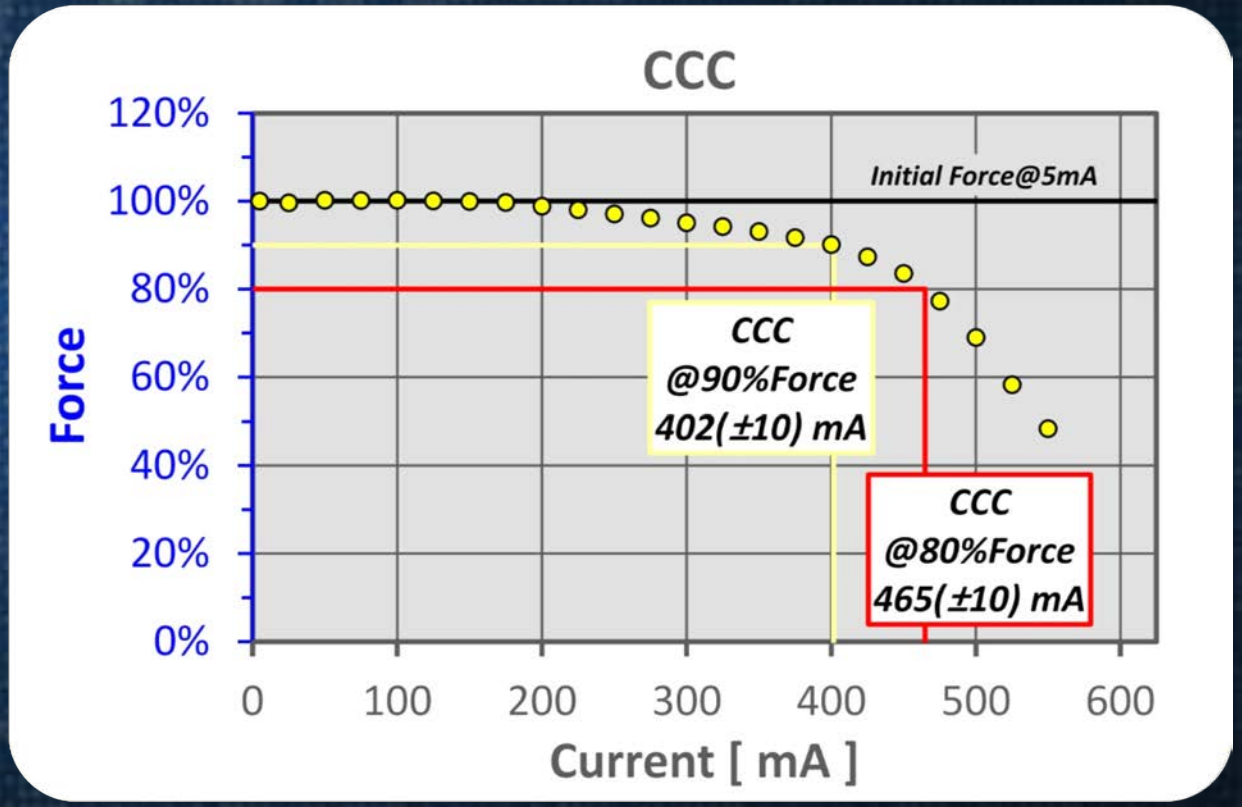




Methods

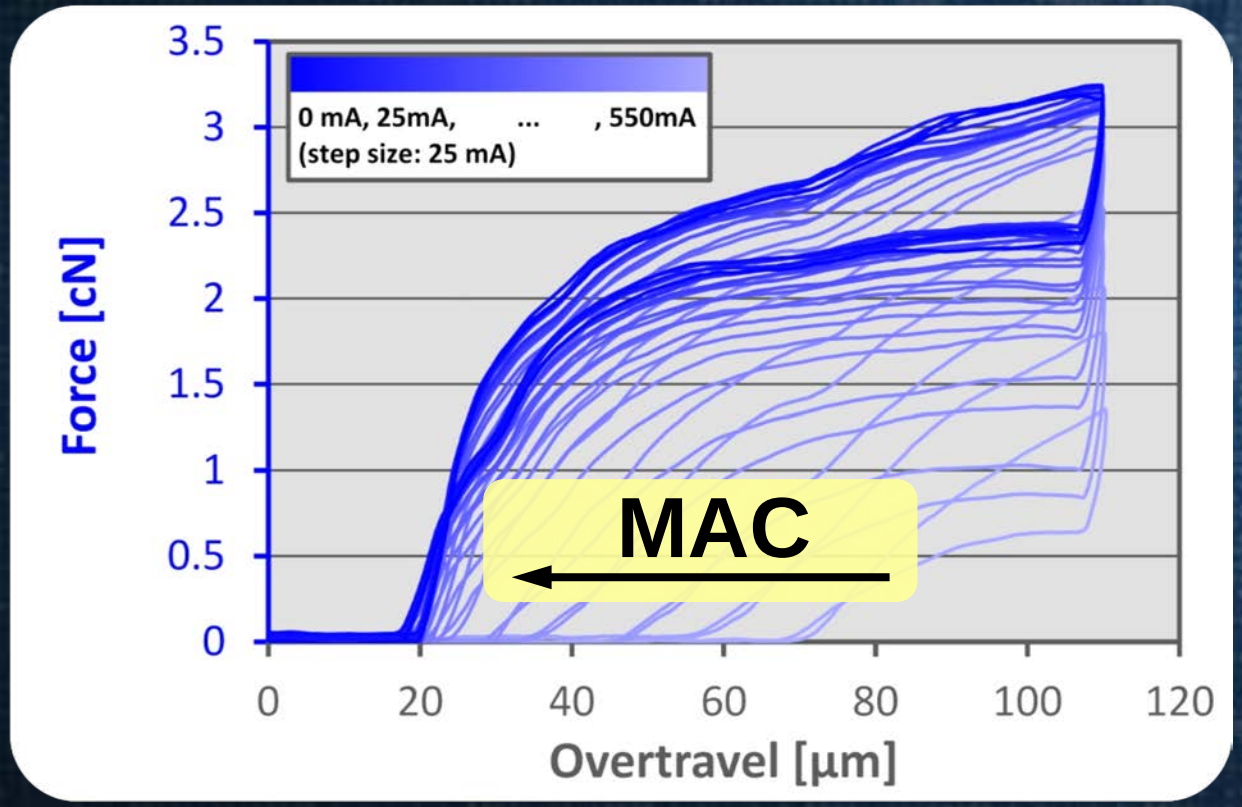
- **Better and More Comparable Method**

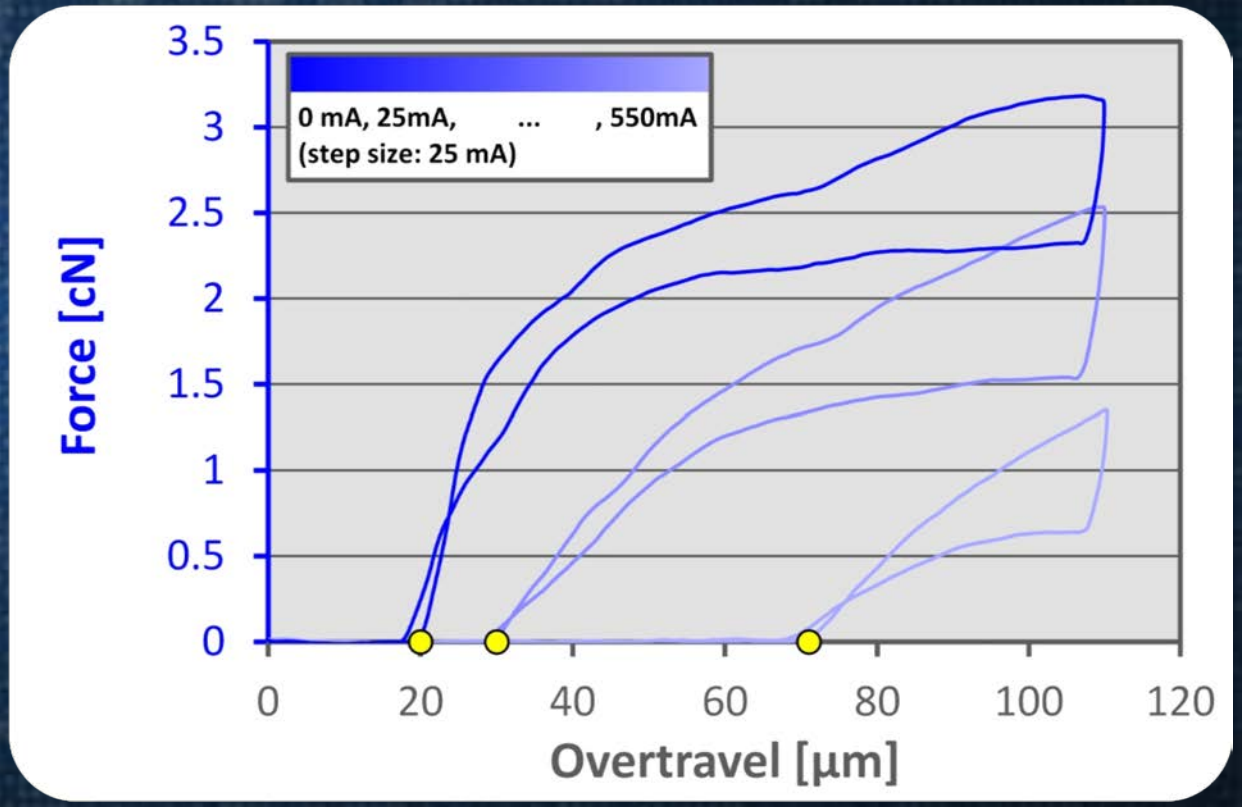




Methods

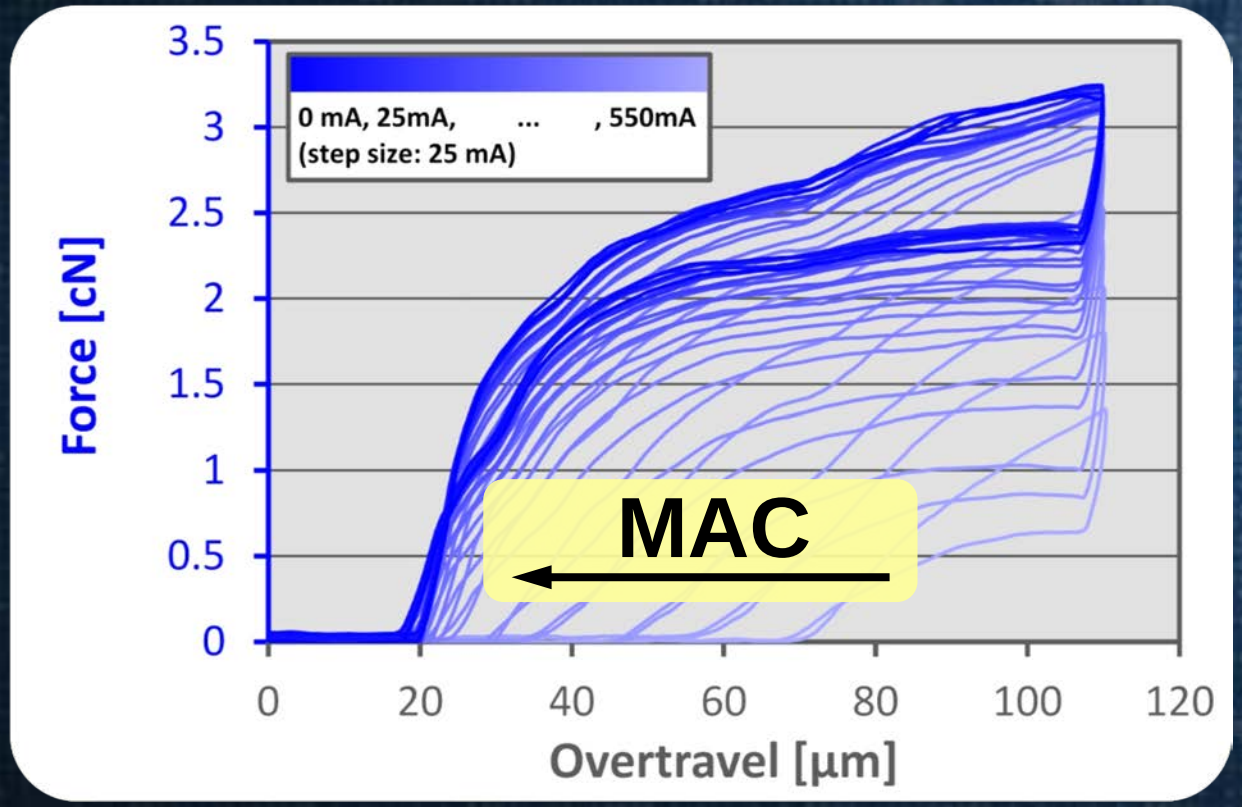
- **Better and More Comparable Method**

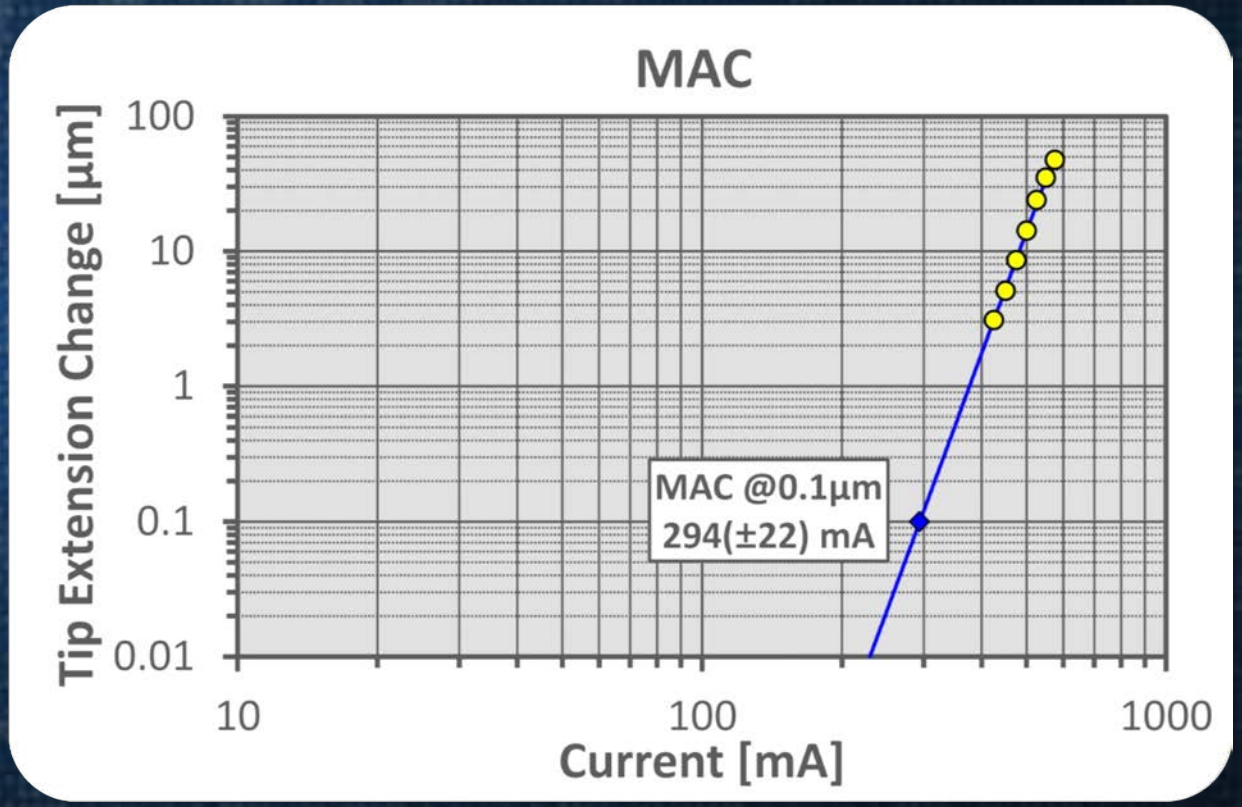




Methods

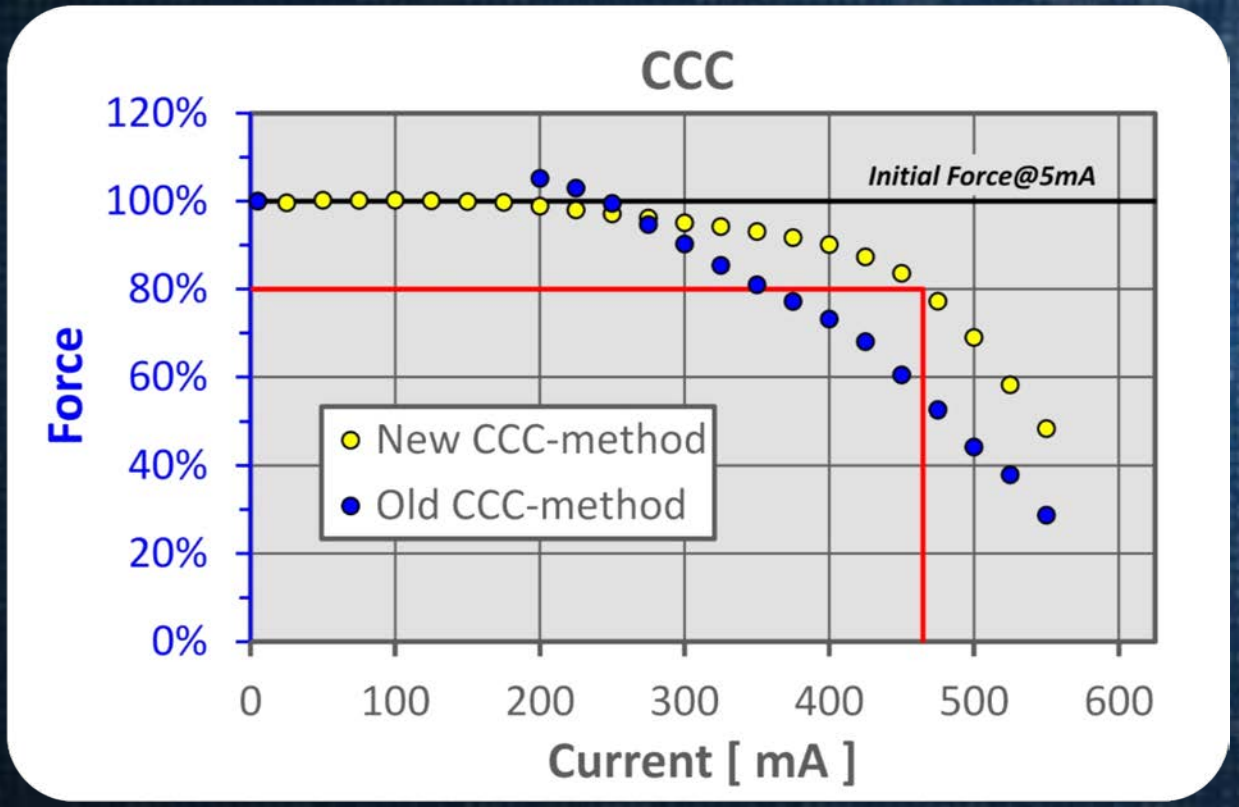
- **Better and More Comparable Method**





Results

- **Comparison: OLD vs. NEW Method**



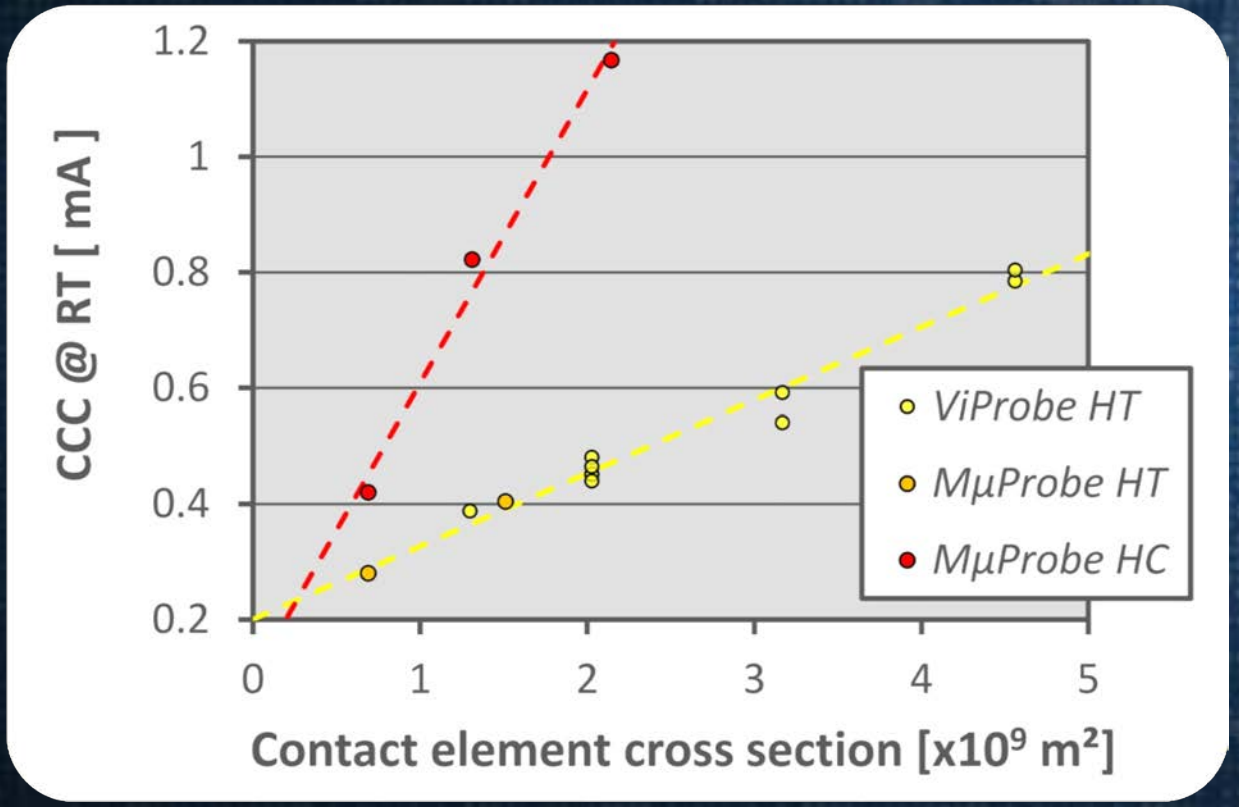
- *Higher CCC with new method*
- *Variance is much better*

(NEW: +/- 3% vs. OLD: +/- 10%)

➔ ***FORCE COMPARISON** is much more reliable*

Results

- **ViProbe & MµProbe**



CCC values correlate very well with the contact element cross-section

➔ ***Comparison of 2 different materials***
High temperature
Vs.
High Current

Conclusion

- **CCC (ISMI 2009)**

➔Vertical Probe Cards

➔ Comparison of not comparable forces

- **New method presented:**
  - CCC
  - MAC

➔Forces are comparable and more stable

Follow-On Work

- Pulsed Current Carrying Capability (PCCC)
- Numerical / Analytical Model (CCC and PCCC)
- Comparison CCC / PCCC with Real Environment Experiments

Acknowledgement

Thank you!

Lutz Benedix FEINMETALL GmbH	-	Head Design
Birgit Walloch FEINMETALL GmbH	-	Head & Probe Assembly, Mechanical Reliability Tests
Daniel Malitius FEINMETALL GmbH	-	Head & Probe Assembly, Mechanical Reliability Tests
Steffen Beutler FEINMETALL GmbH	-	Force & CCC Measurements

SW Test Workshop
Semiconductor Wafer Test Workshop

Advances in MEMS Spring Probe Technology for Wafer Test Applications

Author & Presenter, Koji Ogiwara
Nidec SV TCL – Tokyo, Japan
Co-Author, Norihiro Ohta
Nidec-Read Corporation – Kyoto, Japan

June 3-6, 2018

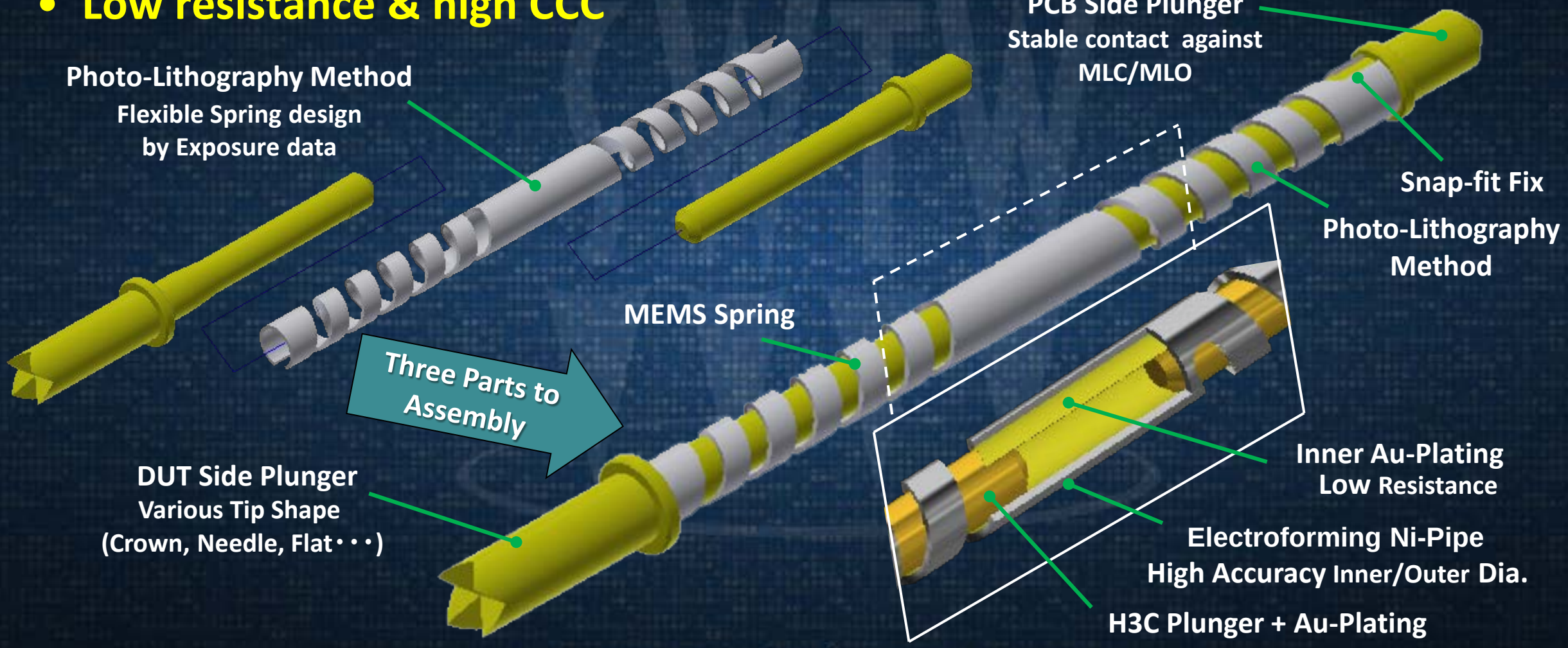
Overview

- Why is it called “MEMS” Spring Probe
- MEMS Spring Probe Card
- Design Feasibility/Customization
- Specification
- Road Map
- Summary

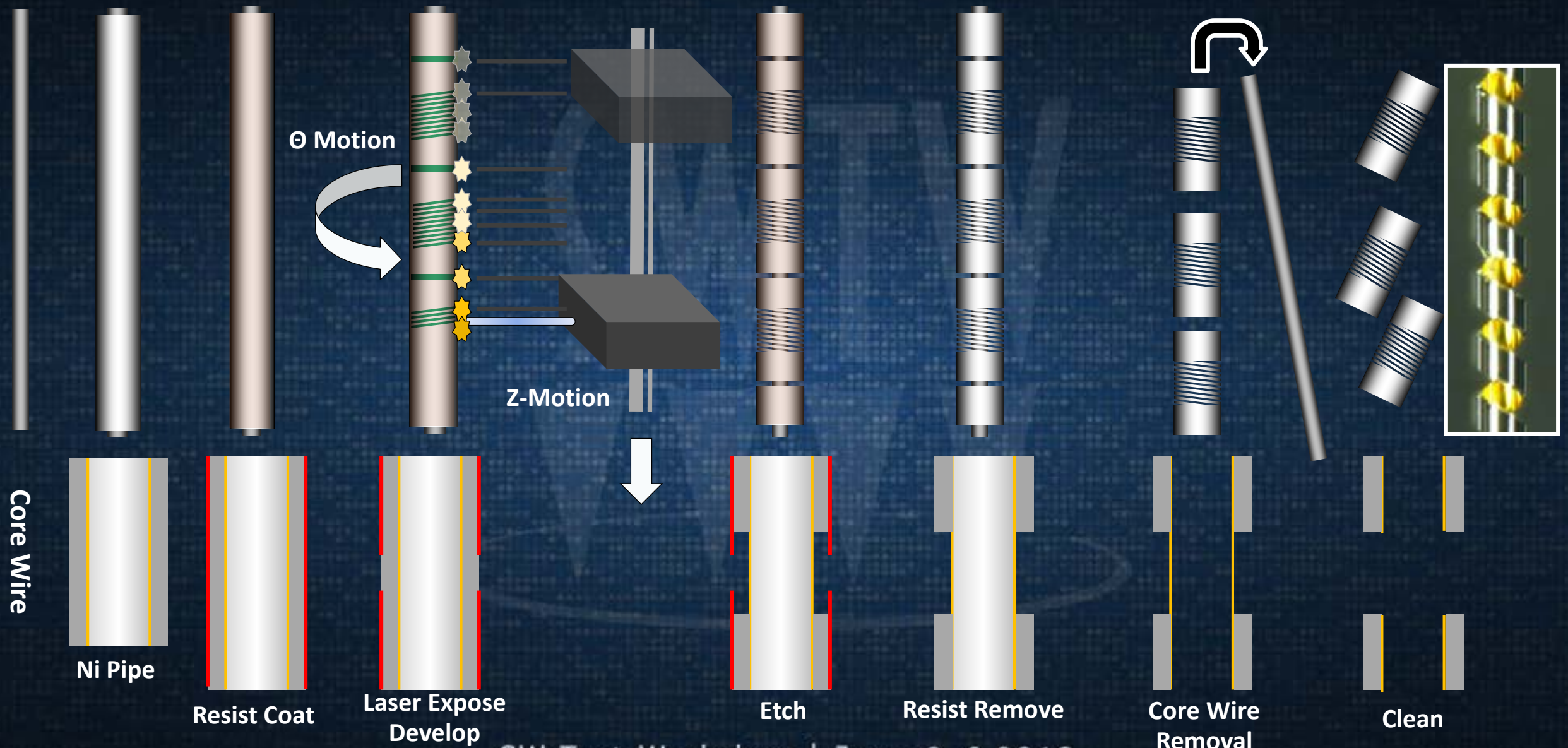
Why is it called "MEMS" Spring Probe?

MEMS Spring Pin Probe Definition

- Simple structure with spring & two snap-fixed plungers
- Low resistance & high CCC



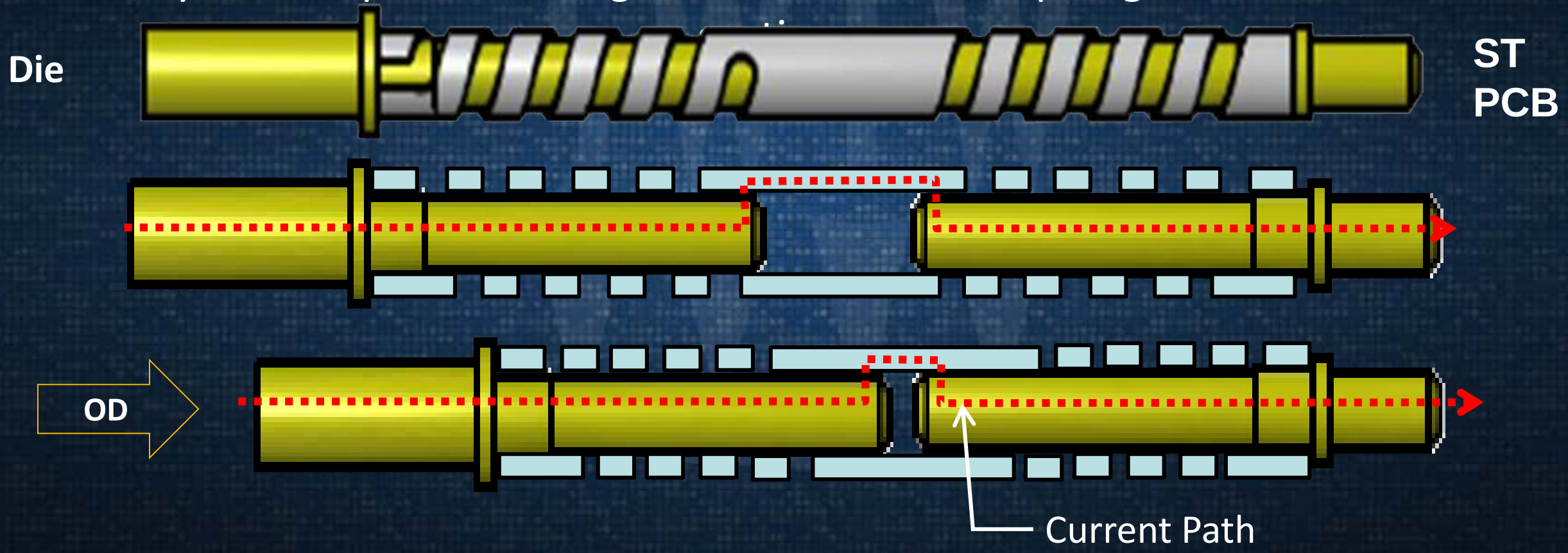
Manufacturing Process – Photolithography



Advanced Features

- **Current Path ･･･ Low Resistance & High CCC**

Primary current path is through the low-resistance plunger & center barrel.



MEMS Spring Probe Card

MEMS Spring Probe
MEMS Spring Probe Card

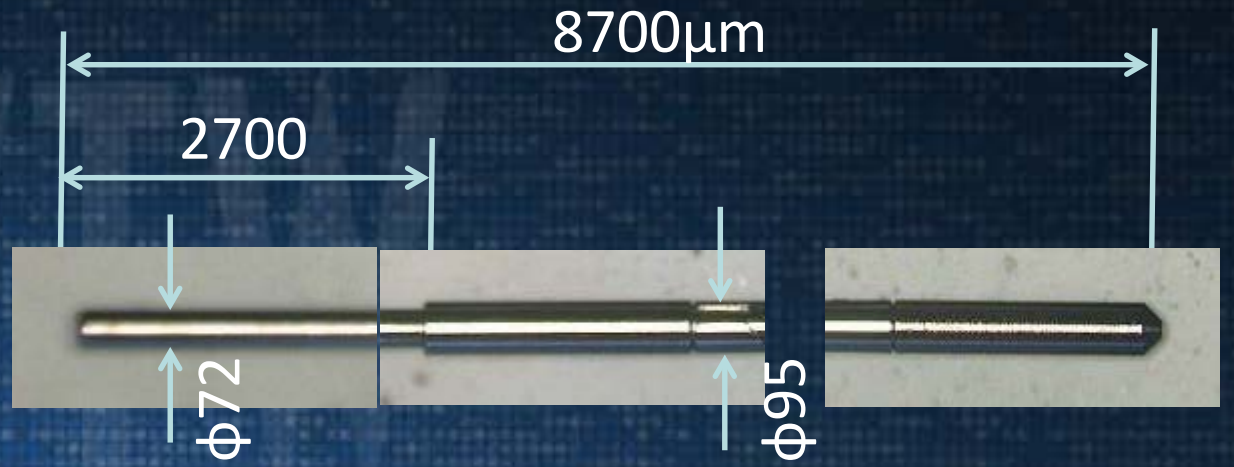
Introduce P147 MEMS Spring Probe

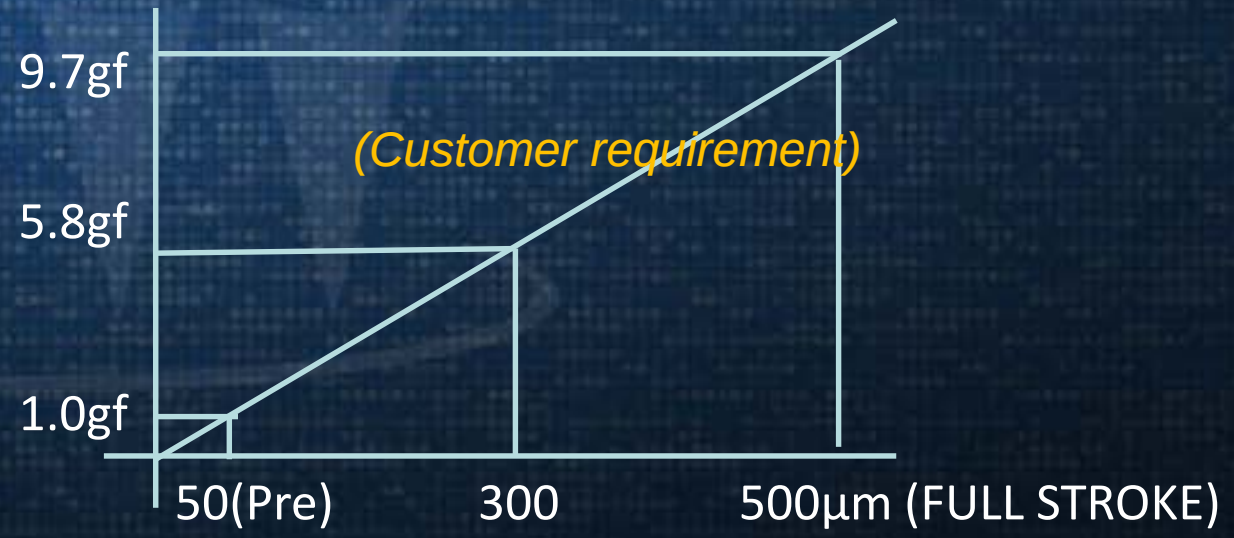
P147 MEMS Spring Probe Specifications

(Customer requirement)

Pitch	147µm
Probe Diameter	ϕ72µm
Probe tip	Flat
Contact Force	5.8gf@300µm OD
Preload	1gf
Max OP OD	350µm *
Max OD	450µm *

* Wider OD range than Conventional Spring probe





P147 MEMS Spring Probe Performance - Contact Force/OD

Graph Indicates

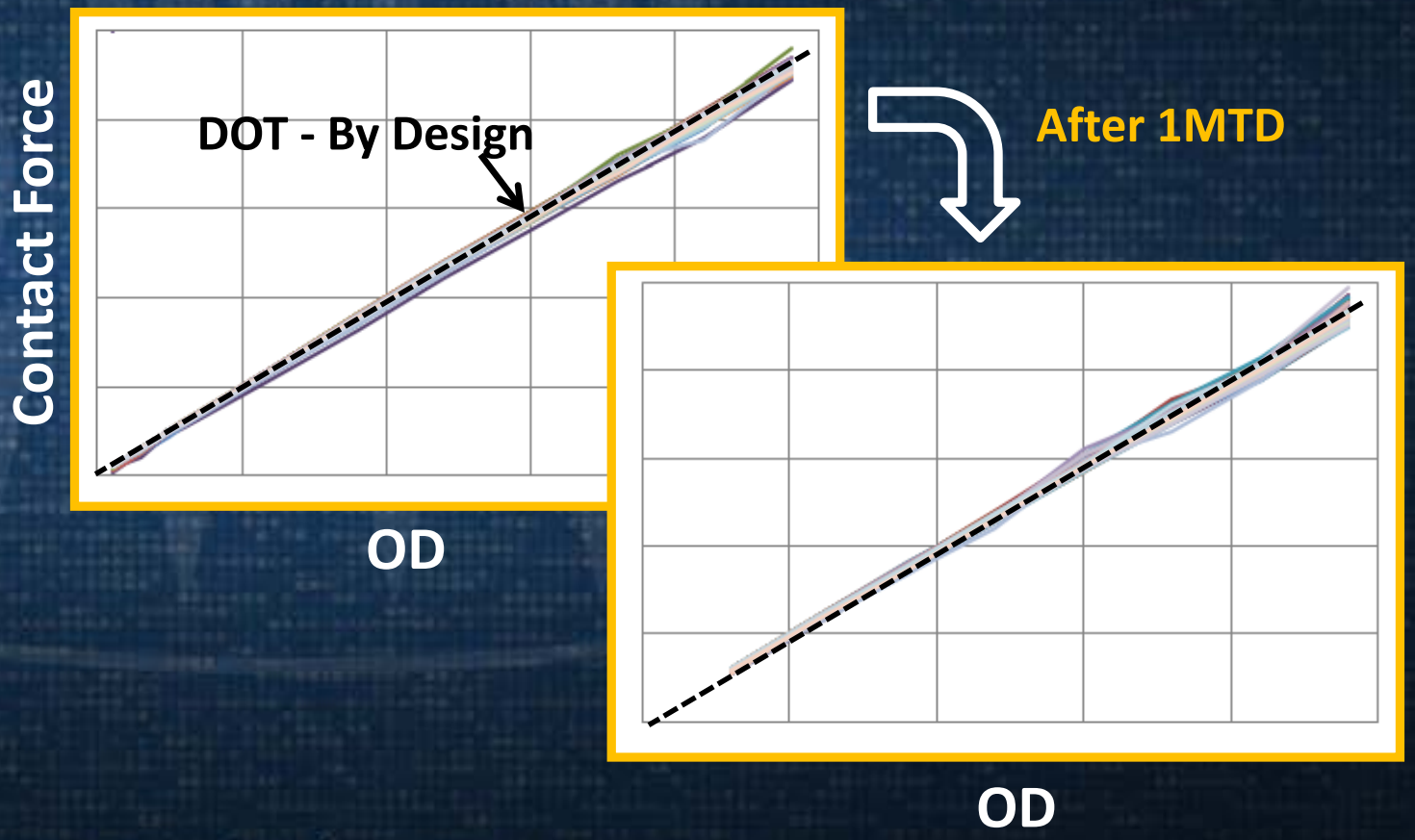
1. Contact Force/OD

Test Condition

- Before/after 1MTD (HT +125℃)
- Change OD from ZERO to 400µm
- N=100
- Room temp

Result

a. Very little Contact Force Variation
b. Right on Design SPEC
c. No Degradation after 1MTD



Additional Sample

P200 MEMS Spring Probe vs. Conventional

Graph Indicates

1. MEMS Spring Probe CF/OD
2. Conventional Spring Probe CF/OD

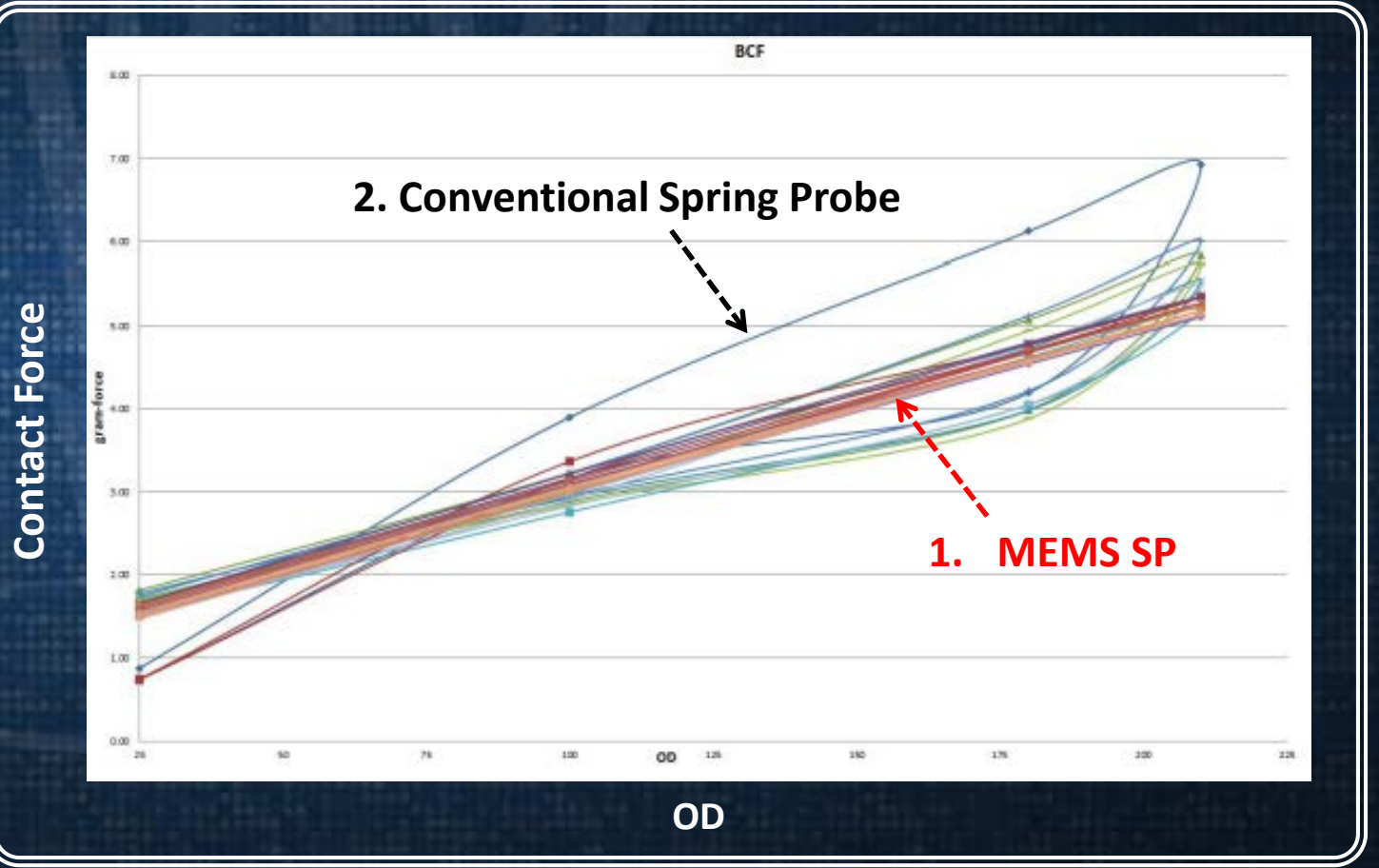
Test Condition

- Change OD from ZERO to 400µm
- Then back to ZERO
- N=7
- Room temp

Result

a. MEMS Spring Probe CF right on design & no variation (even after 130°C24Hrs)

b. Conventional Spring Probe CF more variation



P147 MEMS Spring Probe Performance - CCC

Graph Indicates

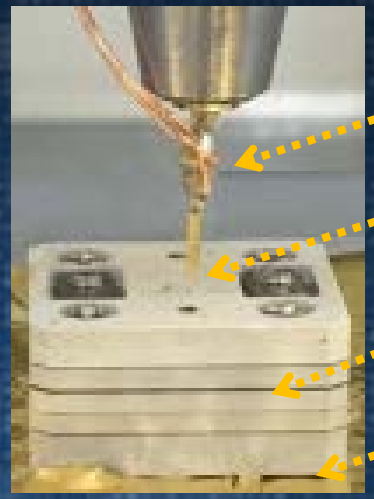
1. Contact Force(%)/Current (mA)

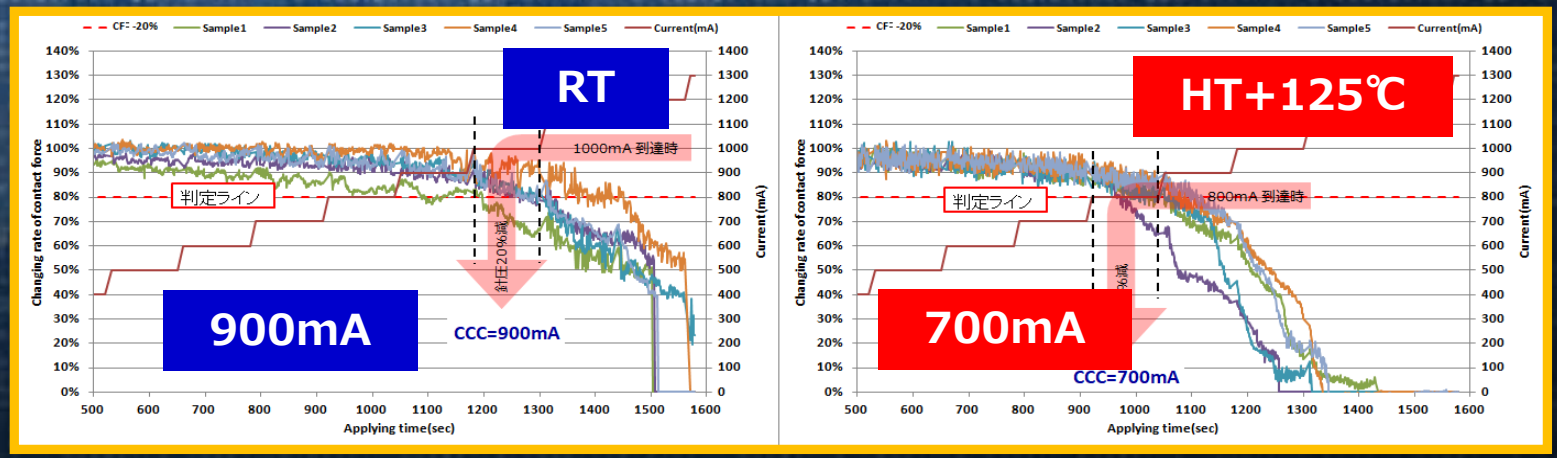
Test Condition

- ISMI STD
- N=5
- Same PH design of probe card
- OD400µm
- RT & HT +125℃

Result

a. Took the worst of five samples
b. RT 900mA
c. HT +125℃ 700mA



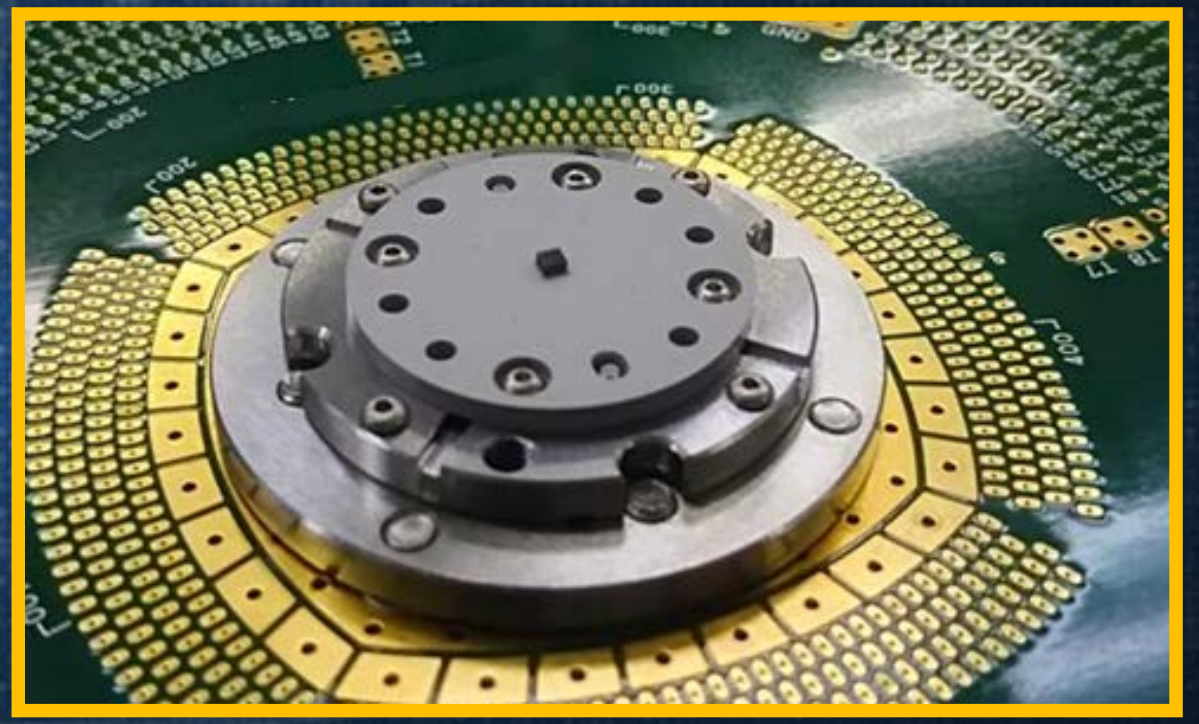


MEMS Spring Probe Card Test Vehicle + P147 MEMS Spring Probe

Test Vehicle Specifications

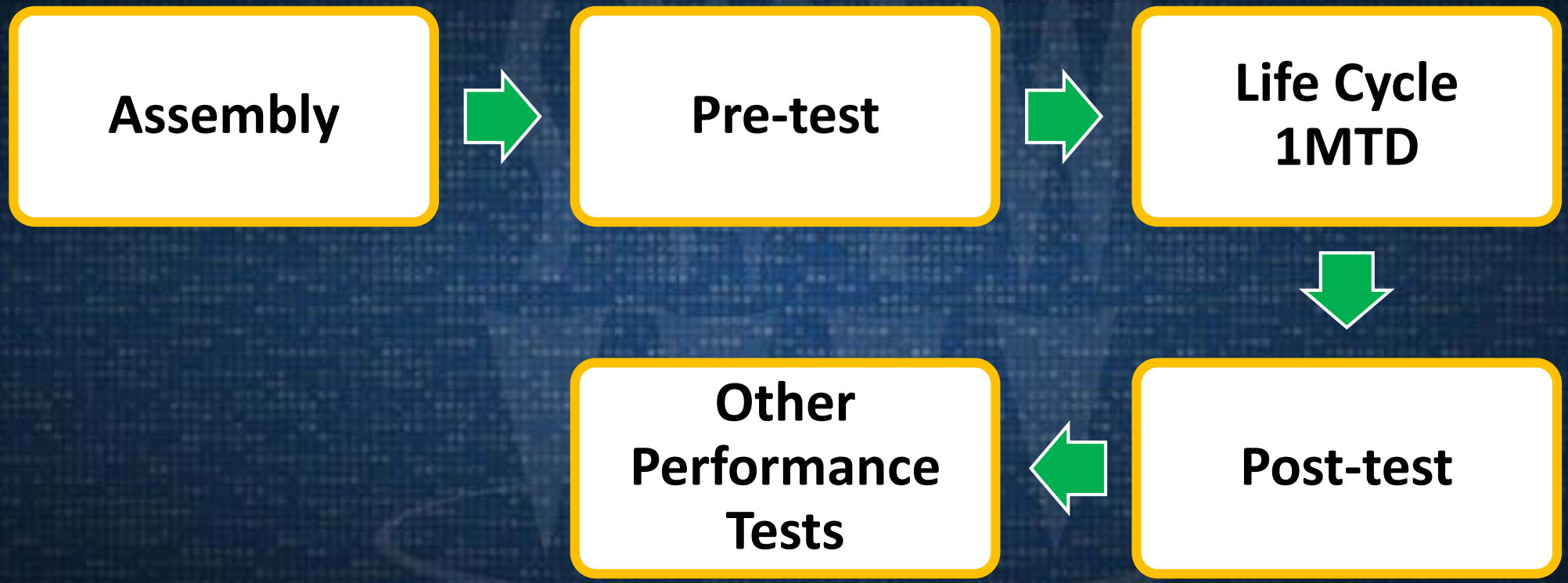
(To evaluate the card performance under Customer requirement)

Pitch	147µm
Probe Diameter	ϕ72µm
Probe tip	Flat
Contact Force	6.8gf@300µm OD
Preload	1gf
Max OP OD	350µm *
Max OD	450µm *
# of Probes	100



* Wider OD range than Conventional Spring probe

MEMS Spring Probe Card Evaluation Flow



MEMS Spring Probe Card Evaluation Parameter

		Key Parameter	Evaluation Parameter	Result
MEMS Spring Probe Card	Pre/Post 1MTD Life Cycle	Probe Position	XY Accuracy	GOOD
			Planarity	GOOD
		Contact Resistance (Single-TD)	CRES/OD	GOOD
			CRES/500TD	GOOD
		Contact Resistance (Multi-TD)	CRES/Multi-TD	GOOD
		Probe Mark	Mark on Bump	GOOD
		Deformation	Tip Length, Barrel Length	GOOD
		Frequency, S21	Probe Only, Probe Card	GOOD
		Inductance	WLCSP 2.78mm long	GOOD

MEMS Spring Probe Card Test Vehicle Performance – XY Position Accuracy

Graph Indicates

1. XY Position [After 1MTD Life cycle]
2. RT

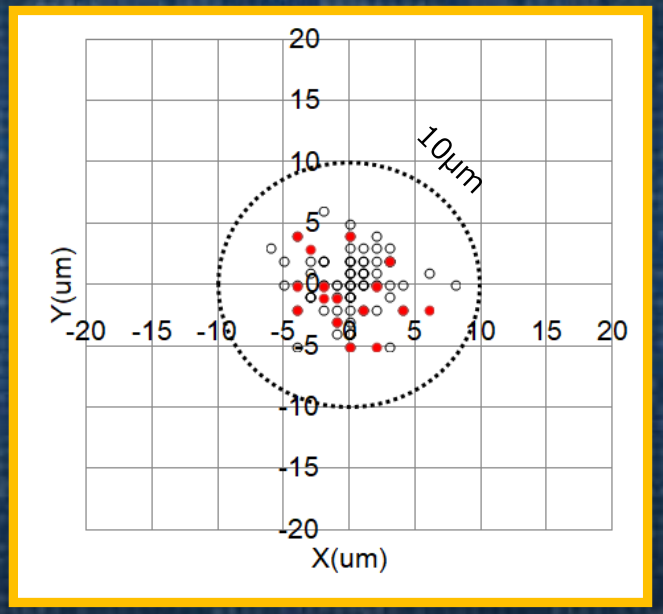
Test Condition

- Target < ±10µm
- N=100
- OD300µm
- IF = 50mA during 1MTD Life (N=20)
- Before/After 1MTD. Show only after 1MTD

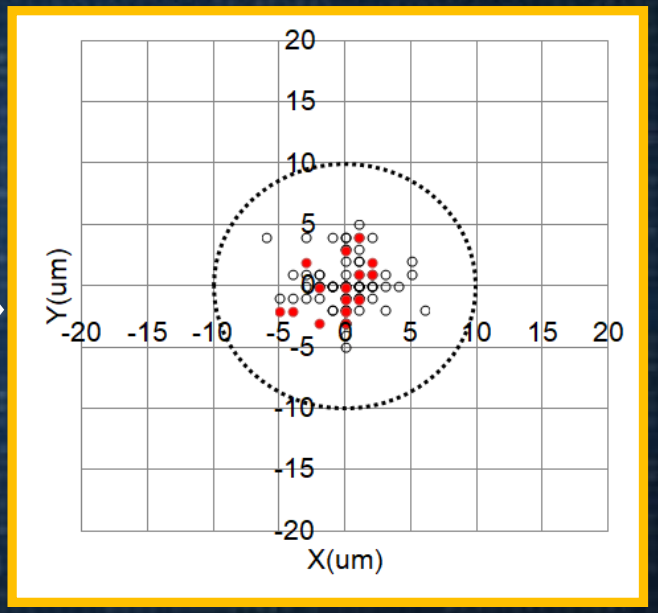
Result

a. Below the target
b. No degradation after 1MTD
c. No difference with IF=50mA

Pre-test



Post-test (1MTD)



● : IF=50mA during Life Cycle

○ : No force current

MEMS Spring Probe Card Test Vehicle Performance – Planarity

Graph Indicates

1. XY Position [After 1MTD Life cycle]
2. RT

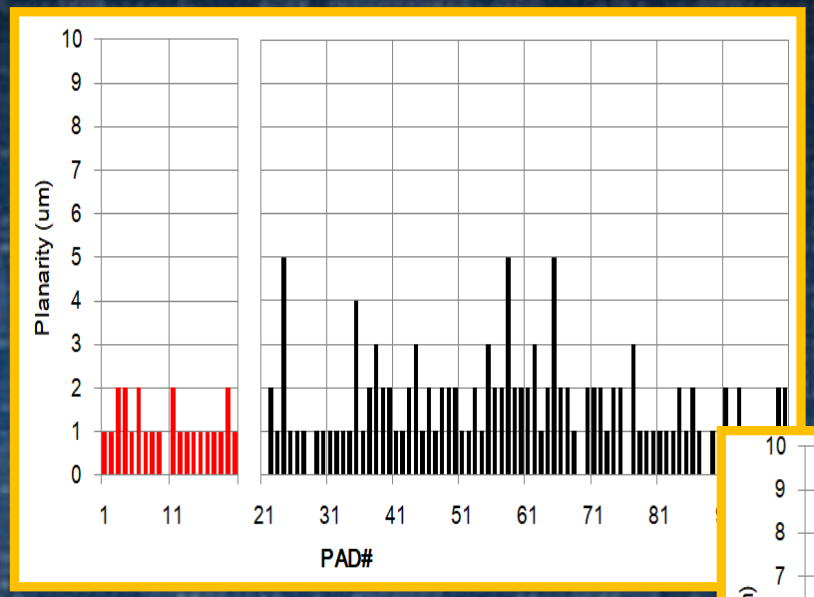
Test Condition

- Target < 20µm
- N=100
- OD300µm
- IF = 50mA during 1MTD Life (N=20)
- Before/After 1MTD. Show only after 1MTD

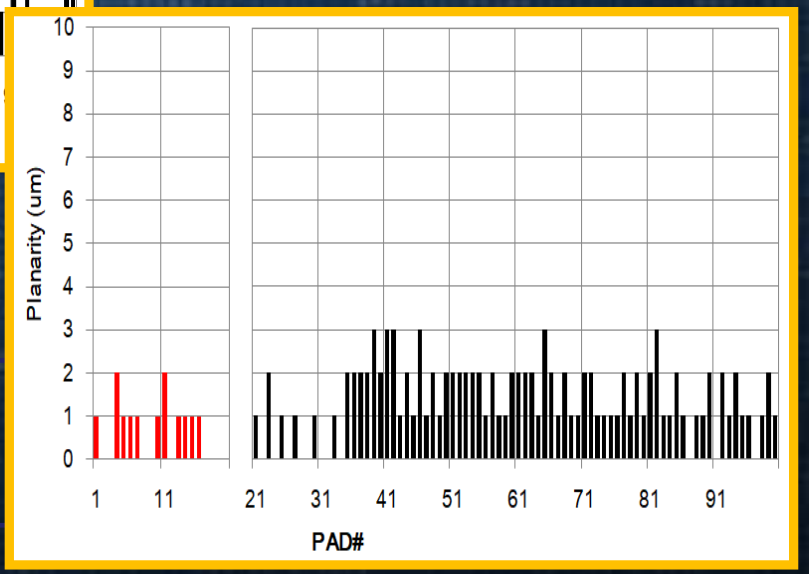
Result

a. Below the Target
b. No Degradation after 1MTD
c. No Difference with IF=50mA

Pre-test



Post-test (1MTD)



● : IF=50mA during Life Cycle

○ : No Force Current

MEMS Spring Probe Card Test Vehicle Performance – CRES Bump Contact/OD

Graph indicates

1. CRES/OD [After 1MTD Life cycle]
2. Tri-Temp (RT, LT -40℃, HT +125℃)

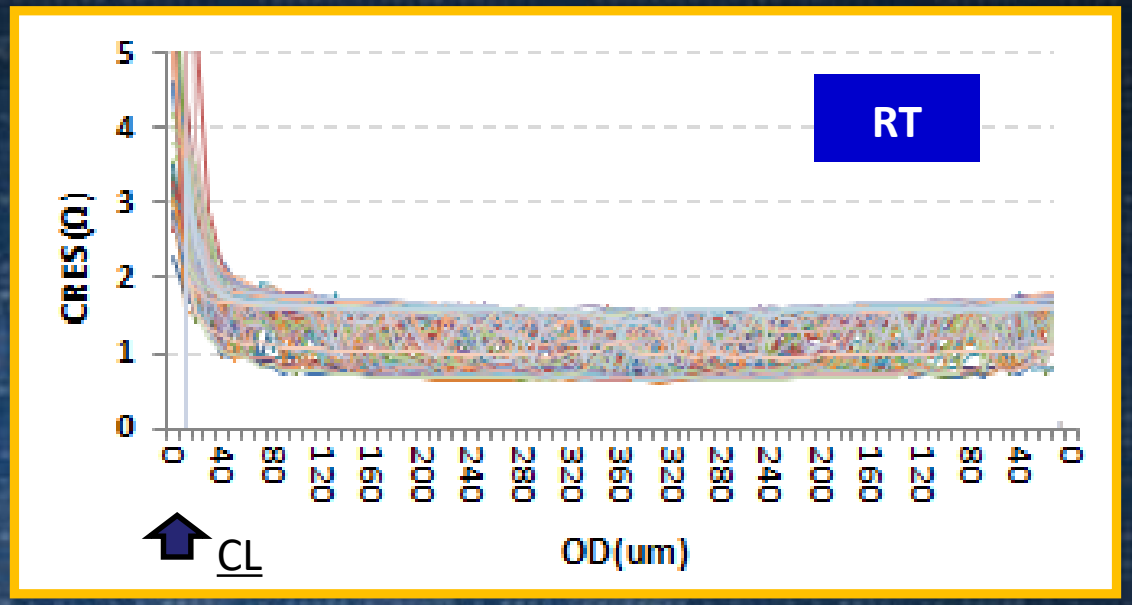
Test Condition

- Target CRES < 2 Ohms
- N=70
- Online Cleaning only before START
- IF = 50mA
- Before/After 1MTD. Show only after 1MTD

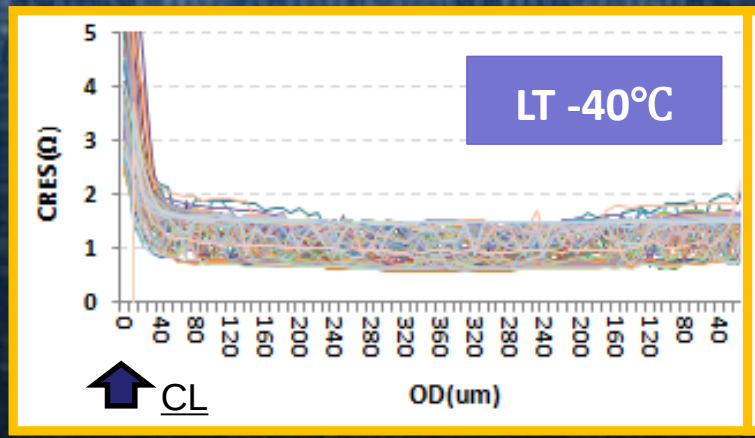
Result

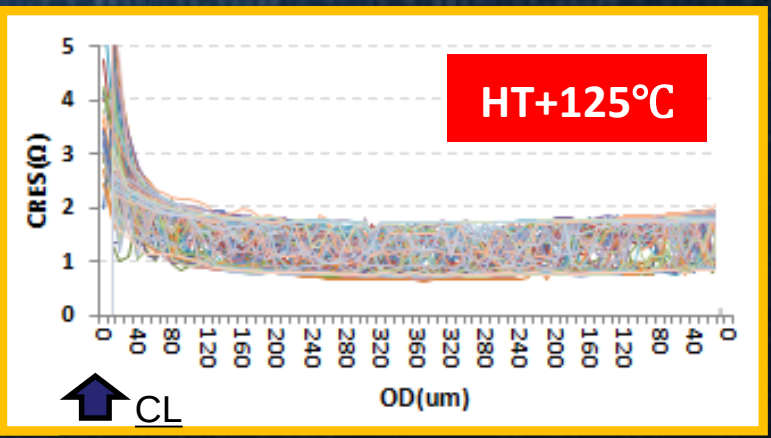
a. Below the target CRES @OD80µm

b. No degradation after 1MTD



Show "after 1MTD" Only





MEMS Spring Probe Card Test Vehicle Performance – CRES Bump Contact/500TD

Graph Indicates

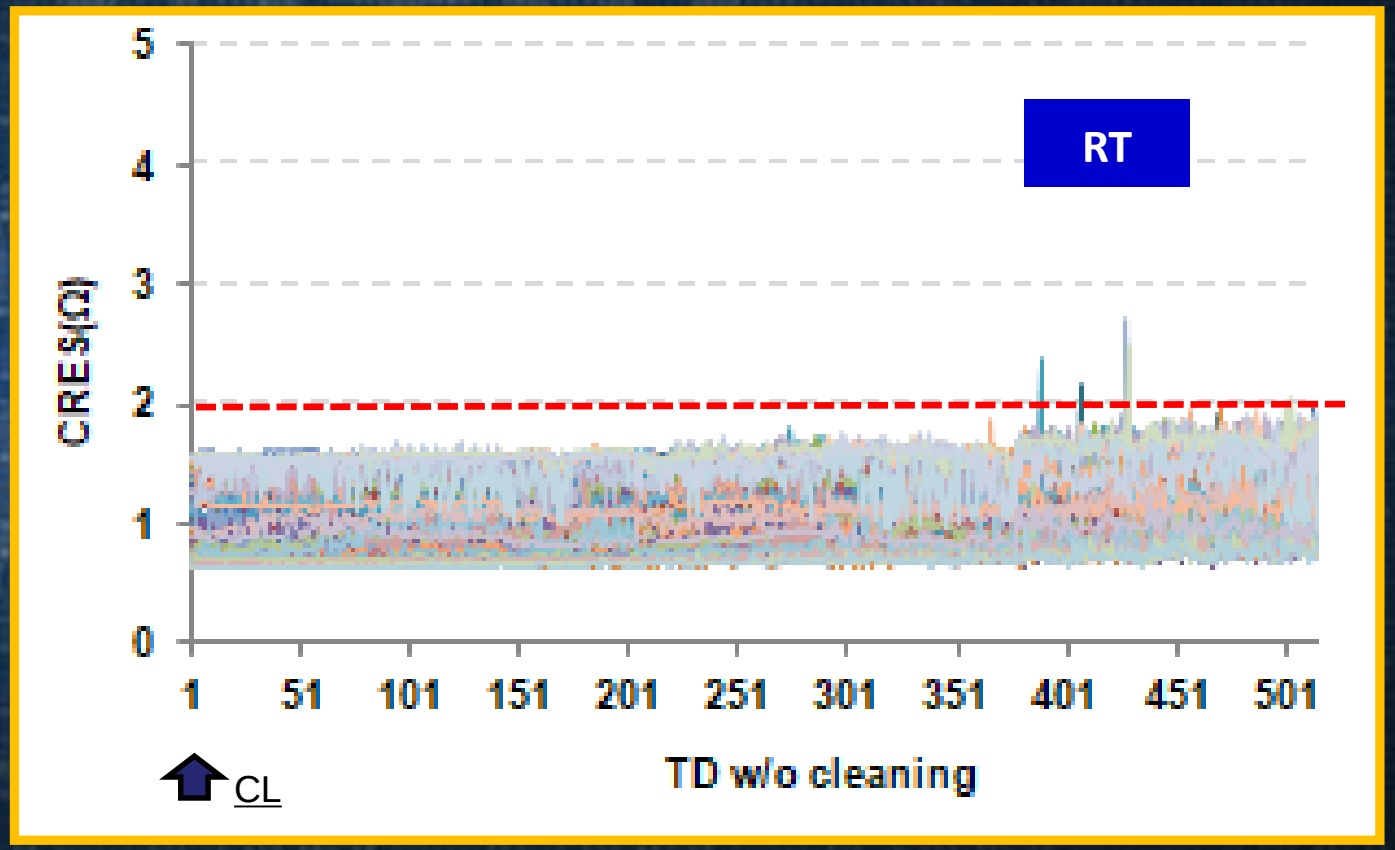
1. CRES/500TD [After 1MTD Life cycle]
2. RT

Test Condition

- Target CRES < 2 Ohms
- N=70
- Online Cleaning only before START
- OD300µm
- IF = 50mA
- Before/After 1MTD. Show only after 1MTD

Result

a. Below the target above 350TD@RT



Show "after 1MTD" Only

MEMS Spring Probe Card Test Vehicle Performance – CRES Bump Contact/500TD

Graph Indicates

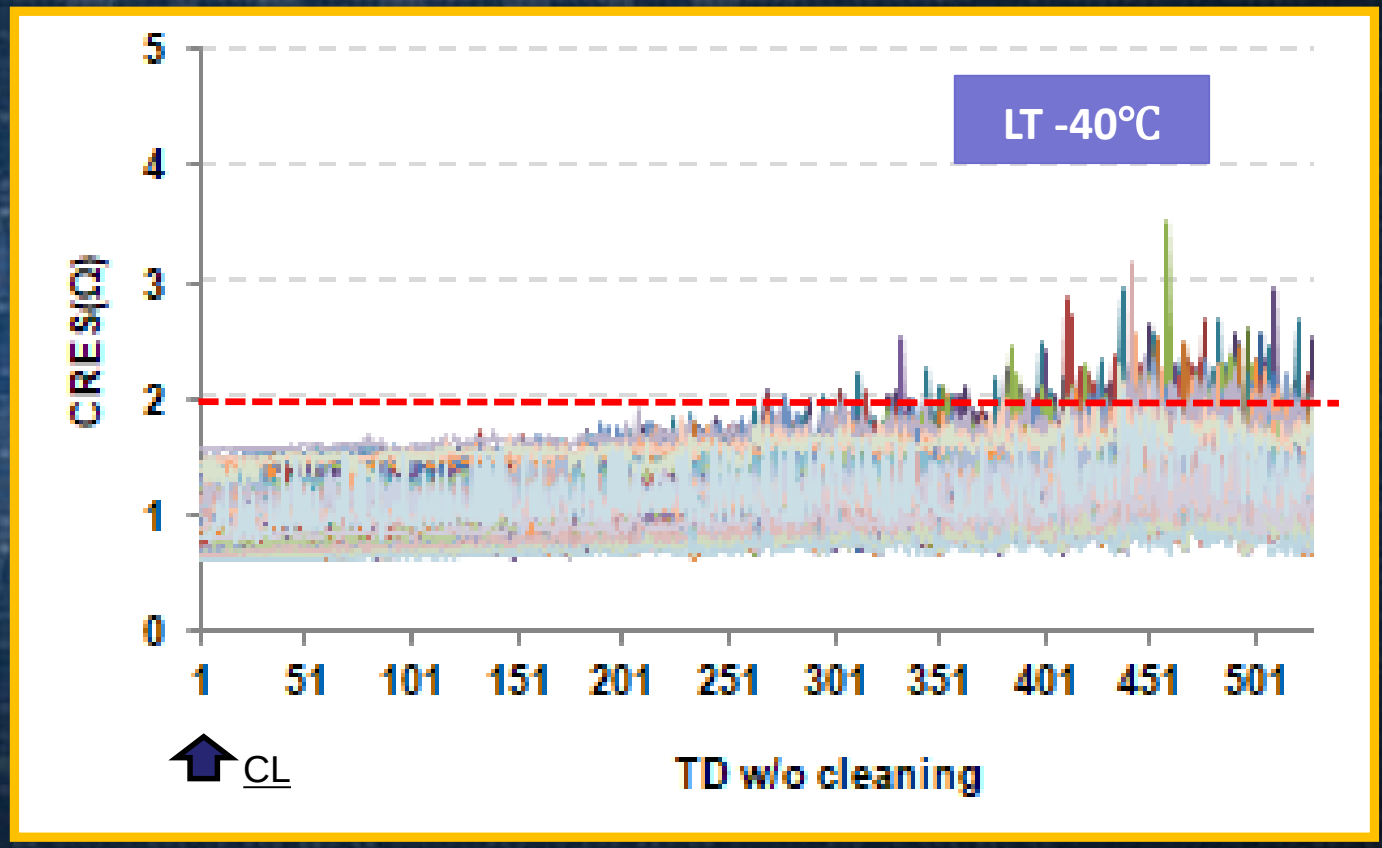
1. CRES/500TD [After 1MTD Life Cycle]
2. LT -40°C

Test Condition

- Target CRES < 2 Ohms
- N=70
- Online Cleaning only before START
- OD300µm
- IF = 50mA
- Before/After 1MTD. Show only after 1MTD

Result

a. Below the target until 300TD@LT



Show "after 1MTD" Only

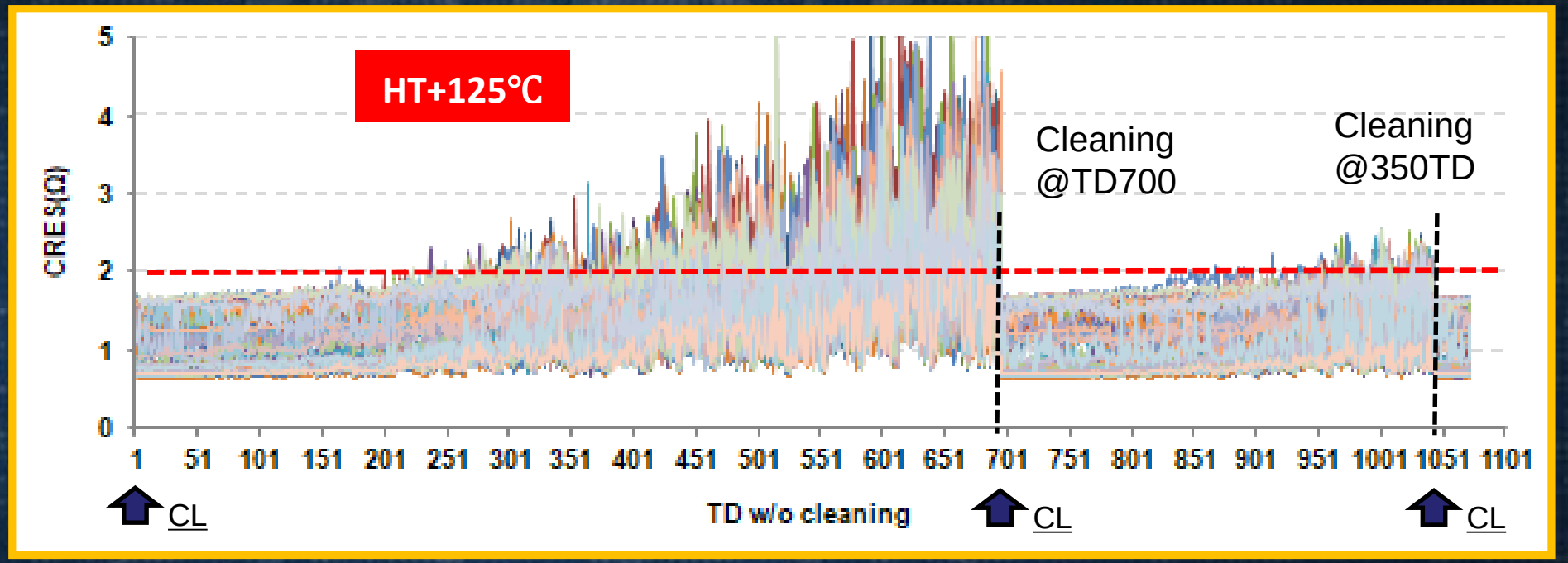
MEMS Spring Probe Card Test Vehicle Performance – CRES Bump Contact/500TD

Graph Indicates

1. CRES/1000TD [After 1MTD Life cycle]
2. HT +125℃

Test Condition

- Target CRES < 2 Ohms
- N=70
- Online Cleaning only before START
- OD300µm
- IF = 50mA
- Before/After 1MTD. Show only after 1MTD



Result

a. Below the target until 200TD@HT
b. CRES performance stabilizes after Cleaning

Show "after 1MTD" Only

MEMS Spring Probe Card Test Vehicle Performance – CRES Bump Contact/Multi-TD

Graph Indicates

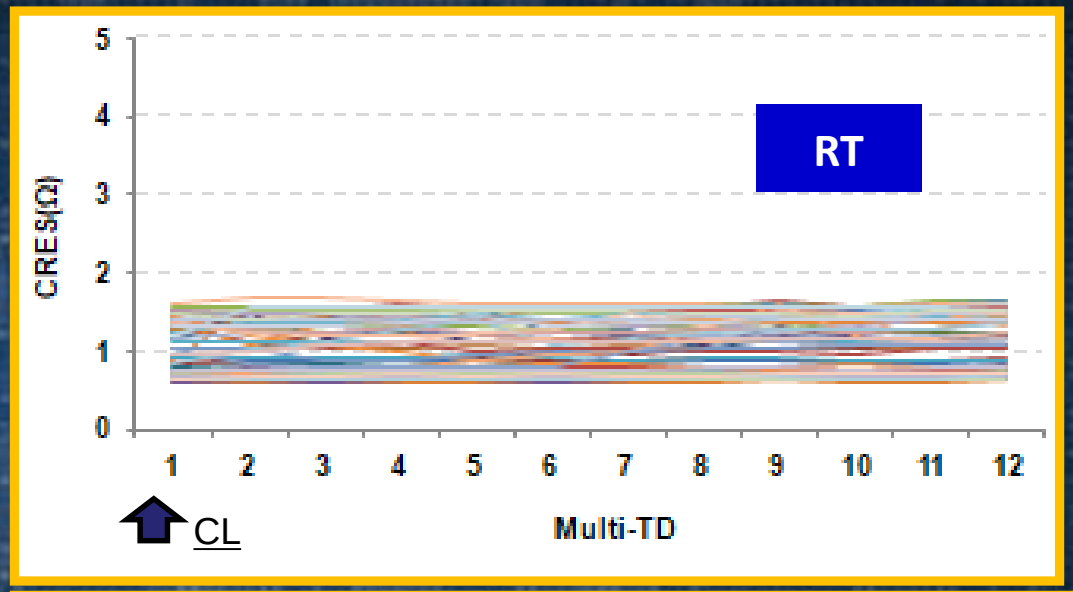
1. CRES/12TD on Same Bump
2. Tri-Temp

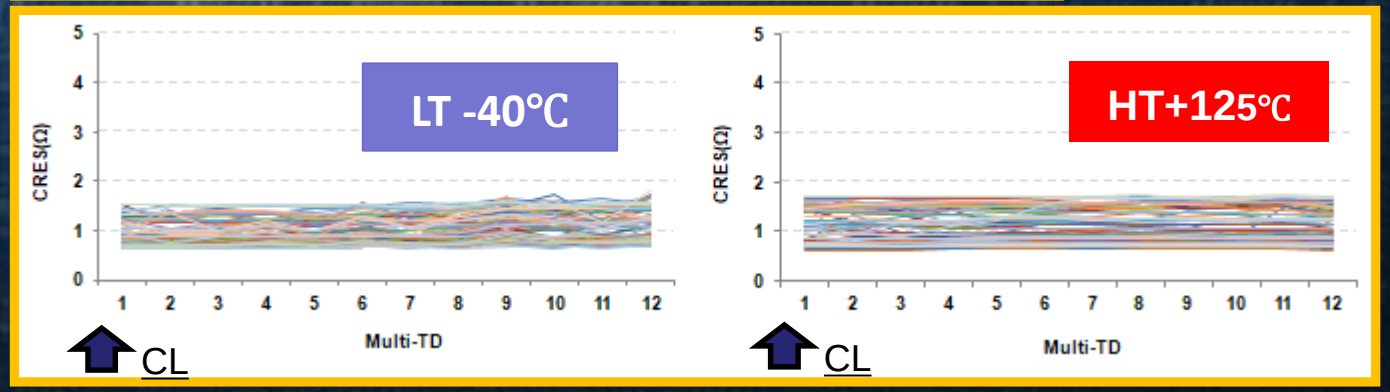
Test Condition

- Target CRES < 2 Ohms
- N=70
- Online Cleaning only before START
- OD300µm
- IF = 50mA

Result

a. CRES performance is stable below 2 Ohms even 12th TD





MEMS Spring Probe Card Test Vehicle
Performance – Probe Mark/Single -TD

Picture Indicates

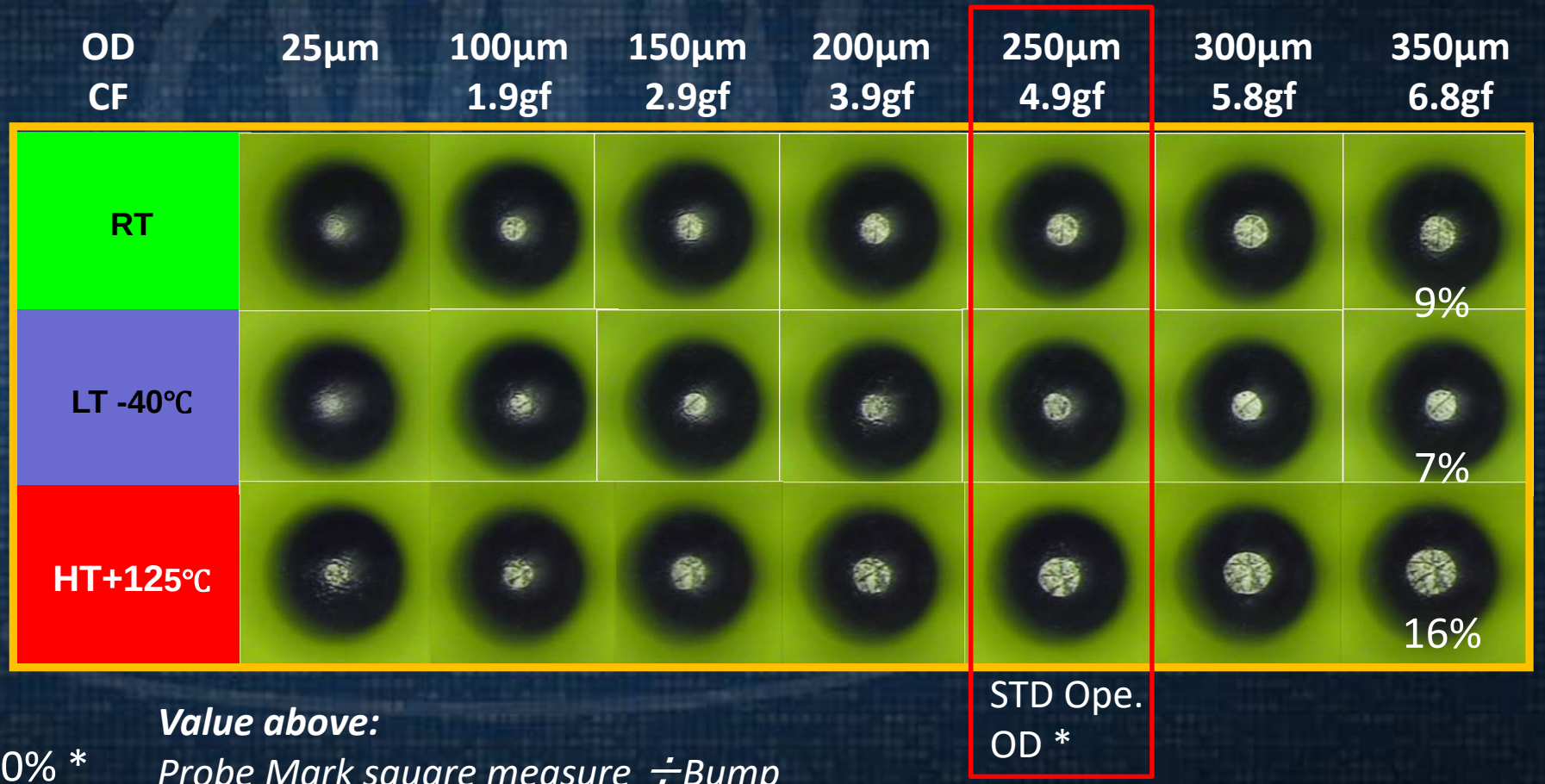
1. Probe Mark on Bump
2. Tri-Temp

Test Condition

- Target below 50% of Bump square size*
- Average values from N=5
- Single TD

Result

1. HT +125℃ showed worst
2. Even HT, Probe Mark 16% < 50% *
   (* Customer specification)



Value above:
Probe Mark square measure ÷Bump

MEMS Spring Probe Card Test Vehicle Performance – Probe Mark/Multi-TD

Picture Indicates

1. Probe Mark on Bump
2. Tri-Temp

Test Condition

- Target below 50% of Bump square size*
- Average values from N=5
- Multi-TD

Result

1. HT +125℃ showed worst
2. Even HT & TD 12 times, Probe Mark 18% < 50% *

(* Customer specification)



Value above:
Probe Mark square measure ÷Bump

MEMS Spring Probe Card Test Vehicle Performance – 1MTD Life Cycle, Barrel Spring Length

Test Condition

- 1MTD Life cycle (HT +125℃, OD 350µm)
- W/O Online Cleaning
- Average values from N=5

Result

1. Barrel length ▲13µm. Deformation per 1MTD under HT.
   Less than 2% of Barrel length. No impact to neither Contact force nor CRES performance (showed previous pages)



MEMS Spring Probe Card Test Vehicle
Performance – Frequency

Picture Indicates

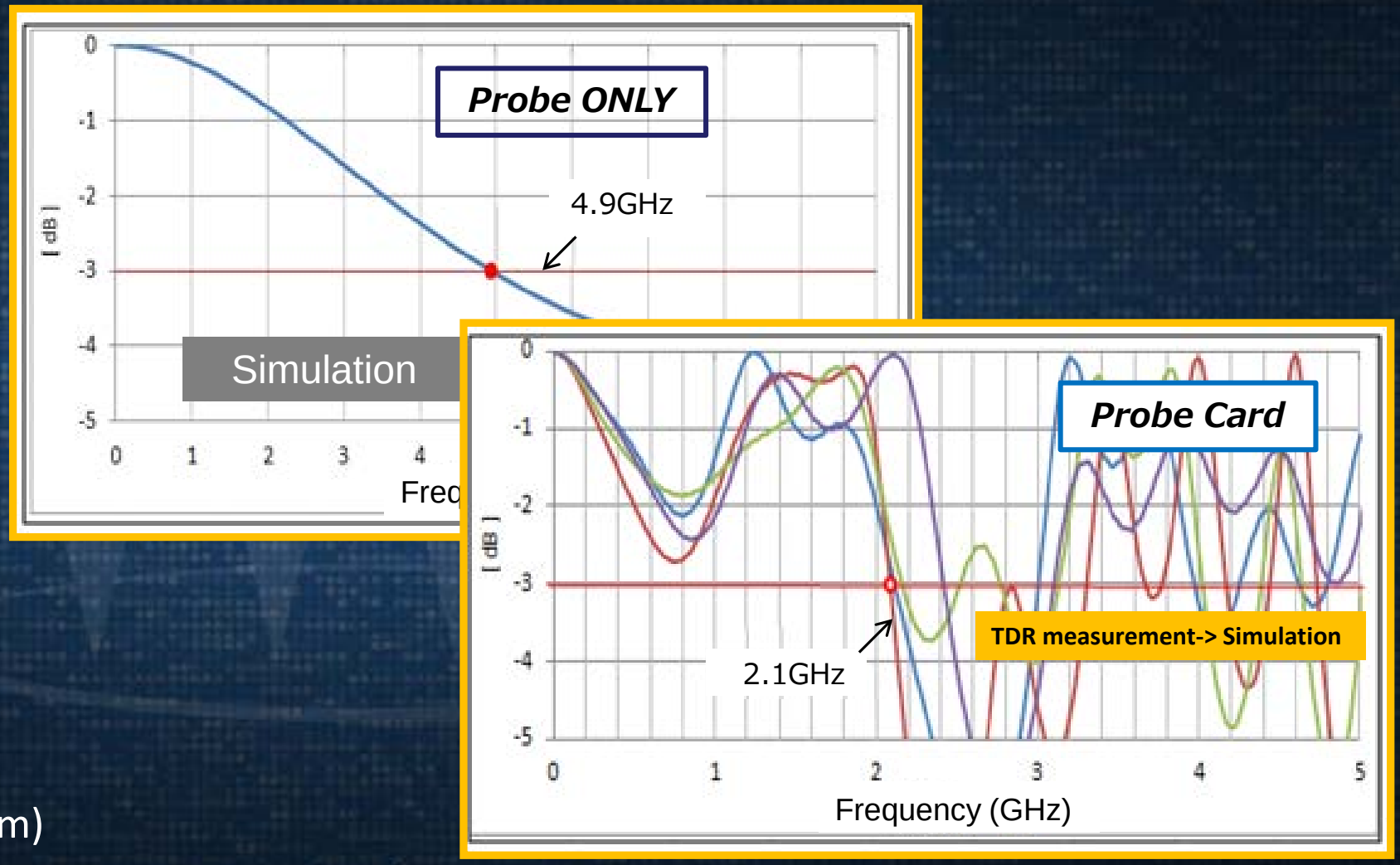
1. S21 Probe Only [Simulation]
2. S21 Probe Card/Wired type [Simulation based on TDR measurement]

Test Condition

- N=1 (Probe Only)
- N=4 (Probe Card)
- Read @-3db. 1/3 to convert to rectangle wave form,

Result

1. 1.6GHz, Probe Only
2. 700MHz, Probe Card (Wire 41mm)



Additional Sample
WLCSP Probe, Measure Inductance

Graph Indicates

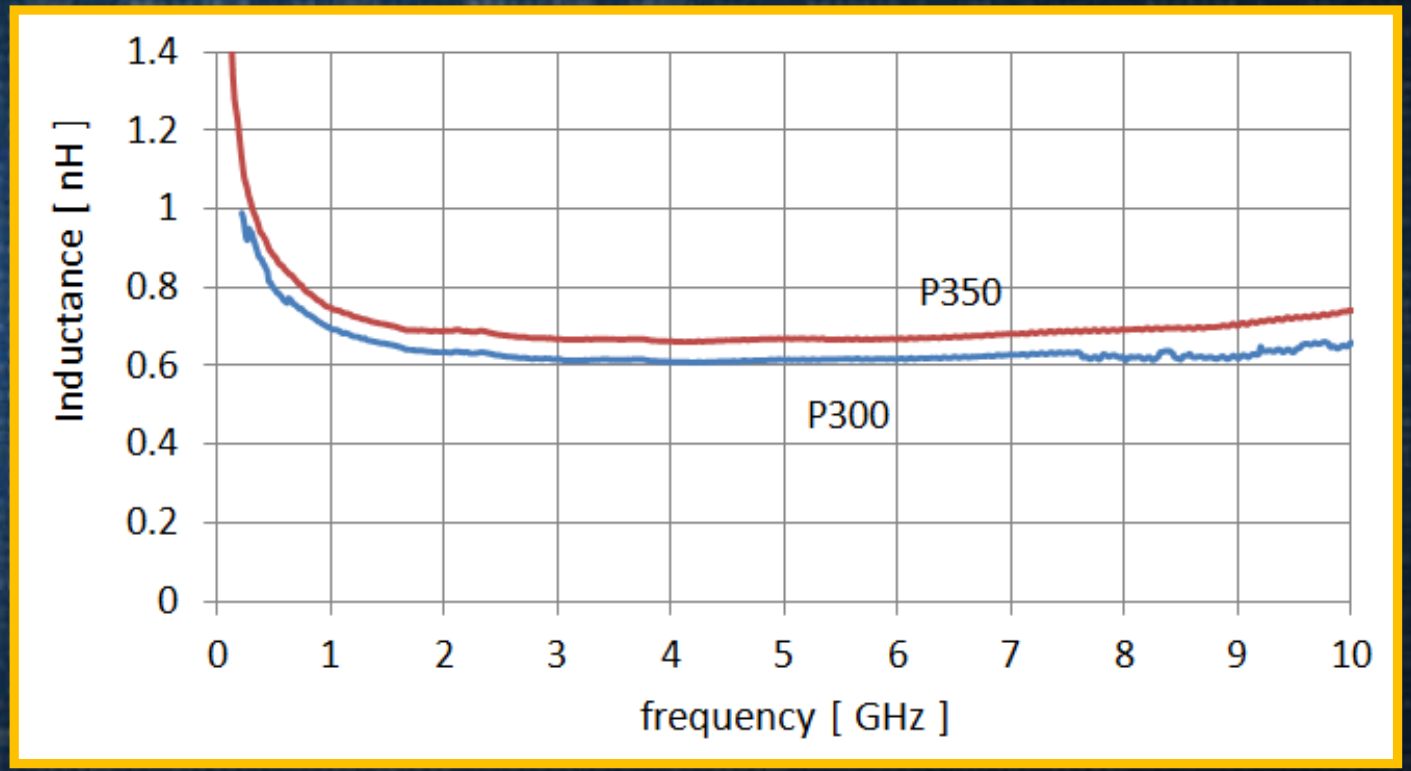
1. WLCSP Probe Inductance
   Φ235µm
   L =2.78mm

Test Condition

- G-S Measurement
- Pitch = 350µm, 300µm

Result

a. Inductance Measurement
   0.6nH/P300
   0.67nH/P350



achieve the required

MEMS Spring Probe Card Evaluation Result

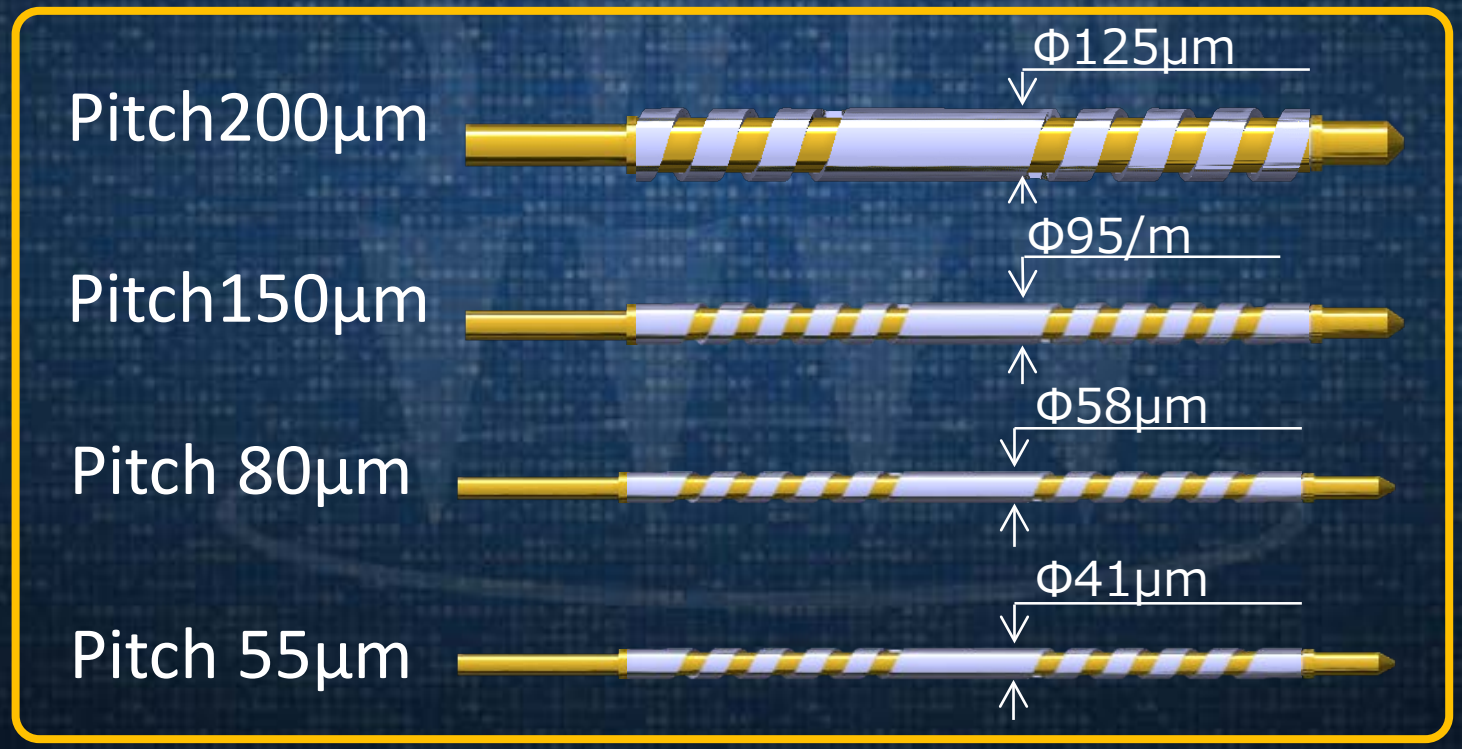
		Key Parameter	Evaluation Parameter	Result
MEMS Spring Probe Card	Pre/Post 1MTD Life Cycle	Probe Position	XY Accuracy	<±10µm, GOOD
			Planarity	<5µm, GOOD
		Contact Resistance (Single-TD)	CRES/OD	<2 Ohms, GOOD
			CRES/500TD	200TD@HT, GOOD
		Contact Resistance (Multi-TD)	CRES/Multi-TD	<2 Ohms@HT, GOOD
		Probe Mark	Mark on Bump	<18% (12TDs,HT), GOOD
		Deformation	Tip Length, Barrel Length	▲13µm Barrel L, GOOD
		Frequency, S21	Probe Only, Probe Card	Wired 700MHz , GOOD MLO/MLC TBD
		Inductance	WLCSP 2.5mm Probe	0.6nH L2.78mm, GOOD
MEMS Spring Probe		CCC	CCC RT/HT+125℃	900/700mA, GOOD
		Contact Force	Contact Force/OD	On Design, little variation

Confirmed to be able to achieve the customer requirement

Design Feasibility

Design Feasibility
Highly Scalable MEMS Technology

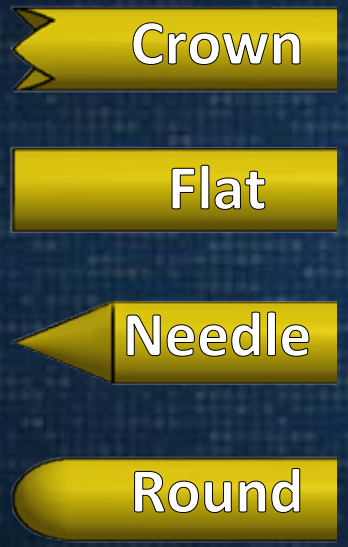
General probe diameter & parts size. It is easy to adapt design from wide pitch to narrow pitch.



Design Feasibility
Highly Scalable MEMS Technology

Four design factors can be used to achieve Design flexibility

(1) Probe Tip



Bump, Pillar, AL, Au

(2) Self Rotation

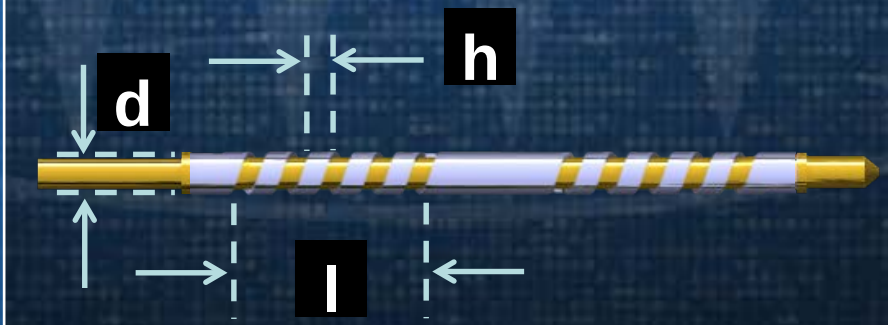
Rotation

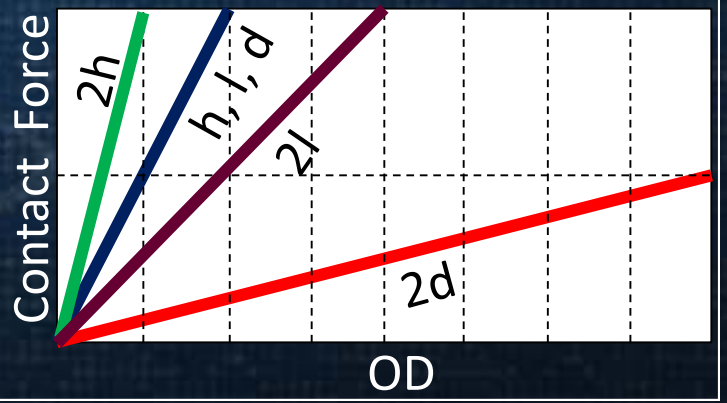


No-Rotation



(3) Probe Force

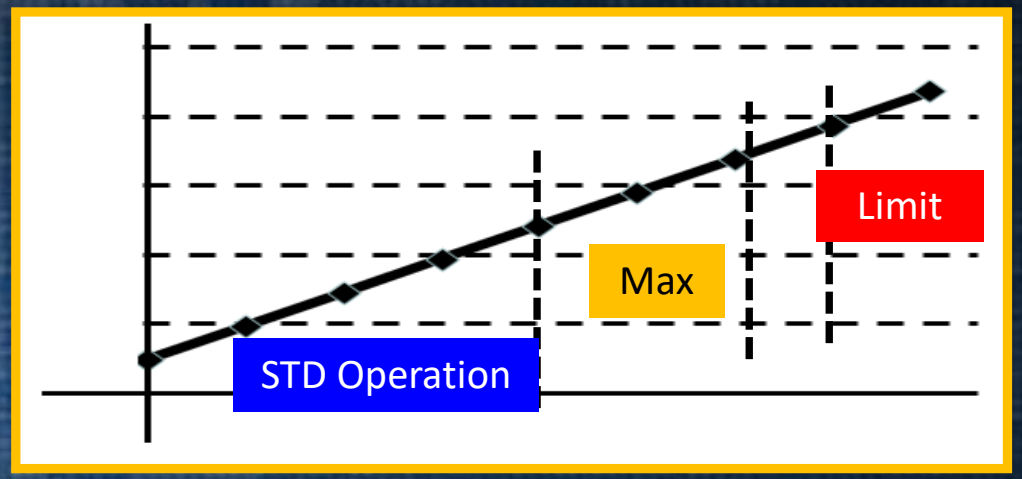


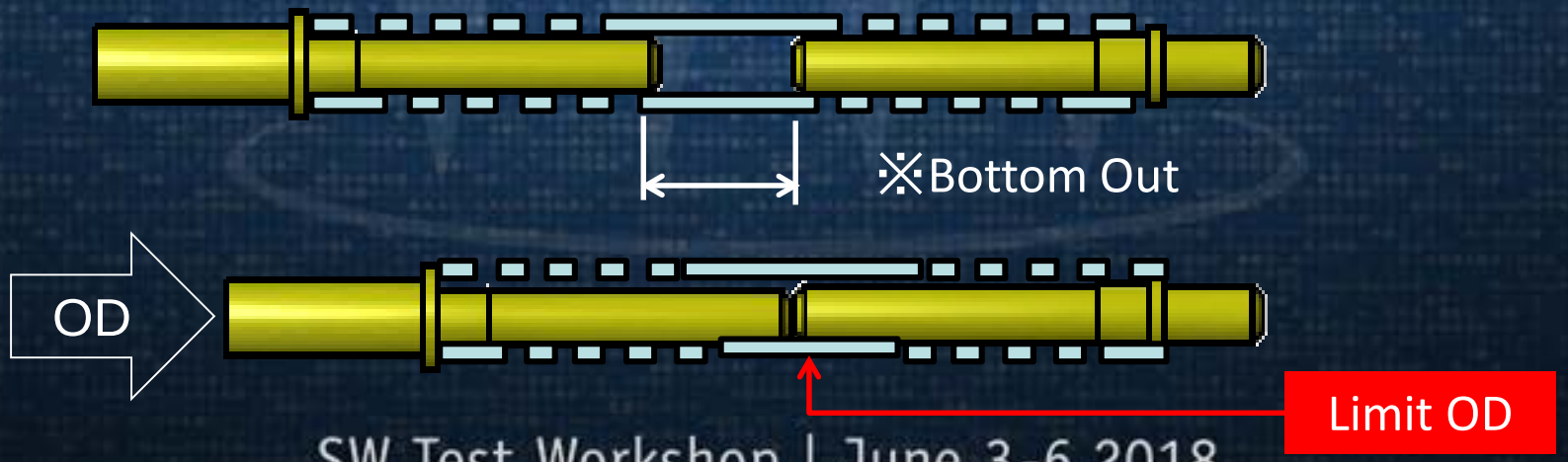


Design Feasibility
Highly Scalable MEMS Technology

(4) Operation OD margin

- Pre-load
- STD Operation OD
- Max Operation OD (=Bottom Out - Margin)
- Limit OD (=Bottom Out)



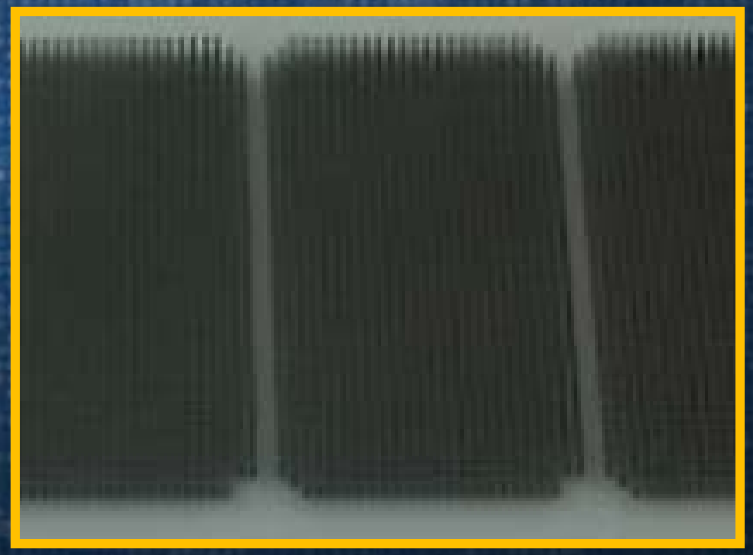


MEMS Probe Card General Specifications

MEMS Probe Card General Specifications

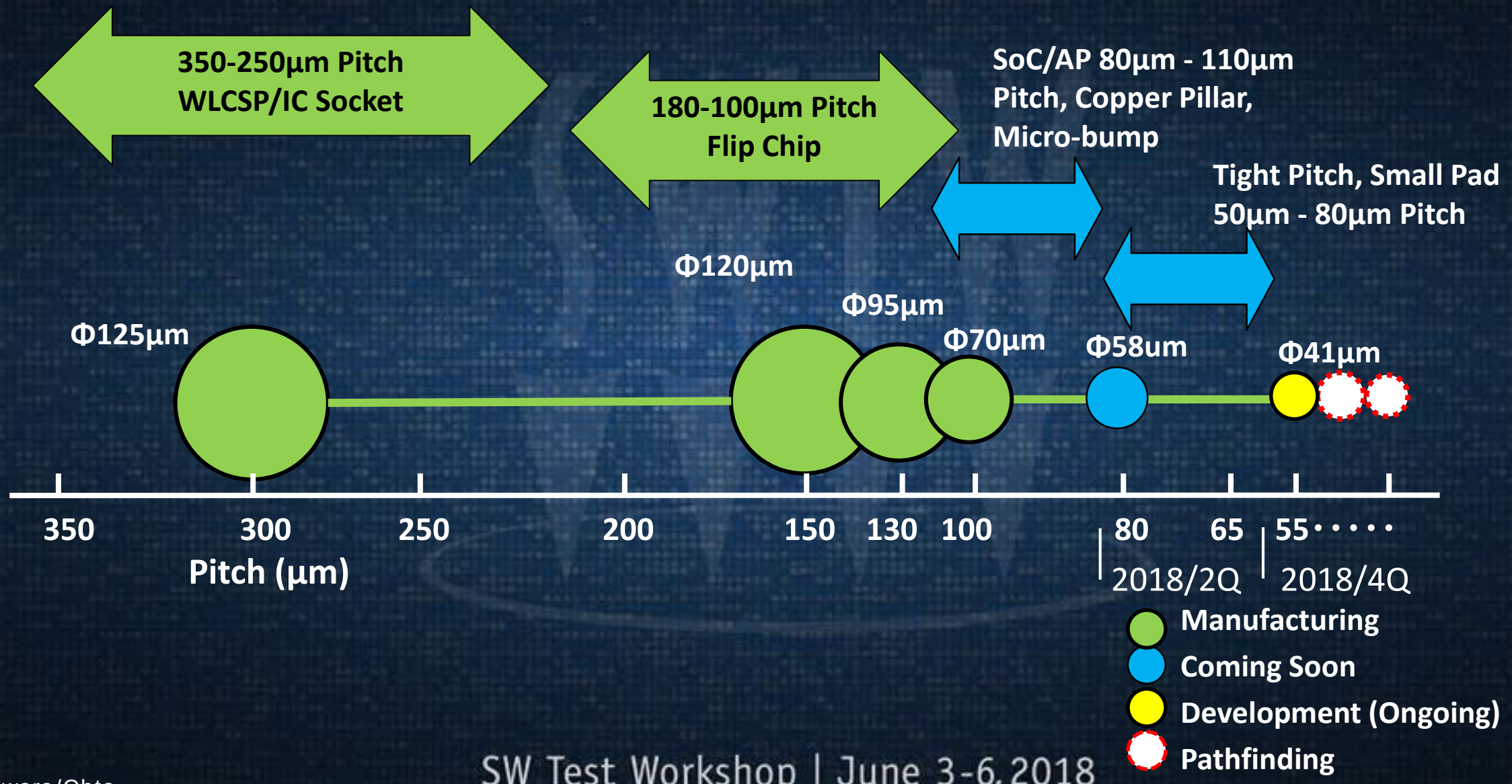
Parameter	SPEC
Pitch	Min 80µm
Planarity	< 10µm
XY Position	< ±10µm
Contact Force	Max 10gf
CRES	< 3Ω
CCC (RT)	P250(Φ125µm) – 1400mA P80(Φ50µm) – 600mA
Temp	-40℃～+180℃
Max OD (Example)	P250 - Max 250µm P150 - Max 400µm P80 – Max 180µm

Tip Motion	Self Rotating or Non-Self Rotating
Tip Shape	Point, Round, Flat, Crown
Material	W+Au, H3C, Rh



Roadmap

Technology Road Map



Future Study

- MAC
  - High temp +180℃
    - MLO/MLC frequency
      - 80um pitch
        - Auto probe insertion machine
          - High volume MFG capacity

Conclusions

- The MEMS SPRING PROBE technology can easily provide small diameter probes that cannot be realized with conventional coil springs.
- Simple structure realizes high CCC & low CRES which is stable over life & temperature.
- Minimize Bump damage by Rotation control & free tip shape.
- Positive performance CRES/OD, CRES/TD at Tri-temp.
- No degradation after 1MTD.
- Roadmap to 55µm pitch.
- Wide variety of pin specs achievable using common manufacturing process & no hard tooling.

Acknowledgements

- End User Test Engineering Team
- MEMS Spring Probe Engineering Team (Nidec-Read & LuzCom)
- SV TCL Engineering Team

Thank you



SW Test Workshop

Semiconductor Wafer Test Workshop

Data-Driven Comparison and Qualification of WLCSP Probes

Show Me the Data



Bert Brost

Xcerra

June 3-6, 2018

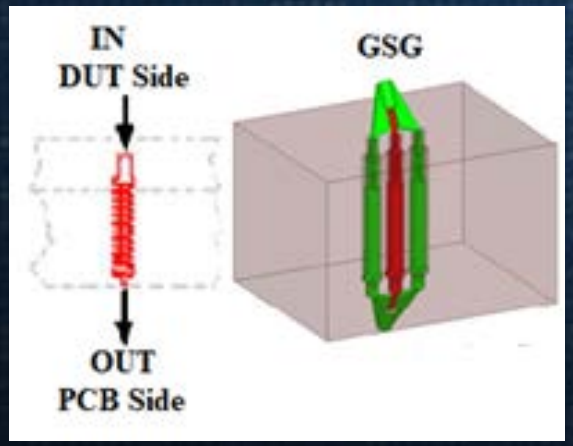
Overview

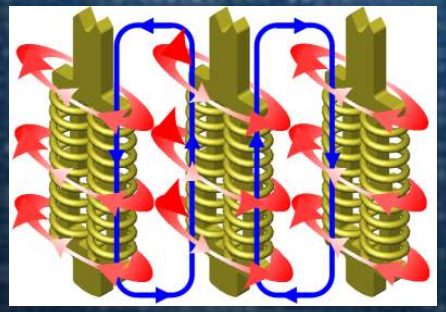
- **Key Performance Measures**
  - Electrical
    - SPICE and S Parameter Models
    - Insertion Loss and Return Loss
    - Crosstalk
    - Eye Diagrams/Patterns
    - Probe Resistance
      - Test Height/ Compliance
    - Current Rating
  - Metrology
- **Conclusion**

Making Informed Data-Driven Decisions

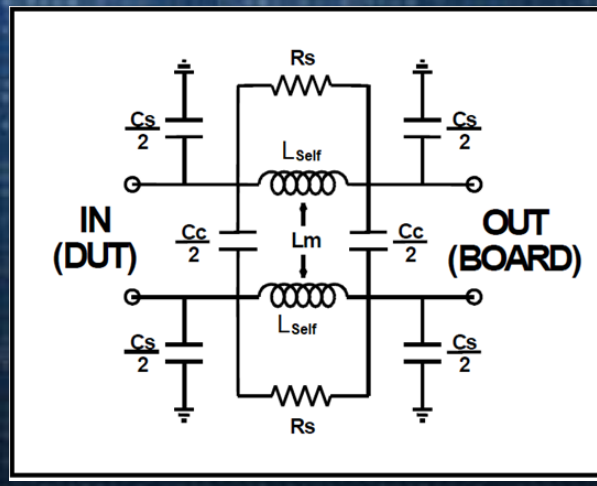
SPICE Models

1. **Most probe suppliers have equivalent circuit SPICE (Simulation Program with Integrated Circuit Emphasis) compatible models.**
2. **Inductance should be specified as loop inductance:**
   a) Loop inductance relates to the actual performance at all frequencies and all probe spacing pitches
   b) Self inductance is close to impossible to measure, and most often determined using approximations



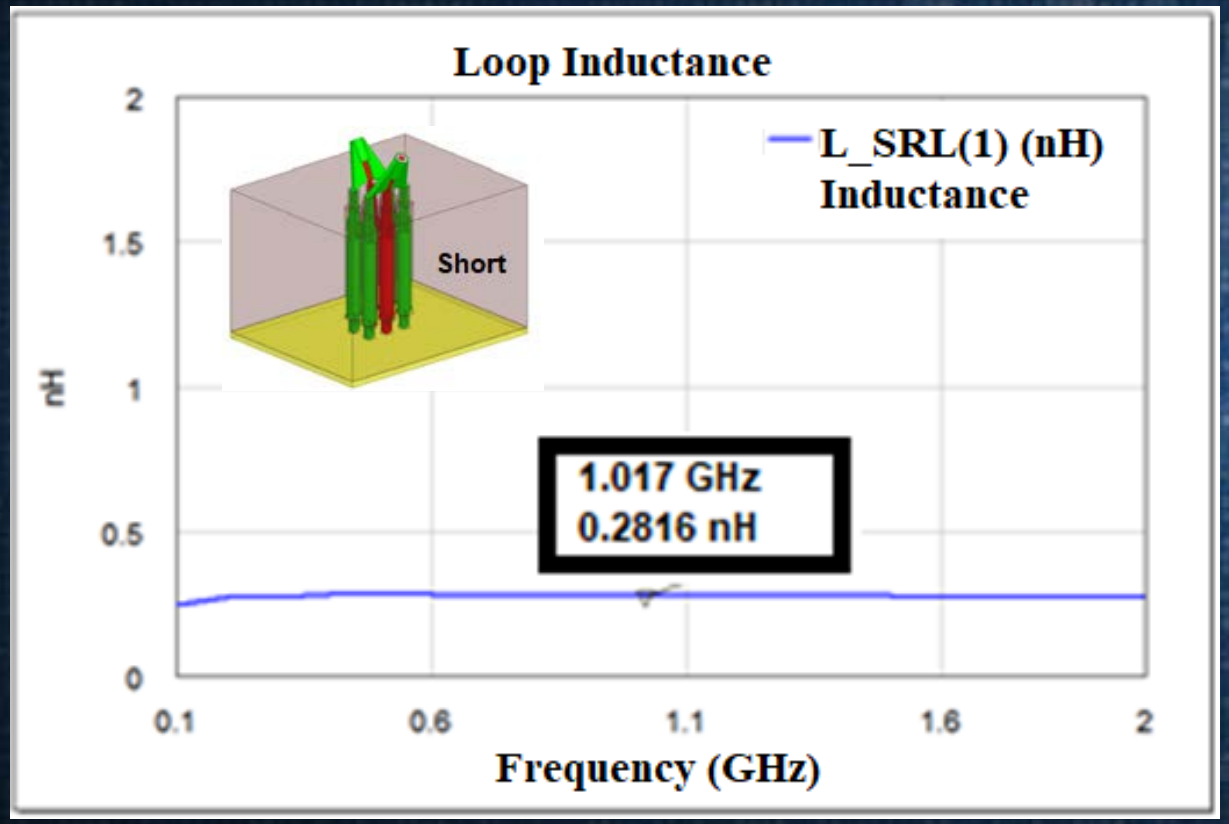


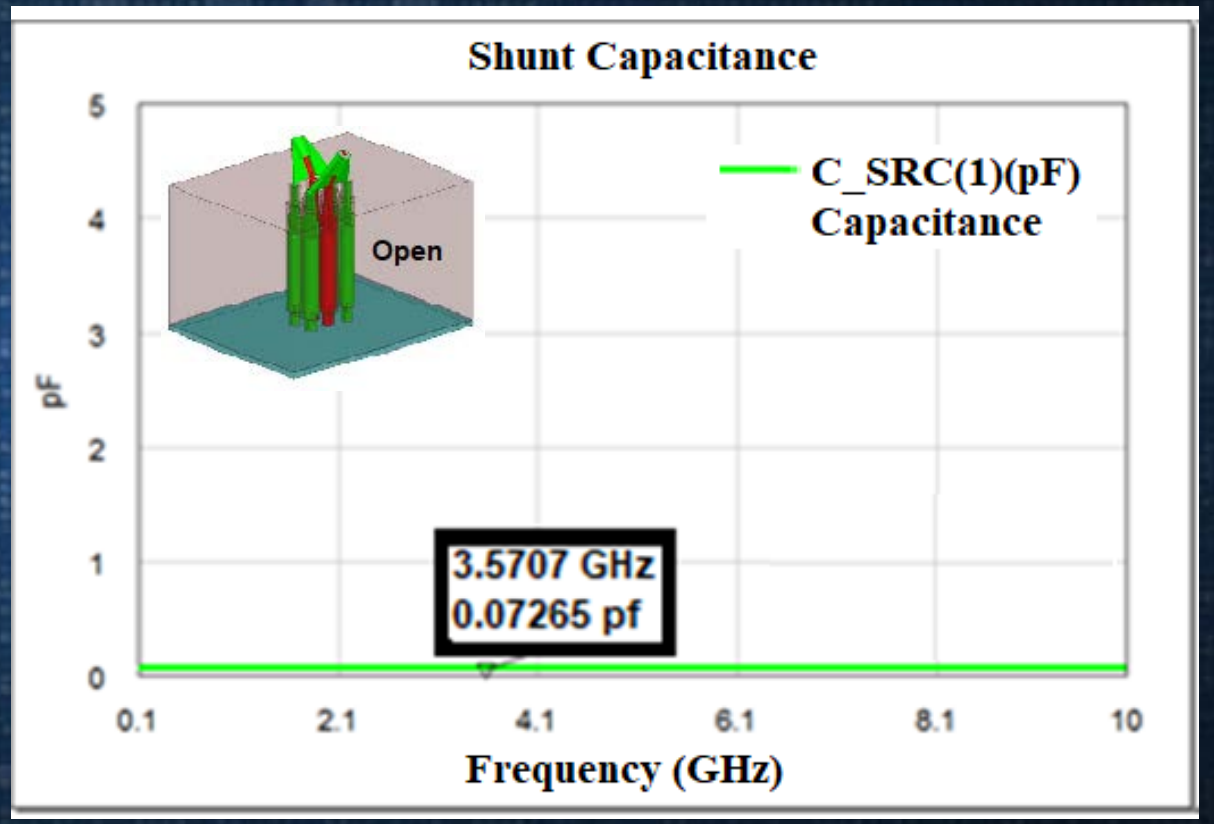
Electric Fields and Current Flow



L_{LOOP}	Loop Inductance	Measured (VNA) and Simulated (HFSS) GGS
C_{SHUNT}	Shunt Capacitance	Measured (VNA) and Simulated (HFSS) GGS
C_{MUT}	Mutual Capacitance	Simulated (HFSS) GSSG
L_{MUT}	Mutual Inductance	Simulated (HFSS) GSSG

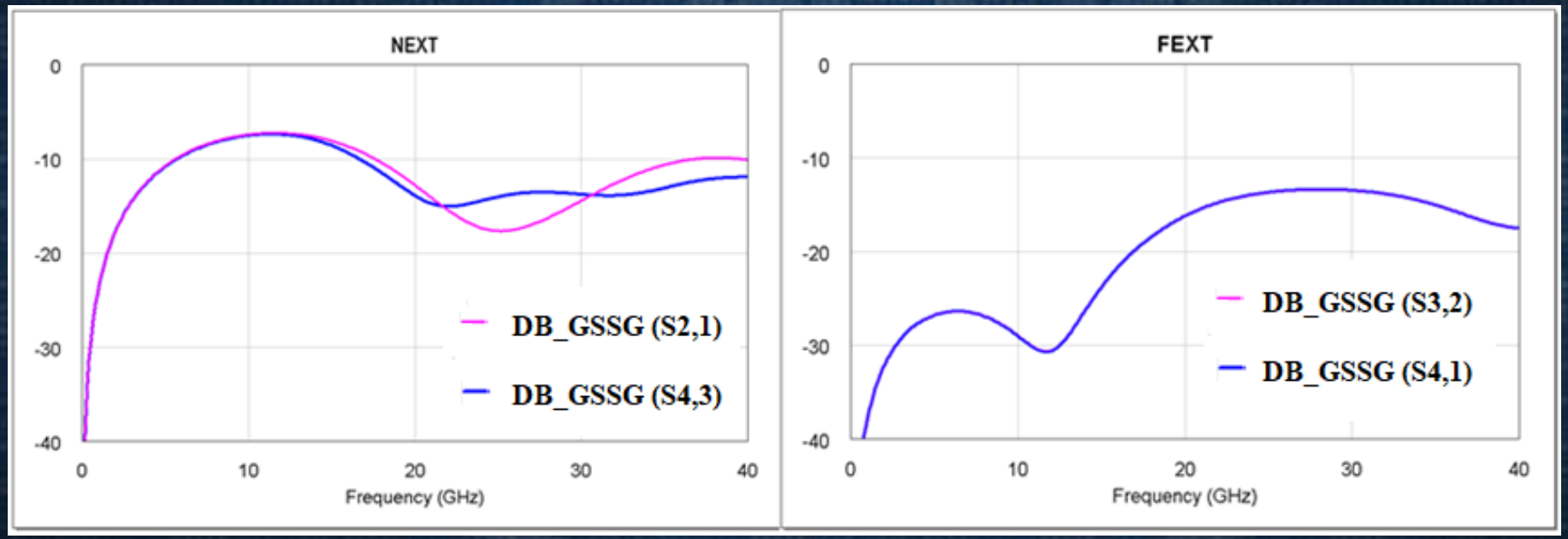
Inductance and Capacitance

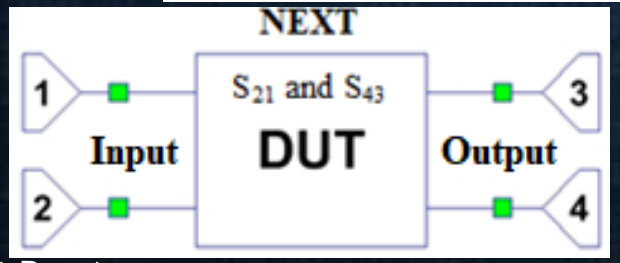




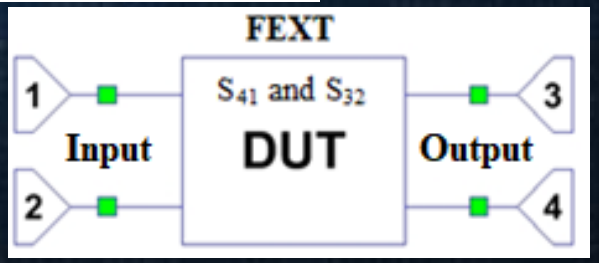
Crosstalk

- Near-End Crosstalk is the crosstalk measured from the input of one signal pin to the input of the adjacent signal pin. It is determined from S2,1 and S4,3 as shown on this slide
- Far-End Crosstalk is the crosstalk measured from the input of one signal pin to the output of the adjacent signal pin. It is determined from S4,1 and S3,2 as shown on this slide
- Crosstalk results shown are determined through 3D Electromagnetic simulation

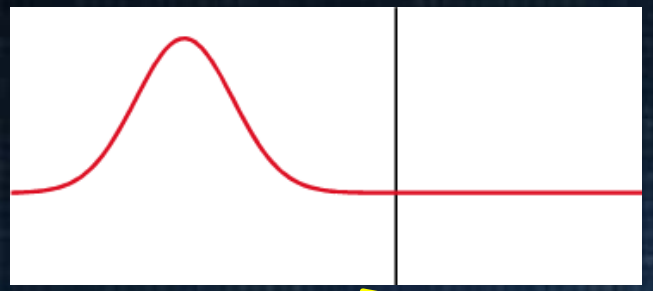




Crosstalk (dB)	Power Ratio	NEXT	FEXT
-20 dB	0.01	1.5 GHz	16.9 GHz
-10 dB	0.1	5.6 GHz	>40 GHz

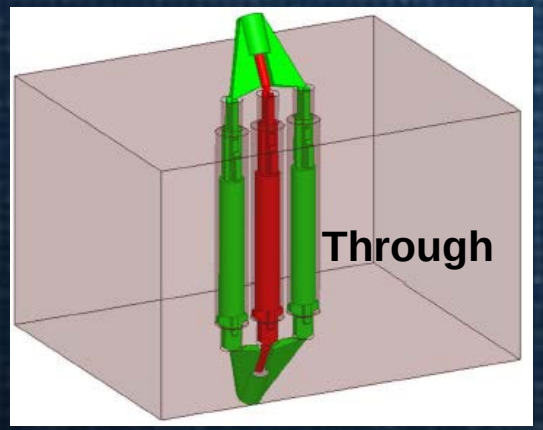


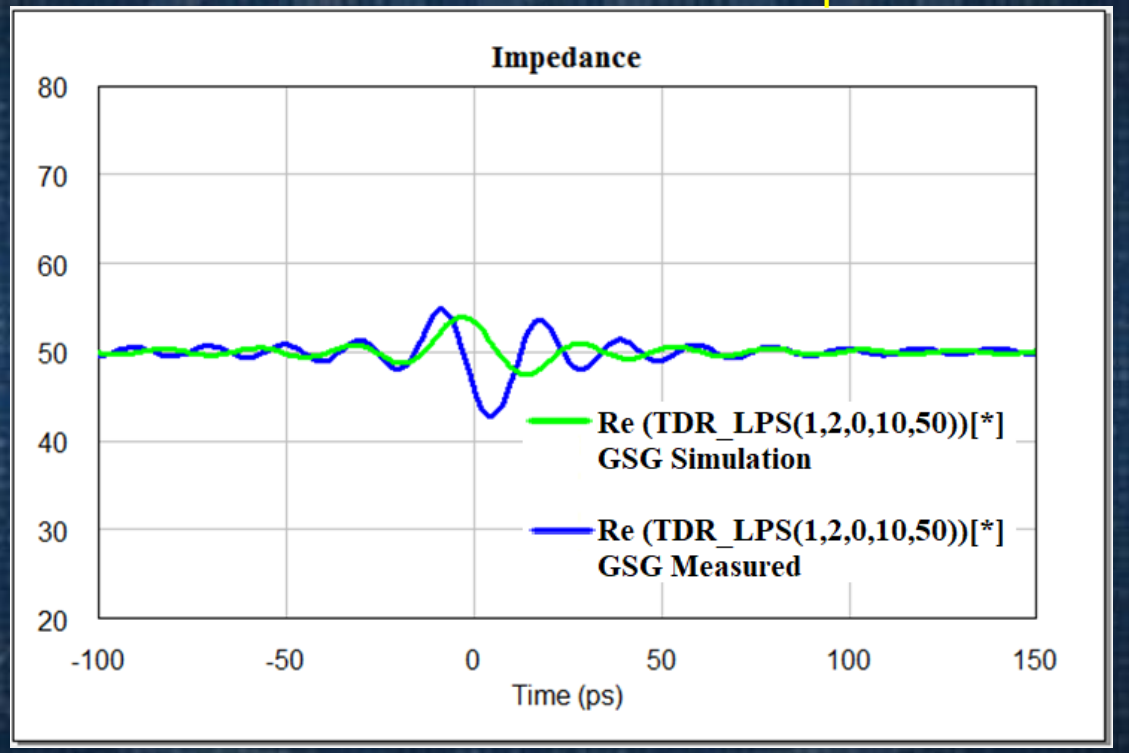
Impedance

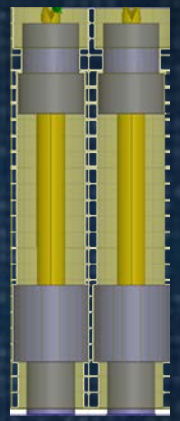


Impedance matching is the practice of designing the path to match the impedance of the signal source and destination. This maximizes power transfer and minimizes reflections

Interconnect Impedance Discontinuity







Impedance Controlled Interconnect: Coaxial Solution

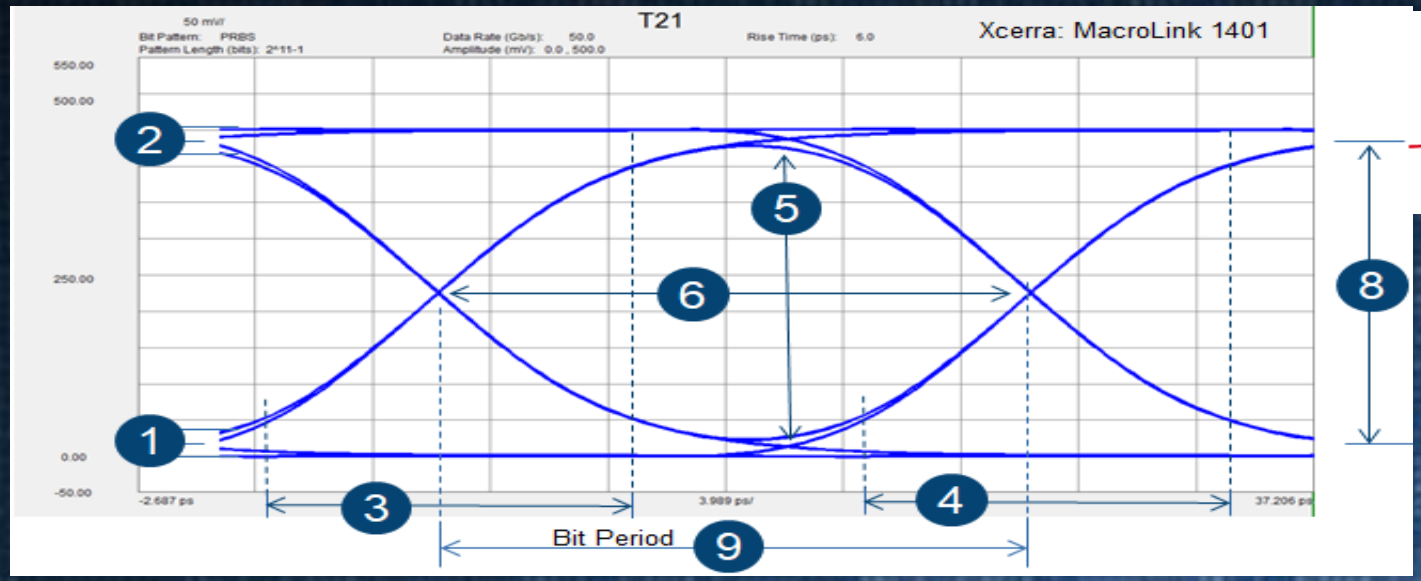


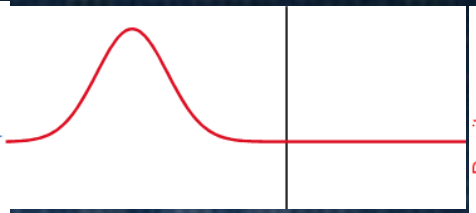
All of These Resist Current

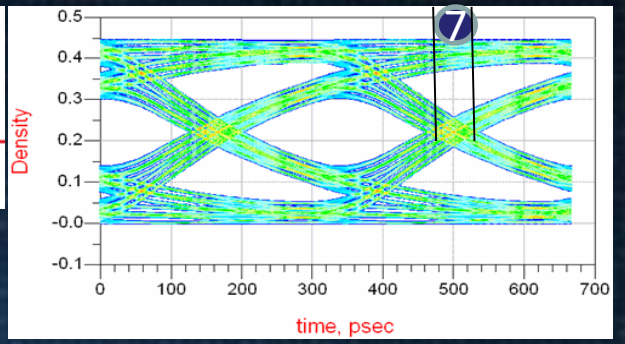
$$Z = \sqrt{R^2 + (X_L + X_C)^2}$$

Circuit Impedance Z

Eye Diagrams / Patterns





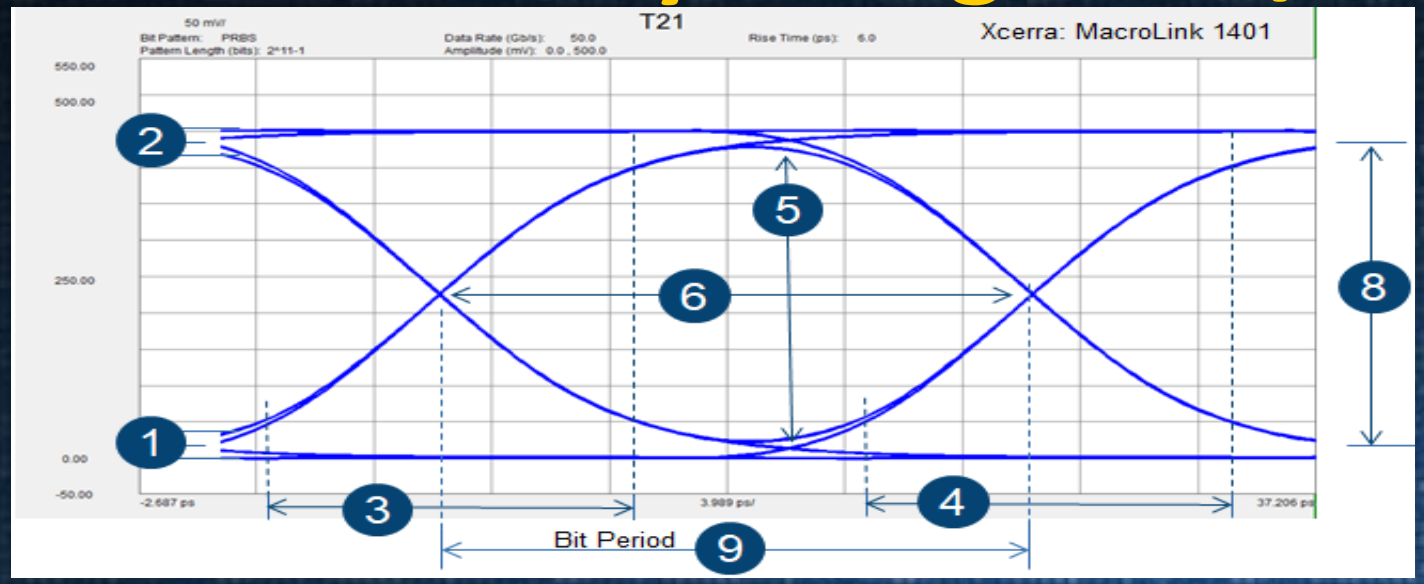


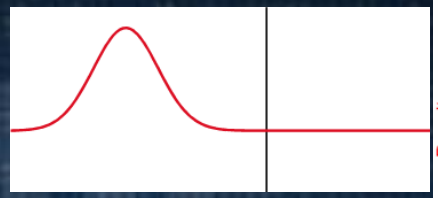
5 Vertical Eye Closure

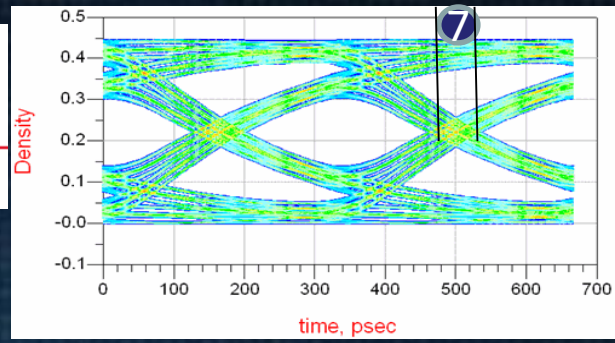
- Ground bounce, Overshoot, Reflection(bad termination)

1. Zero Level: The measure of the mean value of the logical 0 of an eye diagram. *Voltage amplitude variations*
2. One Level: The measure of the mean value of the logical 1 of an eye diagram. *Voltage amplitude variations*
3. Rise Time: The measure of the transition time of the data from the 10% level to the 90% level on the upward slope of an eye diagram.
4. Fall Time: The measure of the transition time of the data from the 90% level to the 10% level on the downward slope of an eye diagram.
5. Eye Height: The measure of the vertical opening of an eye diagram.

Eye Diagrams / Patterns



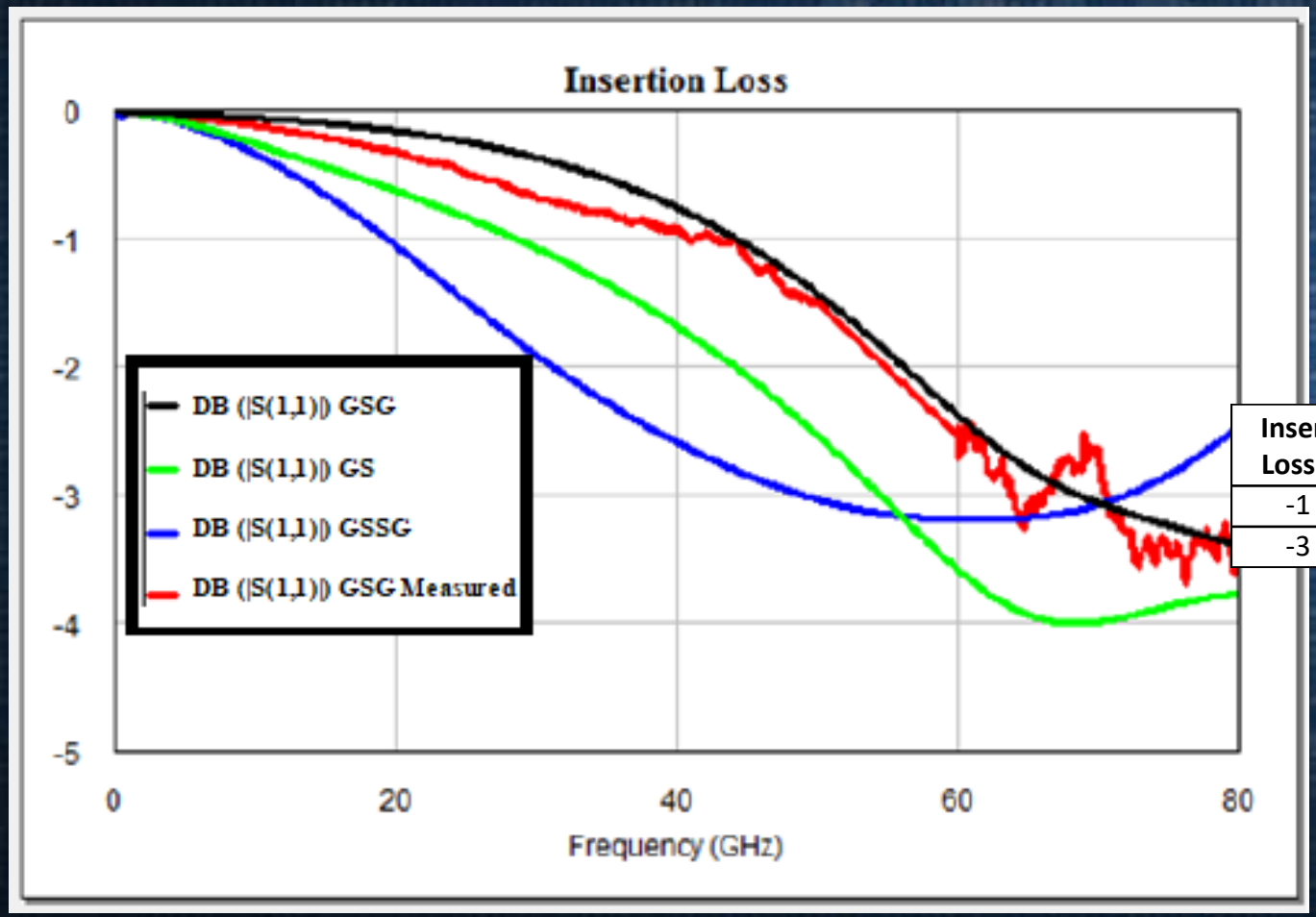


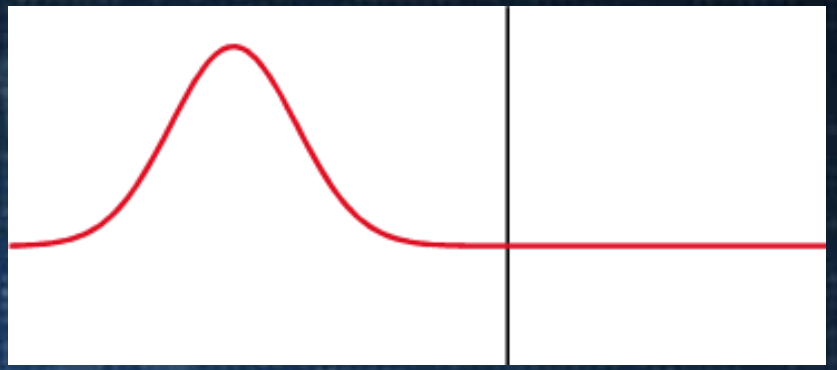


6 Horizontal Eye Closure
- Deterministic Jitter: crosstalk, impedance mismatch, i.e., things in the circuit

6. Eye Width: is a measure of the horizontal opening of an eye diagram.
7. Deterministic Jitter: is the deviation of a transition from its ideal time caused by reflections relative to other transitions. *How far is my edge from the ideal.*
8. Eye Amplitude: is the difference between the logic 1 level and the logic 0 level histogram mean values of an eye diagram
9. Bit Rate: is the inverse of bit period (1 / bit period). The bit period is a measure of the horizontal opening of an eye diagram at the crossing points of the eye

Insertion Loss



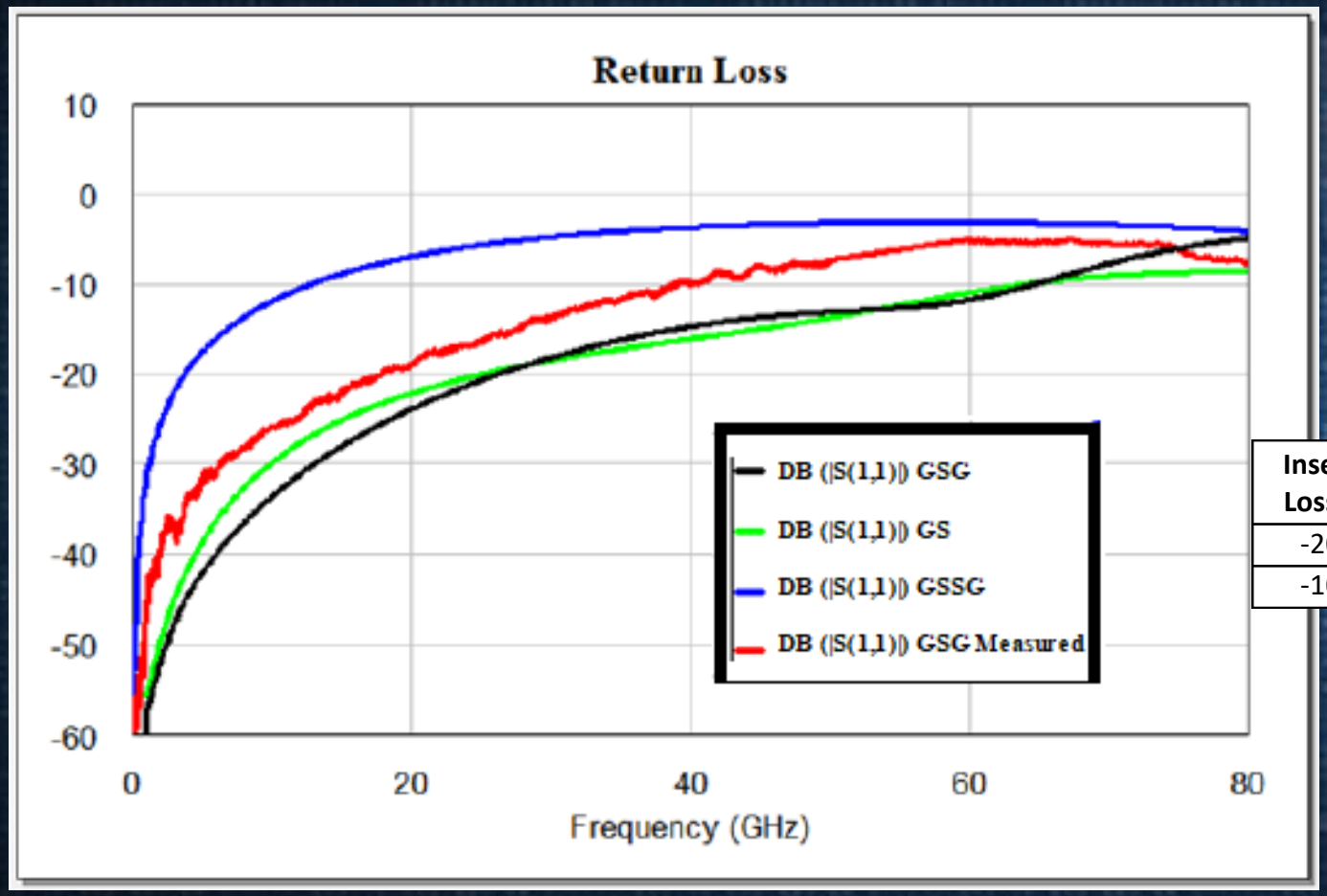


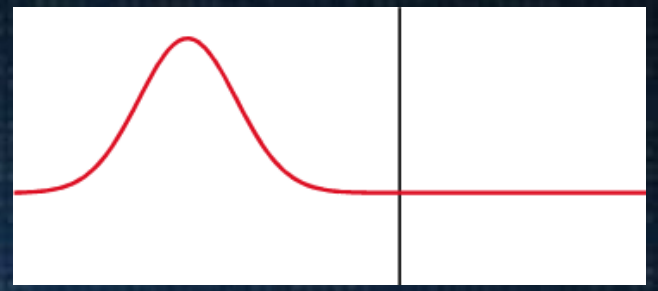
Insertion Loss (dB)	Power Ratio	Single Ended G-S	Single Ended G-S-G	Differential G-S-S-G
-1 dB	0.794	28.6 GHz	42 GHz	19.4 GHz
-3 dB	0.501≅ 1/2	54.5 GHz	64 GHz	49 GHz

Insertion loss is the:

- Ratio of Power Out to Power In
- P_{out}/P_{in} = Power Ratio
- IL=log10 (P_{out}/P_{in})= xdB

Return Loss





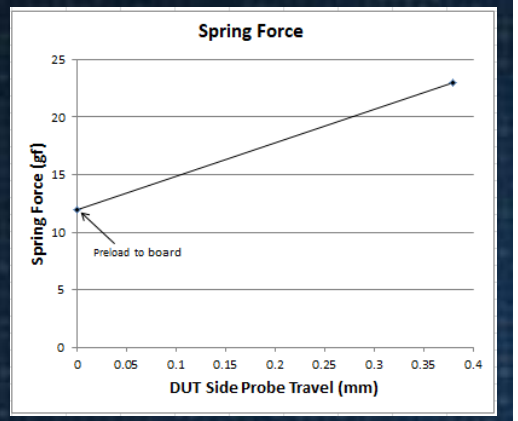


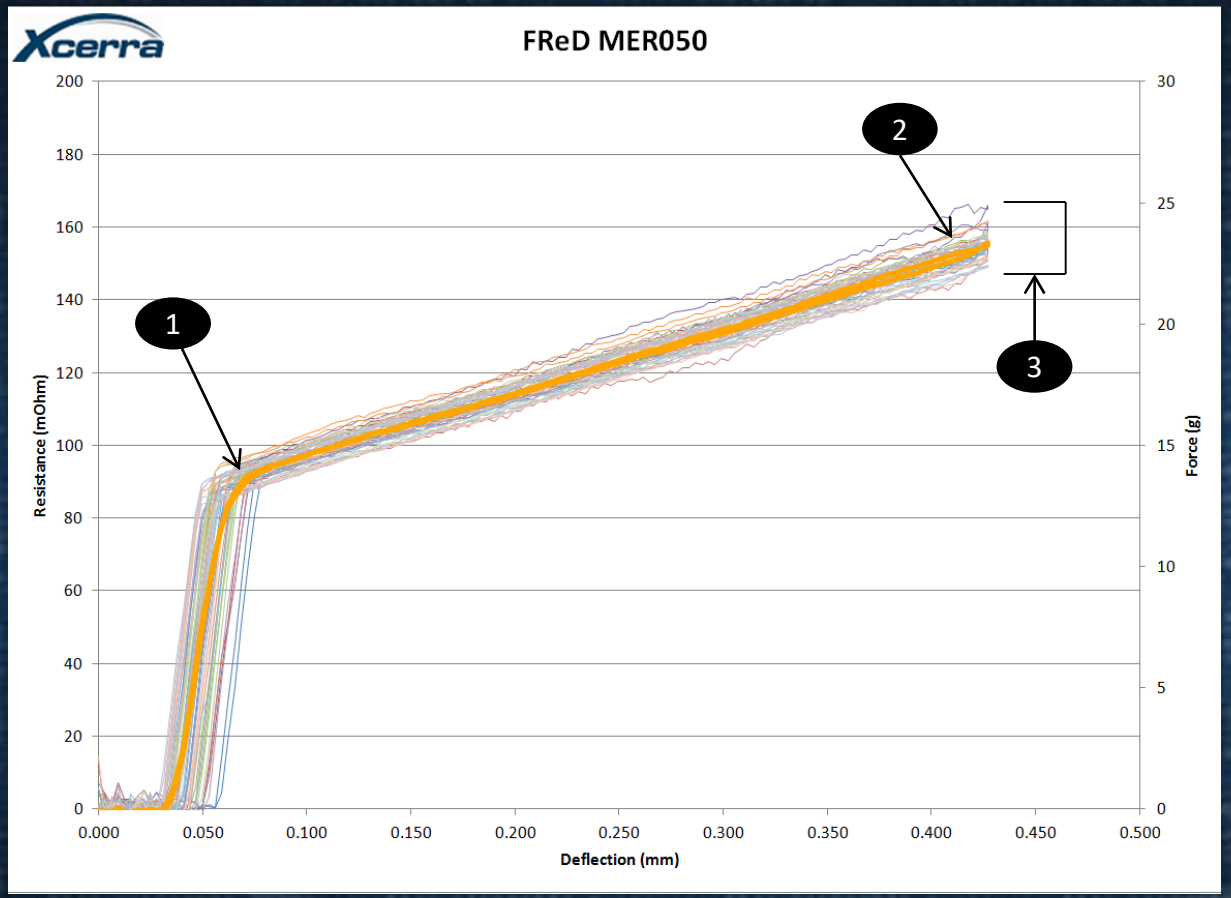
Insertion Loss (dB)	Power Ratio	Single Ended G-S	Single Ended G-S-G	Differential G-S-S-G
-20 dB	0.01	24.8 GHz	17.8 GHz	3.7 GHz
-10 dB	0.1	64 GHz	38.6 GHz	12.3 GHz

Return loss is the:

- Ratio of Power Returned to Power In
- $P_{returned} / P_{in} =$ Power Ratio
- $RL = \log10 (P_{return} / P_{in}$

Probe/Spring Force



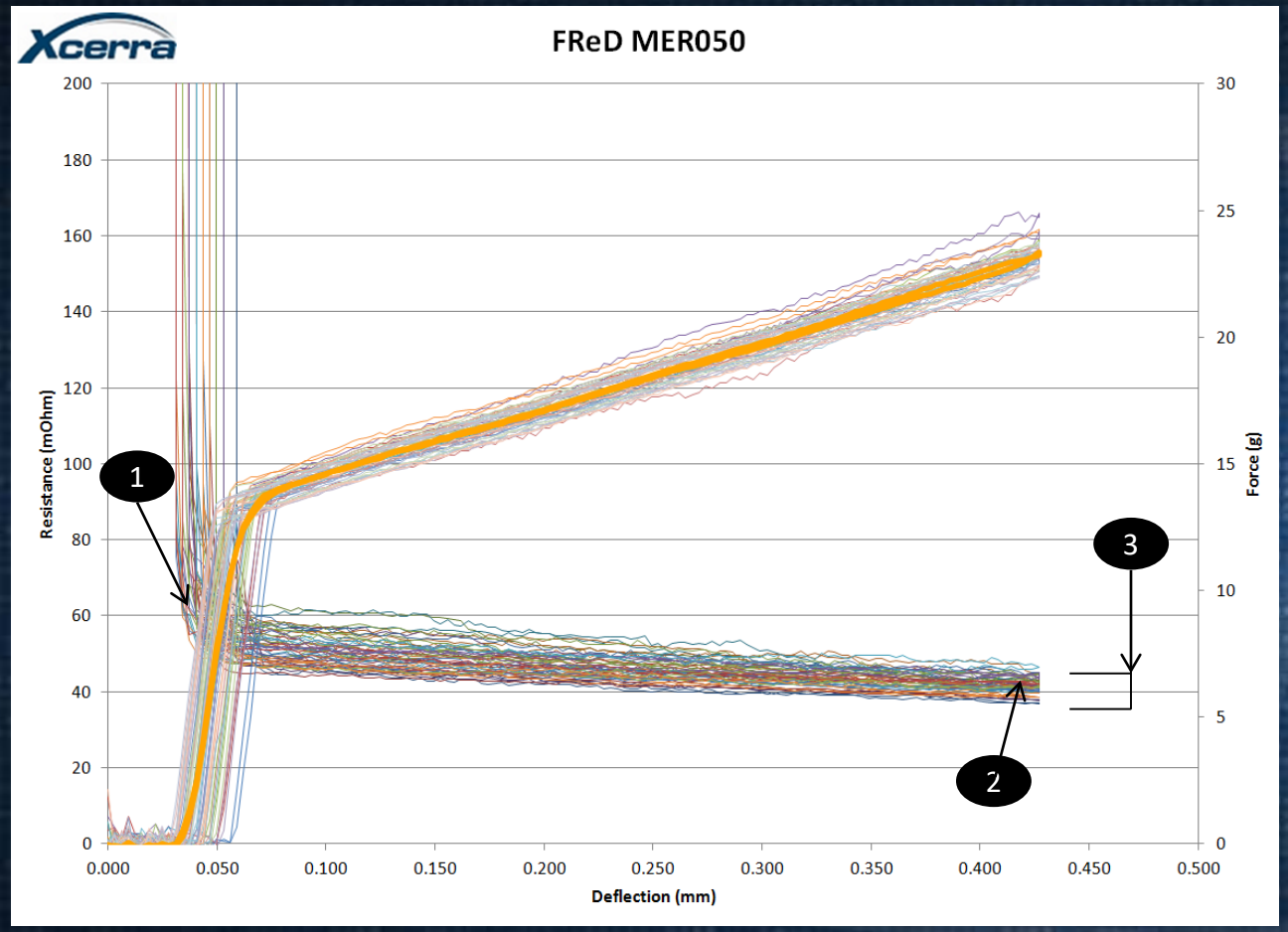


- **F**orce
- **R**esistance
- e
- **D**eflection

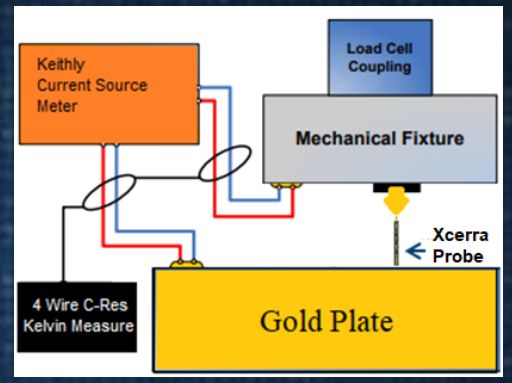
1. Force at Preload
2. Force at Test Height
3. Distribution of Force at Test Height

Force Plot (FReD)
Development of the FReD plot includes the random selection of a number of probes that are mounted in a fixture and then compressed to test height. The result is a systematic measure of the probes performance in the force domain. The sample size is determined to statistically represent a population

Spring force and Probe Resistance



1. Probe Resistance at First Point of Contact
2. Probe Resistance at Test Height
3. Distribution of Probe Resistance

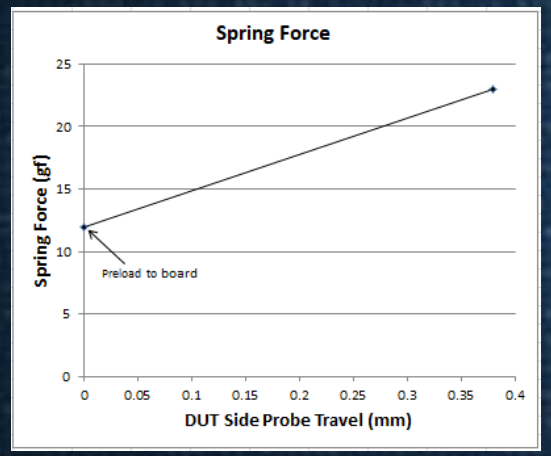


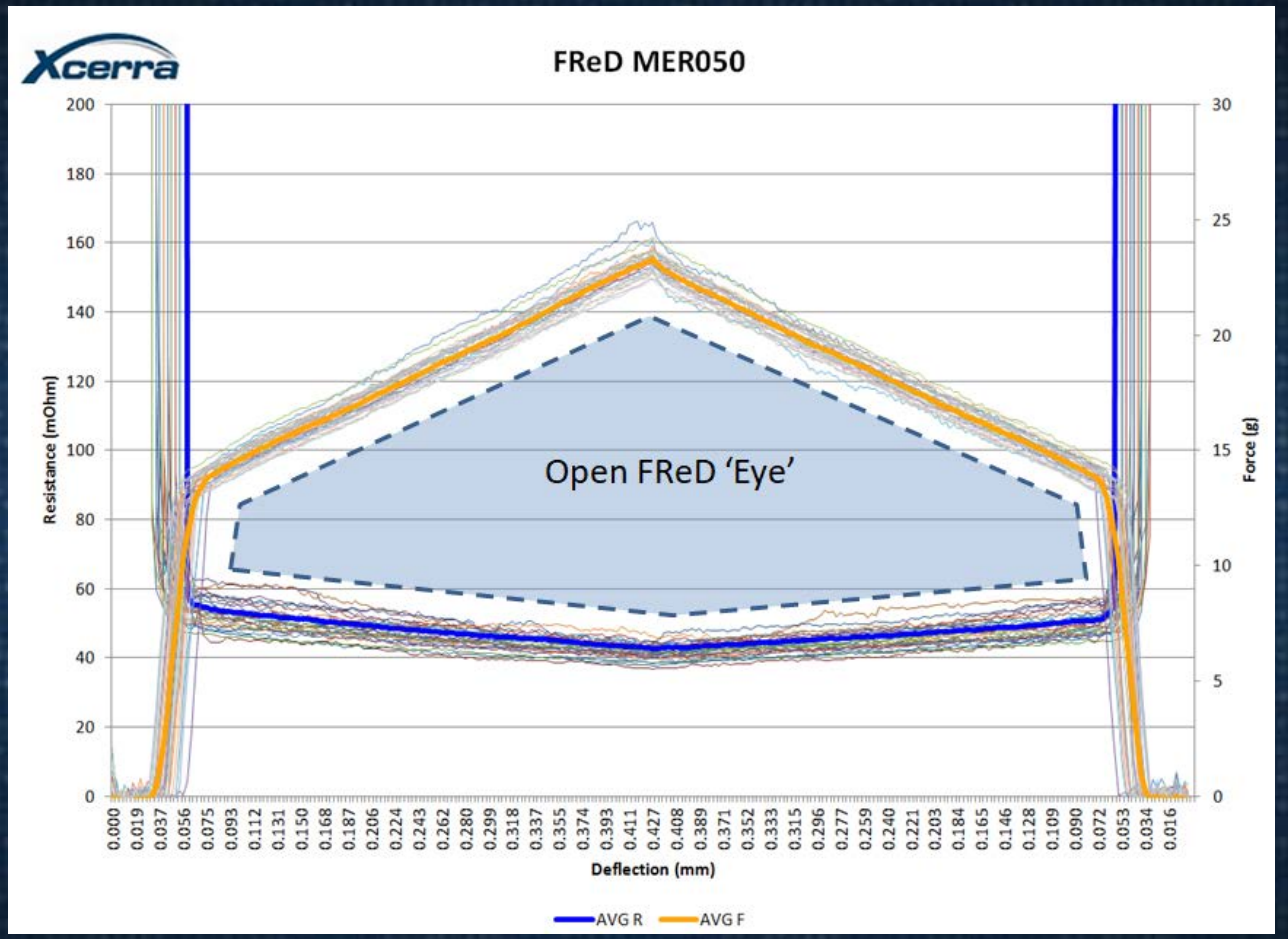
- **F**orce
- **R**esistance
- e
- **D**eflection



The FReD setup allows for measurement of probe resistance during probe compression. This process emulates the resistance of the probe as it contacts a Device-Under-Test.

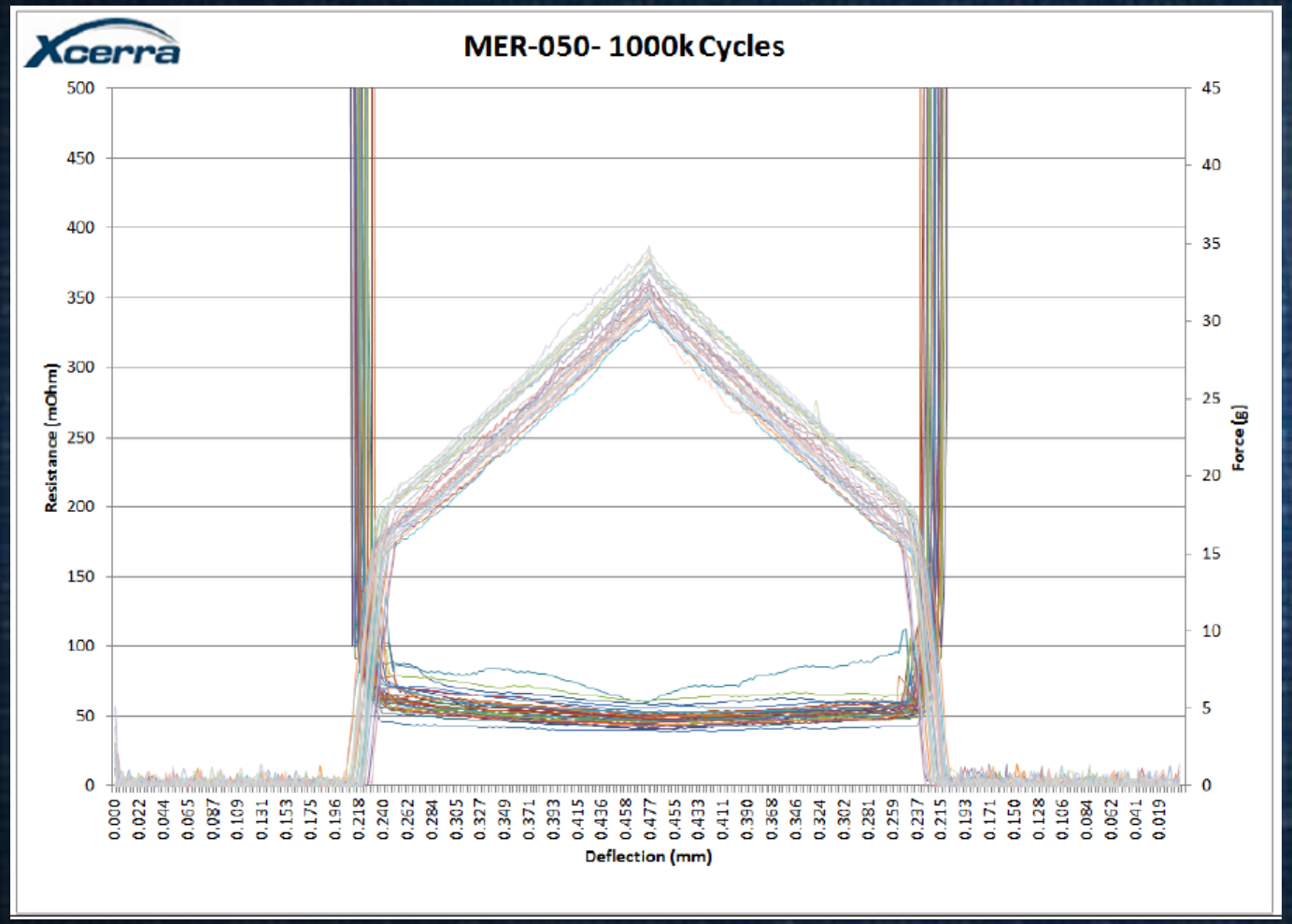
Force-Resistance and Deflection

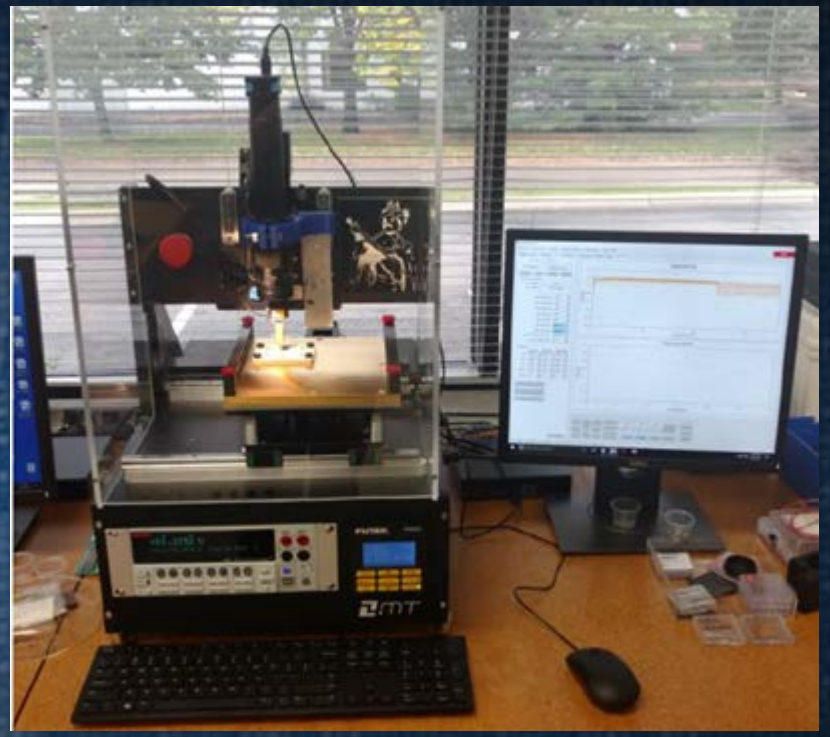




- **F**orce
- **R**esistance
- e
- **D**eflection

Force Resistance Life Cycle Testing

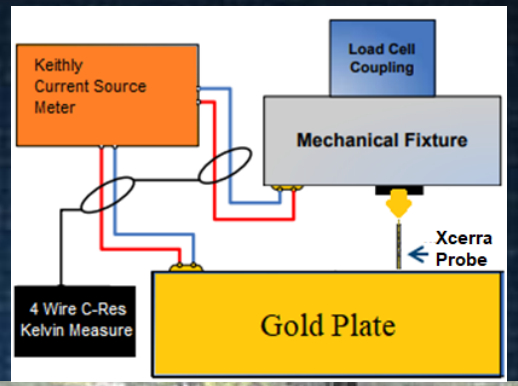


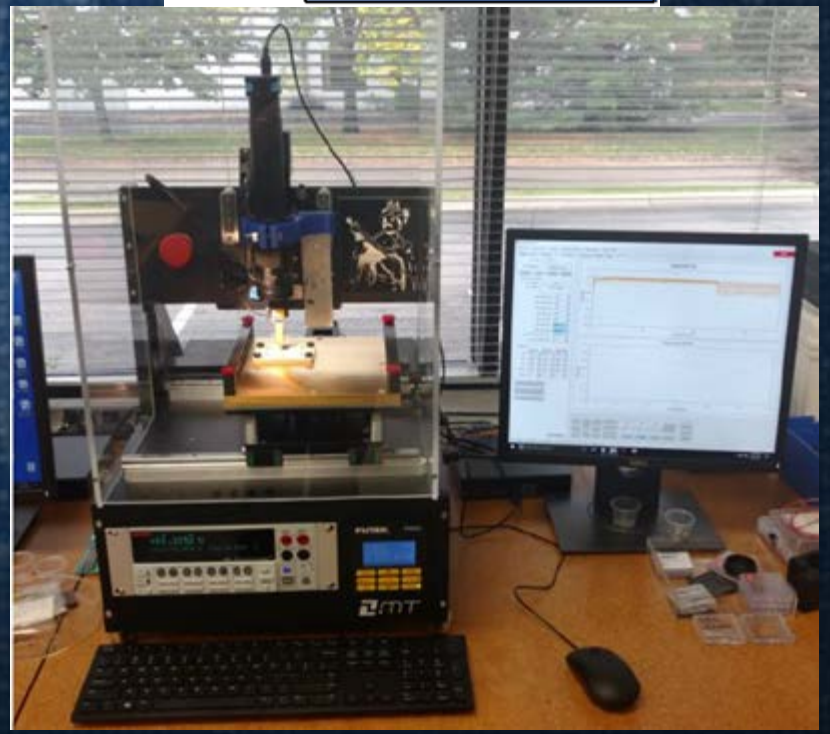


It is good to know the statistical resistance of a probe throughout it's projected life!

Current Carrying Capability Measurement

- ISMI force reduction method for developing a current rating

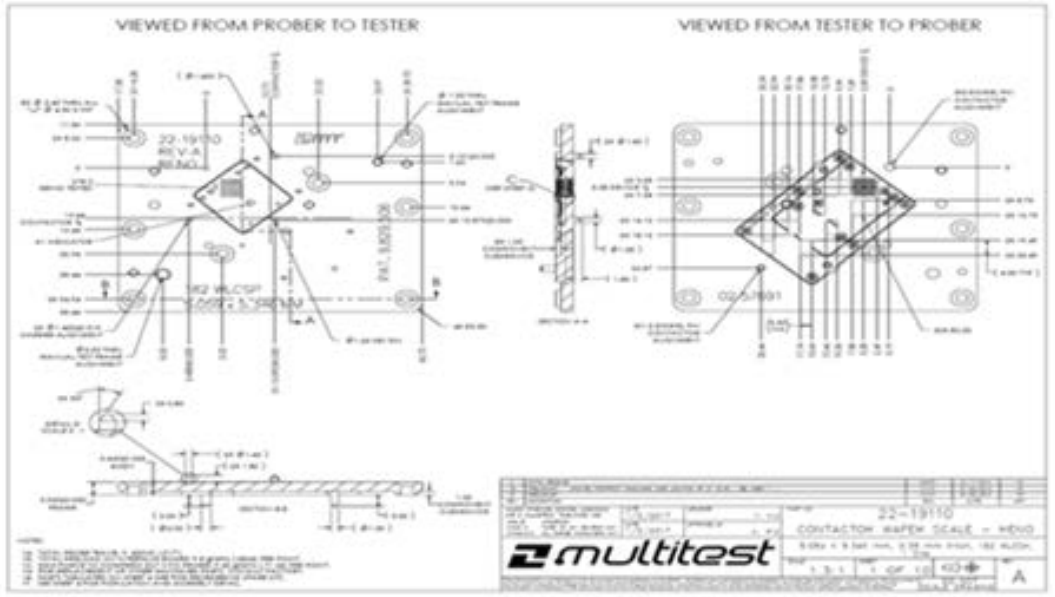




Metrology Cover Sheet and Pass Fail Report

MT Assembly Number: 22-19110
Serial Number:
Inspection Date:
Probe Used: 07-1063 MER-030-DJ-Au
Tester: MTMN FReD 7
Tested by: MBB

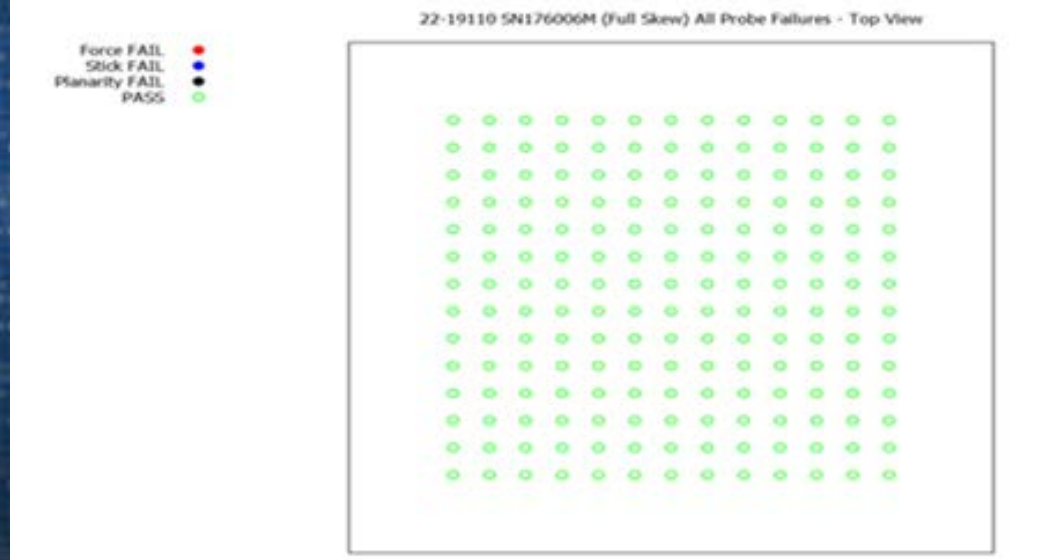
Probe Head Drawing (First Page Only)



MT Assembly Number: 22-19110
Serial Number:
Inspection Date:
Probe Used: 07-1063 MER-030-DJ-Au
Tester: MTMN FReD 7
Tested by: MBB

Probe Head Planarity/Force/Sticking

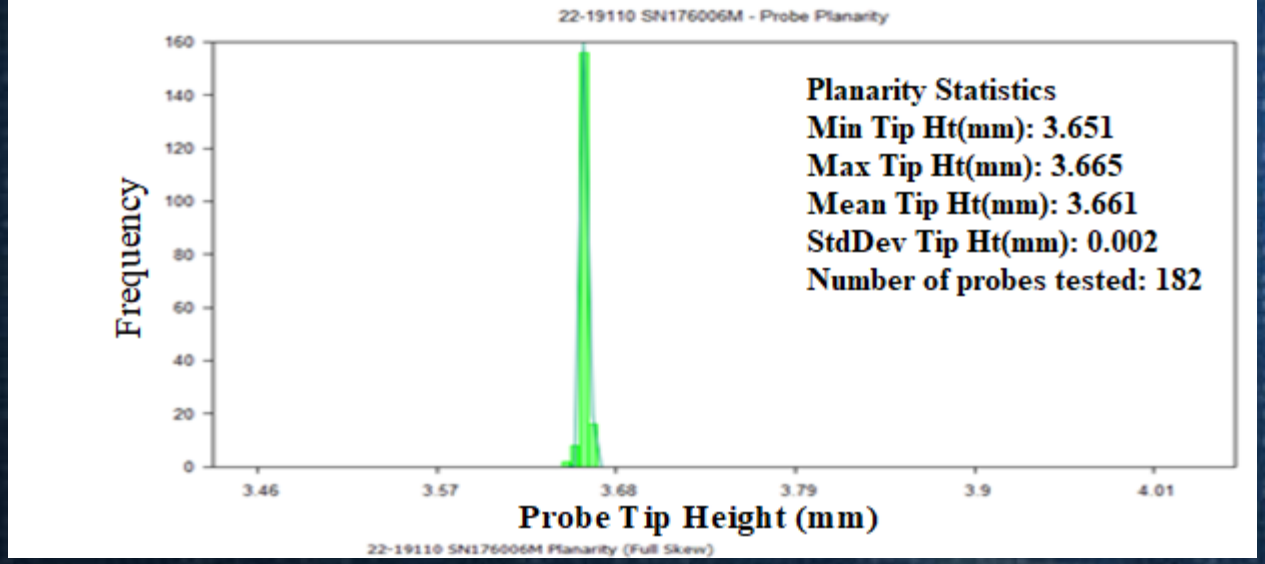
Force Range – Min: 10g
Max: 26g
Min Tip Height: 3.60 mm

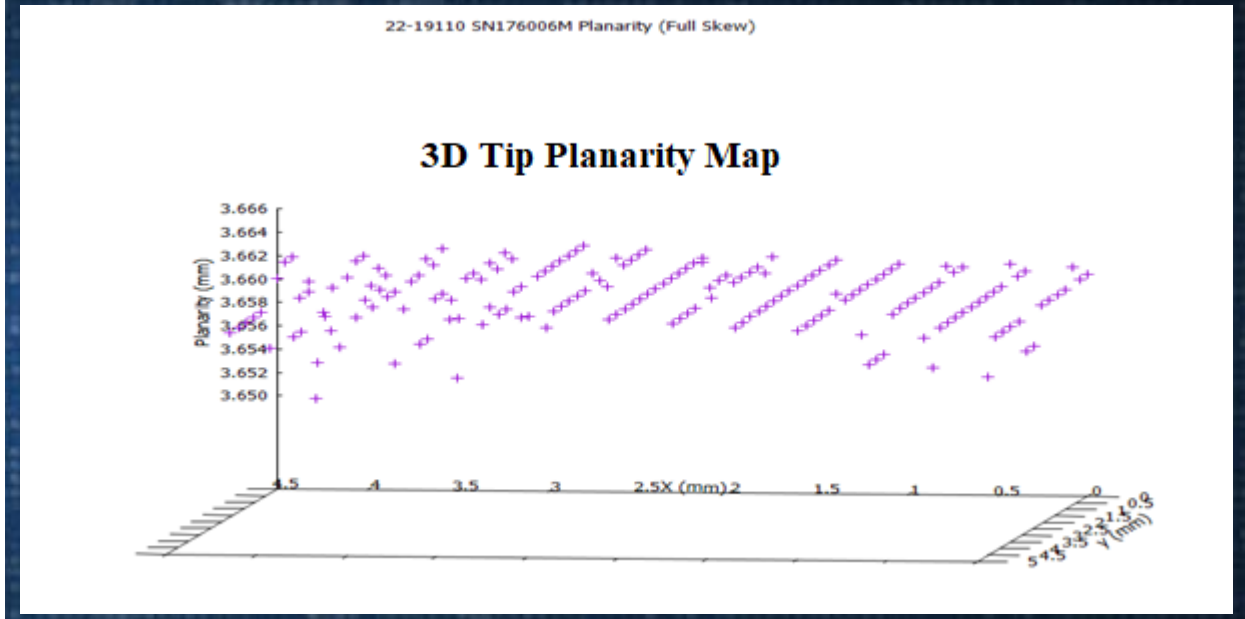


Metrology Report Probe Planarity

MT Assembly Number: 22-19110
Serial Number: SN176006M
Inspection Date:
Probe Used: 07-1063 MER-030-DJ-Au
Tester: MTMN FReD 7
Tested by: MBB

Probe Head Planarity

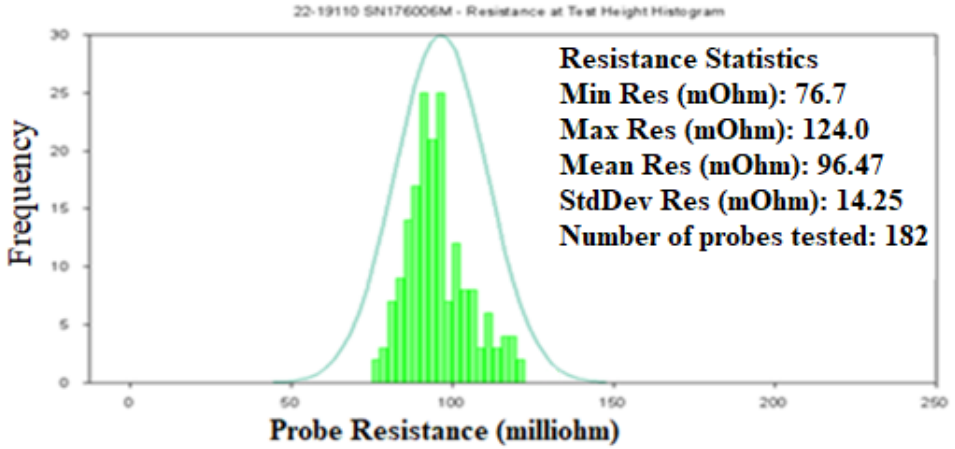


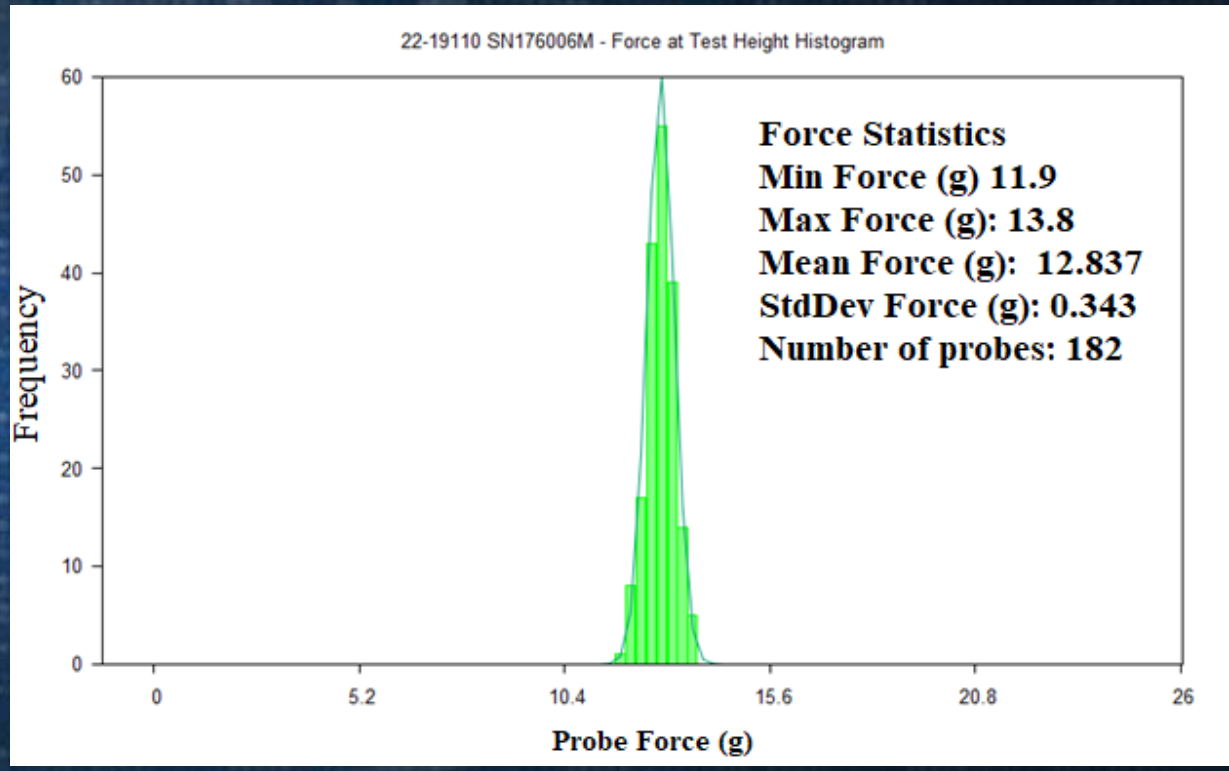


Metrology Report
Probe Resistance and Force at Test Height

Serial Number: SN176006M
Inspection Date:
Probe Used:
Tester: MTMN FReD 7
Tested by: MBB

Probe Resistance





Conclusion

- Not all specification are created equal
- Know and understand how the numbers that specify a probe head and/or probe card were developed.

- Don’t be afraid to say “**Show Me the Data**!”

Contributing Team Members

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Jason Mroczkowski
Marty Cavegn
Nadia Steckler
Valts Treibergs

Thank You for Attending and Listening

Questions Please