

SW Test Workshop

Semiconductor Wafer Test Workshop

Monday, June 4, 2018

PROCEEDINGS

June 3-6, 2018

Rancho Bernardo Inn,
San Diego, CA

www.swtest.org

Chairman's Welcome to SW Test 2018

Wafer Test Technology Conference and EXPO

On behalf of the SW Test Executive Team, Program Committee, and Committee Members, it is my great pleasure to welcome you to the 28th Annual SW Test Conference and EXPO.

I would like to thank all our sponsors (9-platinum, 9-gold, and 7-silver), 64 exhibitors, committee members, and the volunteers who help make the SW Test Conference and EXPO such a valuable event for the wafer test industry.

For the SW Test 2018 program, we received many outstanding submissions for podium and poster presentations. Rey Rincon, Technical Program Chair, and the Program Committee implemented a new review process for building the program. All submissions were reviewed by a 9-member Selection Committee, ranked using a criteria algorithm, and then organized into themed technical sessions. Using this new selection process, we have built a technical program with thirty-one podium and nine poster presentations. It was an extremely competitive selection process and the SW Test Team thanks all of the authors and their companies.

Our goal is to provide all attendees with an informative and diverse technical program that addresses real-world challenges faced by test professionals. Leading technologists will discuss device testing challenges under the most demanding electrical, and environmental conditions.

We encourage and support student participation. This year the William R. Mann Travel Grant with awarded to three student attendees (Alex Poles from The University of Nevada, Reno; Gaurav Rajavendra Reddy from The University of Texas at Dallas; and Mehmet Tas from the University of Surrey, UK).

During the SW Test EXPO, top suppliers will have an opportunity to showcase their latest product offerings and technical services. This year, our available exhibit space has increased from 42 booths to 64 booths. Our goal for the EXPO is to provide attendees unprecedented, focused access to key technologies and services, while not competing with the technical program.

Throughout the year, SW Test Executive Team also works on co-marketing activities with various organizations and other conferences that touch thousands of technical professionals. Our co-marketing relationships have been developed with BiTS Workshop, IS-Test Workshop, IEEE Holm Conference, IEEE NATW, SEMI.org, TEST VISION 2020, and VLSI Research.

The SW Test Team is also proud to announce our 1st Annual SW Test Asia conference to be held in Hsinchu, Taiwan, October 18 to 19, 2018, at the Sheraton in Zhubei City. This one and one-half day conference will be organized in the spirit of SW Test San Diego and will consist of a Technical Program, EXPO, and Technology Showcase. The SW Test Asia Technical Chair is Clark Liu and we are happy to announce that Joey Wu (STAr Technology) and Nobuhiro Kawamata (Formfactor K.K.) have joined the Steering Committee for this conference.

Once again, thank you for being a part of the 28th SW Test and I hope you enjoy San Diego!



Jerry Broz, Ph.D.
General Chair
SW Test
SW Test Asia

2018

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PROGRAM SCHEDULE

SW Test 2018 Platinum Sponsors

(alphabetically)

CHPT

FormFactor™

international TEST SOLUTIONS

JEM

MJC®

MPI

TECHNOPROBE
Wafer Probing Technologies

TERADYNE

Xcerra
measured by your success

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PROGRAM SCHEDULE

SW Test 2018 Gold Sponsors

(alphabetically)

Melexis
INSPIRED ENGINEERING

Nidec SV TCL

PacTech
member of nagase group

RUDOLPH TECHNOLOGIES

STAr Technologies

T.I.P.S.
Technical Innovation - Physical Solutions

TEL
TOKYO ELECTRON

TRANSLARITY

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PROGRAM SCHEDULE

SW Test 2018 Silver Sponsors

(alphabetically)

APS

cmrsummit TECHNOLOGIES

ERS

FEINMETALL Contact Technologies

Johnstech

SEMICS

SCS SPECIALTY COATING SYSTEMS™ A KISCO Company

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PROGRAM SCHEDULE

Sunday, June 3

8 a.m. – 12 Noonish	7th Annual SW Test William Mann Golf Tournament
2:00 PM - 4:00 PM	Tutorials – Challenges for Stable Probing (Santiago Ballroom)
4:00 PM - 6:00 PM	REGISTRATION (Aragon South Foyer)
6:00 PM - 7:00 PM	RECEPTION (Aragon Lawn)
7:00 PM - 8:15 PM	Dinner in the Aragon II/III Ballroom
8:15 PM - 8:30 PM	Welcome SW Test 2018
8:30 PM - 9:45 PM	Keynote Presentation by Brett Debenham, Senior Director of Test Probe Central Engineering, Micron Technology, Inc., Boise, ID

Monday, June 4

7:00 AM - 5:00 PM	REGISTRATION / EXHIBITOR CHECK IN (Aragon South Foyer)
7:00 AM - 8:00 AM	CONTINENTAL BREAKFAST (Aragon Lawn)
8:00 AM - 10:00 AM	Wafer Test Trends and Complications (Aragon I/II)
10:00 AM - 10:30 AM	BREAK (Aragon Lawn)
10:30 AM - 12:00 PM	Advanced Probing Processes
12:00 PM - 1:00 PM	LUNCH (Aragon Lawn)
1:00 PM - 3:00 PM	All About The Probe !
2:30 PM - 3:00 PM	BREAK and POSTER SESSION (Aragon Foyer and Lawn)
3:00 PM - 5:00 PM	Dial Up the Frequency
5:00 PM - 8:00 PM	EXHIBITS OPEN w/ Dinner Served at RECEPTION STATIONS

Tuesday, June 5

7:00 AM - 3:00 PM	REGISTRATION (Aragon South Foyer)
7:00 AM - 8:00 AM	CONTINENTAL BREAKFAST (Aragon Lawn)
8:00 AM - 10:00 AM	Extreme Wafer Probing (Aragon I/II)
10:00 AM - 10:30 AM	BREAK and POSTER SESSION (Aragon Foyer and Lawn)
10:30 AM - 12:00 PM	More … Extreme Wafer Probing (Aragon I/II)
12:00 PM - 1:00 PM	LUNCH (Aragon Lawn)
1:30 PM - 3:00 PM	Probe Cleaning and Wafer Inspection
3:00 PM - 5:00 PM	EXHIBITS OPEN (Refreshments will be served)
6:00 PM - 9:00 PM	WORKSHOP SOCIAL – Drinks, Networking, Dinner and Entertainment in the Aragon Ballroom

Wednesday, June 6

7:30 AM - 10:00 AM	REGISTRATION (Aragon South Foyer)
7:00 AM - 8:00 AM	CONTINENTAL BREAKFAST (Aragon Lawn)
8:00 AM - 10:00 AM	Probe Potpourri (Aragon I/II)
10:00 AM - 10:30 AM	BREAK (Aragon Lawn)
10:30 AM - 11:30 PM	High Performance Space Transformers & PCB's (Aragon I/II)
11:30 AM to 12:00 PM	AWARDS (Aragon I/II)
12:00 PM	ADJOURNMENT (Aragon Lawn) … see you 2018 !

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PROGRAM SCHEDULE

Program Overview

The 28th Annual SW Test Workshop will be held at the Rancho Bernardo Inn in San Diego, California, from June 3-6, 2018. The conference will begin on Sunday morning with a golf tournament and Sunday afternoon with a topical tutorial, followed by a welcome reception, dinner, and a Keynote Speaker. The Technical Program will start Monday morning with 30-minute presentations in theme-oriented sessions. SW Test EXPO 2018 will showcase many of the key suppliers to the wafer probe industry and, as always, there will be ample opportunities for networking. This year, we will also feature two poster sessions during which attendees can meet with authors face-to-face. The conference will conclude on Wednesday at Noon after an awards presentation. Conference registration includes all meals, refreshments, social activities, and technical program and exhibit attendance, as well as the eProceedings.

last revised: 5/30/18

June 3, 2018 (Sunday)

7:00 AM - 1:00 PM	**7th Annual SW Test William Mann Golf Tournament**
7:00 - 8:00	Box Breakfast
8:00AM	Tee Off: Scramble, Reverse Shotgun Format

2:00 PM - 4:00 PM	**Tutorials Chair: Clark Liu (PTI – Taiwan)** **Santiago Ballroom**
	Probe Card Stability during High Temperature Testing Yan Chen (Nidec SV TCL – USA) and Trung Ngoc (Nidec SV TCL – Vietnam)
	A Novel Measurement Method for Measuring CCC and MAC At Once Dr. Matthias Schnaithmann, Achim Weiland, and Gunther Boehm (FEINMETALL GmbH – Germany)
	Advances in MEMS Spring Probe Technology for Wafer Test Applications Koji Ogiwara and Norihiro Ohta (Nidec SV TCL – Japan)
	Data Driven Comparison and Qualification of WLCSP Probe Technologies Bert Brost (Xcerra Corporation – USA)

4:00 PM - 6:00 PM	**REGISTRATION OPEN**
6:00 PM - 7:00 PM	**WELCOME RECEPTION (Aragon Lawn)**
7:00 PM - 8:15 PM	**BUFFET DINNER (Aragon Ballroom)**

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PROGRAM SCHEDULE

Keynote Presentation

8:15 PM - 9:45 PM	Evening Session in Aragon Ballroom
8:15 - 8:30	**Opening Remarks for SW Test 2018** Jerry Broz, Ph.D., SW Test General Chair
8:30 - 9:45	**KEYNOTE** **Leveraging Advanced Manufacturing to Address Challenges in the Automotive Memory Market** **Brett Debenham** *Senior Director of Test Probe Central Engineering* Micron Technology, Inc. Boise, ID **Abstract** Advanced manufacturing is enabling Industry 4.0. We will review key concepts and solutions enabled at Micron. This talk will review industry trends in the automotive market and the resulting memory test challenges needed to support these requirements. Additionally, we will touch on how Big Data can help move manufacturing environments toward the goal of zero-defects.



Mr. Brett Debenham is the Senior Director of Test Probe Central Engineering at Micron Technology, Inc., in Boise, Idaho. Since joining Micron in 1992, he has held various key technical and managerial positions for DRAM Probe and Test Engineering. Currently, he is responsible for managing Micron's global engineering for NVM and DRAM Probe, package test, module test, and SSD. Mr. Debenham earned a B.S. degree in Electrical Engineering from the University of Utah and holds multiple US

9:45 PM NETWORKING / HOSPITALITY SUITES

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SWTW
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PROGRAM SCHEDULE

June 4, 2018 (Monday)	
7:00 AM - 8:00 AM CONTINENTAL BREAKFAST **7:00 AM - 5:00 PM REGISTRATION**	
8:00 AM - 8:30 AM	**Welcome in Aragon Ballroom**
8:00 - 8:30	**Welcome to SWTW-2018** Jerry Broz, Ph.D., General Chair
8:30 AM - 10:00 AM	**SESSION 1: Wafer Test Trends and Complications** **Session Chair: Jerry Broz, Ph.D., SW Test General Chair**
8:30 - 9:00	**Probe Card Market Update** Lin Fu (VLSI Research – United Kingdom)
9:00 - 9:30	**Device interface complexity challenges of the next decade** Steve Ledford (Teradyne – USA)
9:30 - 10:00	**5G: The Next Disruptive Technology in Production Test** Daniel Bock, Ph.D., Mike Bishop, and Jeff Damm (FormFactor – Beaverton) Balbir Singh, Bob Murphy, Michael Hemena, and Michael Engelhardt (Intel – Folsom)
10:00 AM - 10:30 AM COFFEE BREAK	
10:30 AM - 12:00	**SESSION 2: Advanced Probing Processes** **Session Chair: Geert Gouwy (Melexis – Belgium)**
10:30 - 11:00	**Effects of Aluminum Pad Stack Thickness On the AOT/POT of a 1-TD Probing Process** Aaron Woodard and Alistair Laing (Micron Technology, USA) Miho Kitayama and Yuma Tanaka (Micronics Japan Corp. – Japan) Dick Duncan (MJC Electronics –USA)
11:00 - 11:30	**Probing solutions and inherent customization to enable advanced copper-based 3D integration schemes** Dong-pill Yang, and Jung-woo Sung (Samsung Electronics Co., Korea) Daniele Acconcia, Dr. Andrea Calaon, and Raffaele Vallauri (Technoprobe Spa – Italy)
11:30 - 12:00	**Leading-Edge Wide-I/O2 Memory Probing Challenges: TPEG™ MEMS Solution** Ferenc Fodor, and Erik Jan Marinissen (IMEC – Belgium) Raffaele Vallauri and Daniele Acconcia (Technoprobe – Italy)
12:00 NOON - 1:00 PM LUNCH ON THE LAWN	

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1:00 PM - 3:00 PM	SESSION 3: All About The Probe ! Session Chair: Darren James (Rudolph Technologies – USA)
1:00 - 1:30	**TPEG Mantis: a new solution for multiple advanced applications** Davide Sangiorgio, and Marco Sciurba (STMicroelectronics SPA – Italy) Tommaso Masi, and Riccardo Vettori (Technoprobe SpA – Italy)
1:30 - 2:00	**New probe design and development for high current capacity using bi-furcated structure** Joonyeon Kim (Samsung Electronics – Korea)
2:00 - 2:30	**Advanced cantilever probes showing similar advantages as their vertical opponent** Franz Steger (Texas Instruments Deuschland GmbH – Germany)
2:30 PM - 3:00 PM COFFEE BREAK	

Poster Session 1: 2:30 PM - 3:00 PM

Session Chair: John Caldwell (Micron Technology – Boise, USA)

- **Optimizing Probe Tip Cleaning and Shaping using Advanced Polymers**
  Alex Poles (International Test Solutions – USA)
- **Tri-Temperature Probing: -55C to >125C**
  Chris Buckholtz and Roger Sinsheimer (Teradyne, Inc – USA)
- **A second study on chuck automatic tilting and chuck force sensing for minimizing probe pin damage and optimization of overdrive**
  Byung-Hyun Shin (Semics – Korea)
- **Modern Probe Card Analysis… Addressing Emerging Needs Cost-Effectively**
  Kjell Lundberg, Greg Olmstead, Audria Hurst, and John Strom (Rudolph Technologies – USA)
- **Temperature Test on Wafer Level – History and Outlook in the Days of Advanced Packaging in Semiconductor**
  Harald Ibele (ERS electronic GmbH - Germany)

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PROGRAM SCHEDULE

3:00 PM - 5:00 PM	SESSION 4: Dial Up the Frequency! Session Chair: Joey Wu (STAr Technologies – Hsinchu, Taiwan)
3:00 - 3:30	**PCB Test Solution for 5th Generation Mobile Communications Presenter** Ching Fang Tseng and Norman Hsu (Chunghwa Precision Test Tech. Co. - Taiwan)
3:30 - 4:00	**WLCSP xWave for high frequency wafer probe applications** Jason Mroczkowski (Multitest – USA)
4:00 - 4:30	**TPEG™ MEMS RF+ Technology for Vertical Probe Heads** Tommaso Masi, Alberto Berizzi, Raffaele Vallauri, Andrea Calaon,and Daniele Acconcia (Technoprobe – Italy)
4:30 - 5:00	**Enabling High Parallelism in Production RF Test** Patrick Rhodes (FormFactor – Livermore)
EXHIBITS OPEN	

5:00 PM - 8:00 PM	SESSION 4: Exhibits Open in Expo Tent and Bernardo Expo Hall
5:00	**Expo Scavenger Hunt Begins** – Scan all participating exhibitors' bar codes for a chance to win fabulous prizes!
5:00 - 8:00	**Reception & Carving Station Dinner in Bernardo Hall Expo and Expo Tent**
EXHIBITS OPEN	

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PROGRAM SCHEDULE

SW Test 2018 EXPO

2018 EXHIBITORS

Accretech
Aehr Test Systems
Afore
Celadon Systems
Chunghwa Precision Test Tech.Co.,Ltd.
CMR Summit Technologies
Complete Probe Solutions Inc.
Delta V Instruments, Inc
Deringer-Ney Inc.
ERS electronic GmbH
Feinmetall GmbH
Ferrotec (USA) Corp.
FormFactor, Inc.
Harbor Electronics
Heraeus Deutschland GmbH & Co. KG
Hitachi Chemical Co., Ltd.
INNO Global
Instec, Inc.
Integrated Technology Corporation
Integrated Test Corporation
International Test Solutions
InTEST Corporation
IWIN CO.,Ltd.
JEM America Corp.
Johnstech International
K-Jet Laser Tek Inc.
Kanematsu USA Inc.
Kita USA Inc
Kyocera International, Inc.
LEENO Industrial Inc.
Leica Microsystems, Inc.
LeoLSI Co., Ltd.
MarTek, Inc
Melexis
Microfriend Inc.
Micronics Japan Co., Ltd.
MPI Corporation
Nextwave 360
Nidec SV TCL
NTK Technologies
Optec Laser Systems
OpTek Systems Inc.
Oxford Lasers
PacTech USA Inc.
Plastronics
Posalux SA
Prober.com
R&D Altanova
Reid-Ashman Mfg., Inc.
Rika Denshi America Inc.
Rudolph Technologies
Specialty Coating Systems
STAr Technologies, Inc.
T.I.P.S. Messtechnik Gmbh
Tanaka Precious Metals
Technoprobe America Inc.
Teradyne
Tokyo Electron Limited (TEL)
Translarity
Veco USA
Vermont Microtechnologies
WinWay Technology
Wooam Semitech
Xcerra Corporation

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2018 Exhibitors

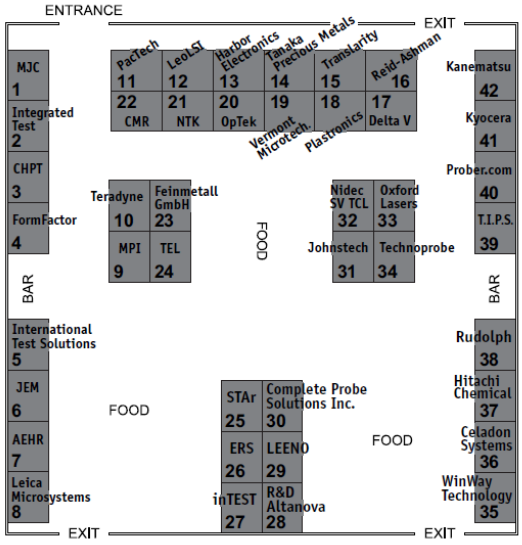
Bernardo Foyer/Ballroom Map



Booth	Company
B1	Heraeus Deutschland GmbH & Co. KG
B2	Nextwave 360
B3	Specialty Coating Systems
B4	INNO Global
101	IWIN Co., Ltd.
102	Posalux SA
103	Microfriend Inc.
104	Instec, Inc.
105	Wooam Semitech
106	Accretech
107	K-Jet Laser Tek Inc.
109	Ferrotec (USA) Corp.
110	Integrated Technology Corporation
200	Melexis
202	Optec Laser Systems
203	Xcerra Corporation
204	Afore
205	Kita USA Inc.
206	Deringer-Ney Inc.
207	MarTek, Inc.
209	Rika Denshi America Inc.
210	Veco USA

2018 Exhibitors

EXPO Tent Map



Booth	Company
1	Micronics Japan Co., Ltd.
2	Integrated Test Corporation
3	Chunghwa Precision Test Tech. Co., Ltd. (CHPT)
4	FormFactor, Inc.
5	International Test Solutions
6	JEM America Corp.
7	Aehr Test Systems
8	Leica Microsystems, Inc.
9	MPI Corporation
10	Teradyne
11	PacTech USA Inc.
12	LeoLSI Co., Ltd.
13	Harbor Electronics
14	Tanaka Precious Metals
15	Translarity
16	Reid-Ashman Mfg., Inc.
17	Delta V Instruments, Inc.
18	Plastronics
19	Vermont Microtechnologies
20	OpTek Systems Inc.
21	NTK Technologies
22	CMR Summit Technologies
23	Feinmetall GmbH
24	Tokyo Electron Limited (TEL)
25	STAr Technologies
26	ERS electronic GmbH
27	inTEST Corporation
28	R&D Altanova
29	LEENO Industrial Inc.
30	Complete Probe Solutions Inc.
31	Johnstech International
32	Nidec SV TCL
33	Oxford Lasers
34	Technoprobe America Inc.
35	WinWay Technology Co., Ltd.
36	Celadon Systems
37	Hitachi Chemical Co., Ltd.
38	Rudolph Technologies
39	T.I.P.S. Messtechnik Gmbh
40	Prober.com
41	Kyocera International Inc.
42	Kanematsu USA Inc.

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June 5, 2018 (Tuesday)	
7:00 AM - 8:00 AM CONTINENTAL BREAKFAST	
7:00 AM - 3:00 PM REGISTRATION OPEN	
8:00 AM - 10:00 AM	**SESSION 5: Extreme Wafer Probing (ONE)!** **Session Chair: Karen Armendariz (Celadon Systems – USA)**
8:00 - 8:30	**Break the Myth of Wafer Probing On Cu for Fan-out Wafer Level Packaging (FOWLP)** Amy Leong and Ashish Bhardwaj (FormFactor Inc. – Livermore) Chang-Hoon Hyun (Samsung Electronics/S.LSI Division – Korea) KH Kim (FormFactor Inc – Korea)
8:30 - 9:00	**Micro burn-in techniques at wafer-level test to implement cost effective solutions** Geert Gouwy and Arnaud Devos (Melexis – Ieper, Belgium) Dr. Alessandro Antonioli and Raffaele Vallauri (Technoprobe Spa – Italy)
9:00 - 9:30	**Carbon Nanotube Based Microprobe Design for Electromechanical Probing Applications at Wafer Level Chip Scale and Wafer Level Packaging** Mehmet Tas, Dr. Vlad Stolojan,and Mark Baker (University of Surrey –UK) Jedidiah Bentz (Smiths Interconnect – USA) Dr. Keir Boxshall (Smiths Group – UK)
9:30 - 10:00	**Test Cell Co-Planarity Optimization** Troy Harnisch (Teradyne, Inc. – USA)
10:00 AM - 10:30 AM COFFEE BREAK	

Poster Session 2: 10:00 AM - 10:30 AM

Session Chair: Mark Ojeda (Cypress Semiconductor – San Jose, USA)

- **Improvements in Laser Drilled Hole Geometries for Probe Card Applications**
  Andrew Webb (OpTek Systems Inc. – Greenville, USA)
  Dr. Mike Osborne (OpTek Systems Ltd. – UK)

- **Improvements in small pitch capability**
  Dr. Alan Ferguson (Oxford Lasers – UK)

- **Effect of Ceramic on Laser**
  Man-Seob Lee (Dawon Nexview – South Korea)

- **Innovative Laser Micro-Machining Improves Probe Card Fabrication in Many Ways**
  Hung-Lung Chen (KJet Laser Tek Inc. – HsinChu City, Taiwan)

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10:30 AM - 12:00	**SESSION 6: Extreme Wafer Probing (TWO)!** **Session Chair: Patrick Mui (JEM America – USA)**
10:30 - 11:00	**Known Good "Power" Die: Diced Wafer Test at 7 kV and 1000 A** Dr. Rainer Gaggl (T.I.P.S. Messtechnik GmbH – Austria), Mauro Serra (CREA s.r.l. – Italy) Ernest Fischer (INFOTECH AG – Switzerland)
11:00 - 11:30	**Vertical MEMS Probe Card Applied to High Speed Loopback Test of Network Communication IC** Haiyong Song, and Zheng Li (Hisilicon Technologies Co., A Huawei Company – China) Adolph Cheng, Fred Chou, Alex Wei, Jessie Deng, Zach Hsieh, and Bobby Chen (MPI Corporation – Chu-Pei, Taiwan)
11:30 - 12:00	**A Real-Life Pad Crack Study** Gunther Boehm (FEINMETALL GmbH – Germany) Jory Twitchell (NXP Semiconductor, USA)
12:00 NOON - 1:00 PM	**LUNCH ON THE LAWN**
1:00 PM - 3:00 PM	**SESSION 7: Probe Cleaning and Wafer Inspection** **Session Chair: Suz Ramsbottom (Texas Instruments – Dallas)**
1:00 - 1:30	**Fast Probe Mark Inspection (PMI)** Imran Ahmed (Texas Instruments Inc – Dallas)
1:30 - 2:00	**Cleaning Material Evaluations on Advanced MEMS and Vertical Technologies** Vincent Ellis (Texas Instruments, Inc. – Dallas)
2:00 - 2:30	**OCR Automation** Hector Moreno (Texas Instruments Inc. – Dallas)
2:30 - 3:00	**New Approach in Pogo Pin Socket Design to Improve Total Cost of Ownership** Richard Incognito (Texas Instruments – Philippines)
3:00 PM - 5:00 PM	**EXHIBITS OPEN**
3:00 - 5:00	**PM Break – Refreshments Served in both Expo Tent and Bernardo Expo Hall** **Expo Scavenger Hunt Continues** – Scan all participating exhibitors' bar codes for a chance to win fabulous prizes!

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PROGRAM SCHEDULE

Tuesday Evening Social Event	
6:00 PM - 7:00 PM	**Cocktails and Networking on the Patio and Lawn**
7:00 PM - 9:00 PM	**Dinner and Entertainment in the Aragon Ballroom with Kim Michael Polote, the "Southern Songstress" and Tony Guerrero, an award winning West Coast jazz entertainer.**



Traveling and hailing from the East Coast, Kim is a world renowned, vocal powerhouse who has performed all over the world. Sharing the stage with several greats including Al Green, Harry Connick Jr, and Charlie Daniels, this award-winning songbird will join forces with the West Coast critically acclaimed entertainer Mr. Tony Guerrero, for a one-night only, first-time appearance together.



Tony is a songwriter, producer and an incredible jazz trumpeter with a career spanning nearly 30 years. He's played on over 200 albums by other artists as diverse as Paul McCartney, Nancy Wilson, Joe Sample and recently Dick Van Dyke and Jane Lynch of the TV series Glee to name a few.

Accompanied by an amazing quartet of stellar musicians, this dynamic duo will take you on an exciting, fun journey celebrating an array of musical selections and genres. The dazzling collaboration of these East/West coast fireball performers is sure to spark an evening of unforgettable musical fireworks!

Join us for an evening of great food and fabulous music and entertainment, as well as the announcement of all the winners of our 1st annual Expo Scavenger Hunt.

9:00 PM	**NETWORKING / HOSPITALITY SUITES**

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June 6, 2018 (Wednesday)

7:00 AM - 8:00 AM CONTINENTAL BREAKFAST	
7:30 AM - 10:00 AM REGISTRATION OPEN	
8:00 AM - 10:00 AM	**SESSION 8: Probe Potpourri!** **Session Chair: Dr. Michael Huebner (FormFactor – Livermore)**
8:00 - 8:30	**Design and Analysis of Space Transformer with Hybrid Circuit Design on Probe Card** Tae Kyun Kim, and Yong Ho Cho (Microfriend Inc. – Korea) SangKyu Yoo (Samsung Electronics – Korea) Jong Gwan Yook (Yonsei Univ. – Korea)
8:30 - 9:00	**Automated Probe-Mark Analysis** Yu-Rong Jian and Prof. Cheng-Wen Wu (National Tsing Hua University – Taiwan) Ferenc Fodor and Erik Jan Marinissen (IMEC – Belgium), Prof. Cheng-Wen Wu (National Tsing Hua University – Taiwan)
9:00 - 9:30	**New Probe Testing Methodology-Over Current Analysis of Probe** Ching Fang Tseng and Norma Hsu (Chunghwa Precision Test Tech. Co.,Ltd. – Taiwan)
9:30 - 10:00	**Advances in metrology for guide plate analysis** Dr. Alan Ferguson (Oxford Lasers – UK)
10:00 AM - 10:30 AM COFFEE BREAK	
10:30 AM - 12:00	**SESSION 9: High Performance Space Transformers & PCB's** **Session Chair: Rey Rincon (SWTest – Austin, USA)**
10:30 - 11:00	**Sub-milliOhm impedances on a thick probe card? No problem!** Sandeep Sankararaman (R&D Altanova – USA)
11:00 - 11:30	**An introduction for novel multi-layer thin film substrates applied in space transformers** Dr. Chih-Kuang Yang (Princotest Co. Ltd. – Taiwan)
11:30 - 12:00	***Awards Presentations*** Jerry Broz and Rey Rincon (SW Test General Chair and Program Chair) Presenter: Jerry Broz (SW Test General Chair)
12:00 NOON – ADJOURNMENT … See you next year in San Diego or at SW Test Asia in Taiwan.	

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PROGRAM SCHEDULE

SWTEST ASIA 2018

Join us for the world premiere of the 1st annual SW Test Asia

October 18-19, 2018
Sheraton Hsinchu Hotel, Zhubei City, Taiwan (R.O.C.)

SW Test Asia is a one and a half day conference located at the beautiful Sheraton Hsinchu Hotel in Hsinchu, Taiwan featuring a perfect mixture of manufacturer and vendor technical presentations highlighting the "Best of SW Test 2018" in San Diego, as well as new regional presentations. SW Test Asia is a probe technology forum where attendees come to learn about recent developments in the industry and exchange ideas and solutions in a relaxed atmosphere.

The conference will also feature an Expo with over 30 exhibiting companies. The Expo will be enhanced with tea breaks, lunch buffets and cocktail receptions in the Expo Hall, providing excellent opportunities to visit with exhibitors and network with friends and colleagues. Also featured will be a Tech Showcase in the Expo Hall with 15-minute presentations from our Platinum Corporate Sponsors.

Join us at SW Test Asia in Hsinchu, Taiwan, October 18-19, 2018 for the semiconductor industry's premiere event!





Check out the SW Test Asia website for more information, to register and to add your name to the mailing list.
www.swtestasia.org

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PROGRAM SCHEDULE



Save The Dates

SW Test Workshop 2019

Rancho Bernardo Inn,
San Diego, CA

June 2 - 5, 2019

Abstract Submission Date
March 5, 2019

Golf Tournament
June 2, 2019

See You Next Year!

TERMS of SERVICE

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Technical Program
SW Test 2018

Monday, June 4, 2018

Monday, June 4, 2018

8:00 AM – Welcome to SW Test 2018

Jerry Broz, Ph.D. (SW Test General Chair)

8:30 to 10:00 AM – Wafer Test Trends and Complications

Probe Card Market Update

Lin Fu, Ph.D. (VLSI Research – UK)

Device interface complexity challenges of the next decade

Steve Ledford (Teradyne – USA)

5G: The Next Disruptive Technology in Production Test

Daniel Bock, Ph.D., Mike Bishop, and Jeff Damm (FormFactor – Beaverton)

Balbir Singh, Bob Murphy, Michael Hemena, and Michael Engelhardt (Intel – Folsom)

Monday, June 4, 2018

10:30 AM to Noon – Advanced Probing Processes

Effects of Aluminum Pad Stack Thickness On the AOT/POT of a 1-TD Probing Process

Aaron Woodard and Alistair Laing (Micron Technology, USA); Miho Kitayama and Yuma Tanaka (Micronics Japan Corp. – Japan), and Dick Duncan (MJC Electronics –USA)

Probing solutions and inherent customization to enable advanced copper-based 3D integration schemes

Dong-pill Yang, and Jung-woo Sung (Samsung Electronics Co., Korea)
Daniele Acconcia, Dr. Andrea Calaon, and Raffaele Vallauri (Technoprobe Spa – Italy)
Presenters - Dr. Emanuele Bertarelli (Technoprobe – Italy) and Daniel Lee (Technoprobe - Korea)

Leading-Edge Wide-I/O2 Memory Probing Challenges: TPEG™ MEMS Solution

Ferenc Fodor, and Erik Jan Marinissen (IMEC – Belgium)
Raffaele Vallauri and Daniele Acconcia (Technoprobe – Italy)

Monday, June 4, 2018

1:00 to 2:30 PM – All About The Probe !

TPEG Mantis: a new solution for multiple advanced applications

Davide Sangiorgio, and Marco Sciurba (STMicroelectronics SPA – Italy)

Tommaso Masi, and Riccardo Vettori (Technoprobe SpA – Italy)

New probe design and development for high current capacity using bi-furcated structure

Joonyeon Kim (Samsung Electronics – Korea)

Advanced cantilever probes showing similar advantages as their vertical opponent

Franz Steger (Texas Instruments Deuschland GmbH – Germany)

Monday, June 4, 2018

2:30 to 3:00 PM – Poster Session 1

Optimizing Probe Tip Cleaning and Shaping using Advanced Polymers
Alex Poles (International Test Solutions – USA)

Tri-Temperature Probing: -55C to >125C
Chris Buckholtz and Roger Sinsheimer (Teradyne, Inc. – USA)

A second study on chuck automatic tilting and chuck force sensing for minimizing probe pin damage and optimization of overdrive
Byung-Hyun Shin (Semics – Korea)

Modern Probe Card Analysis… Addressing Emerging Needs Cost-Effectively
Kjell Lundberg, Greg Olmstead, Audria Hurst, and John Strom (Rudolph Technologies – USA)

Temperature Test on Wafer Level – History and Outlook in the Days of Advanced Packaging in Semiconductor
Harald Ibele (ERS electronic GmbH - Germany)

Monday, June 4, 2018

3:00 to 5:00 PM – Dial Up the Frequency!

PCB Test Solution for 5th Generation Mobile Communications

Ching Fang Tseng and Norman Hsu (Chunghwa Precision Test Tech. Co. - Taiwan)

WLCSP xWave for high frequency wafer probe applications

Jason Mroczkowski (Multitest – USA)

TPEG™ MEMS RF+ Technology for Vertical Probe Heads

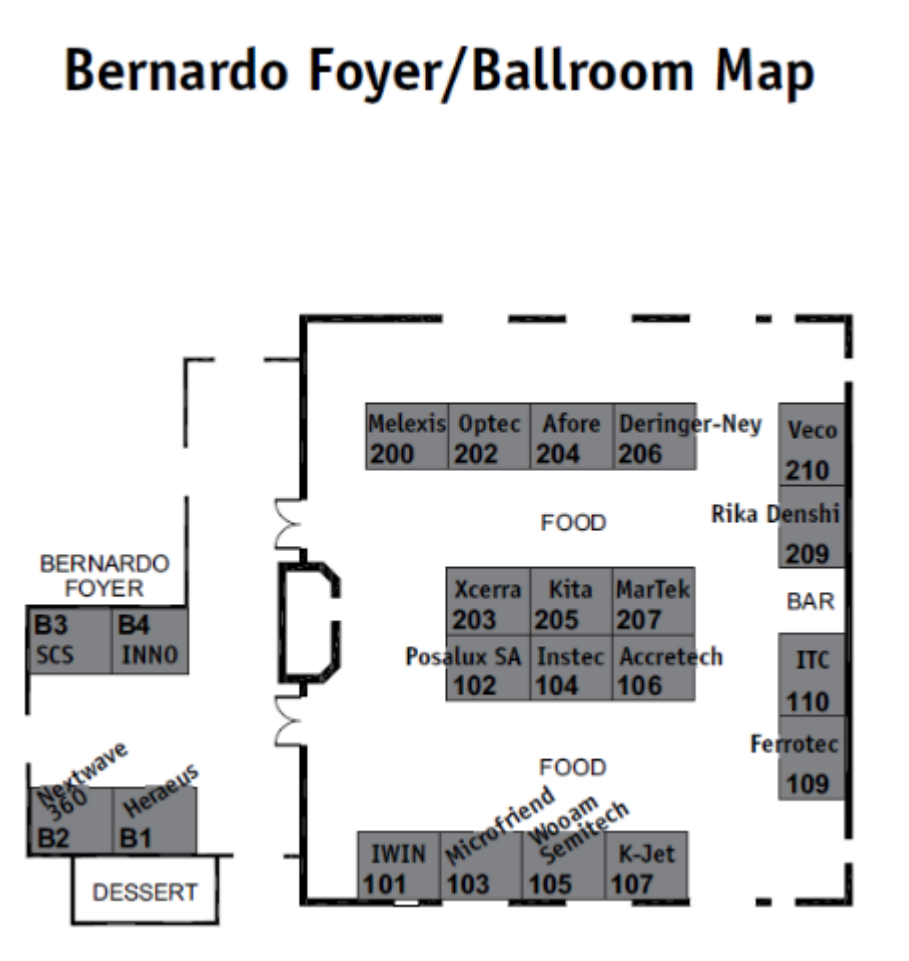
Tommaso Masi, Alberto Berizzi, Raffaele Vallauri, Andrea Calaon, and Daniele Acconcia (Technoprobe – Italy)

Enabling High Parallelism in Production RF Test

Patrick Rhodes (FormFactor, Inc. – Livermore)

Monday, June 4, 2018

5:00 to 8:00 PM – SW Test EXPO

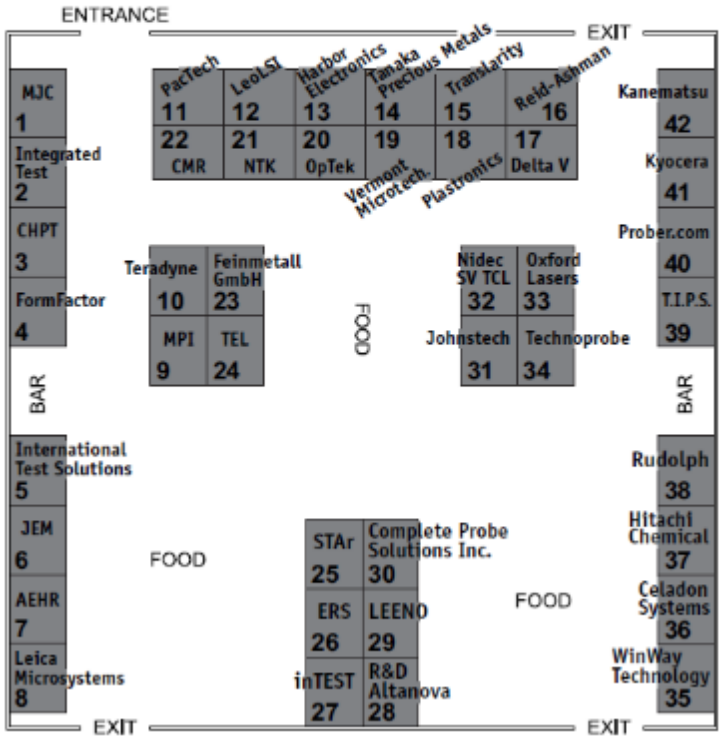


Booth	Company
B1	Heraeus Deutschland GmbH & Co. KG
B2	Nextwave 360
B3	Specialty Coating Systems
B4	INNO Global
101	IWIN Co., Ltd.
102	Posalux SA
103	Microfriend Inc.
104	Instec, Inc.
105	Wooam Semitech
106	Accretech
107	K-Jet Laser Tek Inc.
109	Ferrotec (USA) Corp.
110	Integrated Technology Corporation
200	Melexis
202	Optec Laser Systems
203	Xcerra Corporation
204	Afore
205	Kita USA Inc.
206	Deringer-Ney Inc.
207	MarTek, Inc.
209	Rika Denshi America Inc.
210	Veco USA

Monday, June 4, 2018

5:00 to 8:00 PM – SW Test EXPO

EXPO Tent Map



Booth	Company
1	Micronics Japan Co., Ltd.
2	Integrated Test Corporation
3	Chunghwa Precision Test Tech. Co., Ltd. (CHPT)
4	FormFactor, Inc.
5	International Test Solutions
6	JEM America Corp.
7	Aehr Test Systems
8	Leica Microsystems, Inc.
9	MPI Corporation
10	Teradyne
11	PacTech USA Inc.
12	LeoLSI Co., Ltd.
13	Harbor Electronics
14	Tanaka Precious Metals
15	Translarity
16	Reid-Ashman Mfg., Inc.
17	Delta V Instruments, Inc.
18	Plastronics
19	Vermont Microtechnologies
20	OpTek Systems Inc.
21	NTK Technologies

Booth	Company
22	CMR Summit Technologies
23	Feinmetall GmbH
24	Tokyo Electron Limited (TEL)
25	STAr Technologies
26	ERS electronic GmbH
27	inTEST Corporation
28	R&D Altanova
29	LEENO Industrial Inc.
30	Complete Probe Solutions Inc.
31	Johnstech International
32	Nidec SV TCL
33	Oxford Lasers
34	Technoprobe America Inc.
35	WinWay Technology Co., Ltd.
36	Celadon Systems
37	Hitachi Chemical Co., Ltd.
38	Rudolph Technologies
39	T.I.P.S. Messtechnik Gmbh
40	Prober.com
41	Kyocera International Inc.
42	Kanematsu USA Inc.

Come visit SW Test Asia …



See you Next Year in San Diego …



Technical Program
SW Test 2018

Monday, June 4, 2018



SW Test Workshop

Semiconductor Wafer Test Workshop

Welcome to the 28th Annual SW Test Workshop

Jerry Broz, Ph.D.

SW Test General Chair

June 3-6, 2018

Welcome Rancho Bernardo Inn !





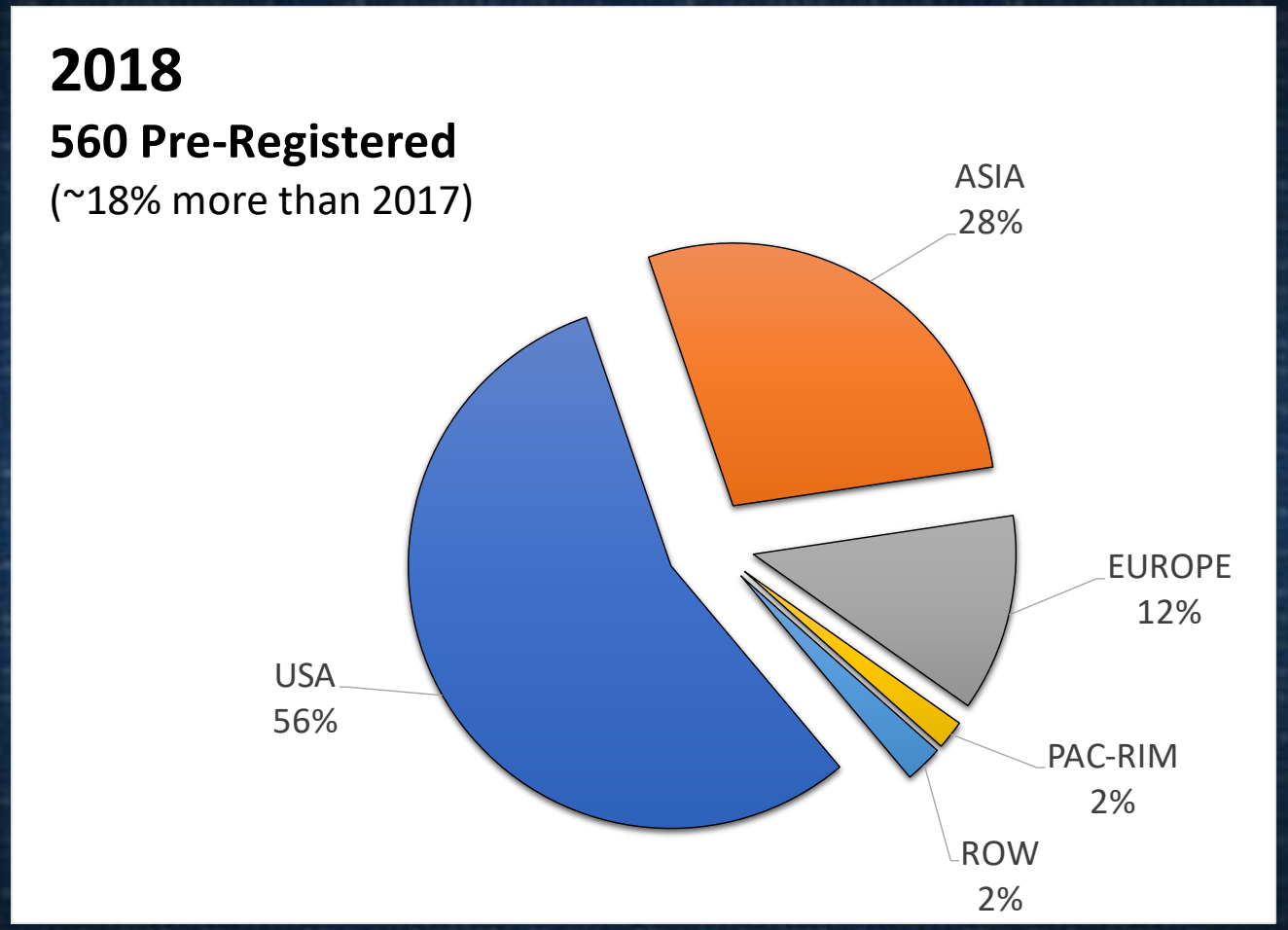
Twenty-Eight Years of Probe Technology !

More than 9000 total attendees in 28 years !



SW Test Workshop | June 3-6, 2018

SW Test 2018 International Participation



30 out of the 48 Presentations have at least one international author !

Semiconductor Wafer Test – SW Test

- **SW Test IS a Probe Technology Forum …**
  - It is "*THE*" Conference for Wafer Test Professionals
  - Practical solutions to real problems
  - Balanced mixture of semiconductor manufacturer, and supplier as well as collaborative presentations
- **Informal Conference …**
  - Grass roots workshop style conference that is focused technical exchange
  - Great social activities and informal discussions
  - Meet new people and have a little fun !
- **"Green Initiative" …**
  - eProceedings and enviro-friendly practices

SW Test 2018 eProceedings



Password for Sunday = mockingbird

Password for Monday = bunting

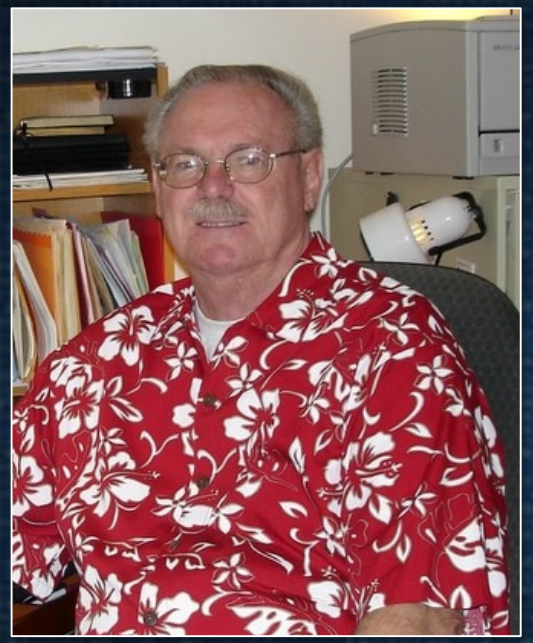
- Each day of the conference will be available in an e-Version for download in a password protected file.
  - Go to … http://www.swtest.org
  - Ballroom WiFi Password = aragon2018
- Free WiFi access will be available during the entire conference to allow attendee access to the downloads.
- Daily passwords to the download files will be announced through each day, respectively.
- The non-password locked files will be made available in the SW Test Archives after the conference adjourns.

New for 2018 … SW Test Mobile App



- Up-to-the-minute “Event Info”
- Schedules of the “Sessions”
- Meet the “Session Chairs and Presenters”
- Network with the “Attendees”
- Get important updates with “SW Test News”
- Connect with the “Sponsors” and “Exhibitors”
- Attend the “Social Events”
- Find treasure during the “Scavenger Hunt”
- Get oriented on the “Map”
- Learn about “SW Test Asia”

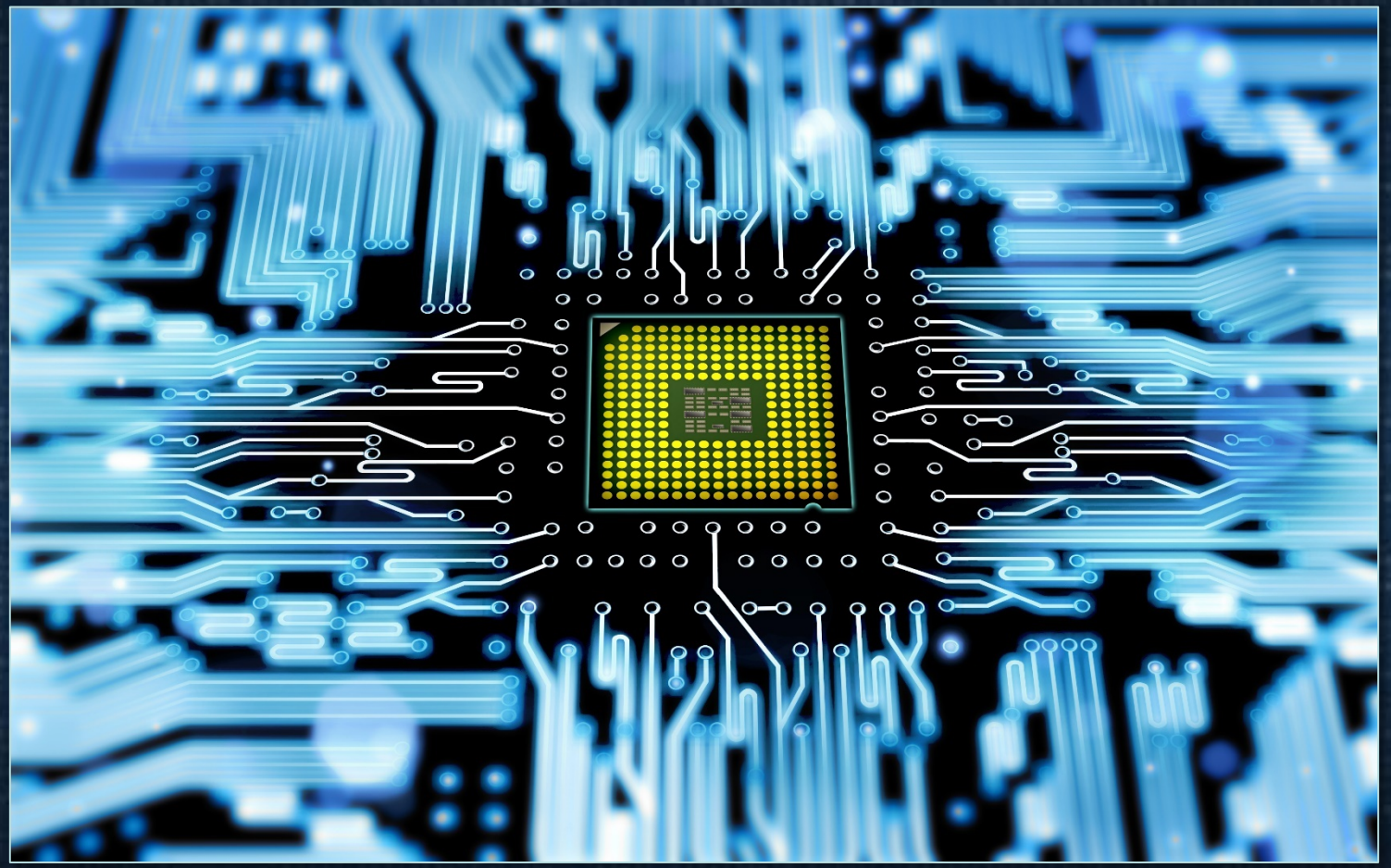
William R. Mann Student Travel Grant



Bill Mann
Founder of SW Test
Chair Emeritus

- **Partially funded by the SW Test annual Golf Tournament's "Beat the Pro" hole contest and several hundred dollars each year.**
- **"William R. Mann Student Travel Grant" is being awarded to three recipients in 2018.**
  - **Alex Poles, a B.Sc. Student from The University of Nevada, Reno.**
  - **Gaurav Rajavendra Reddy, a Ph.D. Student, from The University of Texas at Dallas.**
  - **Mehmet Tas, a Ph.D. Research Student, from University of Surrey, Guildford, Surrey, UK**
- **SW Test provides a stipend of up to $1,000 to cover expenses for travel, hotel accommodations and student registration.**

Ever Changing Semiconductor Landscape



WOW ! … 2017 Was A Great Year for SEMI !

- Semiconductor revenue grew 21.7% … reaching $429.1 billion !
- Overall, the memory device sector grew the most at 60.8%.
  - DRAM grew 76.7%
  - NAND grew 46.6%
  - Highest growth rate for both memory subcategories in 10 years.
  - Increase was based on higher prices and increased demand for memory chips, relative to tight supply.
- Samsung had a YoY growth of 53.6% and displaced Intel as top supplier.
- Hynix and Micron had record YoY growth at 81.2% and 79.7%, respectively.
- Overall, the semiconductor industry grew 9.9% over last year
  - Solid unit-sales growth and strong demand across all applications, regions and technologies.

Worldwide Rankings of Top 10 Suppliers

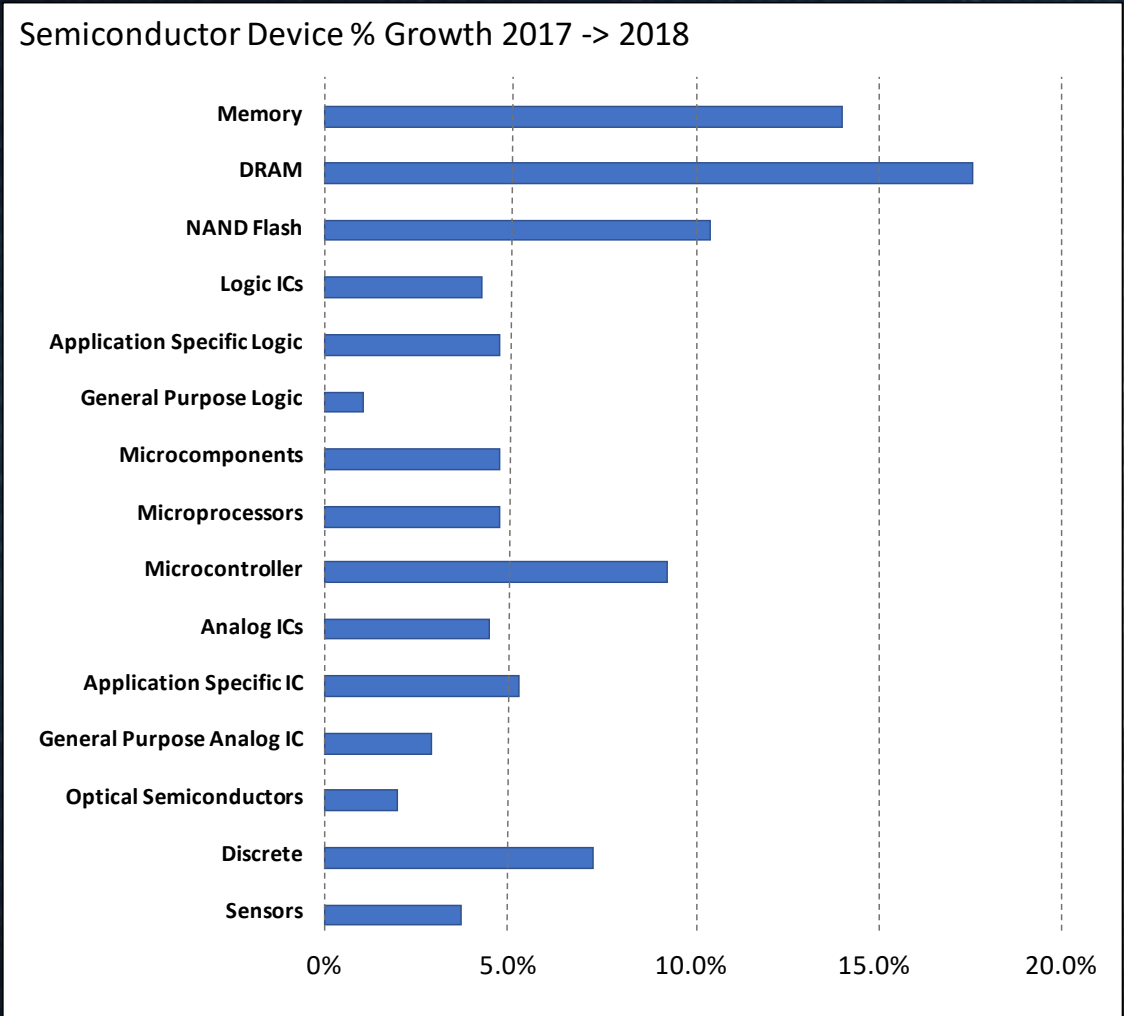
Worldwide Ranking of the Top-10 Suppliers of Semiconductors in 2017
(Ranking by Revenue in Millions of USD)

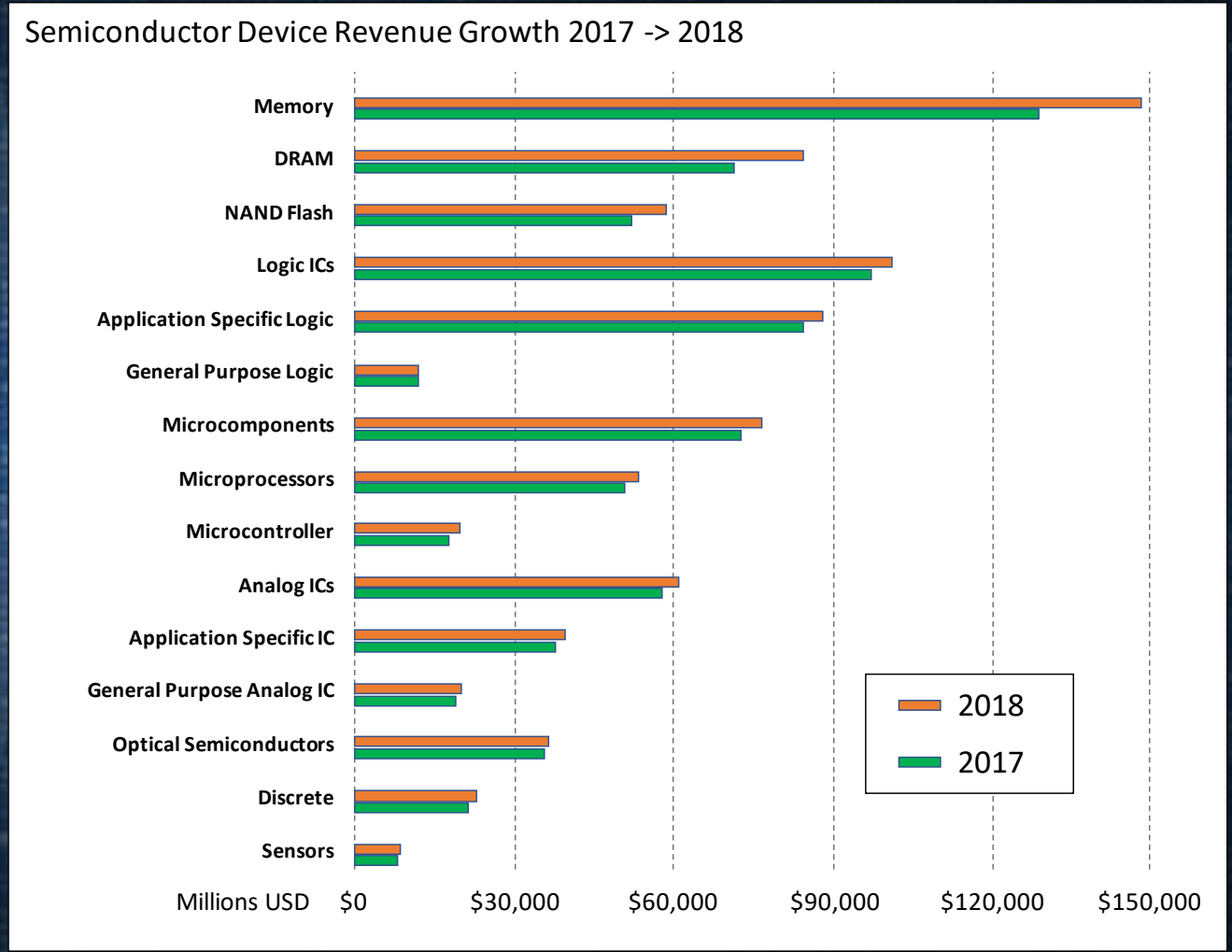
2016 Rank	2017 Rank	Company Name	2016 Revenue ($)	2017 Revenue ($)	Revenue Percent Change	Revenue Percent of Total
2	1	Samsung Electronics	40,389	62,031	53.6%	14.5%
1	2	Intel	54,980	61,406	11.7%	14.3%
5	3	SK Hynix	14,699	26,683	81.2%	6.2%
7	4	Micron Technology	12,210	22,843	79.7%	5.3%
4	5	Broadcom Ltd	14,979	17,375	16.0%	4.0%
3	6	Qualcomm	15,405	16,872	9.5%	3.9%
6	7	Texas Instruments	12,836	14,525	13.2%	3.4%
8	8	Toshiba	9,904	11,864	19.8%	2.8%
9	9	NXP	9,306	8,864	-4.7%	2.1%
13	10	nVidea	6,030	8,578	42.3%	2.0%
		Top 10 Companies	191,923	250,996	31.2%	58.5%
		All Others	161,356	178,112	10.4%	41.5%
		Total Semiconductor	352,594	429,108	21.7%	100.0%

Source: HIS Markit Q1 2018 Competitive Landscape

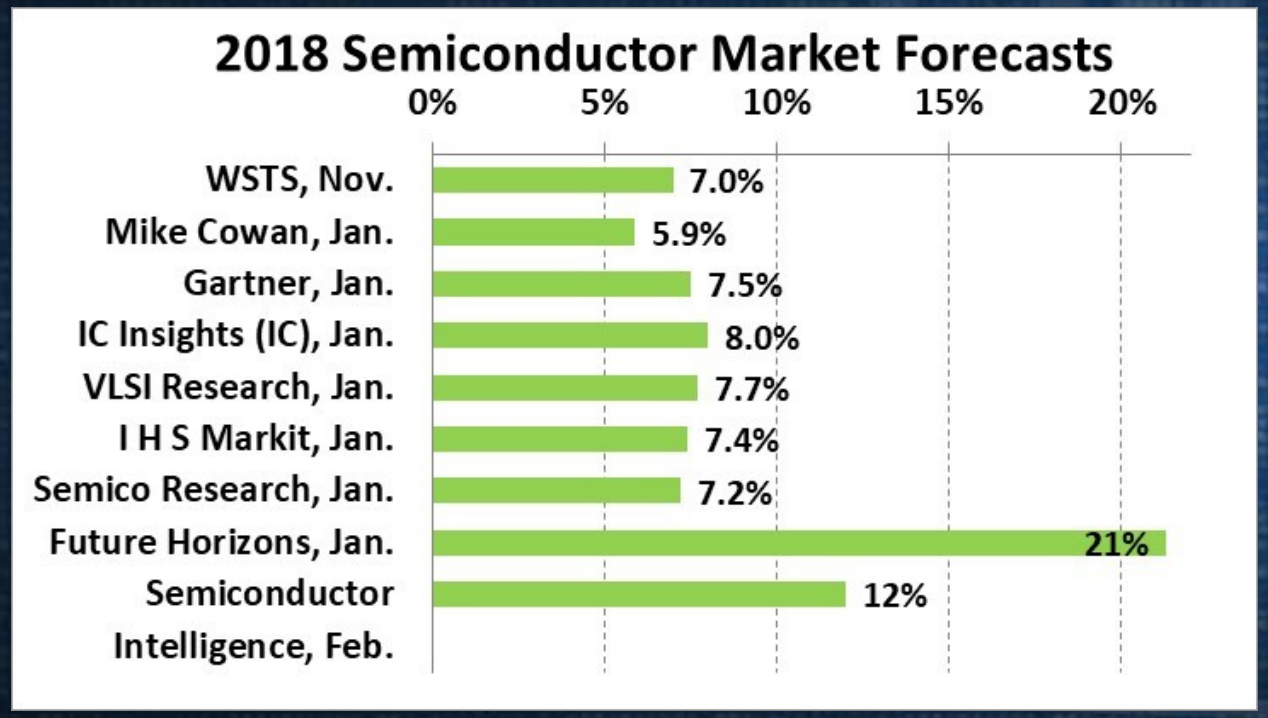
2018 HIS Markit

Where Are The Chips Going ?

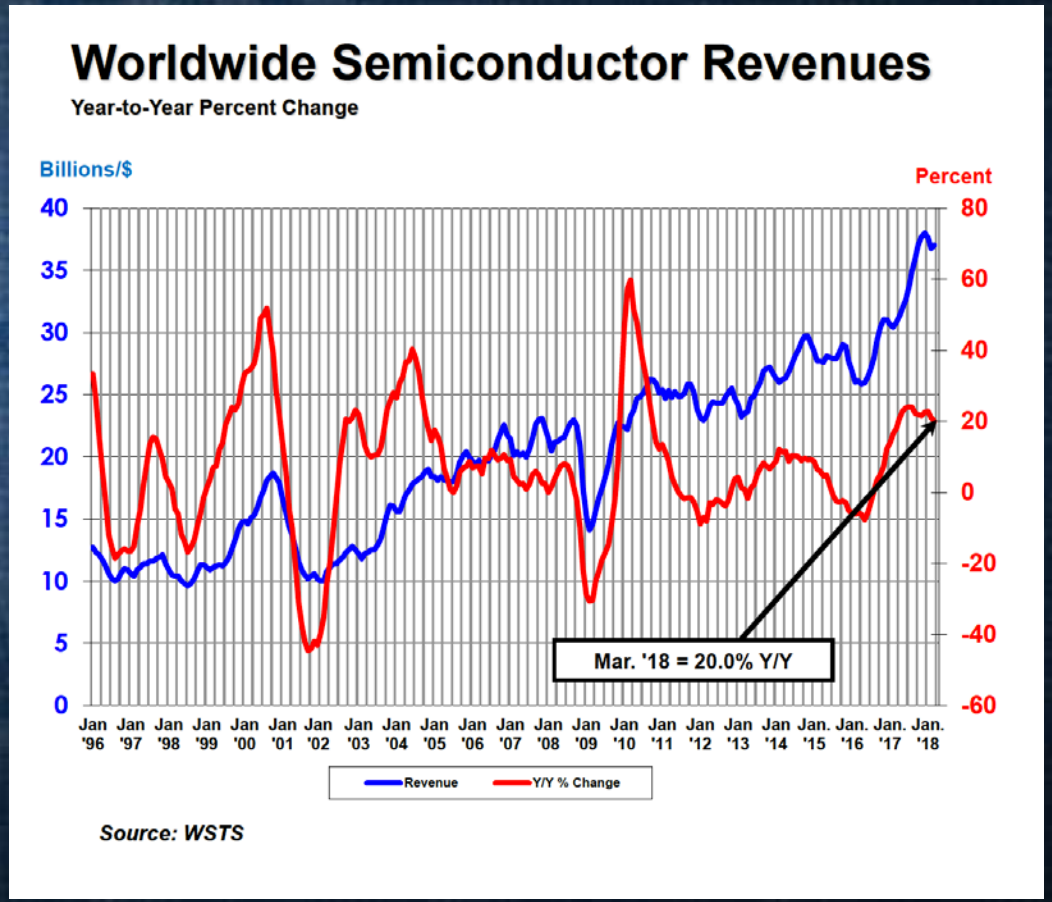




Semi Market Growth Predictions



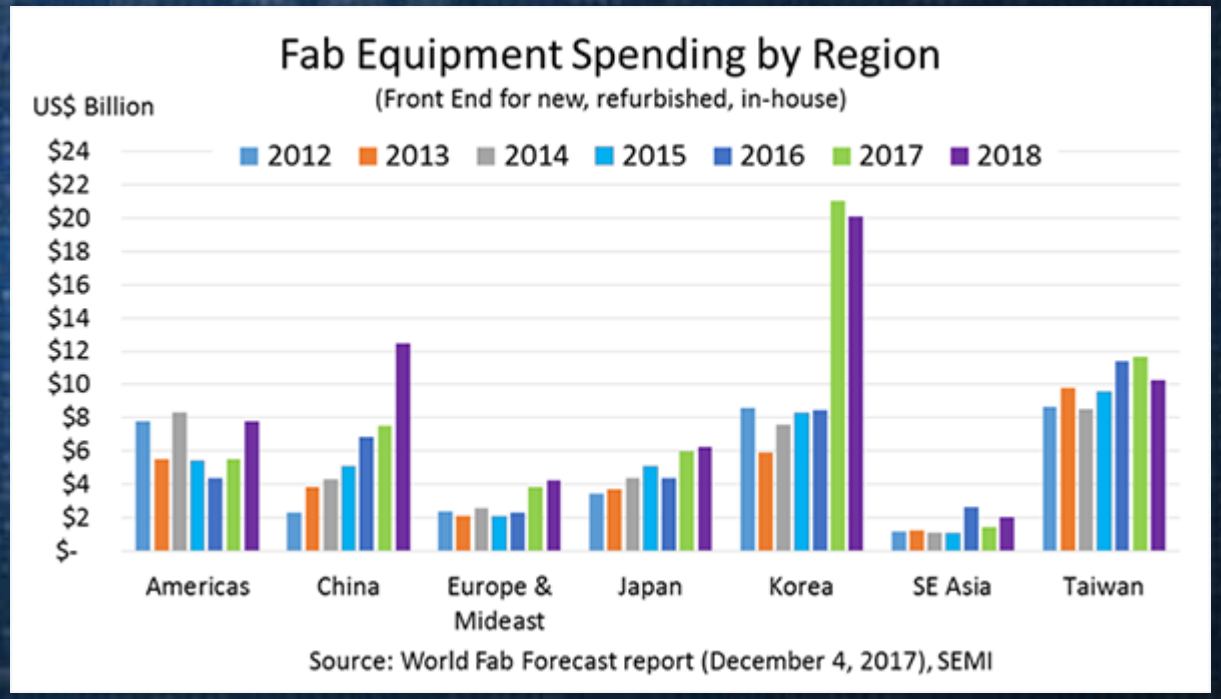
Q1-2018 is far exceeding sales through the same point in 2017, which was a record year !



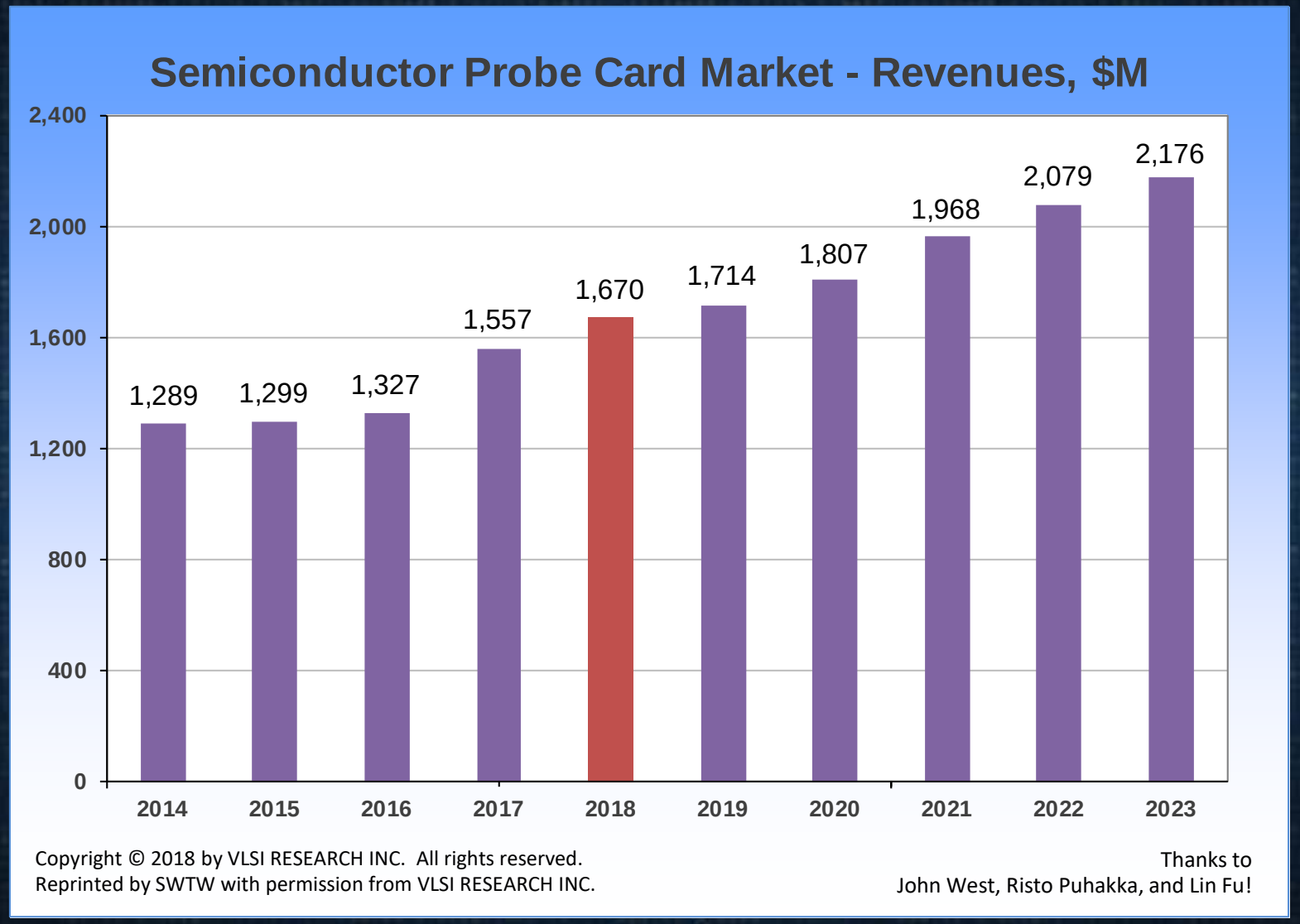
Changes to the Semiconductor Landscape

China keeps moving from a #1 Consumer to becoming a Device Producer

- **China Integrated Circuit Investment Fund of $47.4 billion for the development of China's semiconductor industry.**
- **Once (if) all FABs move into production**
  - China's total 300mm-equalvent output is projected to more than triple
  - From 400,000 wafer starts per month today to more than 1.4 million by 2020
  - 60% of the output for memory and 40% for logic.



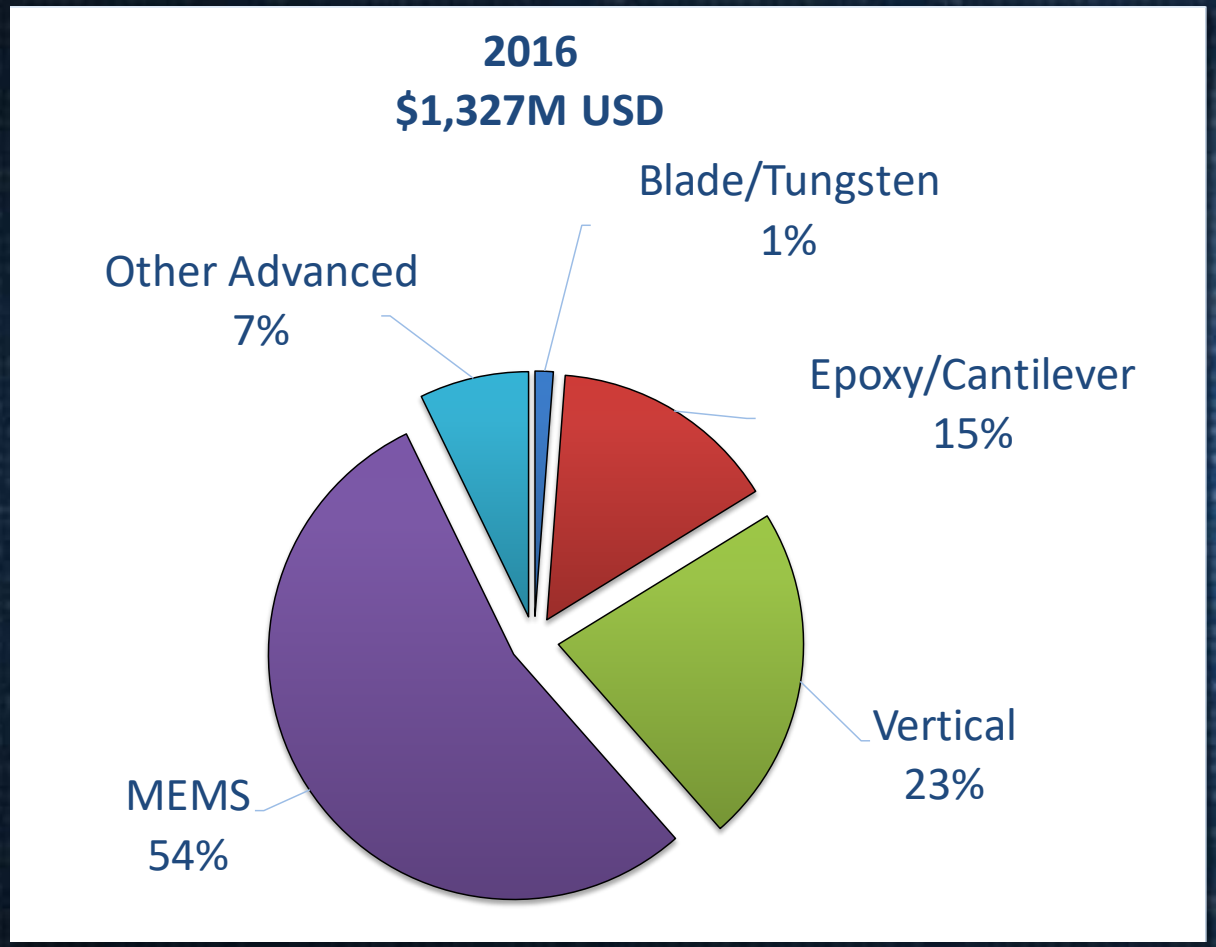
Probe Card Industry Revenues

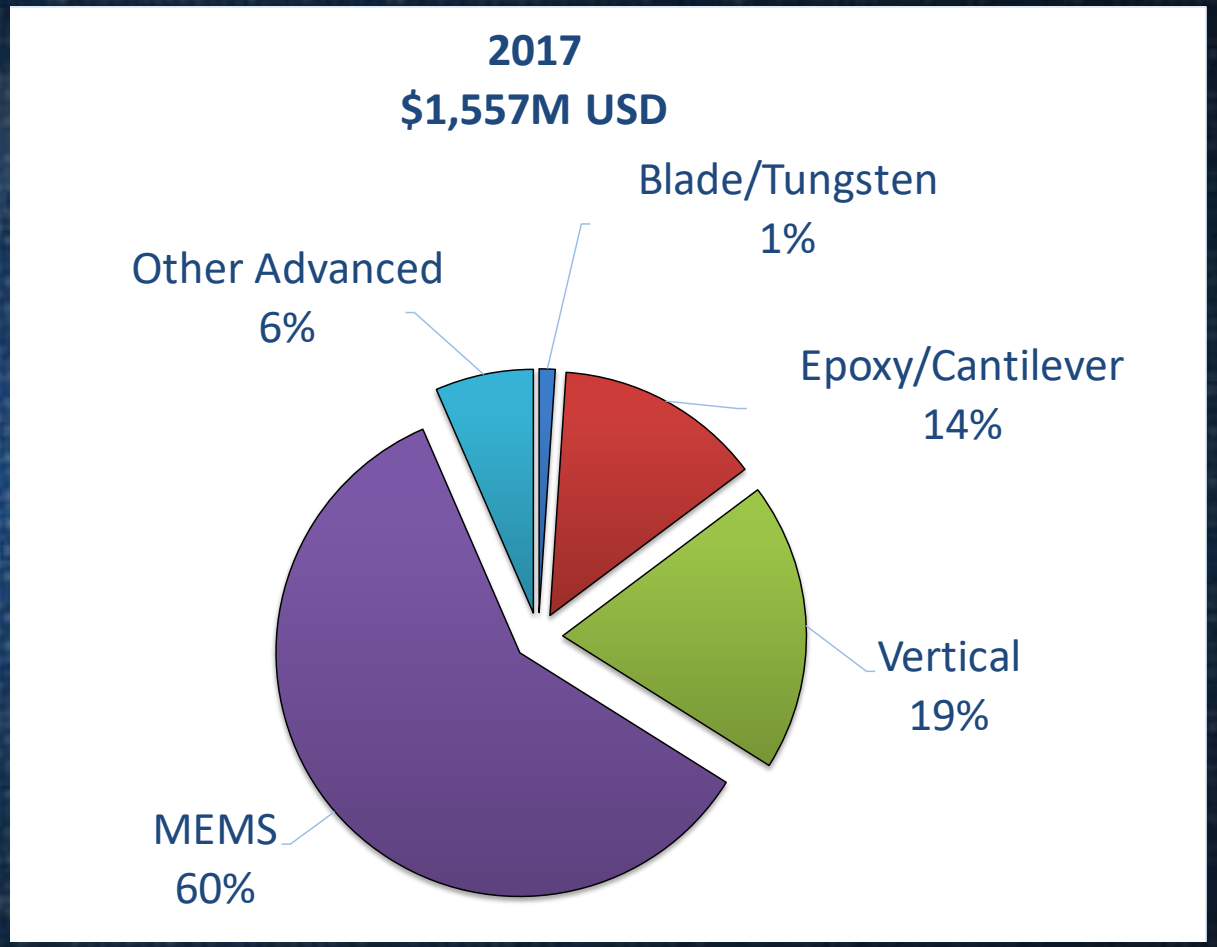


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2017 Revenues by Technology

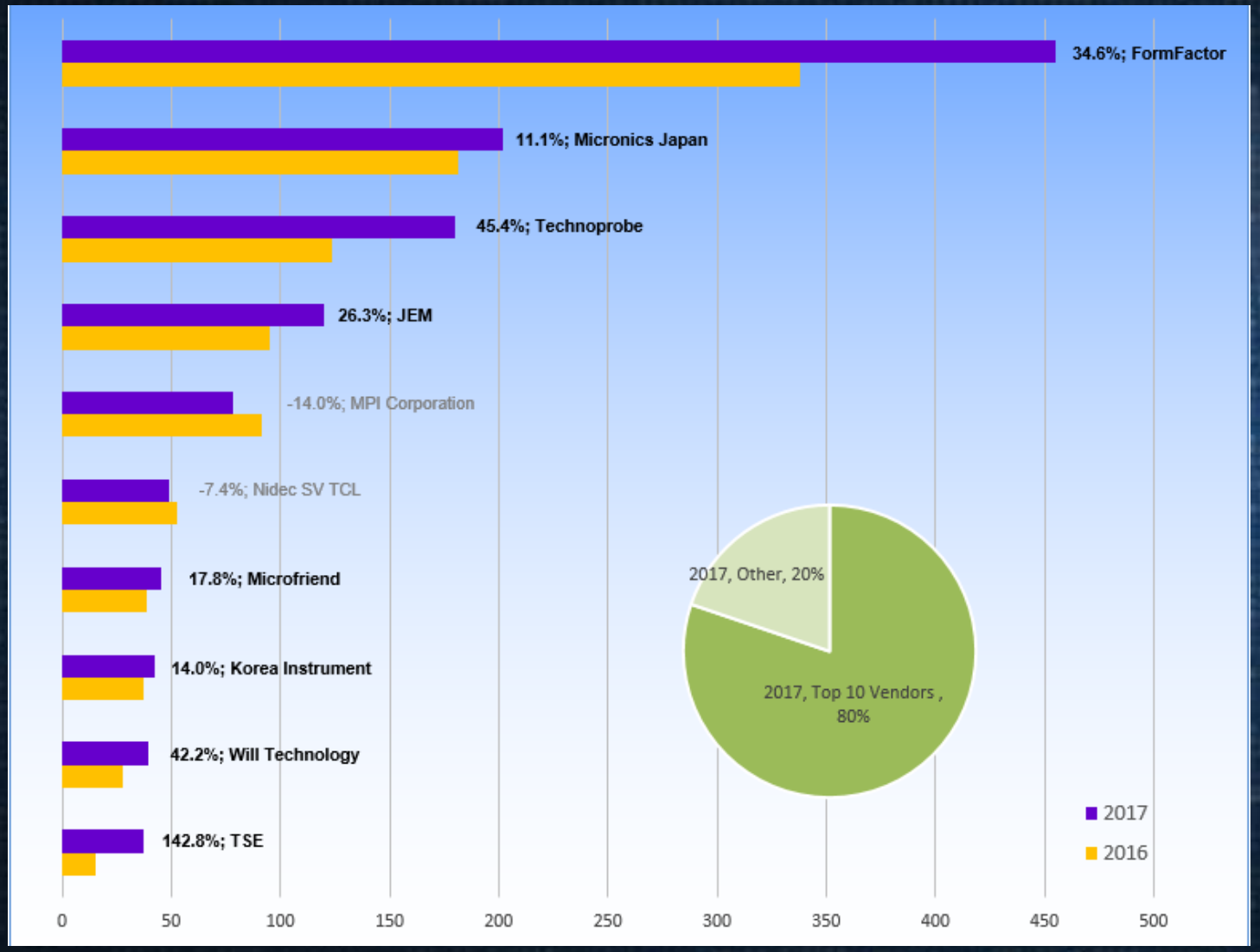




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Thanks to
John West, Risto Puhakka, and Lin Fu!

Top Probe Card Vendors in 2017



Rank	Company	2017
1	FormFactor	454.79
2	Micronics Japan	201.80
3	Technoprobe	179.88
4	JEM	120.13
5	MPI Corporation	78.60
6	Nidec SV TCL	49.10
7	Microfriend	45.42
8	Korea Instrument	42.41
9	Will Technology	39.80
10	TSE	37.01
	Other	308.07
	Semiconductor Probe Cards	1557.01
	Annual Growth	17.35%

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28th Annual SW Test Workshop

- **Technical Program for 2017**
  - Technical Tutorial on Sunday
  - Nine Podium Sessions and Two Poster Sessions across Three Days
  - 32 Podium and 9 Poster Presentations
- **Products / Services EXPO**
  - 64 full size booths … SOLD OUT !
  - EXPO does not compete with Technical Program
- **Corporate Sponsors Program … MANY THANKS !**

Sunday Keynote Speaker

Leveraging Advanced Manufacturing to Address Challenges in the Automotive Memory Market

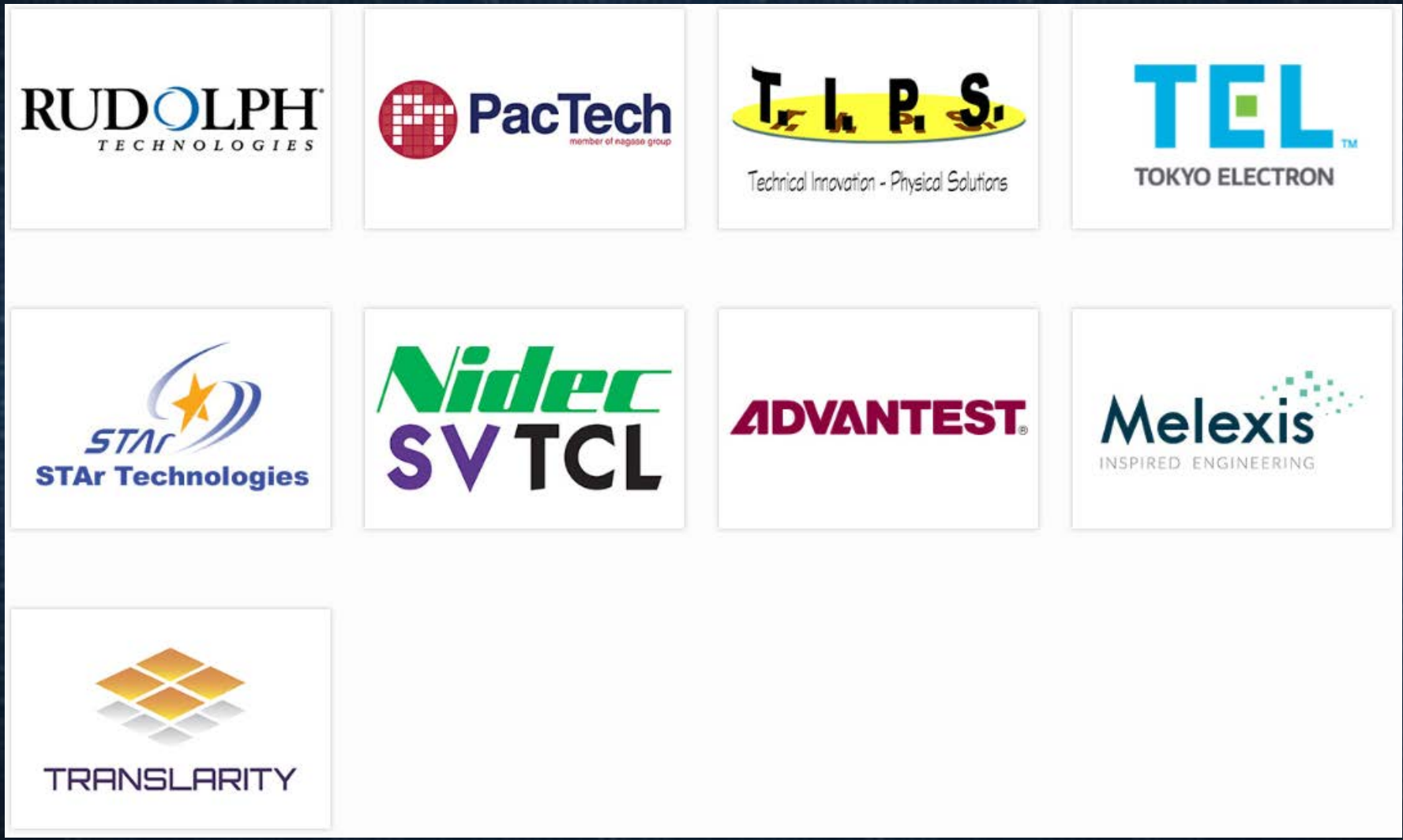
Brett Debenham
Senior Director, Test Probe Central Engineering
Micron Technology, Inc.



Platinum Sponsors



Gold Sponsors



Silver Sponsors



“We’re not in it for the money …”

- **SW Test Team works closely with the RBI staff to have free parking, in-room internet, no resort fees, WiFi access during the entire workshop, and the best on-site conference room rate for this level of property.**

- **SW Test Executive Team …**
  - Jerry Broz, Ph.D., General Chair and Sr. Member IEEE
  - Rey Rincon, Technical Program Chair
  - Maddie Harwood, Finance Chair & Registration Coordinator

"Who's Really to Blame …"

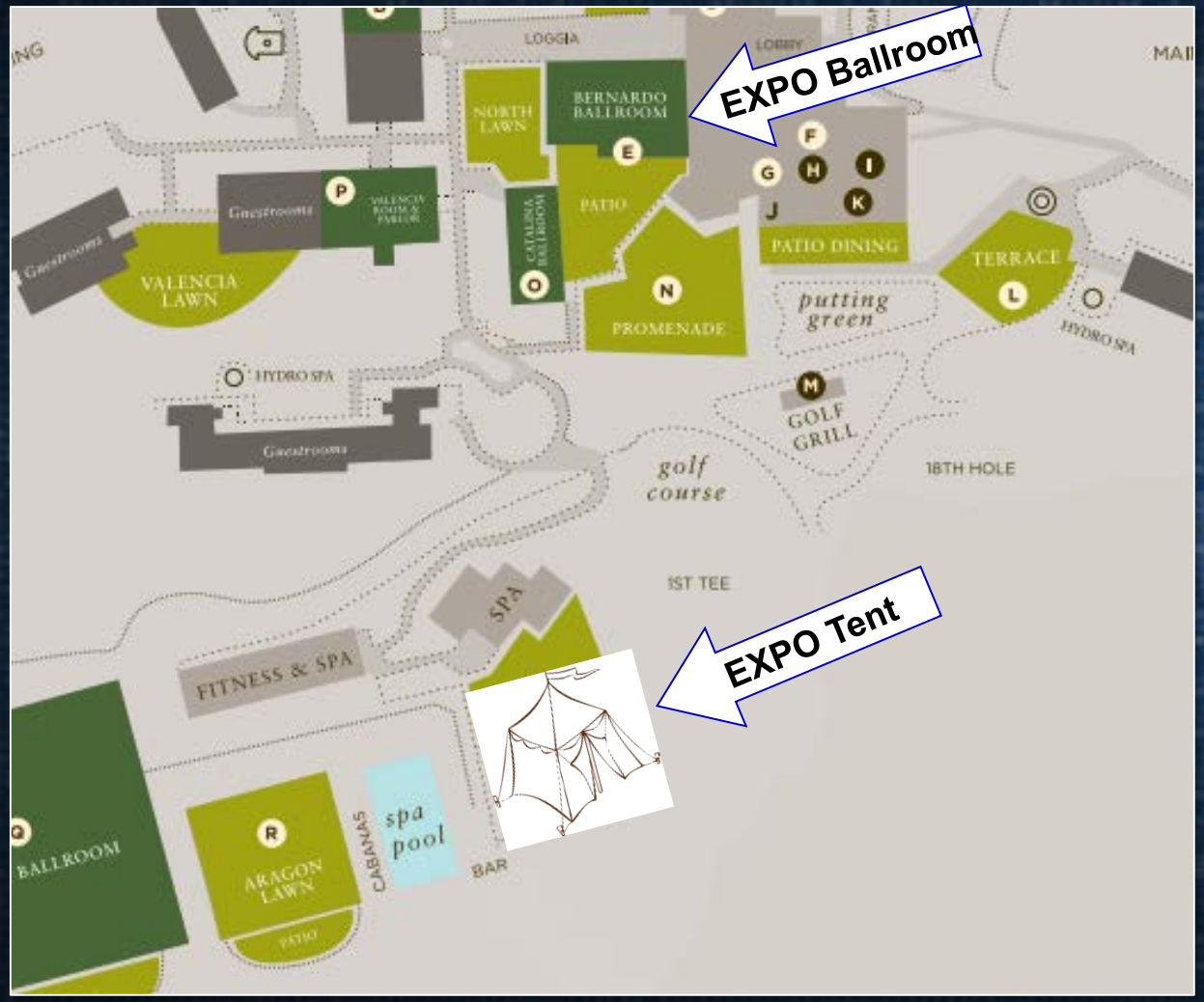
- **Technical Program Committee**
  - John Caldwell, Micron Technology
  - Darren James, Rudolph Technologies
  - Clark Liu, Powertech Technology, Inc. (Taiwan)
  - Patrick Mui, JEM America
  - Mark Ojeda, Cypress Semiconductor
  - Raffaele Vallauri, Technoprobe (Italy)
  - Joey Wu, STAr Technologies (Taiwan)
- **Steering Committee**
  - Karen Armendariz, Celadon Systems
  - Gunther Boehm, FeinMetall GmbH (Germany)
  - Geert Gouwy, Melexis Semiconductor (Belgium)
  - Michael Huebner, Ph.D., FormFactor
  - Amy Leong, FormFactor, Inc.
  - Suz Ramsbottom, Texas Instruments, Inc.
  - Alex Yang, MPI Corporation (Taiwan)
  - Sang Kyu (SK) Yoo, Samsung Electronics (Korea)

SW Test is organized, coordinated, and executed through the efforts of your colleagues.

Technical Program / Agenda

- **Monday, June 5**
  - Technical Program with 4-podium sessions and 1-poster session
  - SW Test EXPO 2018 w/ Dinner served that the Reception Stations
- **Tuesday, June 6**
  - Technical Program with 3-podium sessions and 1-poster session
  - SW Test EXPO 2018
  - Tuesday nigh social and entertainment
- **Wednesday, June 7**
  - Technical Program with 2-podium sessions

SW Test 2018 Expo



- **64 Exhibits**
  - 42 in EXPO Tent
  - 22 in EXPO Ballroom
  - Food and Beverages in both locations
- **3 golf cart shuttles will make the rounds between locations.**
- **Win some prizes with the Scavenger Hunt.**

Tuesday Evening Dinner and Social

- Cocktails and Networking on the Patio and Lawn
- Dinner and Entertainment with Kim Michael Polote and Tony Guerrero



Kim is a world renowned, vocal powerhouse and entertainer.



Tony is a songwriter, producer and an incredible jazz trumpeter.

Recognition & Awards

- **Most "Inspirational" Presentation**
- **Best Presentation, Tutorial in Nature**
- **Best Data Presentation**
- **Best Overall Presentation**
- **Best Poster Presentation**

- **A presentation from SW Test 2018 will be selected for the TEST VISION 2020**
  - Program on July 11 to 12, 2018
  - SW Test will award a travel grant to support participation



SW Test 2017 Awards

Most Inspirational Presentation

A Study on Chuck Automatic Tilting and Chuck Force Sensing for Minimizing Probe Pin Damage and Optimizing Overdrive

Byung-Hyun Shin (Semics - Korea)



Best Presentation, Tutorial in Nature

New Inspection Solution for Probing Technology

Clark Liu (PTI – Taiwan)



SW Test 2017 Awards

Best Data Presentation

Challenges of Minimizing Scrub Mark Depth while Maintaining Low Contact Resistance on Extremely Thin Probe Pads

Blake Rapp, Kurt Guthzeit and Aaron Woodard (Micron Technology, Inc. - USA)



Best Poster Presentation

Development of Latest Generation Hole Geometries for Probe Card Applications

Andrew Webb (OpTek Systems Inc. - USA)
Dr. Mike Osborne (OpTek Systems Ltd. - United Kingdom)



SW Test 2017 Awards

Best Overall Presentation (tie)

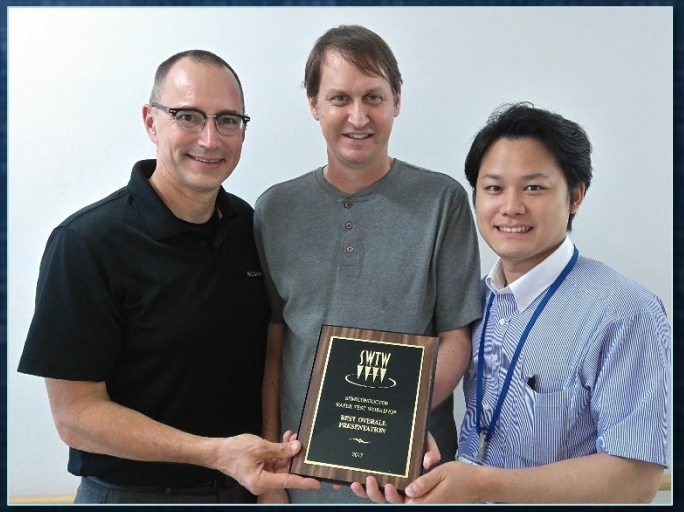
HBM Micro Pillar Grid Array Probing Challenges

Raffaele Vallauri (Technoprobe - Italy), Dr. Yun Jinyeong and Dr. Kim Jaehong (Samsung - Korea), Marco Prea (Technoprobe - Korea) and Daniele Perego (Technoprobe - Italy)



Advanced Vertical Technologies for Low Damage Probing of Bumps, Pillars, and Pads

Jerry Broz, Ph.D. (MJC Electronics – USA), Darren Aaberge and Shota Hetsugi (Micronics Japan – Japan), Gwen Gerard and Jean-Pierre Gibaux (Texas Test Corporation – Taiwan)



That “Special” Award …



Bill Mann’s Poorest Disguised Sales Pitch

“What happens at SW Test stays at SW Test !!”

SW Test Asia 2018 on Oct 18 to 19, 2018



Sheraton Hsinchu Hotel, Zhubei City, Taiwan

- **One and one-half day conference**
  - Technical Program
    - Abstract Submissions will open at end of June
  - 30 Booth EXPO (already 90% sold-out)
  - Technology Showcase
    - Focused Presentations made by Platinum Sponsors
  - Relaxed Networking in the "Spirit of SW Test"

- **SW Test Asia Committee Members**
  - Clark Liu (PTI Taiwan) – Technical Program Co-Chair
  - Joey Wu (STAr Technology)
  - Nobuhiro Kawamata (Formfactor K.K.)

Want to Learn More ?

- IEEE Holm Conference on Electrical Contacts
  http://www.ieee-holm.org



- IS-Test Workshop
  http://www.is-test.com



- SEMI TESTVISION 2020



- IEEE North Atlantic Test Workshop
  http://www.is-test.com



- Burn In & Test Strategies Workshop
  http://www.bitsworkshop.org



- Electronic Components and Technology Conference
  http://www.ectc.net



- VLSI Research
  https://www.vlsiresearch.com/



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See you Next Year in San Diego …



SW Test Workshop | June 3-6, 2018

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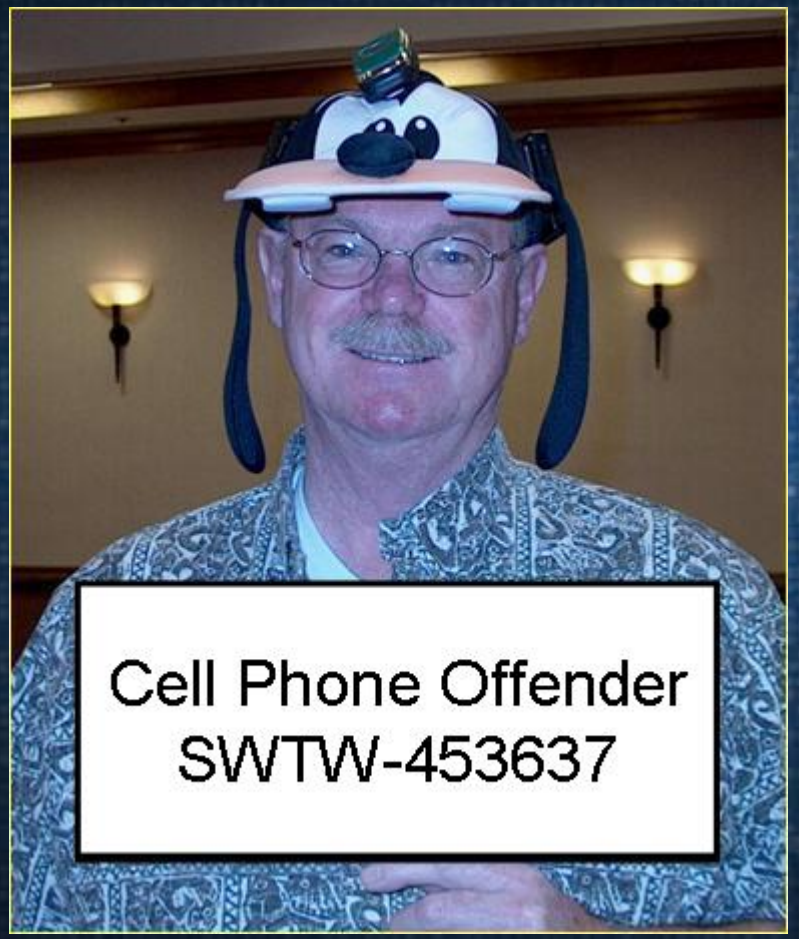
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Silence your cell phone !!!





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- **Contact the SW Test Team with any questions …**

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SW Test Workshop

Semiconductor Wafer Test Workshop

Probe Card Market Update

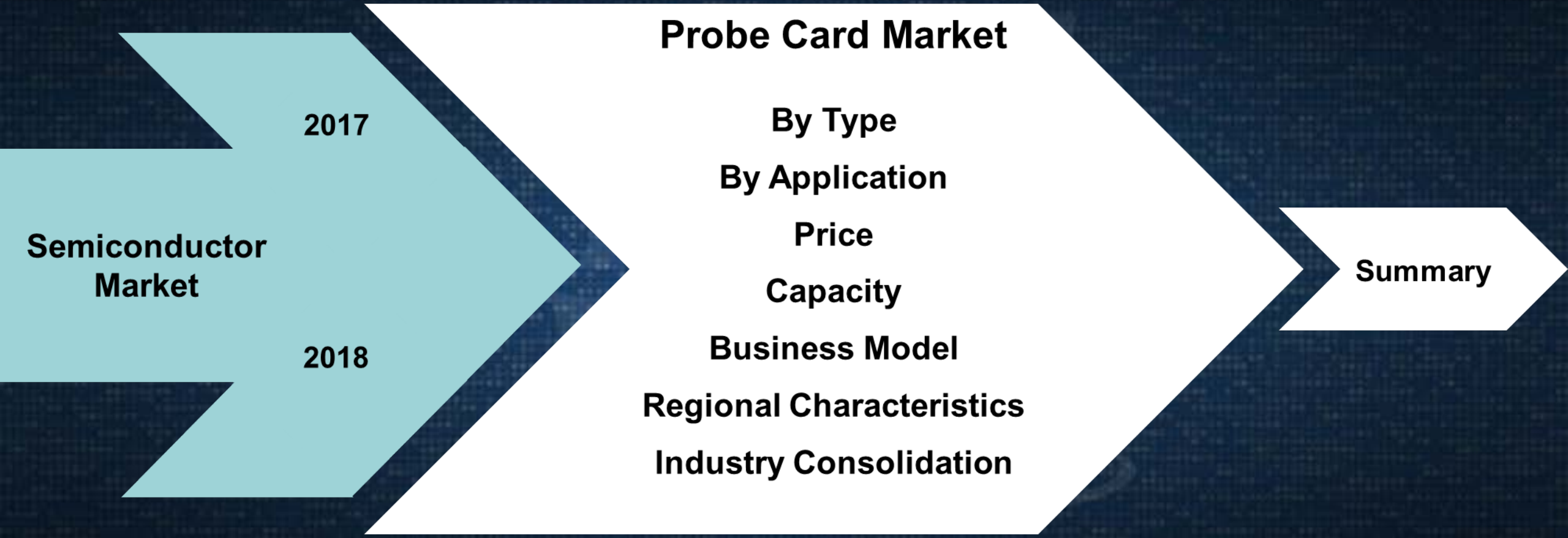
VLSIresearch

Lin Fu

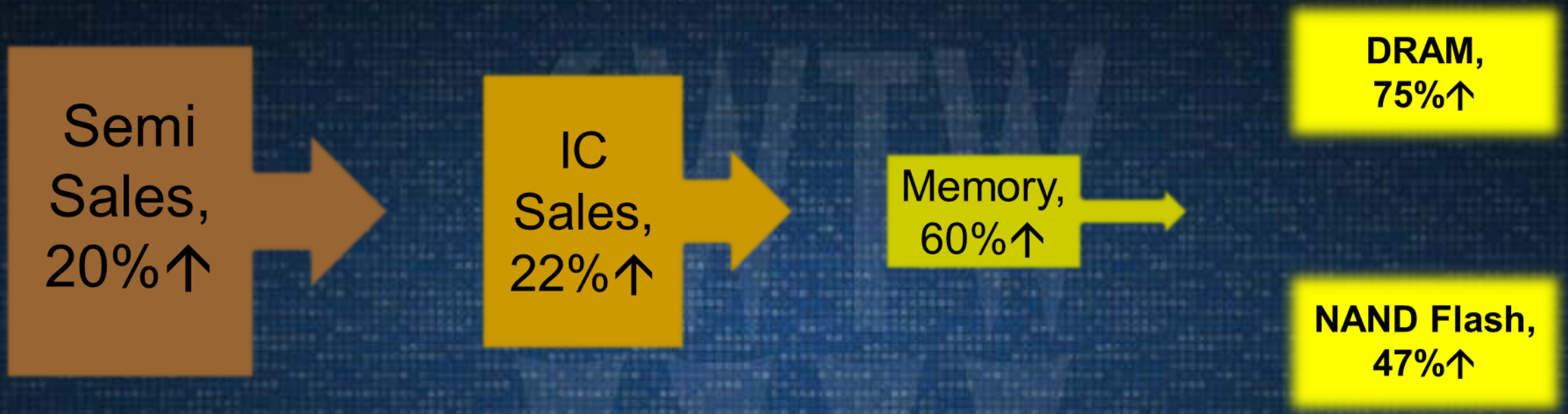
VLSI Research

June 3-6, 2018

Overview


Semiconductor Market
2017
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2017 Semiconductor Market



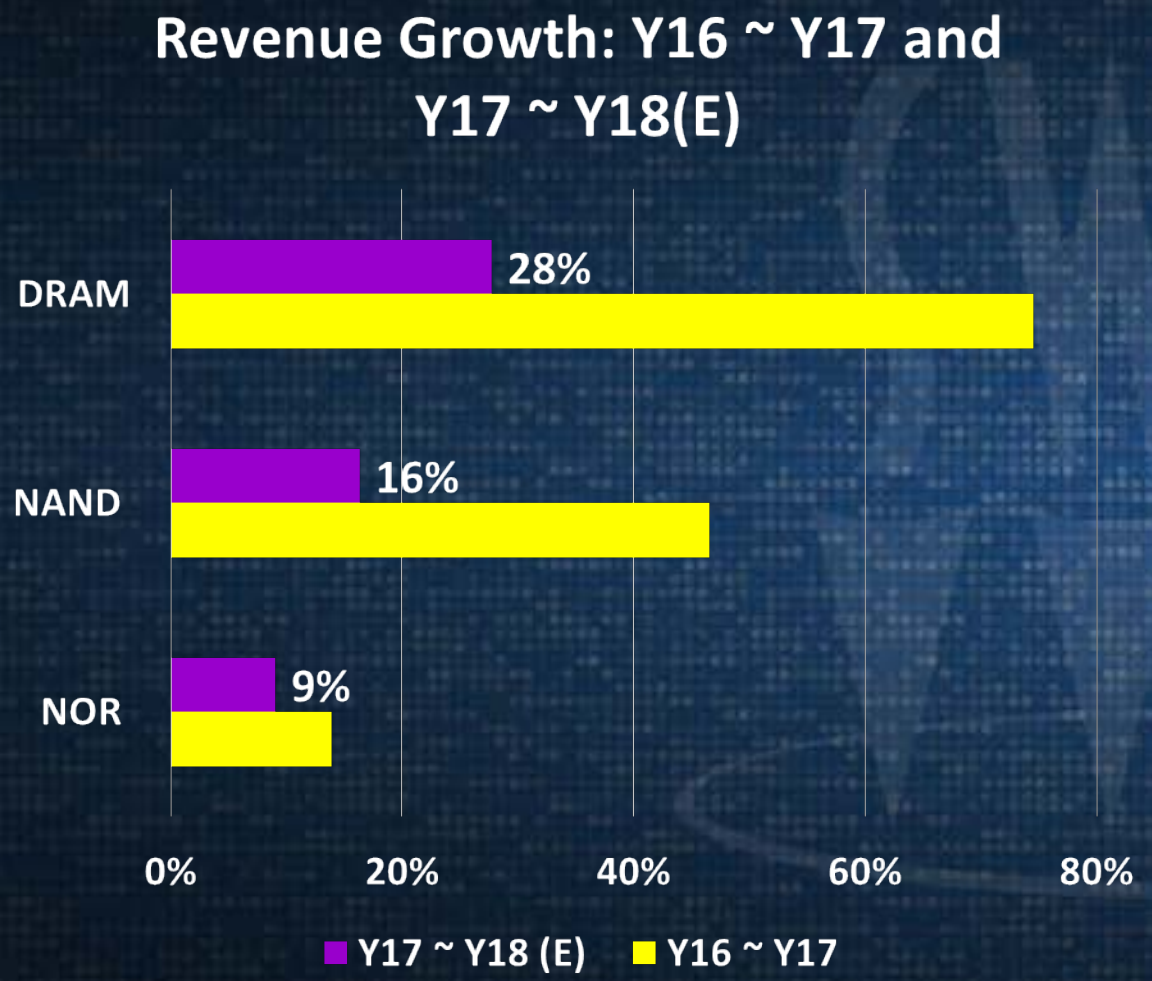
- **2017 was an exceptional year for semiconductors with sales exceeding $400Bn**
- **Memory revenues increased 60% in 2017 compared to revenues in 2016. Key drivers: DRAM and NAND Flash**

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2018 Semiconductor Market Outlook

- **Peak growth in semiconductors reached at end of March 2018**
  - Sales of semiconductors in the last week of March 2018 were 30% higher than the same week in 2017
- **Weakening of demand due to falling memory prices**
- **Underlying demand still strong**
- **Chip inventories at a healthy 1.2 months**
  - Currently growing fast (in line with demand) but could spike if demand drops suddenly
- **Expect growth of 12.5% in 2018**

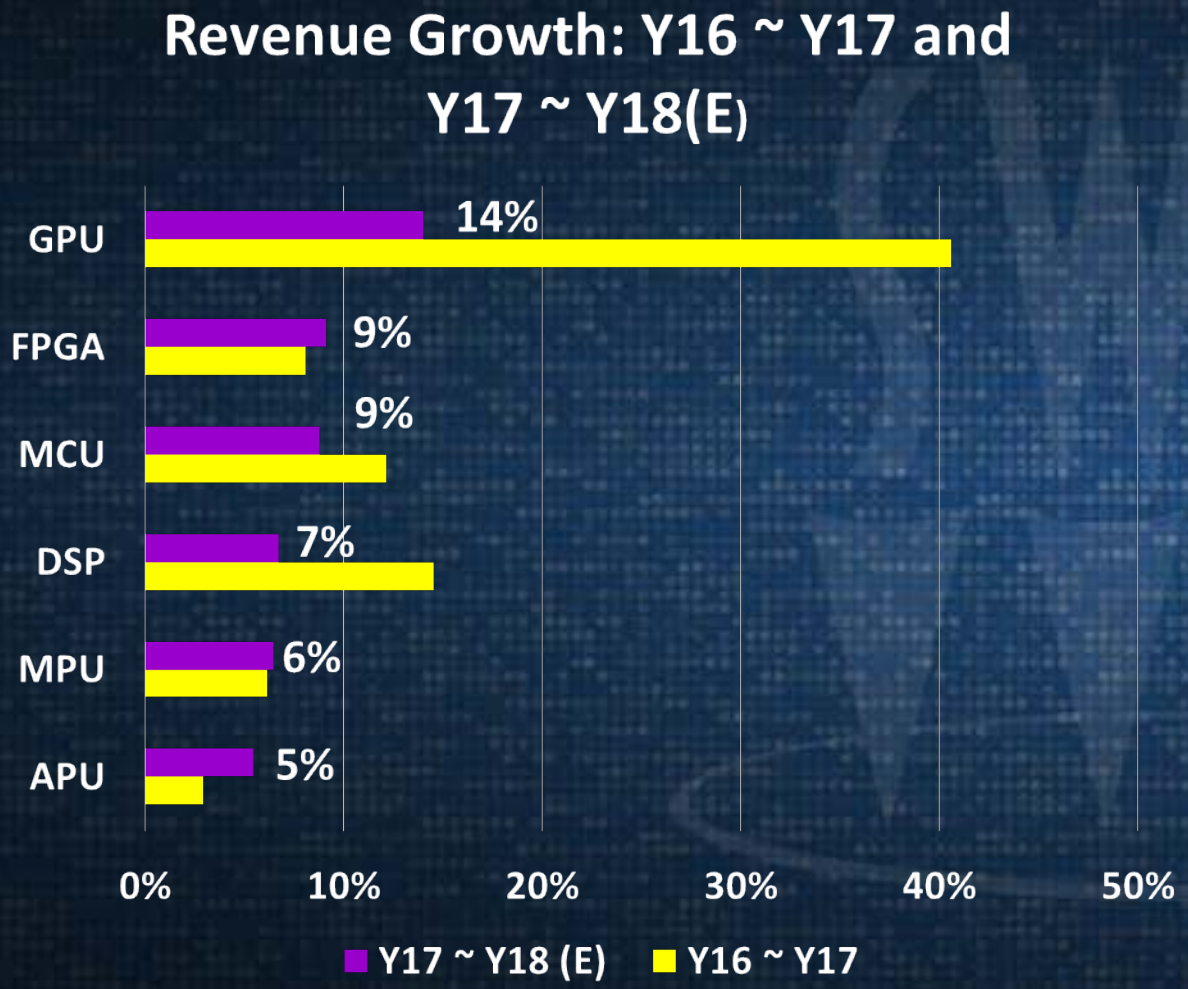
Semiconductor Memory Market



- DRAM added $30Bn to semiconductor revenues in 2017
- DRAM will be biggest growth driver in 2018
- Weakening NAND prices will affect NAND growth
- DRAM, NAND Flash and NOR Flash are expected to grow in 2018

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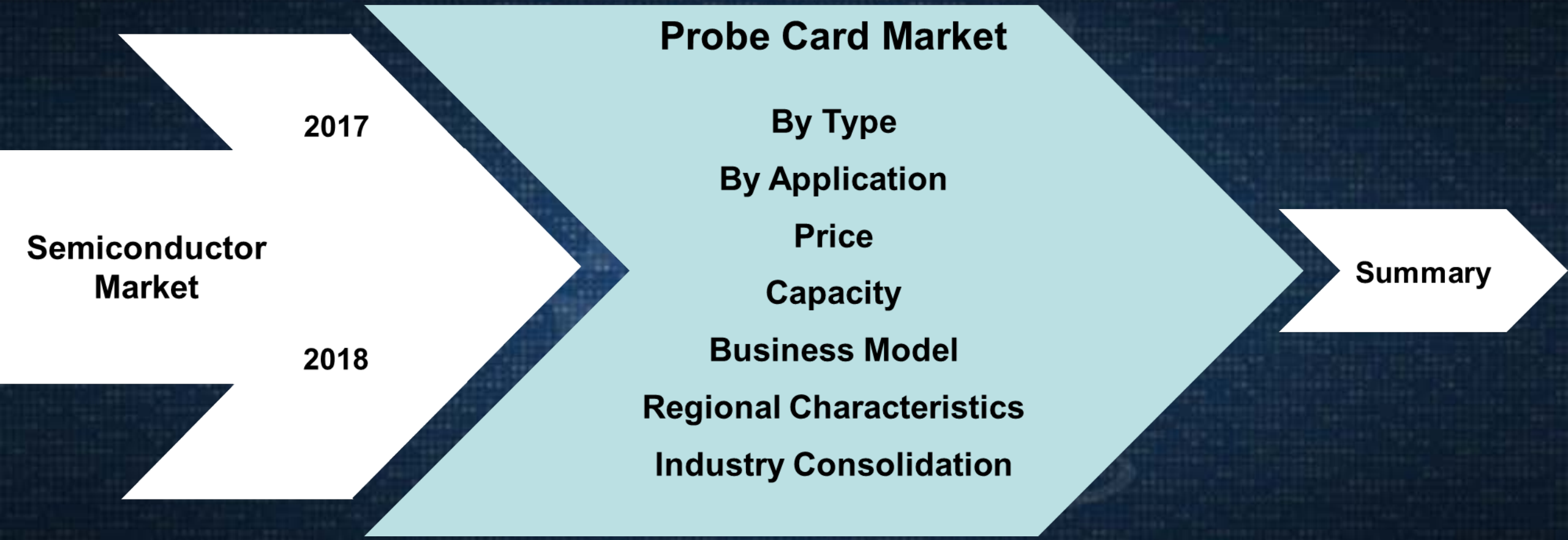
Semiconductor Non-Memory Market



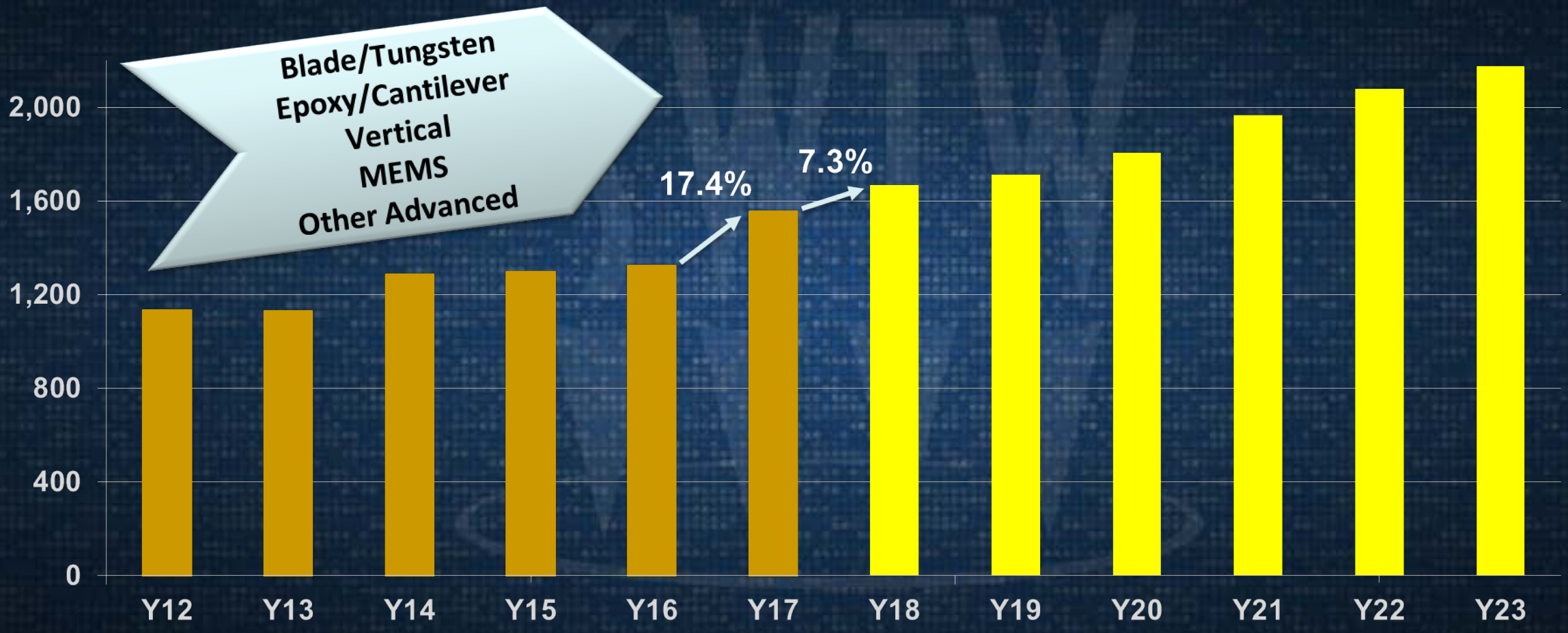
- Logic markets set to grow steadily
- Graphics processor sales strong due to AI and Blockchain
- Applications processor sales weak as smartphone and tablet sales mature

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Overview

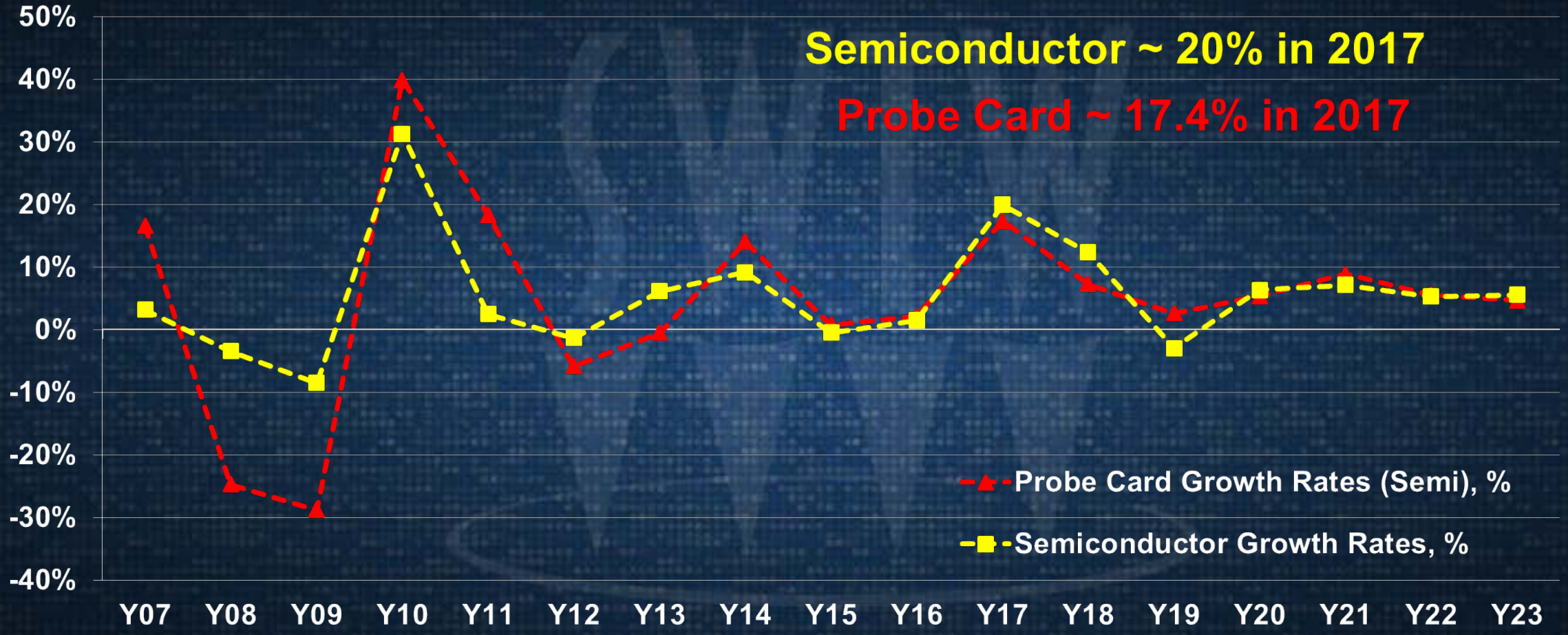

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Probe Card Market Overview, $M



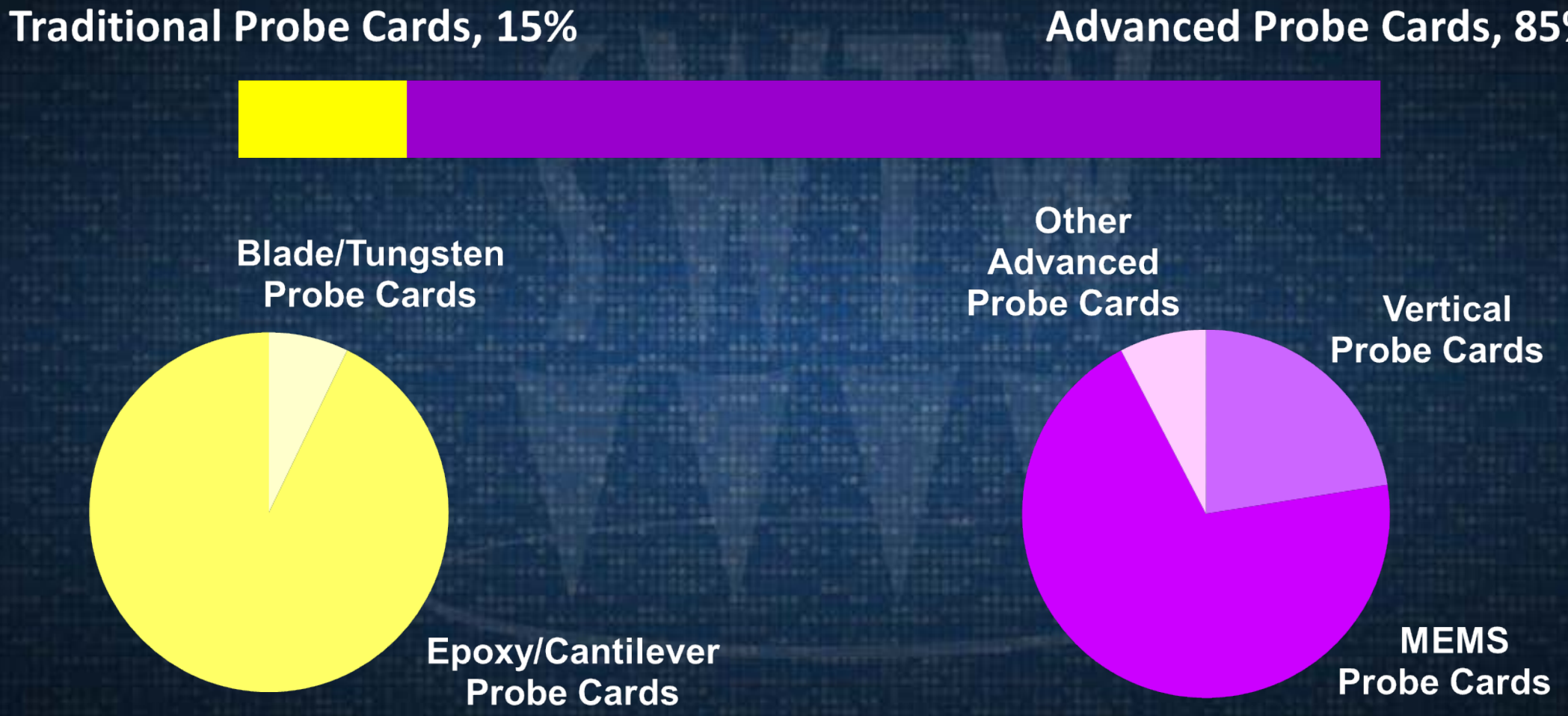
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Probe Card Growth vs. Semiconductor Growth, %



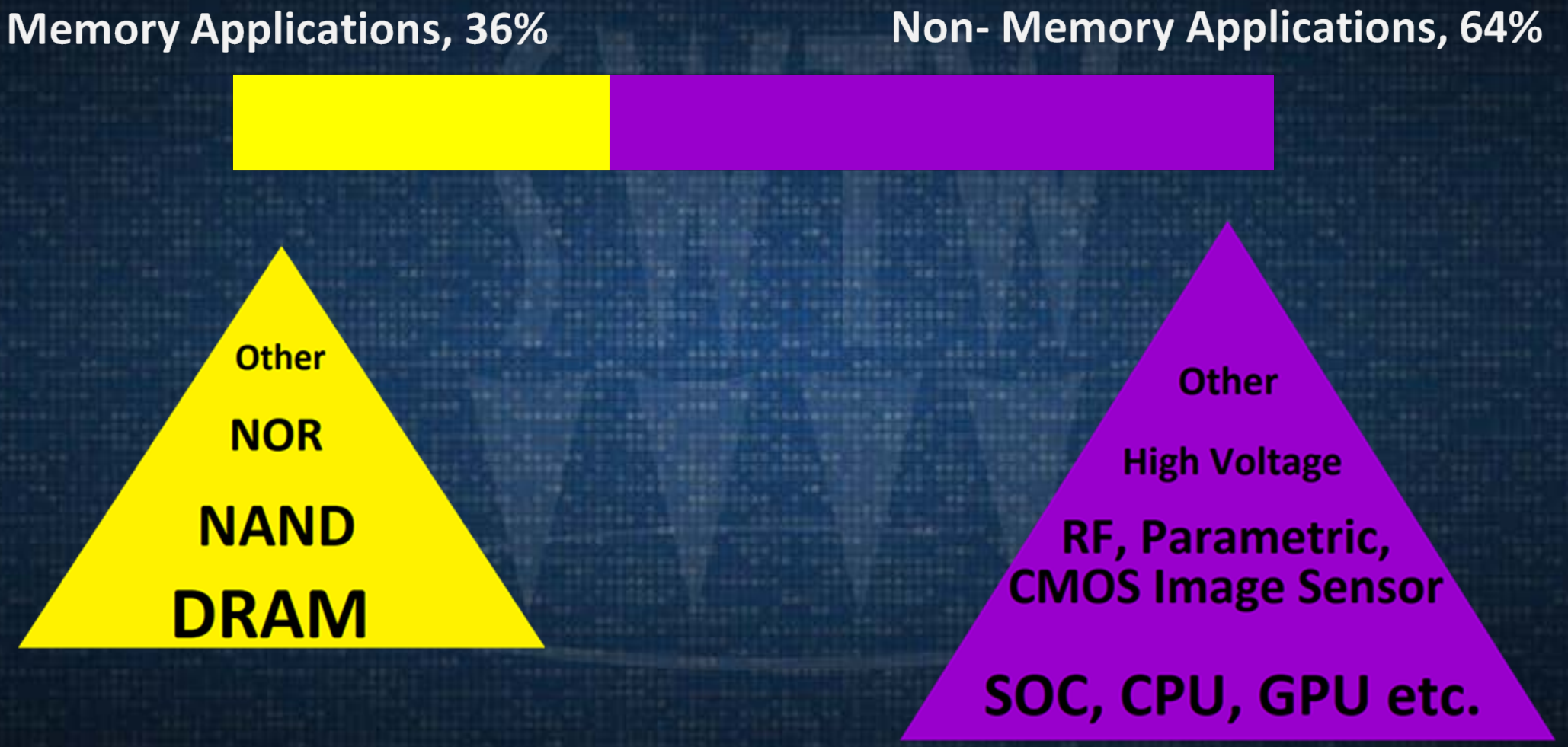
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2017 Probe Card Revenues by Type, $M%



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2017 Probe Card Revenues by Application, $M%



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Price Trend of the Most Expensive Probe Cards, $

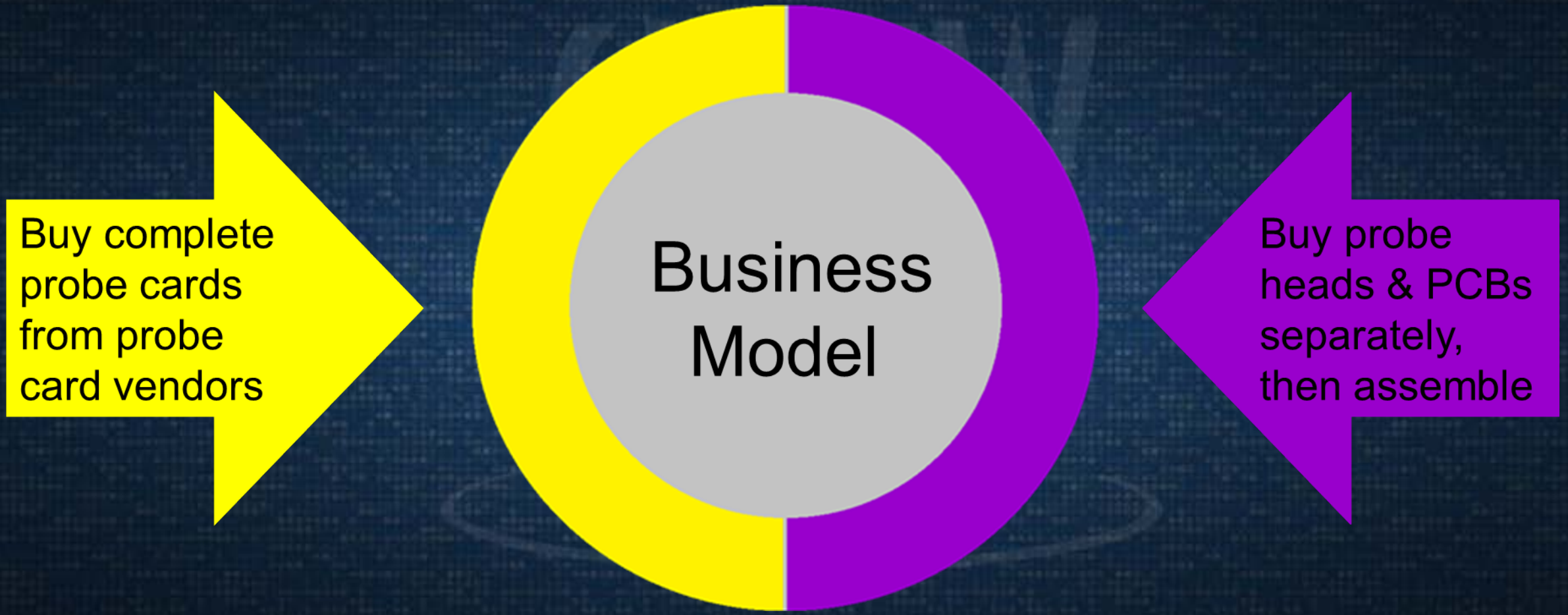


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Capacity Managing

- In 2017, revenues of MEMS probe cards increased at the fastest rate compared to other types: well above average
- In 2017, Technoprobe built a new factory in Italy to support the increasing demand for high-end probe cards
- At the beginning of 2018, JEM decided to invest a new fab to expand their capacity in 2019

Business Model of Buyers



Regional Distribution of Main Suppliers



Main probe card suppliers' HQ located :

Europe
Japan
Korea
North America

Supply 90% ($M%) probe cards in 2017

Regional Performance of Main Suppliers

7 Main Probe Card Regions of Consumption:

China, Europe, Japan, Korea, North America, Singapore, Taiwan

Suppliers HQ Location	*2nd Strongest area in above list (Strongest area ~ locally)*	*Weakest area in above list*
Europe	North America	China
Japan	Korea	Europe
Korea	China	Europe
North America	Taiwan	Singapore

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2017 Industry Consolidation

In 2017, total probe card revenues were $1.56B

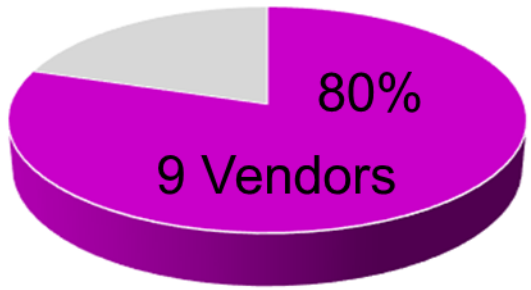


The top 10 vendors accounted for 80% market share

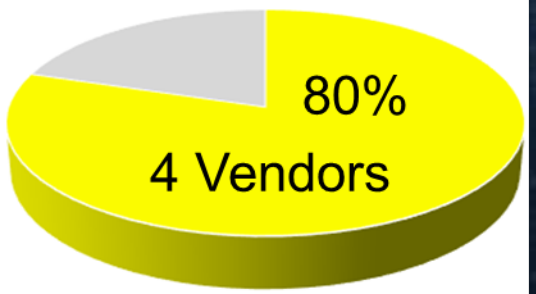
Fragmented ***Concentrated***



Epoxy/Cantilever



Vertical



MEMS

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2017 Customer Satisfaction Survey

Surveyed Categories

Company
Trust in supplier
Support after sales
Recommend supplier
Commitment
Partnering
Field engineering support
Technical leadership
Spares support
Process support

Product
Quality of results
Usable performance
Uptime
Product performance
Overall Value

THE 2018 HIGHEST- RATED TEST CONNECTIVITY SUPPLIERS

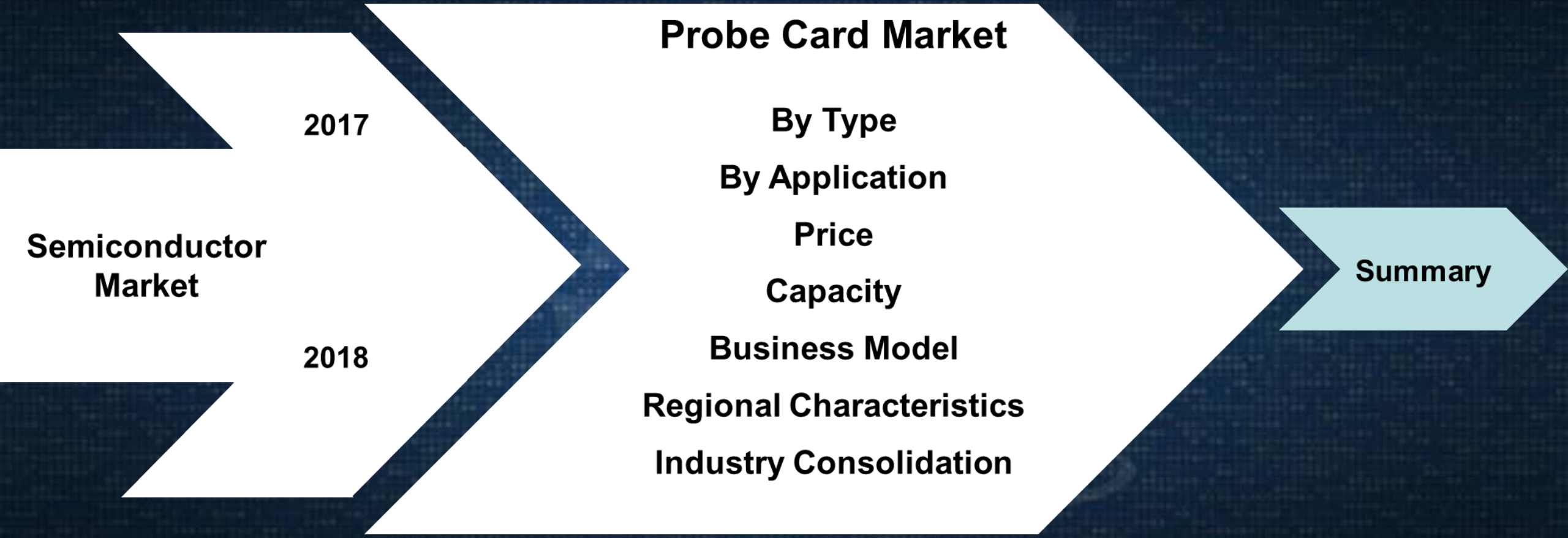
Supplier	Rating	VLSI Stars	Highest-Rated Categories
TECHNOPROBE Wafer Probing Technologies	9.81	★★★★★	• Support After Sales • Trust in Supplier and Partnering
FormFactor™	9.15	★★★★★	• Recommend Supplier • Technical Leadership
Nidec SV TCL	9.03	★★★★★	• Partnering • Commitment
Xcerra measured by your success	8.70	★★★★½	• Spares Support • Support After Sales
JEM JAPAN ELECTRONIC MATERIALS	8.12	★★★★	• Partnering • Recommend Supplier

Source: VLSIresearch
Doc: css_testconnectivity_v18.05

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Summary

- Semiconductor sales slowing in 2018 but it is still expected to be another great year with sales growth of 12.5%
- As new memory capacity comes on line, rapidly falling memory prices are likely to result in an overall semiconductor sales decline (-3%) in 2019
- Sales of Analog and Logic chips to grow 8% in 2018 and 2.5% in 2019
- Driven by the semiconductor market, sales of probe cards are expected to be increase by 7.3% in 2018



SW Test Workshop

Semiconductor Wafer Test Workshop

Device Interface Challenges of the Next Decade

TERADYNE

Steve Ledford

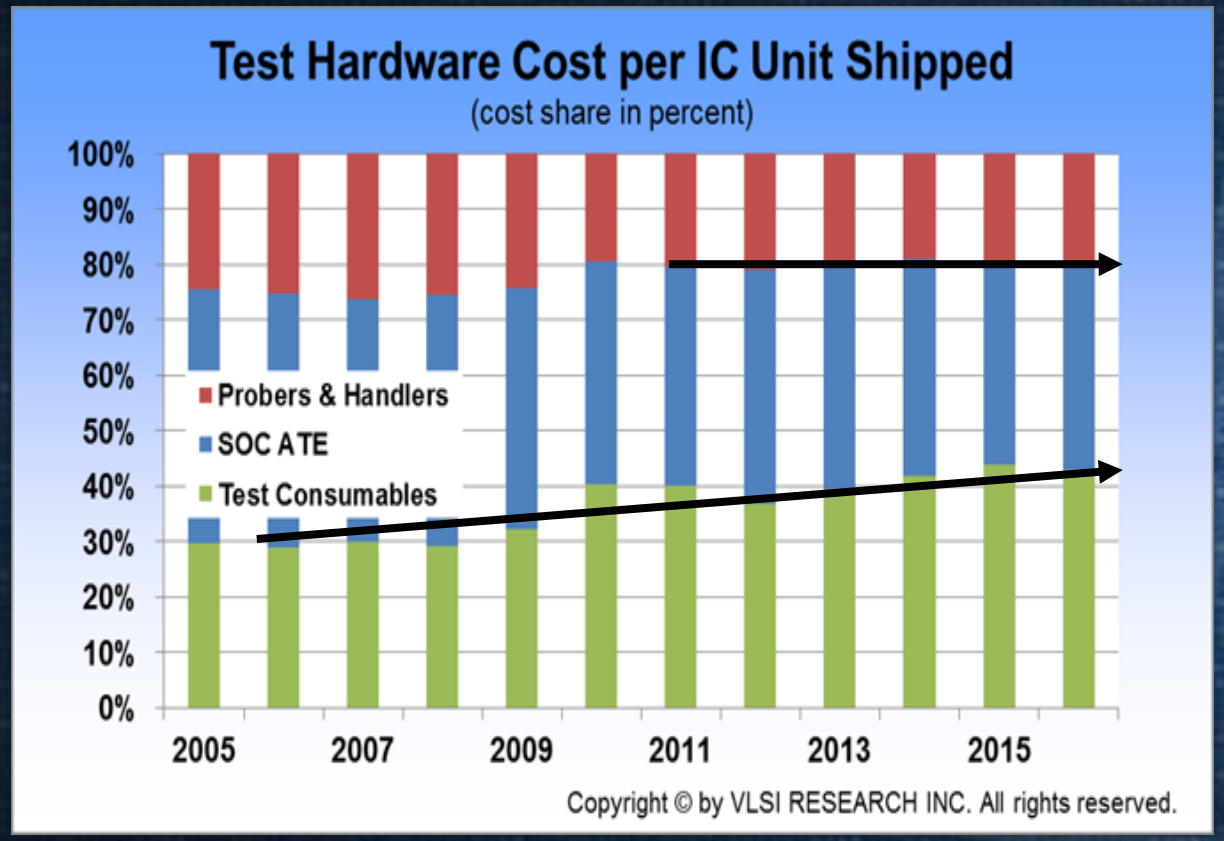
Teradyne

June 3-6, 2018

Outline

- Situation today
- End market drivers
- Importance of Time to Market & Time to Volume
- Density: I/O, power, and components
- “Sub-micron scale” Device Interface paradigm

Device Interface Challenges (today)



Handler/Prober Cost % → Flat

ATE Equipment Cost % ↘ Decreasing

Test Consumables Cost % ↗ Increasing

Consumable spend = Tester spend!

Device interface complexity doubles every 4 years

- Decreasing pin pitch
- More pins, more components
- Higher performance: electrical & mechanical
- In the same area or larger

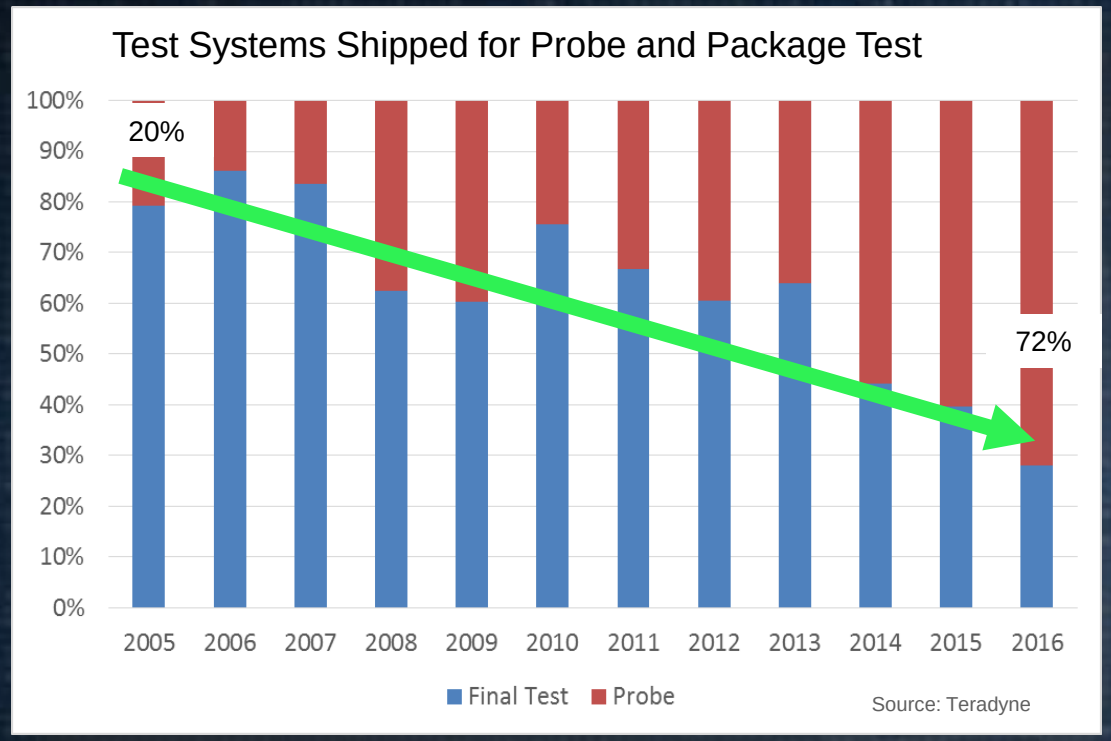
Site count limitations emerging

- Touchdown efficiency @ wafer sort decreasing
- Handler limitations @ final test

Declining DIB execution metrics

- Defect density limits scaling
- Poor yields with new materials and processes
- Long leadtime – longer than time to make silicon wafers!

Transition to More Probe Test



- Greater % of Complex SOC ATE is sold for Probe test
- Most AP and PMIC devices are trimmed at probe
- Multi-chip packaging (logic + memory) economics require KGD
- Major drivers are cost reduction (final test insertions to Probe) or size (chip scale packaging)

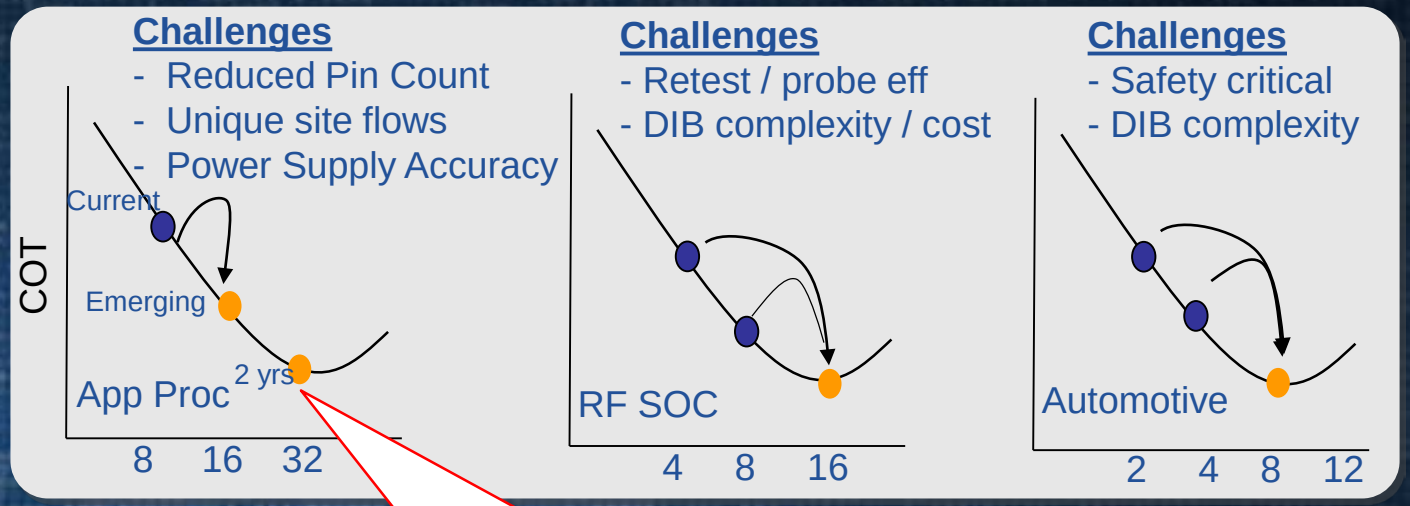
Wafer Level Packaging





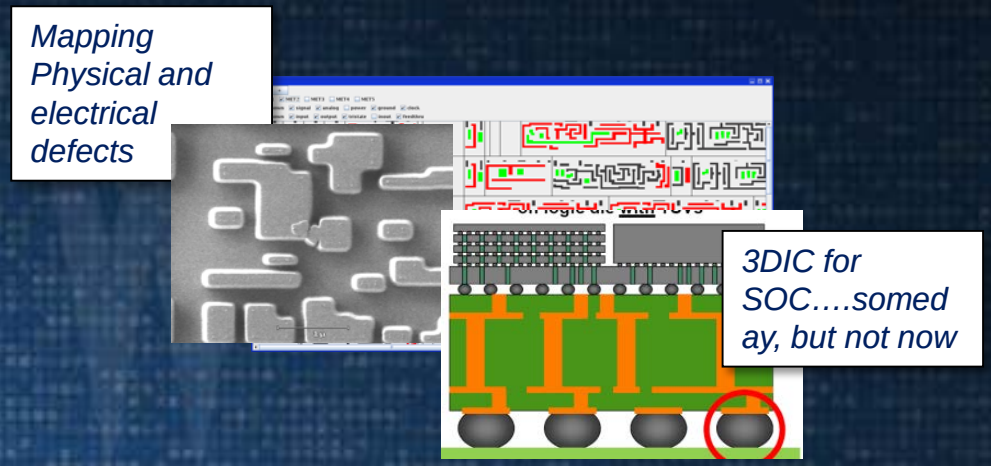
Complexity Inflection Point

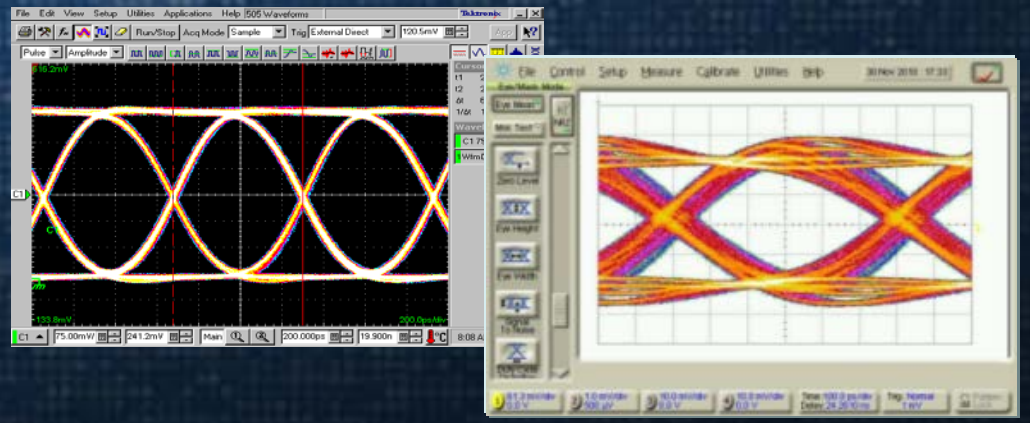
- **IO density problem – lots of great tester resources, but how do I get them to the DUT?**
- **Dimensions of the problem:**
  - **DUT area I/O & power density**
  - **Performance vs density**
  - **Process scaling**
  - **Speed of execution**
- **“It is a system problem at the test cell level”**



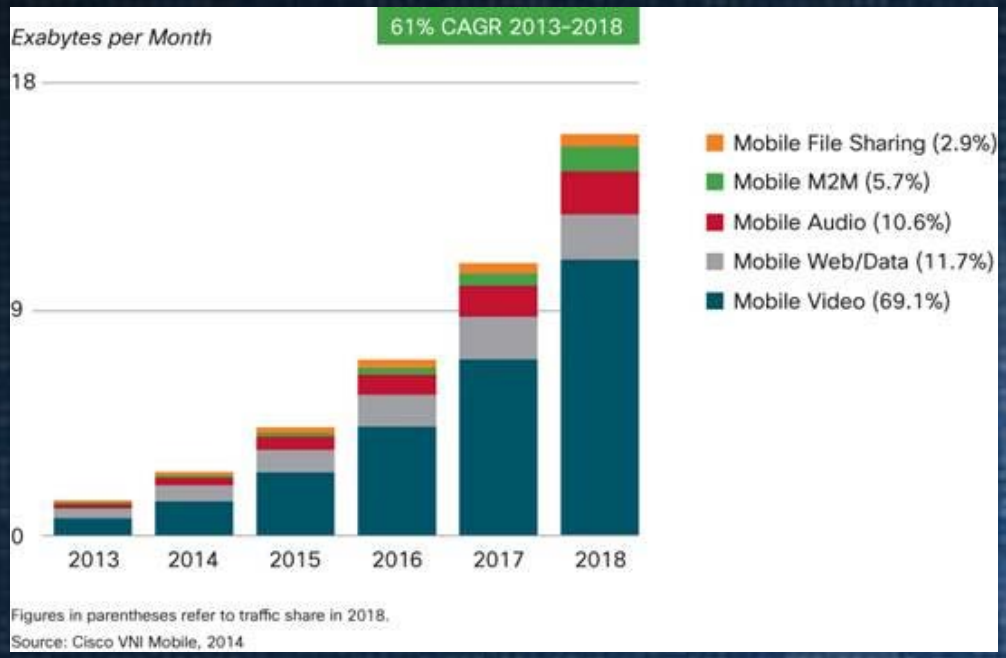
Mobile Processor Trends

- **More Cores, More Gates ➔ More I/O & power pins**
  - Test Times increasing ~ 10 to 20% per year just due to device complexity
  - Increasing parallelism is typically the counter, but worsening TDE is eating up gains.
- **Cost per transistor is not going down fast enough, driving multi-die packages**
- **Increased challenges with high speed IO**
  - DDR Interfaces as fast or faster than traditional PC memory
  - High Speed Serial Tests
  - DFT will get more difficult at higher speeds

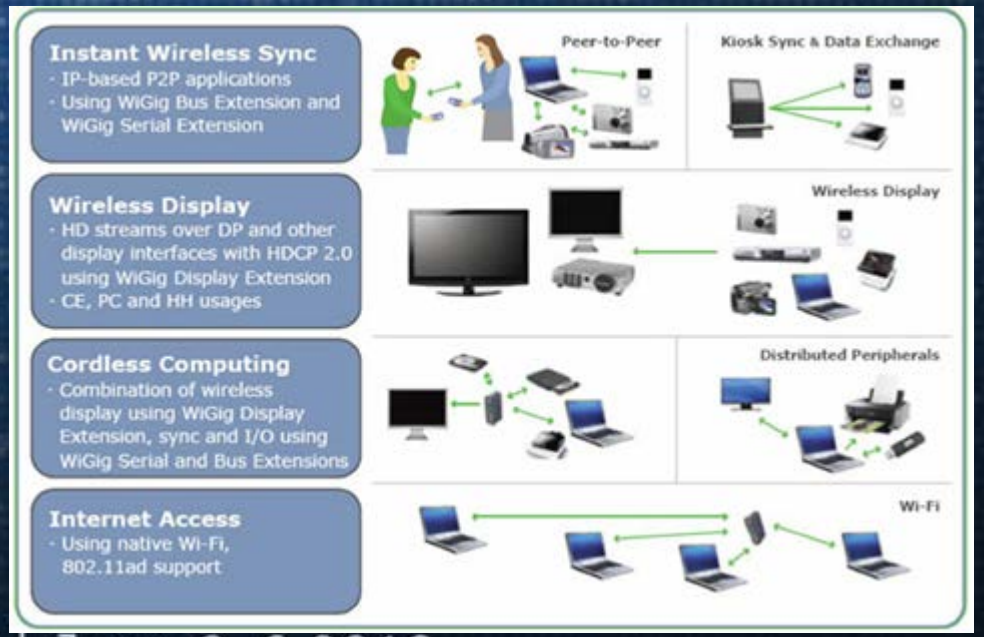




Wireless (RF & mmWave) Trends

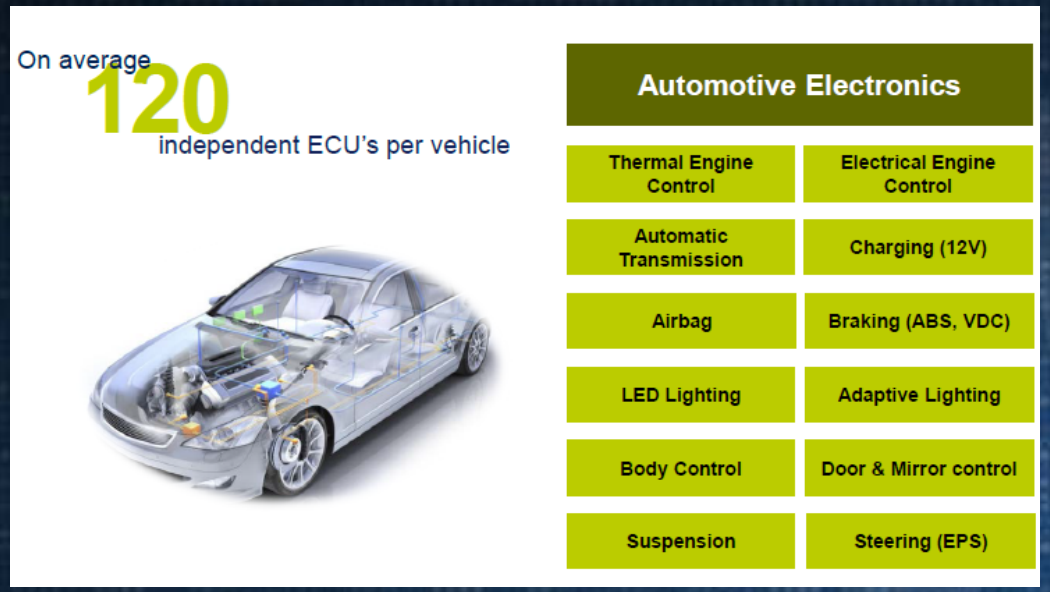


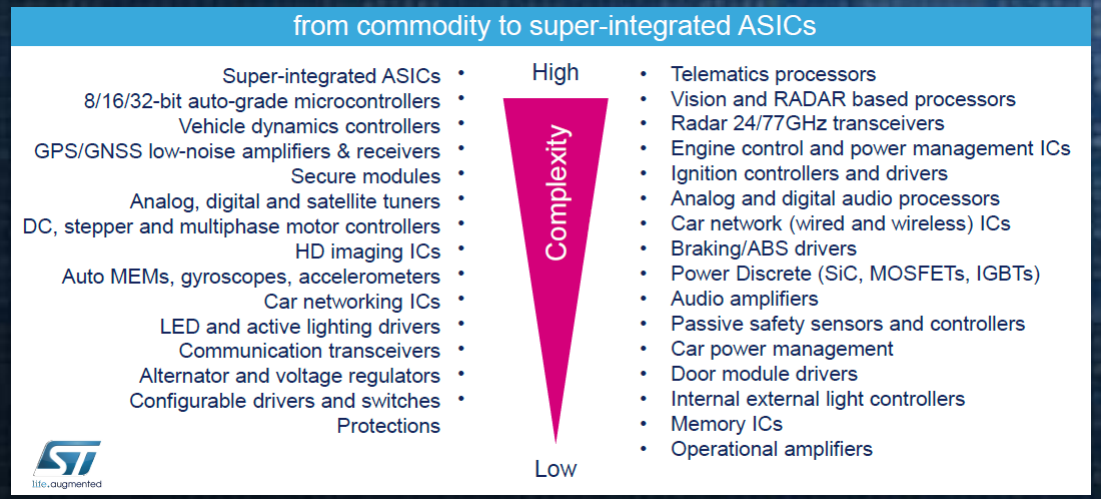
- **Increase Demand for Higher Data Rate & Connectivity**
  - Overall mobile data traffic is expected to grow at a 61% CAGR to 15.9 Exabytes per month by 2018
  - MIMO & Carrier Aggregation requiring 2x-3x more active RX & TX device ports
  - Cell and backhaul infrastructure improvements needed to support higher data capacity



- **Expanded use of mmWave for Consumer Applications**
  - Line-of-site data transfer for uncompressed video and infotainment
  - Wireless “Last Mile” (+29GHz and above)
  - Auto Radar (+72 GHZ)

Automotive Trends





Improvement in emissions, performance, and safety are due largely to advances in semiconductor technology

High performance semiconductor products have made their way to the car:

- Vehicles are a "rolling supercomputer"
- Automotive reliability adds at speed tri-temp testing (-40 to +150C) and more….

New electrical components bring new device interface requirements:

- Packaging & handling: power modules
- High voltage: +1kV
- High current: +1kA

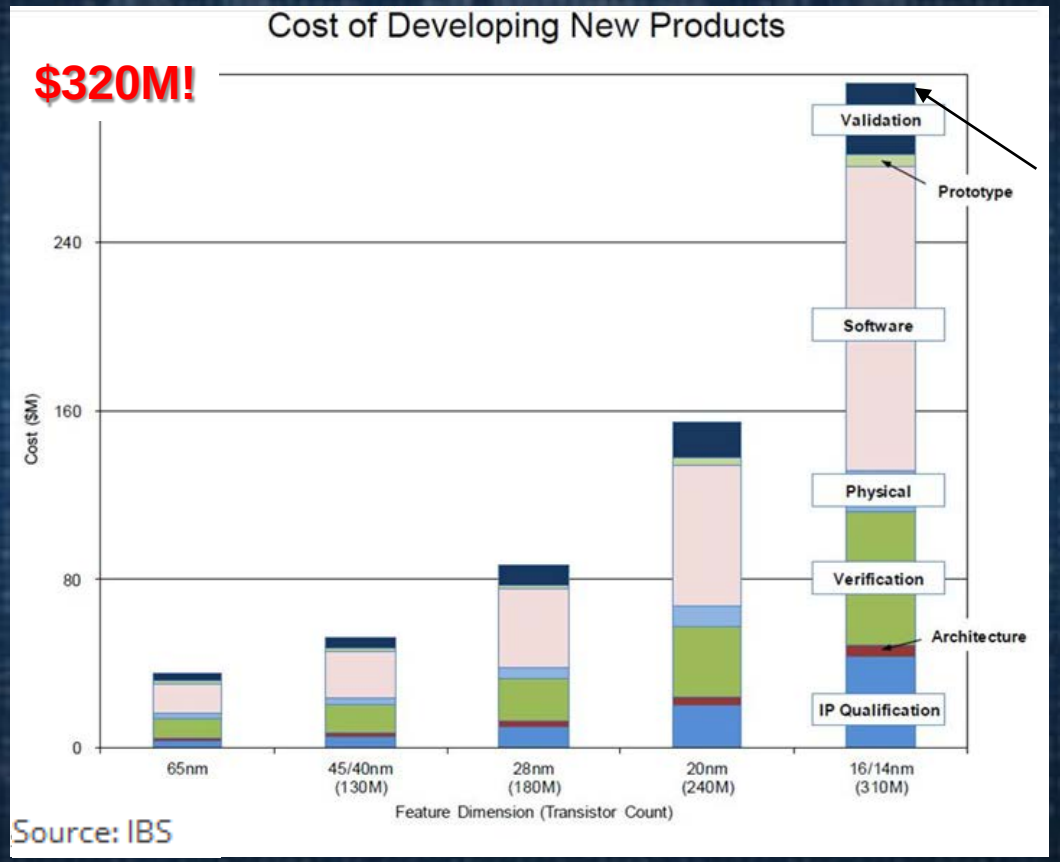
Product safety and reliability take on significant role in ATE applications

- Power ratings can hurt or kill people if not properly safe-guarded or fail.

IC Development Costs – Time to Market

Time to Market & Time to Volume requires:

- **First pass device interface NPI success: functional and full performance**
- **OTD at +95%**
- **Manufacturing leadtime matching first silicon run time, generally 21 to 28 days from silicon tapeout to wafer out**

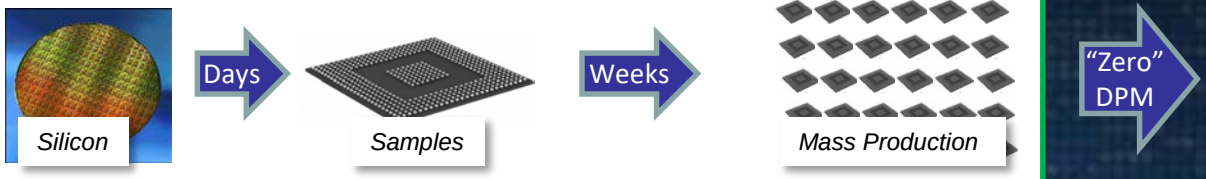


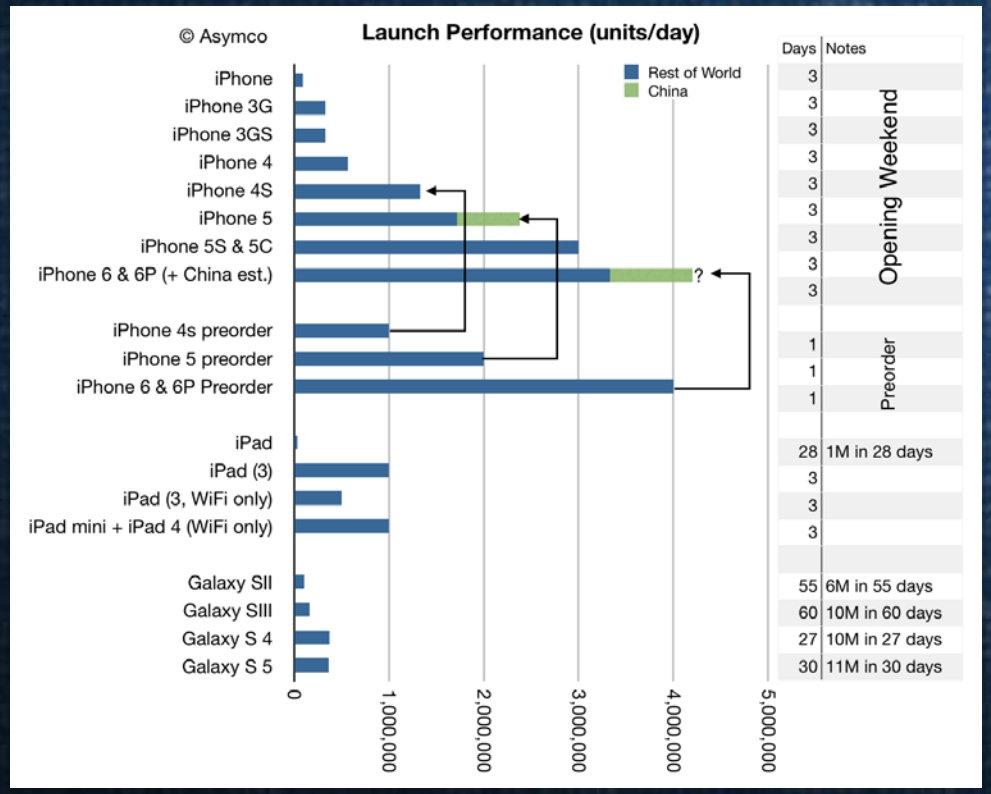
Cost of Test Development (<1%)

Risk mitigation cost to ensure first pass NPI success (leadtime, OTD, quality) has high leverage to maximize return to silicon dev expense

Time to Volume

COT is important but getting to market quickly with the best quality is what really counts!



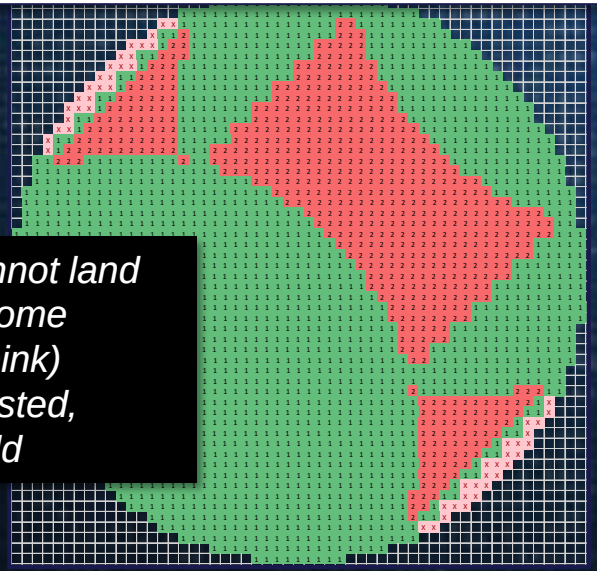


- **Fast Ramps: Essentially full volume from product launch for high profile new products**
- **Must bring up new silicon process at the same time (example: 14nm FinFET)**
- **Yield must be good to reduce cost but defect rate must be extremely low**
- **Device Interface must be perfect on first iteration: functionality & performance**

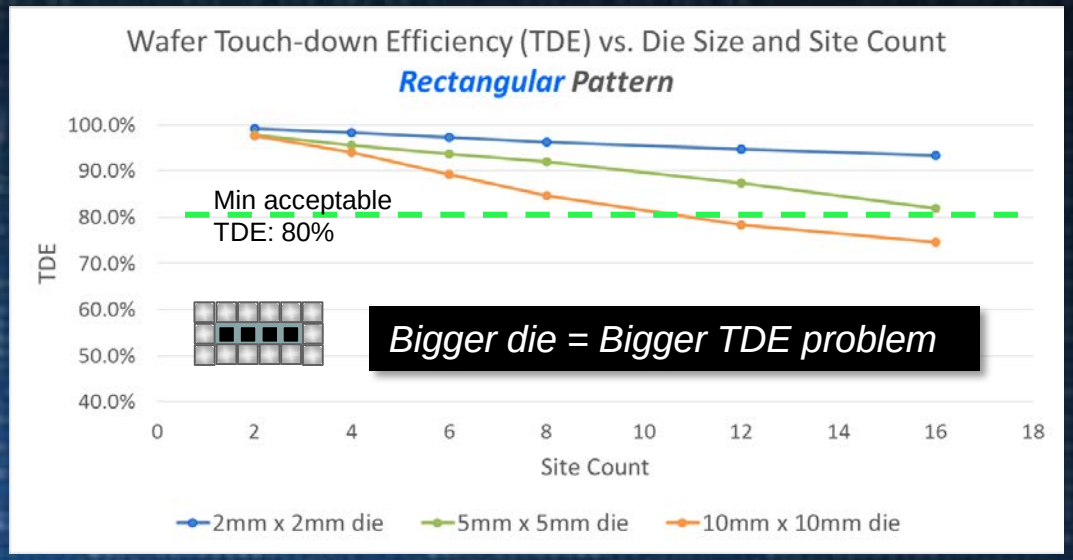
I/O Density – TDE problem

- **Throughput gain by increases in wafer test site count is destroyed by poor touch-down efficiency (TDE)**
- **TDE limited by I/O & power routing density**

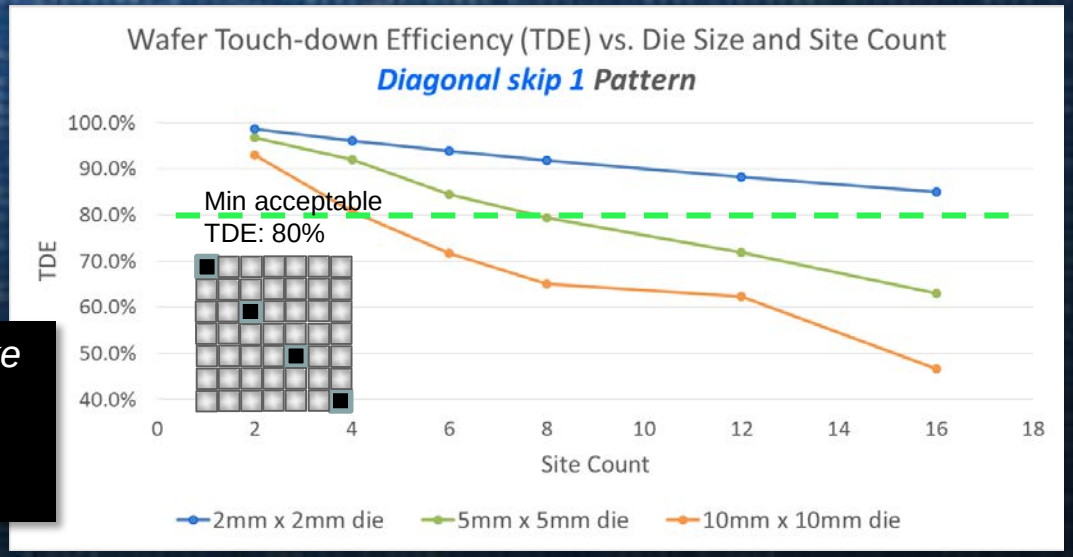
Touchdown pattern, 8 site diagonal 5mm wafer without going off-die



If probes cannot land off the die, some devices (in pink) cannot be tested, reducing yield

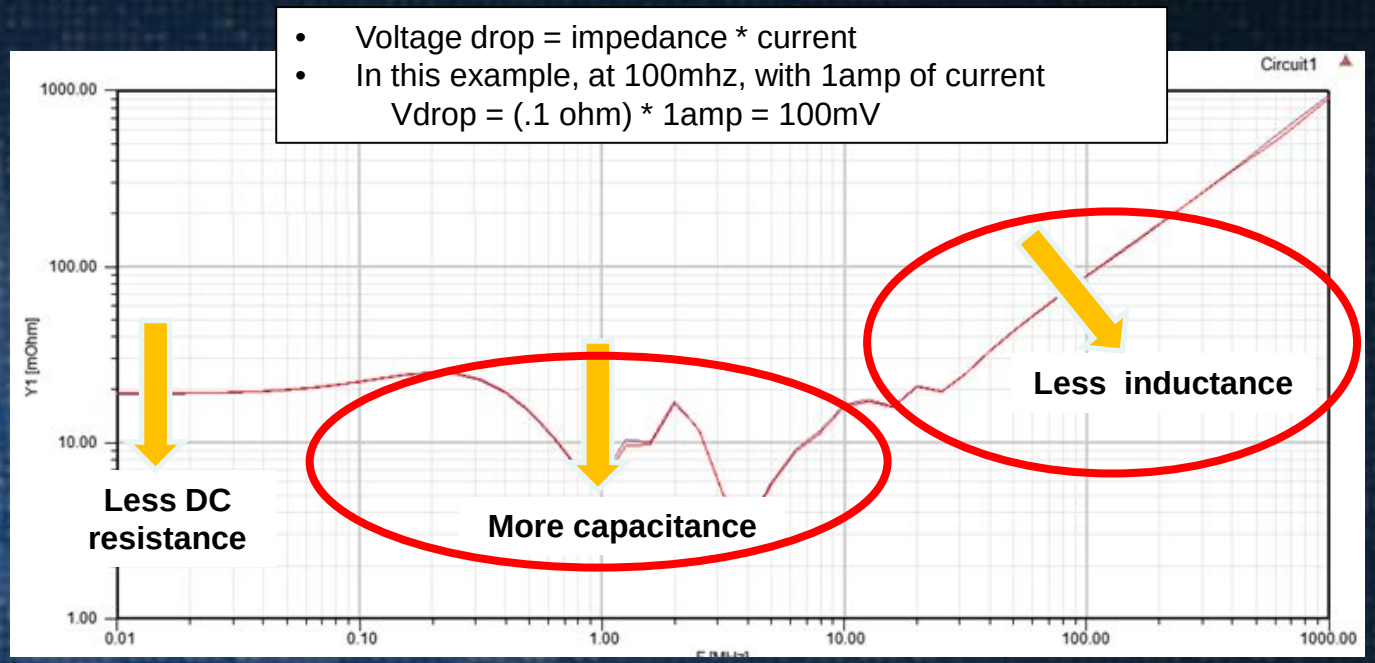


Skipping die to make probe card layout easier makes TDE even worse



Power Density - Power Impedance

- **Many devices need less than 10% voltage drop from nominal power input without impacting yield**
  - Power rails continue to decrease in maximum voltage as transistor size shrinks
  - 900mV (today) ➔ 600-700mV (2020).
  - 90mV droop (today) ➔ 60mV (2020)
- **Number of power rails continues to increase:**
  - App Processor: 20+ rails / DUT
  - Auto MCU: 10+ rails / DUT
  - RF: 8+ rails / DUT
- **Challenges:**
  - Site matching: <2-3% site/site variance
  - Power rail density: ~4 rails / layer (today)
  - Needle / socket pin impedance. Contact technology is limiting performance gains.



	Rails / DUT	Site Count	PCB Layers
AP	20	8	40
Auto MCU	10	16	40
RF	8	16	32
PMIC	20	8	40

+60% of PCB layers and increasing. Already limits site count increases

Component density - yield & diagnostics





AOI

Fault Coverage: 30%*

Limitations: small component (< 0201 body) faults need 10um defect resolution to identify

Flying Probe

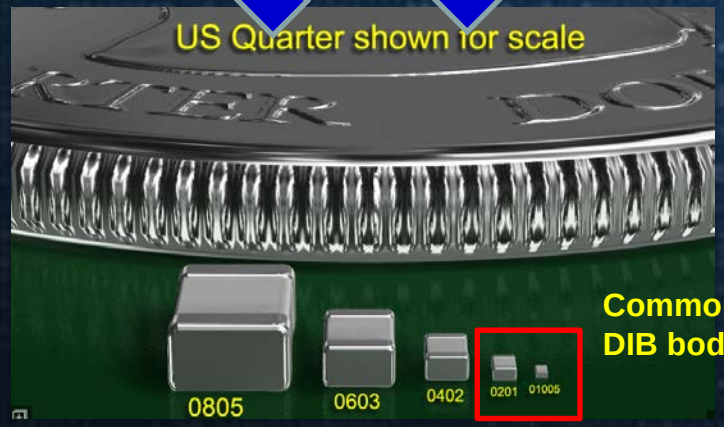
Fault Coverage: 37%*

Limitations: small component (below 0201) cannot be accessed to probe

In Circuit Test

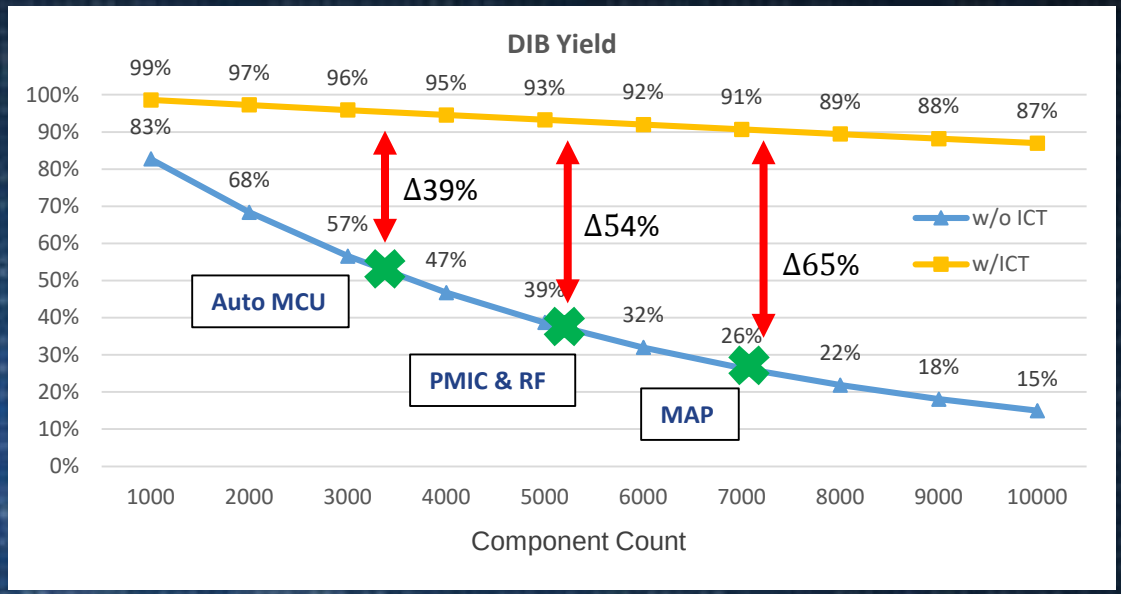
Faults Found: >80%*

Limitations: lead time (>6 wks), cost prohibitive ($+60K) , and intrusive (test point insertion)



Common ATE DIB body sizes

High component count + small body size = poor yield



Assembled DIB / probe card yields impact new silicon bring up time:

- Unknown, random assembly defects are difficult to differentiate from defects in new silicon or test programs.
- Conventional practices (AOI & Flying Probe) have low fault coverage, ICT not feasible for custom DIBs (long lead time, test point insertion)
- Physical defects: DUT area scratches, pad planarity all at micron scale

Component counts will continue to grow

- Application space is fixed, site count will continue to grow
- Application circuits becoming more complex, more like the end application

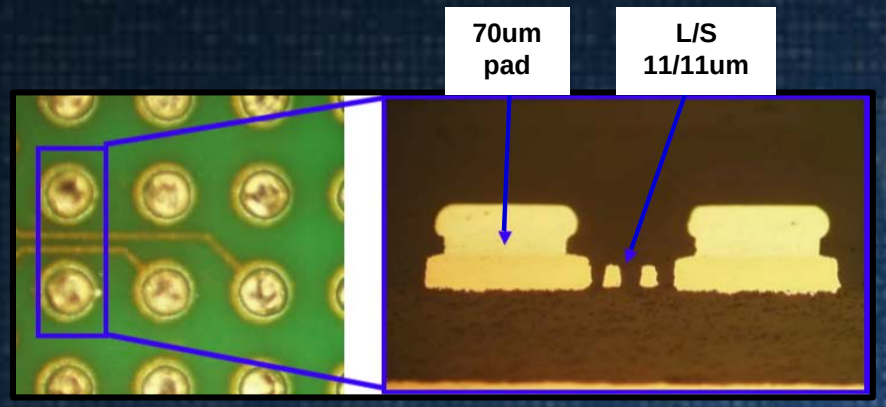
DIB 2028 targets

		2018 (today)	2028 (future)
Pin density	The number of DUT sites and DUT pin count in the same or smaller area drive up the pin area density. **Challenge**: Routing out the signals to the instruments and power supplies becomes increasingly difficult.	4,000 I/O per sq in 80um C4 pitch	16,000 I/O per sq in 40 um C4 pitch
I/O Performance	Increased challenges with high speed I/O (PCIe, DDR Interfaces, mmWave) to support BW intensive end products. **Challenge**: Increasing test standards (signal integrity, eye opening) including safety to insure quality for the end applications.	32 Gbps (dig) 6 GHz (RF) 1 kVA (power)	128 Gbps (dig) +100 GHz (RF) 10 kVA (power)
Power Performance	Device Supplies < 700mV require excellent accuracy. Increasing power rails per DUT consumes high PCB layer count. **Challenge:** Increasing test standards (power impedance curve) to insure quality for the end applications.	4 power rails / layer (PCB) 20mOhm @1MHz 100mOhm @ 100 MHz	16 power rails/layer (PCB) 5mOhm @1MHz 20mOhm @ 100 MHz
Components	Application circuit complexity increases component count per DUT site. **Challenge:** Use of smaller foot print components make diagnosing and repairing defects increasingly difficult to detect and time consuming	70 comp per sq in (0201 body size) 1st time BIN1: 50%	200 comp per sq in (sub-01005 body size) 1st time BIN1: +95%
Execution	Delivery of the device interface from pin-out freeze to wafer out for first probe contact with full performance **Challenge:** Increasing DI complexity increases risk of design or mfg defects. Complex mfg processes take longer.	75% OTD 6 week leadtime	95% OTD 3 week leadtime

Must achieve these targets in combination to best optimize:

- COT reduction
- TTM & TTV
- Test quality

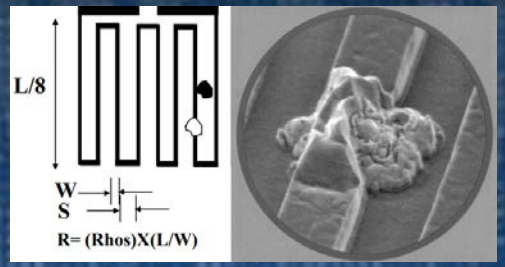
Device Interface at Sub-micron Scale



- Fine pitch DUT area routing escape is an enabler to increase I/O density
- Smaller line / space enables more than one signal to escape on a single layer requiring fewer toal layers
- As pin pitch decreases the L/S becomes smaller, requiring sub-micron scale process capability and control

Defect Density

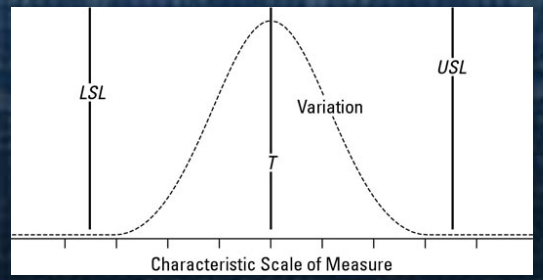
Size and frequency of a random defect that can cause a short / open



- Cleanliness is a function of all critical inputs: people, process, tools.
  - Requires a wholistic yield management system.
- Characterization & testing is required to set process targets and drive continuous improvement
  - DIB TTM & quality standards don't allow experimentation on a live project
- To achieve a viable yield
  - < 0.1 defects / DIB @ 400x400mm
  - A 10um process requires Class 100

Process Capability

The ability of a process to produce output within specification limits



- For a 11/11um L/S feature, to maintain impedance control:
  - +/- 5% = +/- 2.5um
  - To meet a Cpk of 1.67 requires measured std deviation of ***0.5um!***
- L/S control is the outcome of process capability of photo & etch
  - Since the processes are sequential the individual process capability must be even better!

“Sub-micron scale” Device Interface Era

Emerging paradigm: “It is a system problem at the test cell level”

- **Engineer the full path taking into account everything from Instrument to DUT contact**
- **Sustainable pin scaling curve: “2 x 4 scaling” – 2x pins, 2x performance every 4 years**

This paradigm will require a significant change in how designers and suppliers approach the problems:

- **Sub-micron scale resolutions & accuracy enabled by semiconductor class capabilities and processes**
- **Collaboration among industry specialists: ATE, Probe / Handler equipment, manufacturing, socket / probe head, etc.**
- **Major upgrades in engineering skill, discipline, and investment**

People	Process	Tools
• Management • Design: architecture, PI & SI • Process engineering • Quality engineering • Line operators	• Design: concurrency • Materials characterization • Process characterization • Quality management • Business & Operations	• Design: layout, sim, mechanical • Automated process control • Yield/Defect management • Inspection & Diagnostics • Risk management & mitigation



SW Test Workshop

Semiconductor Wafer Test Workshop

5G: THE NEXT DISRUPTIVE TECHNOLOGY IN PRODUCTION TEST

Daniel Bock, Ph.D.
Mike Bishop
Jeff Damm

FormFactor™

Michael Engelhardt
Michael Hemena
Robert Murphy
Balbir Singh

intel®

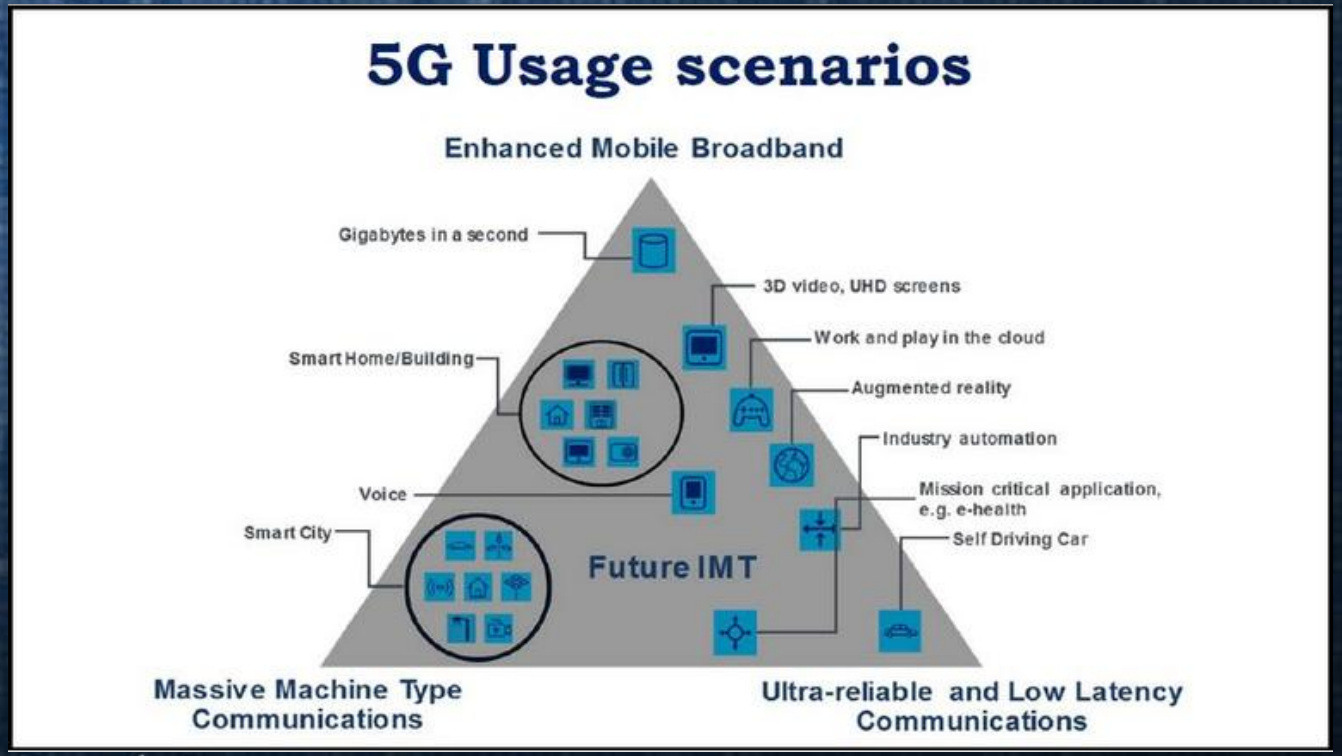
June 3-6, 2018

Introduction

- ***The development of 5G / WiGig products are creating a unique challenge for high volume production testing of the radio devices.***
- ***These devices operate at multiple frequencies throughout the 24 GHz to 86 GHz range, well beyond the 6GHz RF capabilities of most existing production ATE 's.***
  - *Design of the test solution requires creation of up/down converter circuits to reach 5G frequencies.*
- ***These devices may incorporate phased array beam-forming antennae for improved gain.***
  - *Beam-forming requires that a single DUT have a large number of RF, with many chips including more than 24 RF channels*
  - *Multi-DUT x8 test cell could require more than 256 RF channels.*
- ***The test solution for 5G devices as well as future WiGig products, will require testing of BGA, WL-CSP and DIE using both conducted and radiated methods in a full test cell.***
  - *The final HVM test solution design needs to have low installation cost and high volume test capabilities.*
- ***Results will be presented that illustrate initial testing of both conducted and radiated methods on test devices.***

What is 5G?

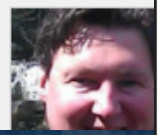
- *'It is a capital improvement project the size of the entire planet, replacing one wireless architecture created this century with another one that aims to lower energy consumption and maintenance costs. Sure, you'll download movies faster on your phone, but that's not the real reason 5G's arrival is being accelerated'. – Scott Fulton III, ZDNet*
- 5G will include:
  - *Fixed wireless data connectivity*
  - *Edge computing services*
  - *Machine-to-machine communications*
  - *Video delivery services*



Who is 5G?

- All of the major players in semiconductor are working on pathfinding devices
- 5G is broadly seen as a paradigm shift and market entry opportunity

DT Poised for 5G Launch as Huawei Antennas Go Up in Berlin



Digi and Ericsson tested live 5G connections showing the evolution from 4G

Facebook's New Focus On 5G and Golden Opportunity for Entrepreneurs

WIRELESS TECHNOLOGY

U.S.-China Competition Over 5G Likely to Increase, Even Without Trade War

Qualcomm Has Made It Cheaper To License Its 5G Technology

MACOM and STMicroelectronics to Bring GaN on Silicon to Mainstream RF Market

Like 0 Share Tweet Share

February 06, 2018 16:07 ET | **Source:** STMicroelectronics N.V.

- *Combines manufacturing scale, supply security, and surge capacity from ST with MACOM's GaN on Silicon RF power products to address m consumer, automotive, and wireless basestation programs*
- *ST licenses MACOM's technology to supply GaN on Silicon RF power products*
- *Anticipated breakthrough cost structure and power density of GaN on Silicon would enable 4G/LTE and massive MIMO 5G antennas*

Nokia, Telia and Intel carry out 5G manufacturing trials

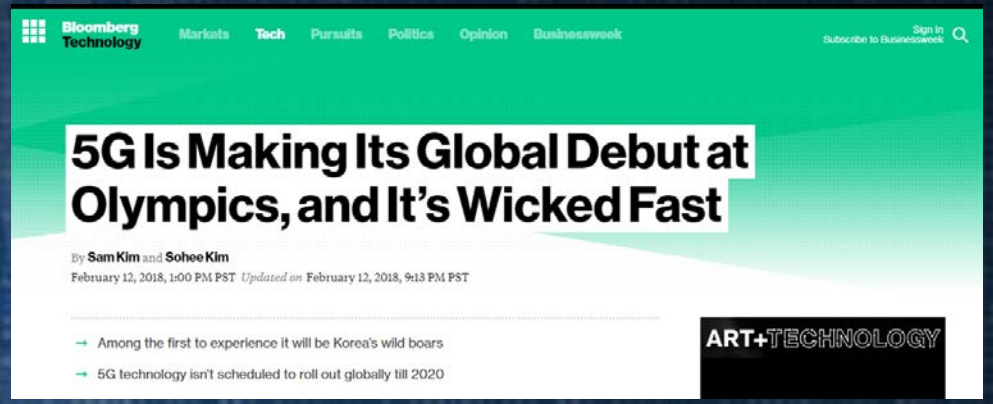
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13 April 2018 | Natalie Bannerman

Nokia, Telia and Intel have successfully carried out an industrial trial using 5G to improve the time sensitive applications and enhance productions in manufacturing.

5G Field Trials Olympics

- **Intel and Korea's mobile carrier KT were showcasing some of the possibilities at the 2018 winter Olympics:**
  - Provided tablets equipped with faster speeds in "spectator zones"
  - Buses with no drivers
  - 360 degree VR in real-time for figure skaters



- **Japan 2020 Summer Olympics is expected to have the largest commercial deployment of 5G – Intel w/ NTT Docomo partnering**
  - Intel is promising 8k 360 degree video streams

What are we seeing with 5G devices?

- **The efforts to develop 5G fall under 3 main categories:**
  - –Spectral Efficiency: Better use of the RF spectrum for greater bandwidth over farther distances of communication
    - 30 GHz, 40 GHz, and 60 GHz bands are being added
  - –Energy Efficiency: Reduce power usage for lower cooling costs and longer lifetimes of battery operated devices
    - Beamforming for antenna gain, requiring more antenna channels
  - –Utilization: Infrastructure overhaul with more distributed, high speed digital devices
    - More high speed devices with a larger number of base stations

What does 5G Production Test Require?

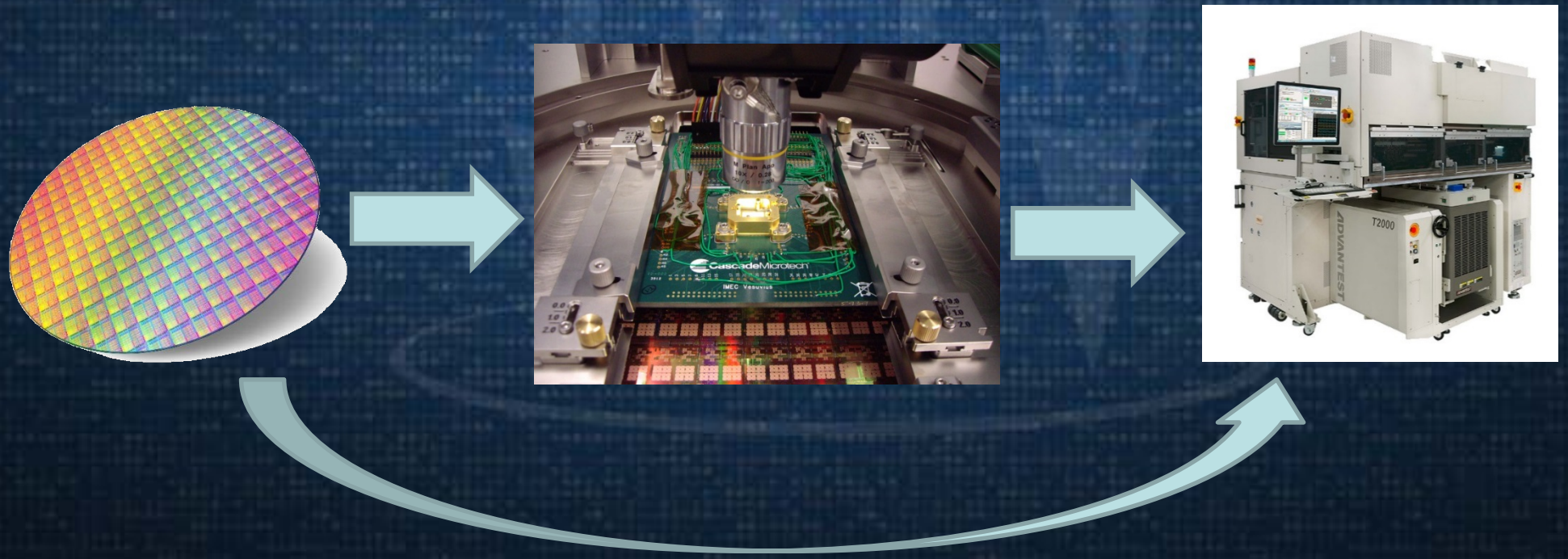
- **5G components testing will require:**
  - New test equipment:
    - Higher frequencies than current ATE testers are capable of measuring
    - Higher number of channels
  - Time of test as low as possible with high throughput
    - Parallel test (multi-site)
  - High Accuracy
    - Good Signal integrity at high RF frequency
    - Prevent packaging bad devices due to yield

Possible 5G Wafer Test Methods

Test Method	Wafer Test Cost	Functional Test Coverage	Full RF Bandwidth Test	Probe Card Complexity
Full Channel				
Loopback				
Baluns, Switches, Combiners				
DC Test				
Antenna Coupling				
No Wafer Test				

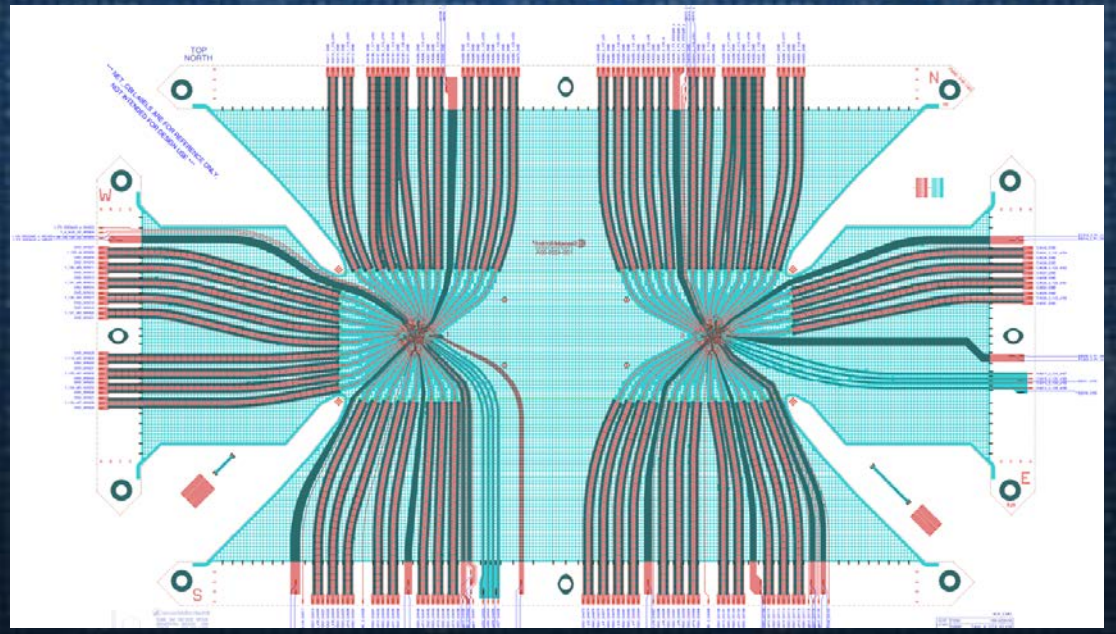
Wafer Test vs Final Test

- *Advantages:* Reduces lost cost from packaging bad parts when there is low yield; final test cannot do parallel test
- *Disadvantages:* Adds in cost to final product; additional time in the process flow prior to packaging; if yield is low, than a lot of packaged parts are thrown away



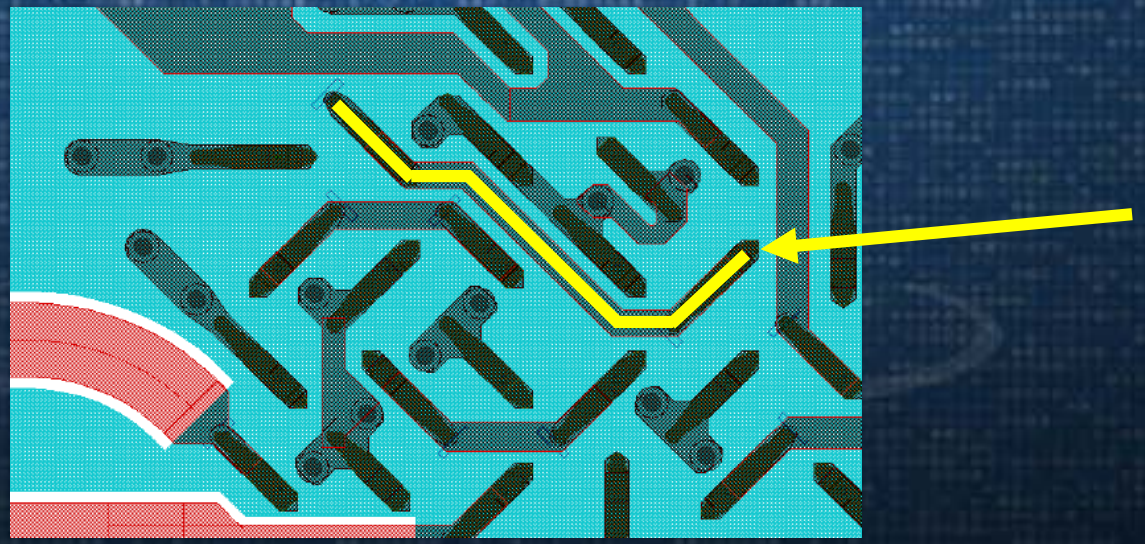
Full Tester Channel Count

- *Advantages:* Full test coverage and very fast
- *Disadvantages:* Very expensive tester; high channel count required; space transformation difficulties likely with the high number of I/O



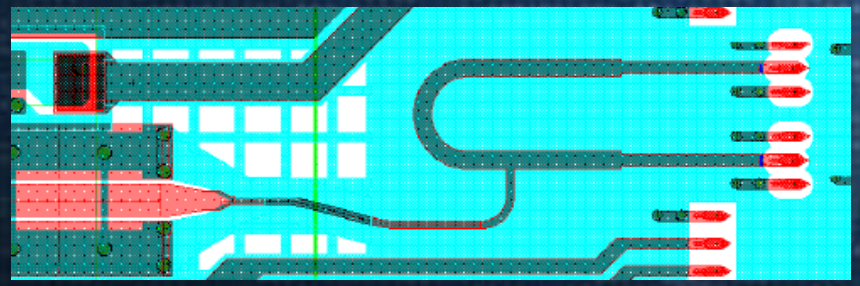
Probe Head Loopback

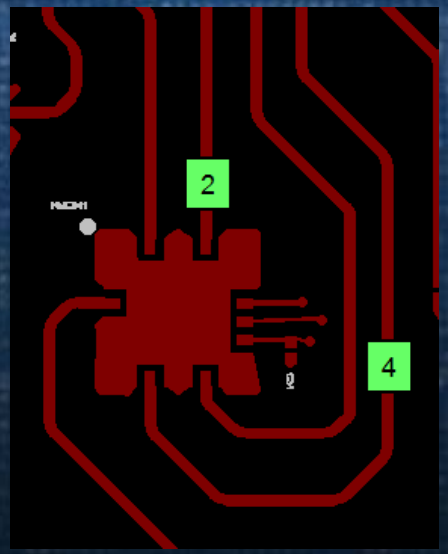
- *Advantages:* Does not need high number of channels and minimal space transformation
- *Disadvantages:* No access to die by tester and depends upon the DUT to know if it fails; and routing requires no crossing

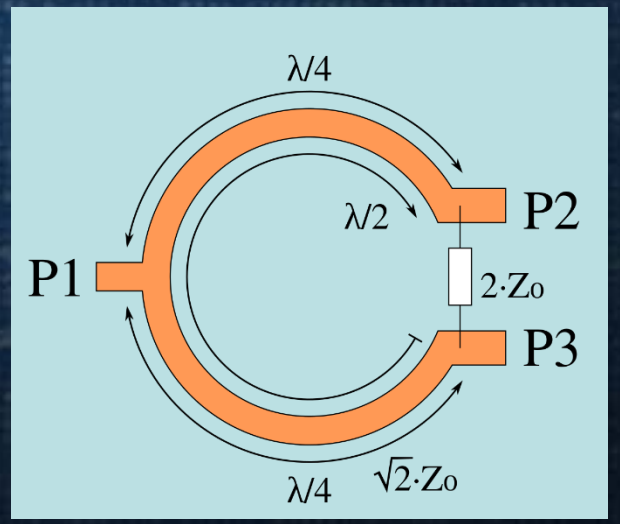


Baluns, Switches, Combiners

- *Advantages:* these are known methods of reducing total channel count in a tester, and there are some COTS parts available
- *Disadvantages:* Can have minimal effect in space transformation, increased loss compared to direct connection, and most parts can only operate up to maybe 50 GHz

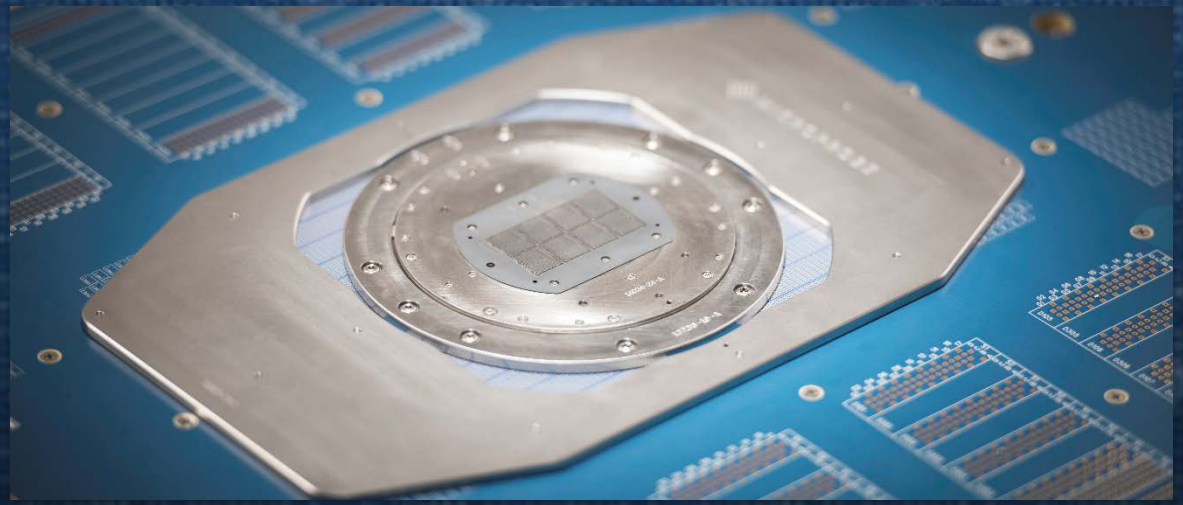






DC Test

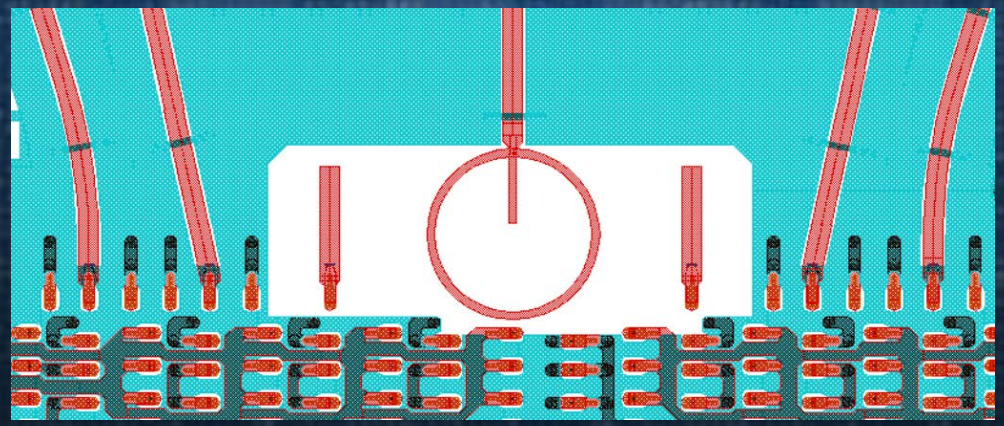
- *Advantages:* Lower cost tester; does not need impedance control for cheaper interconnects
- *Disadvantages:* does not test actual part operation; checks connectivity only, not KGD



MF80 Probe Card

Antenna Coupling

- *Advantages:* can be used to reduce total channel count (4:1 combining); mimics OTA test
- *Disadvantages:* more loss than conducting measurements, need open space in the area to fit an antenna large enough

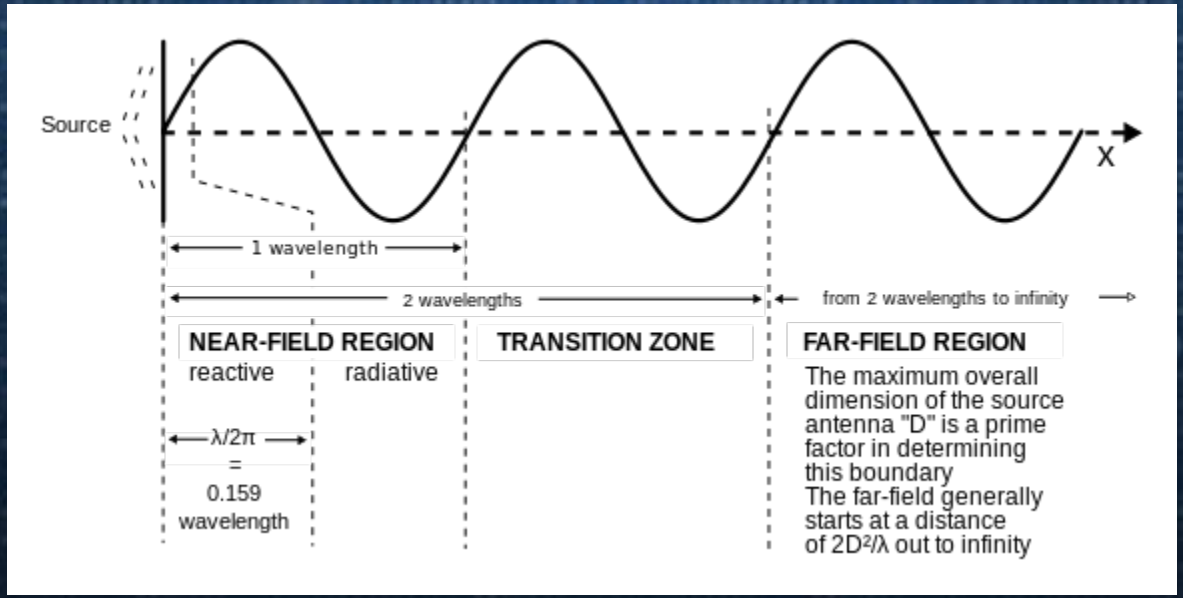


Wafer Test Methodology Summary

Test Method	Wafer Test Cost	Functional Test Coverage	Full RF Bandwidth Test	Probe Card Complexity
Full Channel	🔴	🟢	🟢	🔴
Loopback	🟢	🔴	🟢	🟡
Baluns, Switches, Combiners	🟡	🟢	🟢	🔴
DC Test	🟢	🔴	🔴	🟢
Antenna Coupling	🟢	🟡	🟢	🟡
No Wafer Test	🟢 / 🔴	🔴	🔴	🟢

Distance to Antenna – Near field vs. Far-field

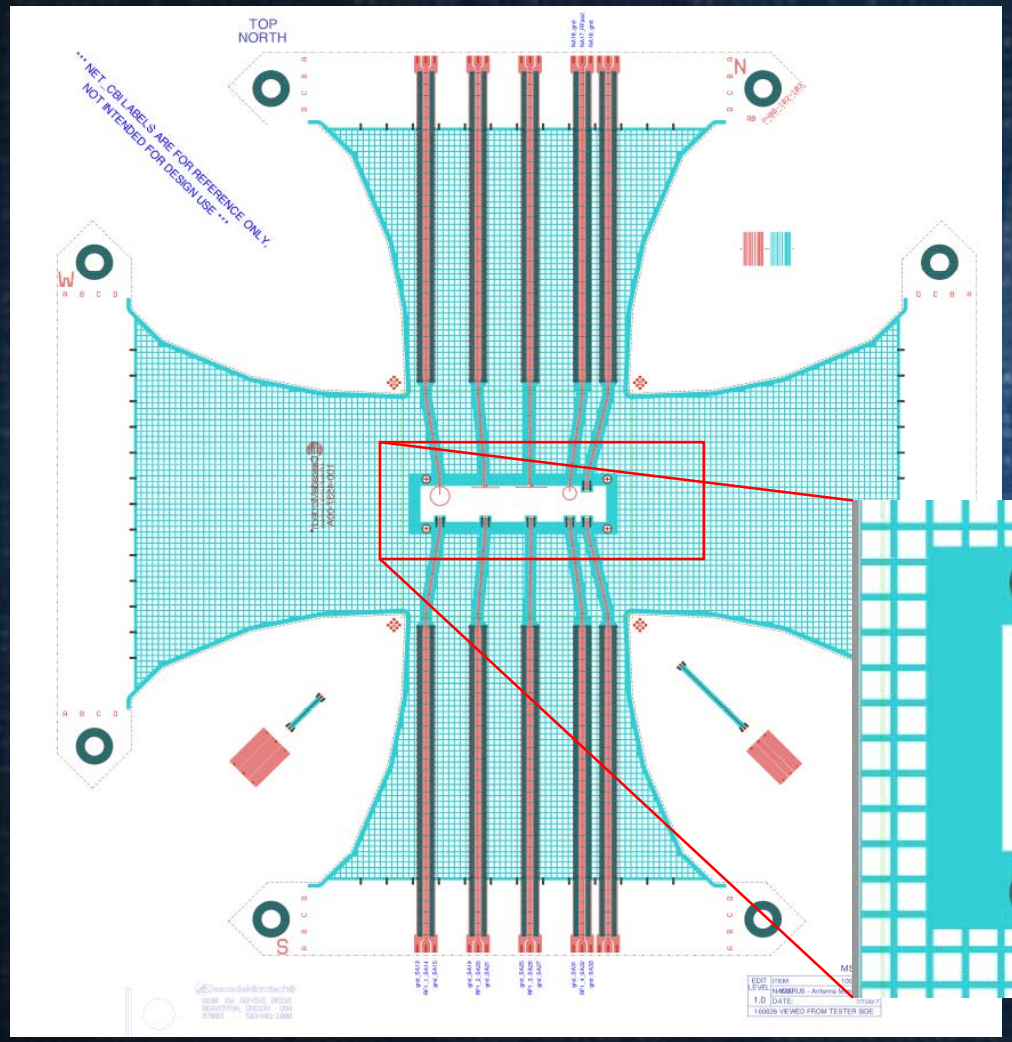
- **The membrane is so close, does it need to be a full antenna?**
  - The distance from the antenna will be well below one wavelength (30 GHz λ = 10 mm), so the field distribution will depend upon the distance from the antenna



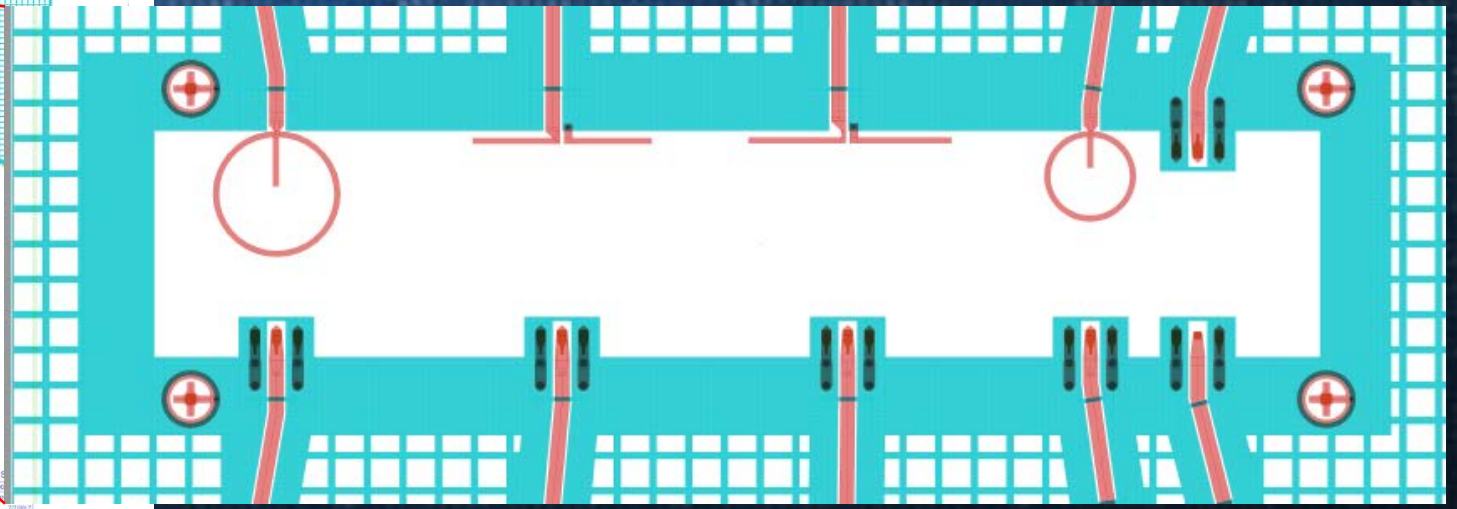
Antenna Uses in RF wafer test

- **Interrogate on die antennas**
  - It can be used for packages with antennas added
  - Can a bump or pad be interrogated?
  - Can it help with the high channel count to reduce the number of RF channels being measured?

Layout of Test

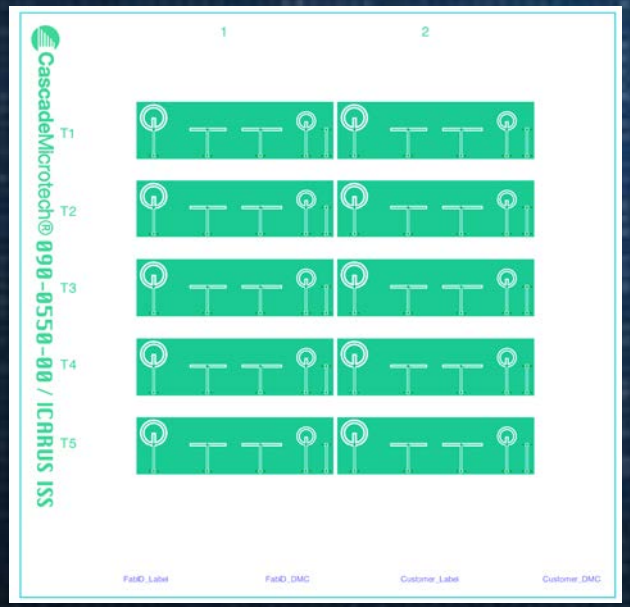


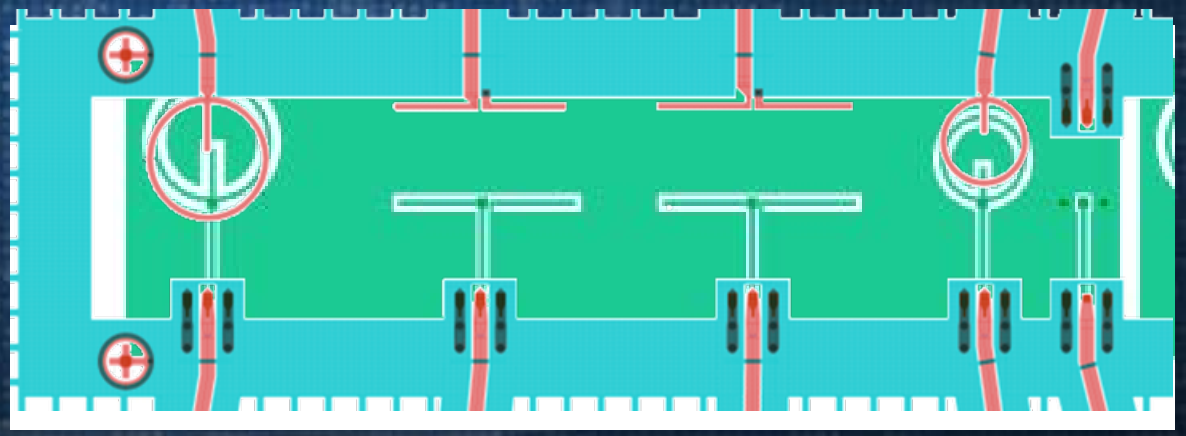
- The test layout has 2 dipoles, and 2 ring antennas
- It also has a pad for transmission with no antenna on the DUT



ISS for reception

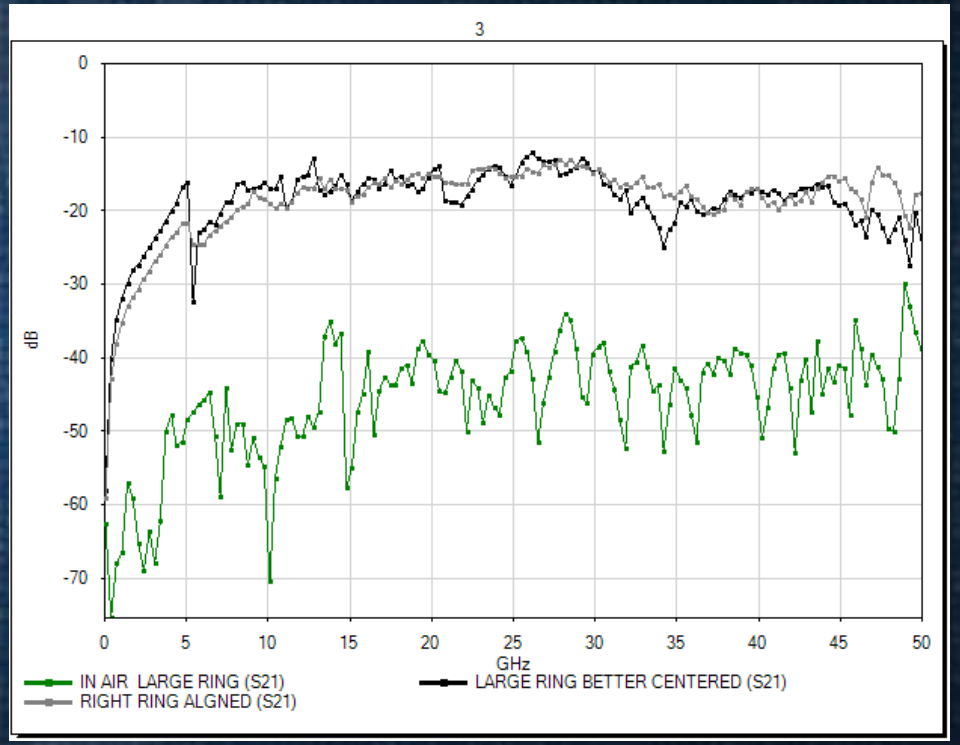
- An ISS was made for reception of the signals, which would then go back to the membrane using a GSG pair at the and of the transmission line





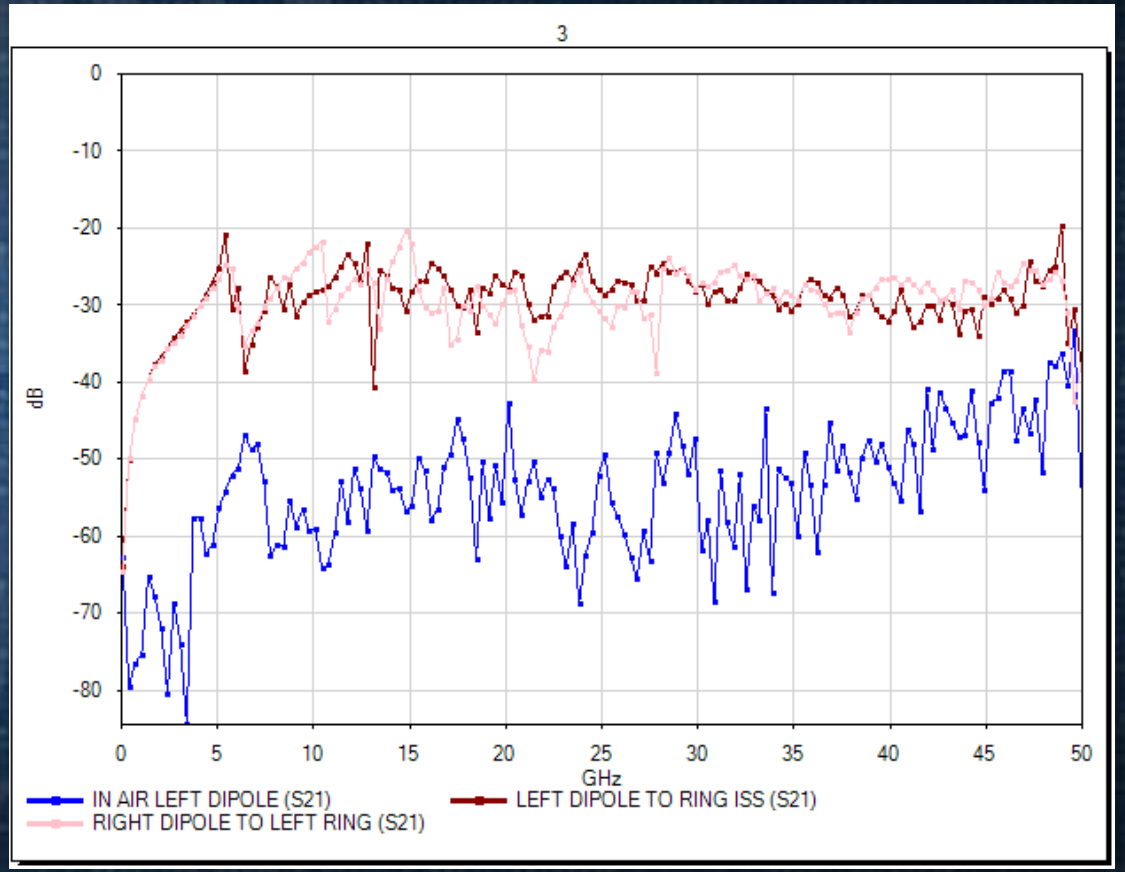
IL measurement of the large/small ring

- **Looking at transmission of the two rings, the amount of energy on IL is about 20 dB higher than the noise**
  - Noise is measured in the air, not in contact with the ISS for reception
  - The bandwidth is very wide because of the near field coupling in a wafer probing application



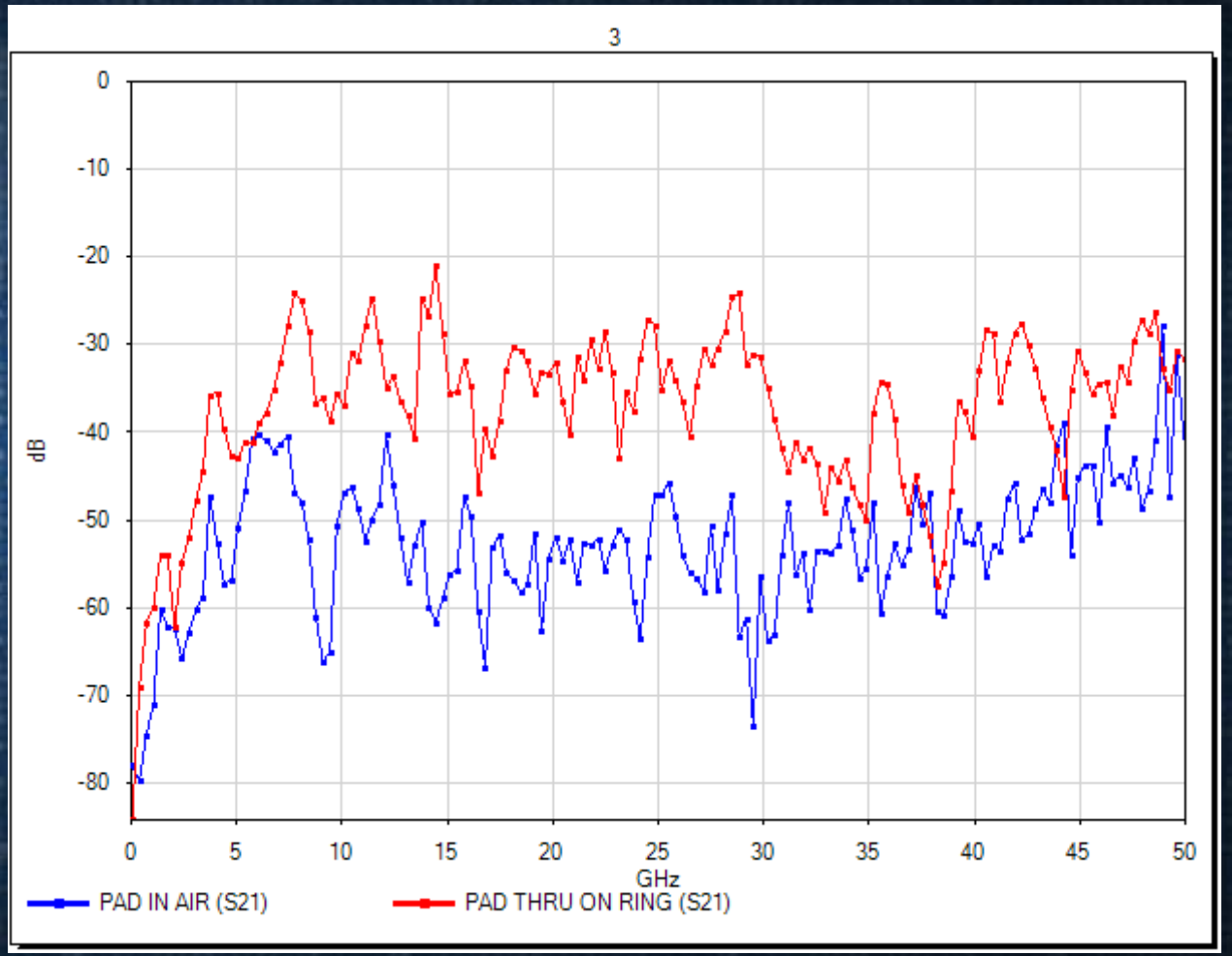
IL measurement of the large/small dipole

- **Looking at transmission of the two dipoles, the amount of energy on IL is about 20 dB higher than the noise**
  - Noise is measured in the air, not in contact with the ISS for reception
  - The received signal is ‘noiser’ than that of the ring antenna



IL from pad on ISS to Ring

- **The IL where the pad on the ISS is used with the ring antenna is used for reception, the signal is seen**
  - However, the reception is not as clean across frequency as seen on the other transmissions



ATE Testing of mm Wave at Intel

- **Test Setup**
  - Advantest 93000 PSRF ATE System was used to generate an up-converted 38 GHz signal and measure a down-converted 38GHz signal
  - SIU PCB (Wafer Sort Interface Unit) with mm Wave UDC (UP/Down Converters)was developed using off the shelf components.
    - The UDC up converts an IF signal from the ATE resulting in CW signal that was in the 38GHz band.
    - Similarly the UDC down converts a signal from the DUT to a signal that was within the measurement range of the ATE (< 6GHz)

Membrane Probe-head mmWave Testing on SIU

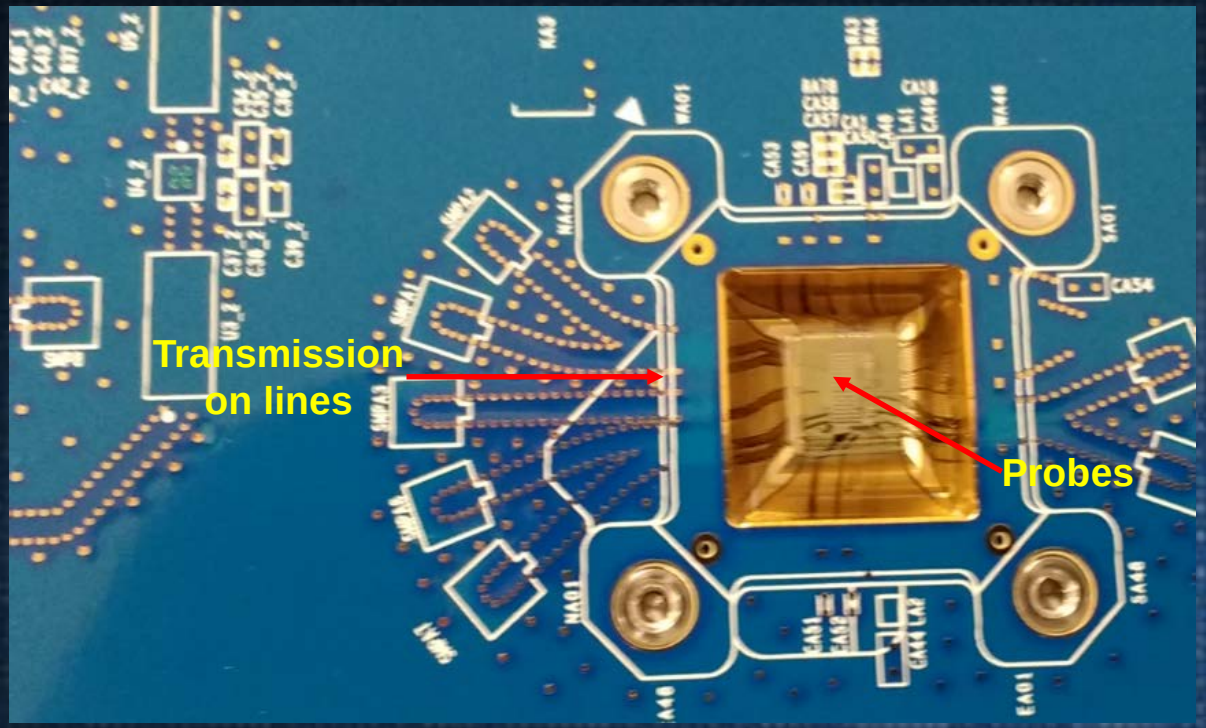
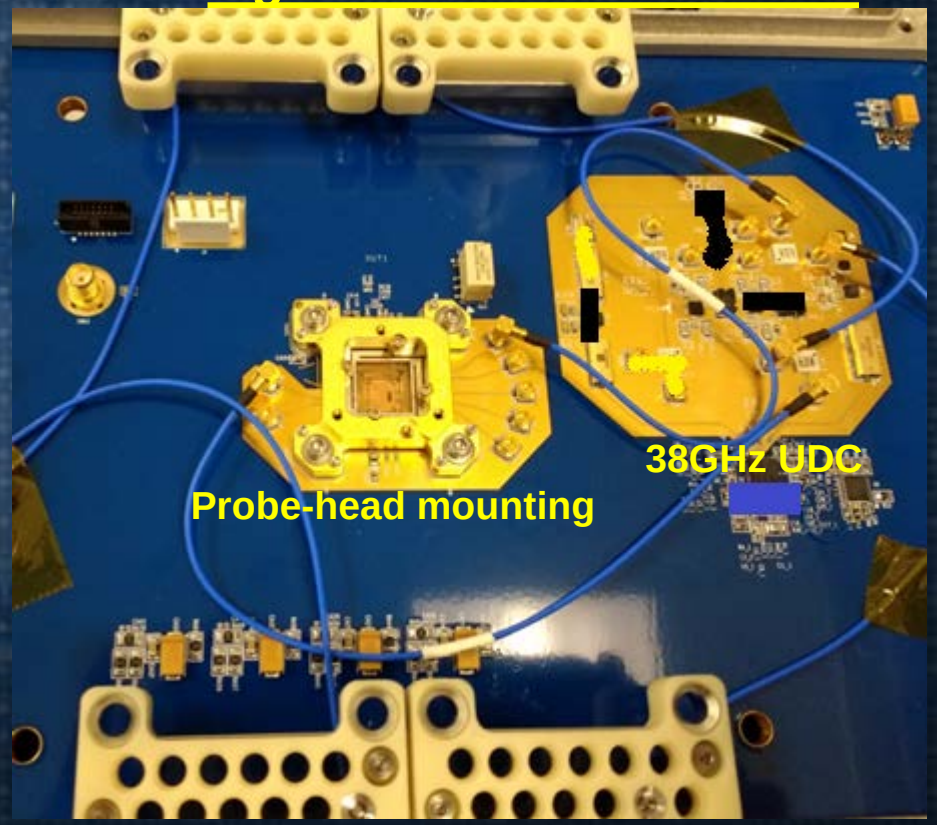


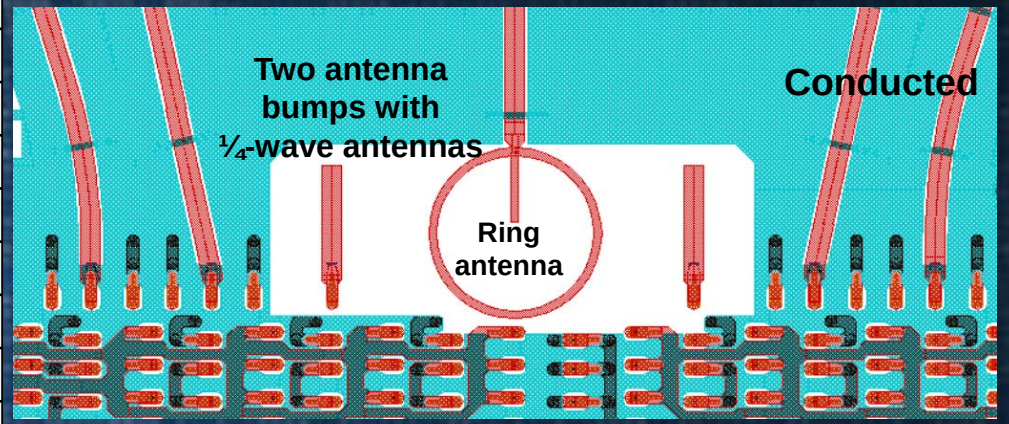
Figure 1: Wafer Sider of SIU

Figure 2: ATE Side of SIU



Repetability measuremnts at 38.56 GHz

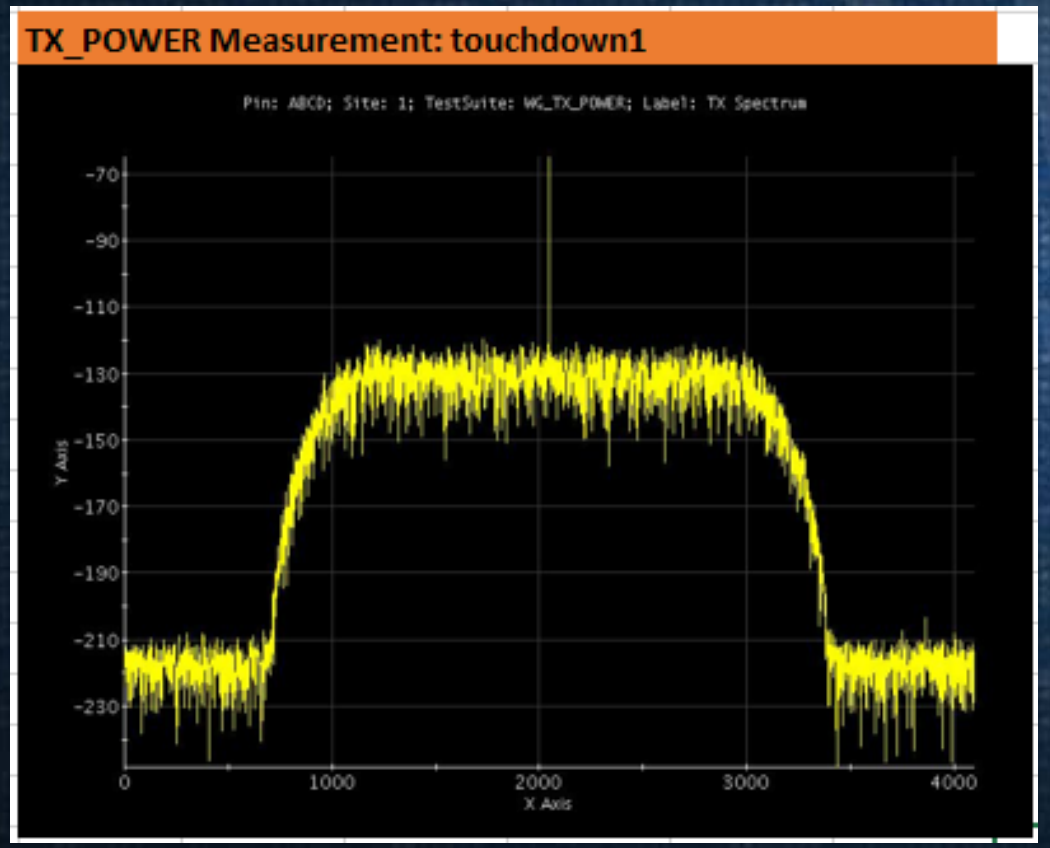
Probe touchdown	Transmit Power from Same DIE (dBm)		
	1/4λ to Ring Antenna	Ring Antenna only	Fully Conducted Path
1	-63.27	-86.67	-38.593
2	-63.169	-85.95	-38.594
3	-63.8	-86.68	-38.588
4	-63.825	-86.62	-38.589
5	-63.636	-85.63	-38.59
6	-63.687	-85.51	-38.597
7	-63.793	-86.62	-38.602
8	-64.043	-86.23	-38.61
9	-64.728	-85.14	-38.616
10	-64.673	-85.98	-38.615
11	-64.955	-86.69	-38.634
12	-64.866	-85.43	-38.649
13	-65.111	-85.95	-38.648
14	-65.785	-84.65	-38.698
15	-65.826	-84.25	-38.711
16	-65.854	-84.13	-38.757
17	-65.748	-84.32	-38.762
18	-65.831	-84.61	-38.766
19	-65.696	-84.21	-38.753
20	-65.692	-84.74	-38.778

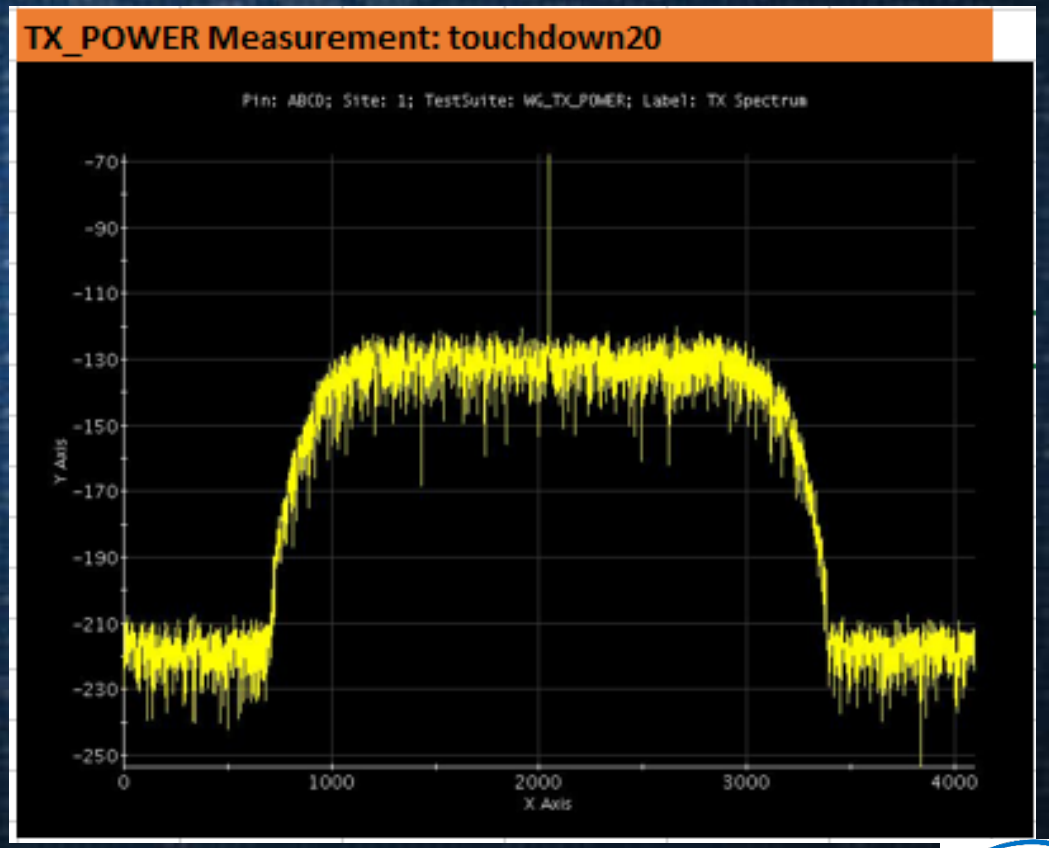


mm Wave Probe Connection: 2 to 1 combining with ¼-wave antennas

38 GHz CW Spectrum showing repeatability

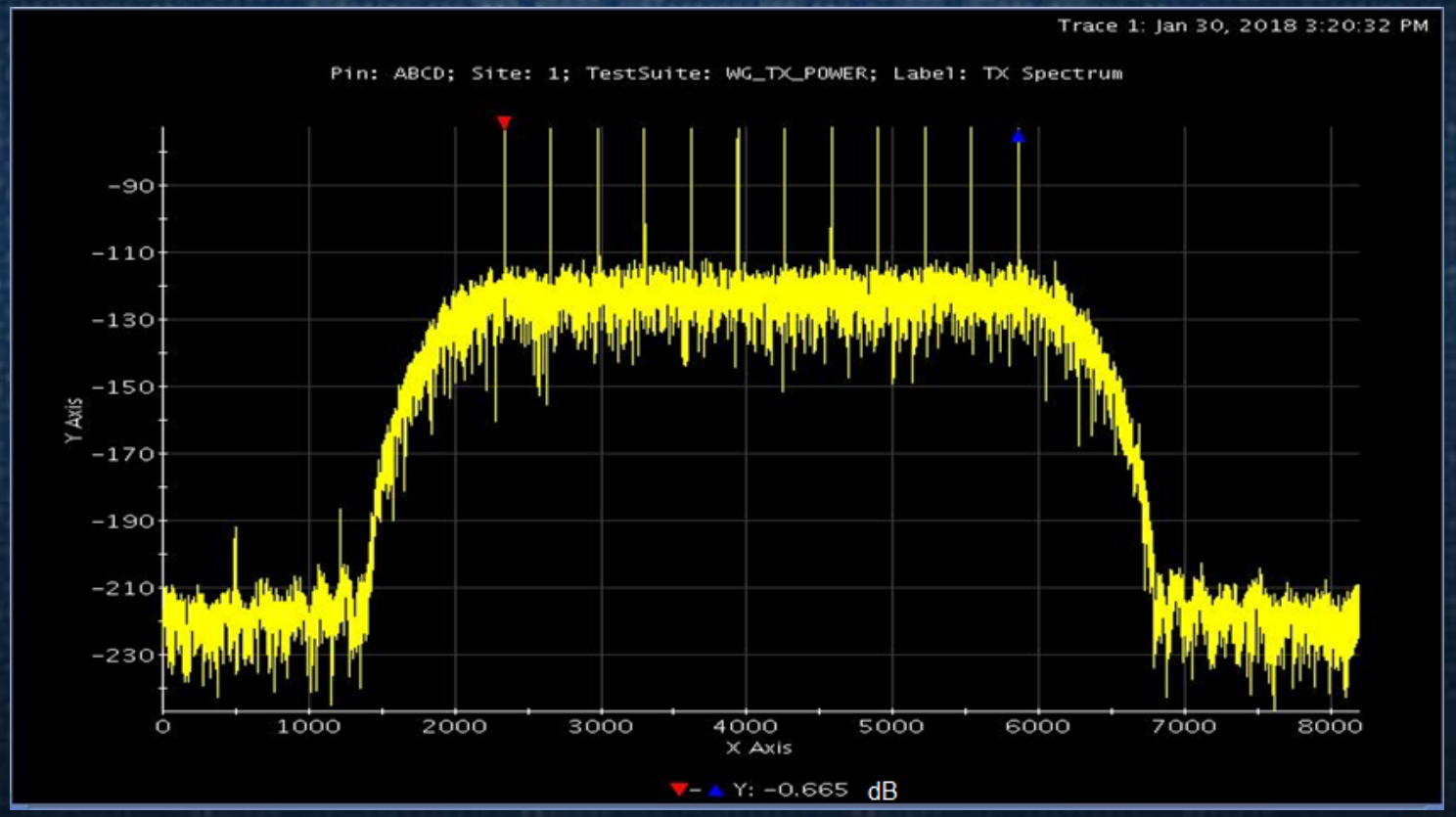
- This is CW Spectrum measured with the ¼-antenna





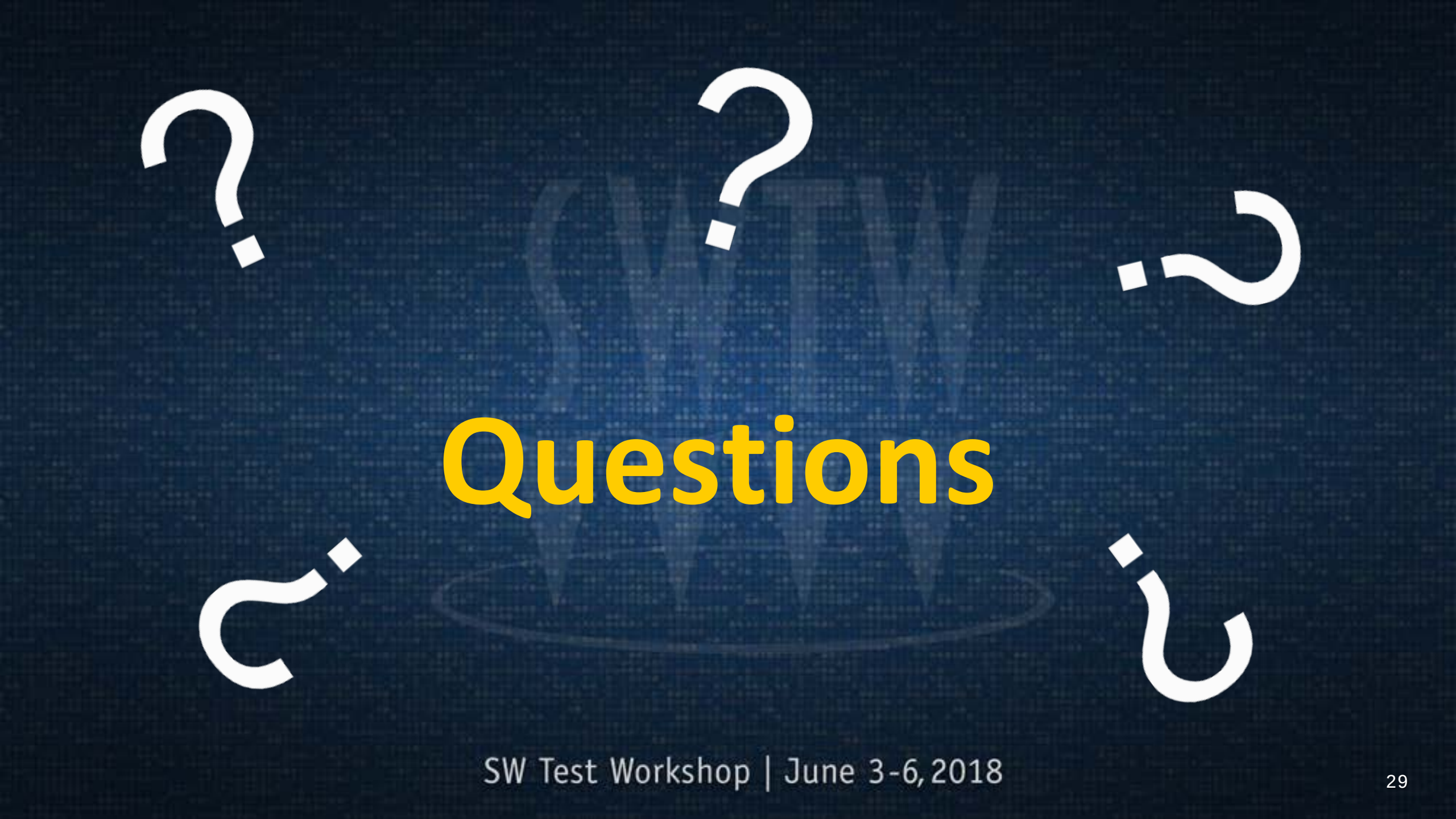
Multi-tone Spectrum's at 38 GHz

- **This spectrum is measured with the ¼-antenna**
  - 12 tone linearity using an IQ waveform



Summary

- **We have shown that using in membrane antennas is a feasible method for wafer production test**
  - It can reduce the total number of RF channels without expensive tester upgrades
  - Does not require large areas in the membrane
  - Has good signal integrity that will support 5G production test


Questions



SW Test Workshop

Semiconductor Wafer Test Workshop

Effects of Pad Structure on the Scrub Performance of MEMS Probes for Memory Devices



Aaron Woodard

Micron Technology, Inc

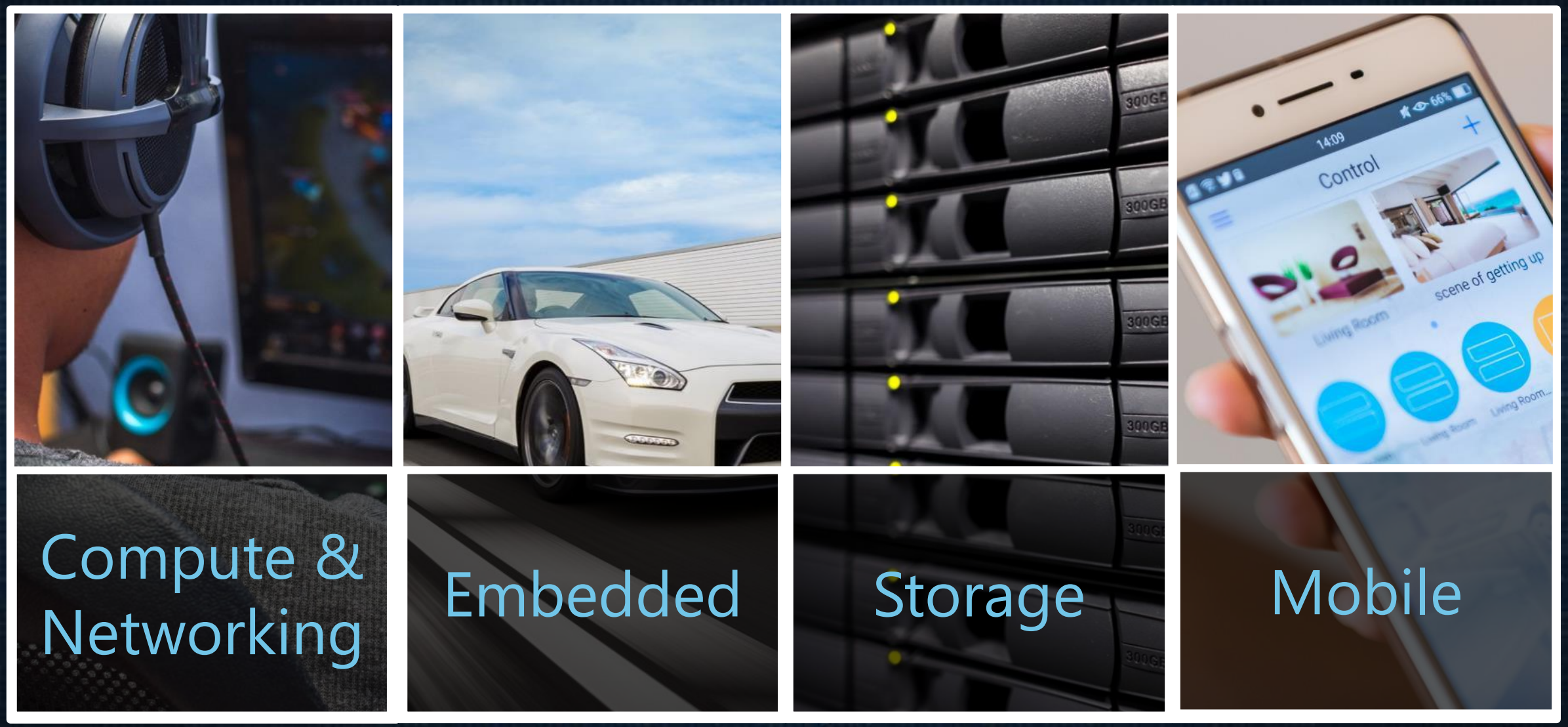
June 3-6, 2018

Outline

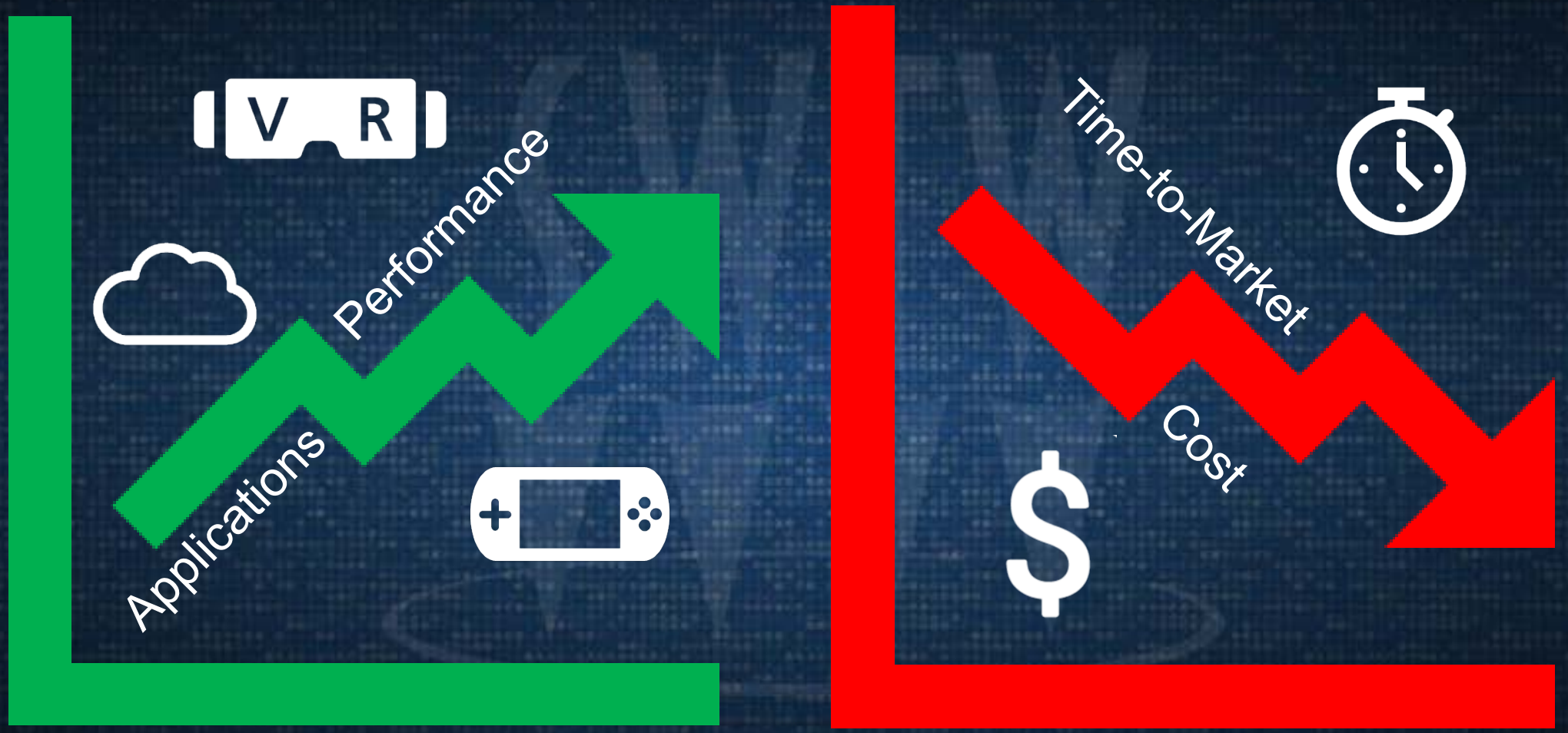
- Background / Trends / Test Requirements
- Experiment Design
- Results
- What Ifs
- Summary

Background

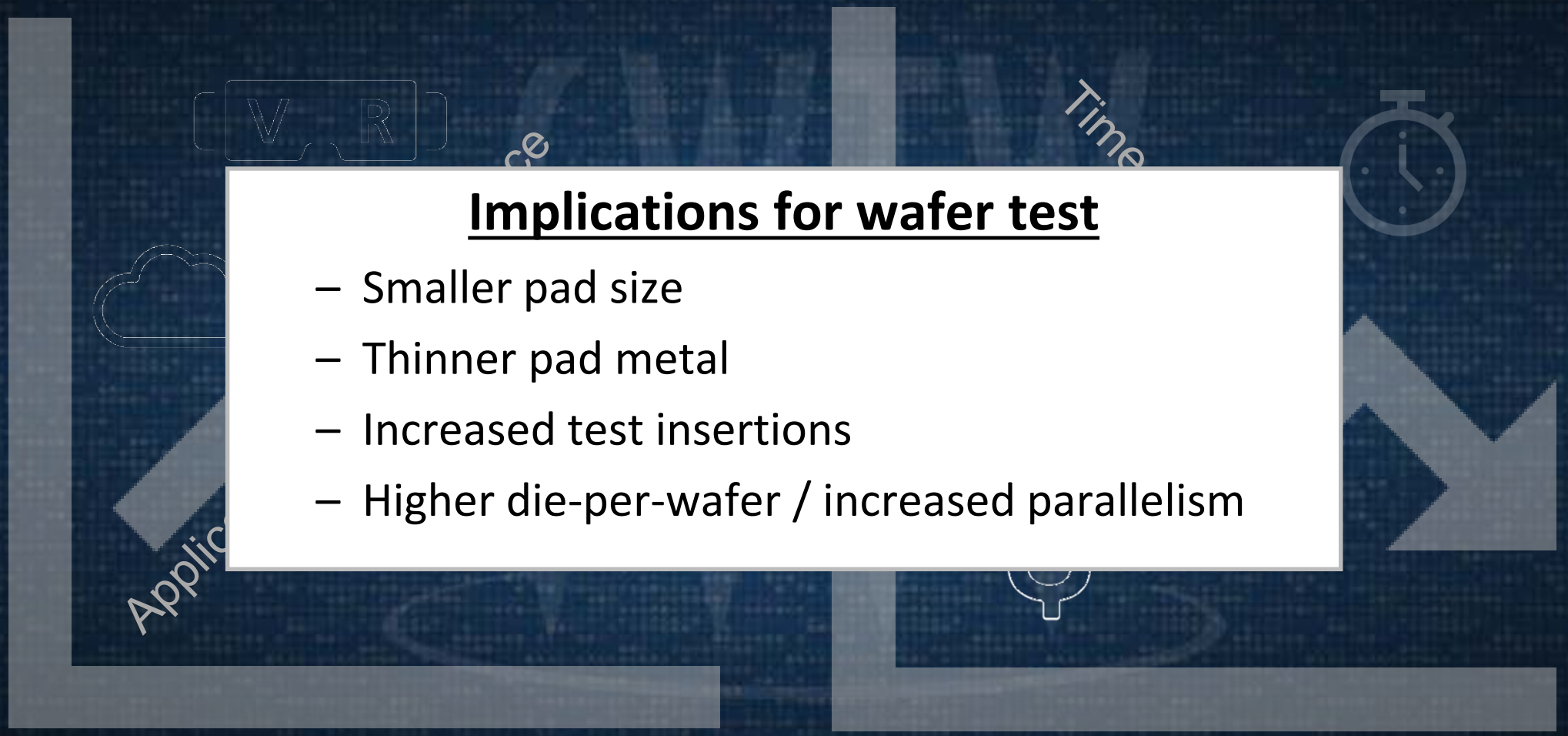
Diversified Memory Market



Industry Trends



Industry Trends



Implications for wafer test

- Smaller pad size
- Thinner pad metal
- Increased test insertions
- Higher die-per-wafer / increased parallelism

Generic Wafer Test Requirements



Scrub Depth < Pad Thickness



All Probe Marks Inside the Pad Boundary

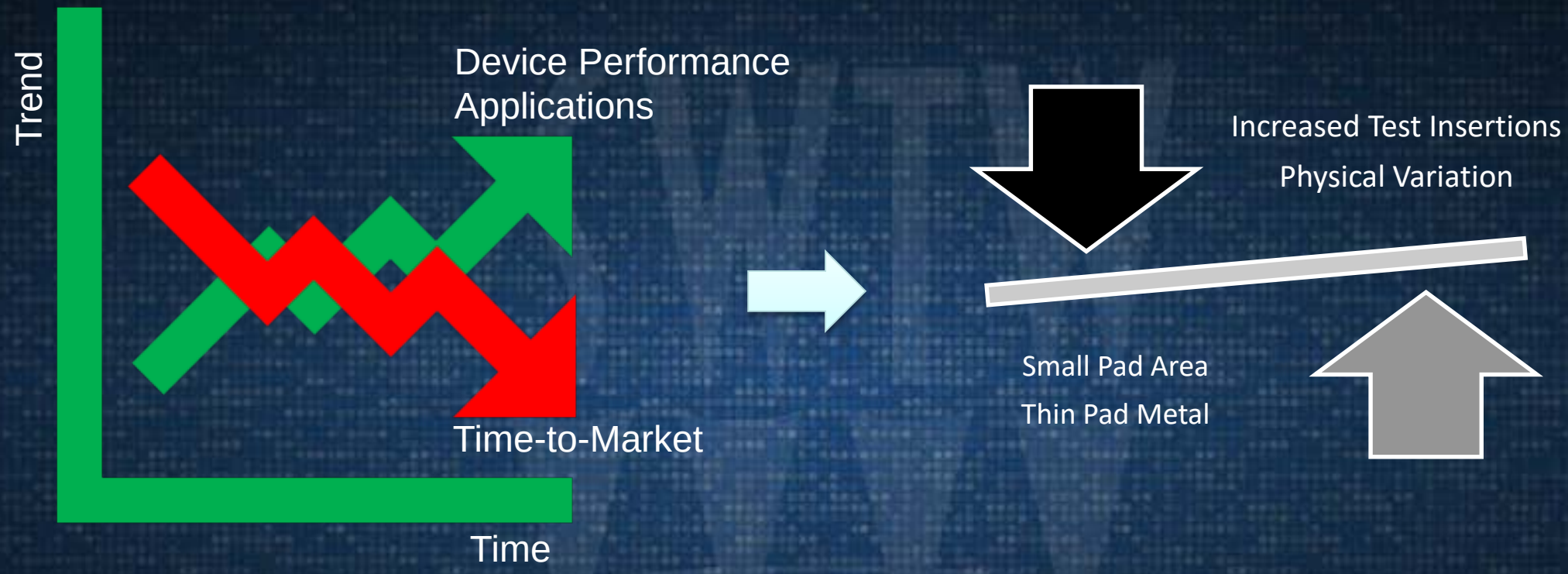


100% Electrical Continuity



Dual Temperature Capability

The Challenge

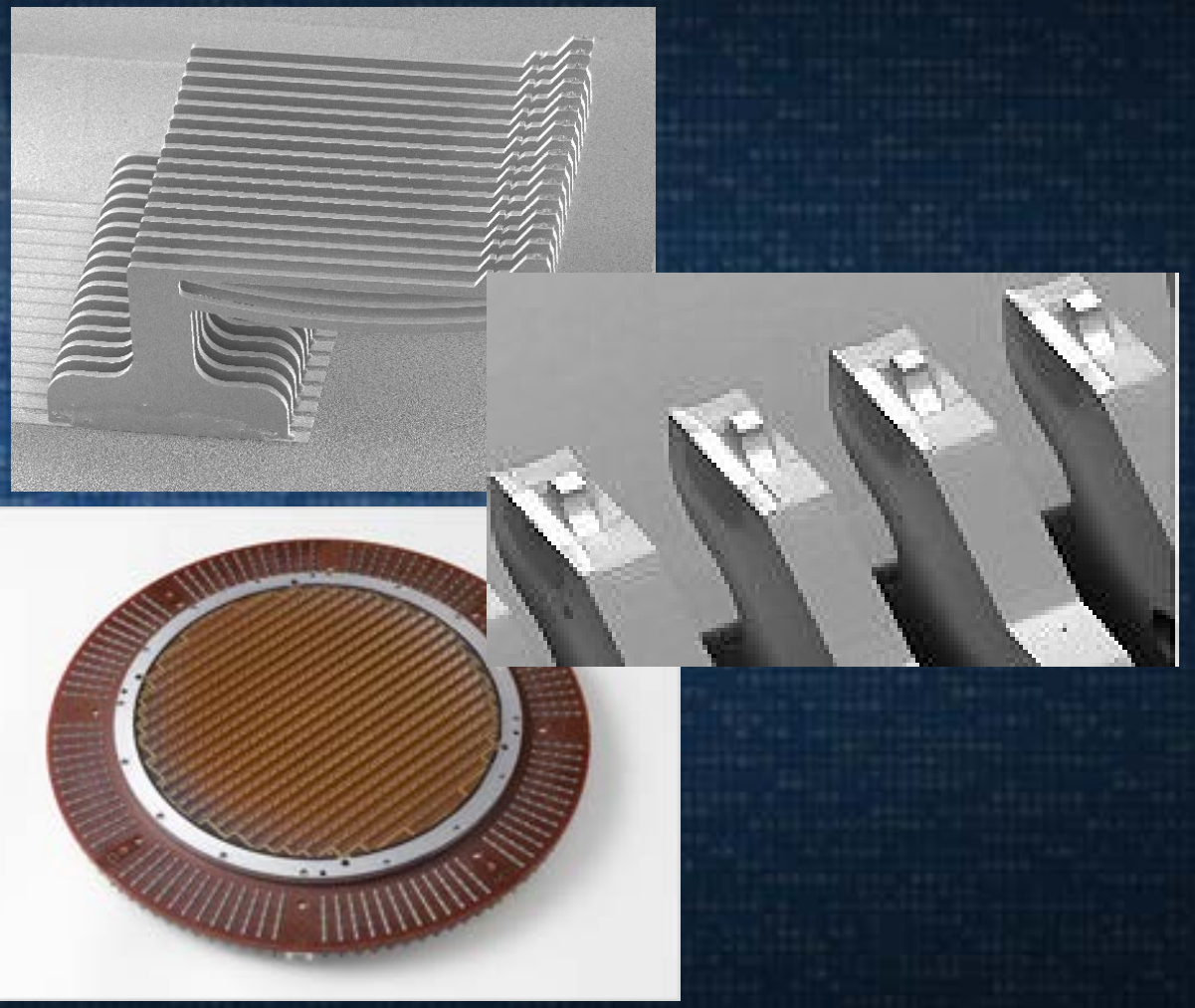


- **Balance scrub depth vs. scrub size to meet pad dimension reductions for devices with a breadth of physical properties**

Experiment

Advanced Probe Cards for Memory Devices

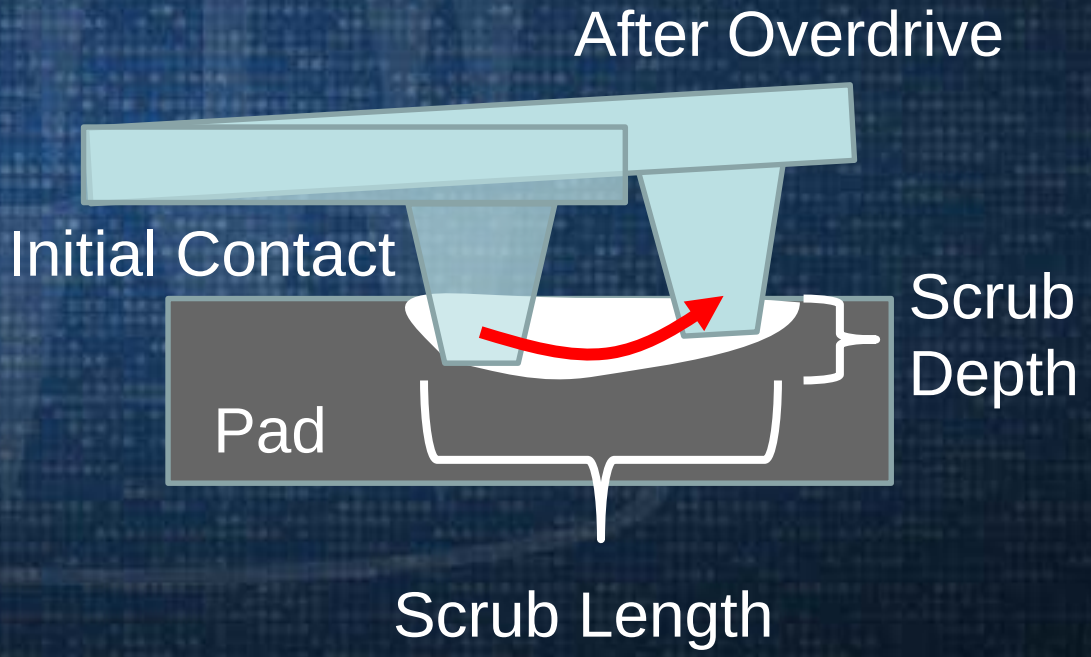
- "Micro-Cantilever" MEMS
- Full 300mm Probe Arrays
- >100,000 Probes per Array



MEMS Probe Key Characteristics

- **MEMS "Scrub" – Vertical + Lateral Pad Contact**
  - Scrub Ratio (Length vs. Overdrive)
  - Probe Force





Evaluation Items

- **Micron and MJC evaluated the following:**

Evaluation Item	Variables	Measured Value
Scrub Characteristics Single Contact	Overdrive Tip Size	Length Width Depth
Scrub Characteristics Multi-Contact	Overdrive Tip Size Contact Count	Length Width Depth

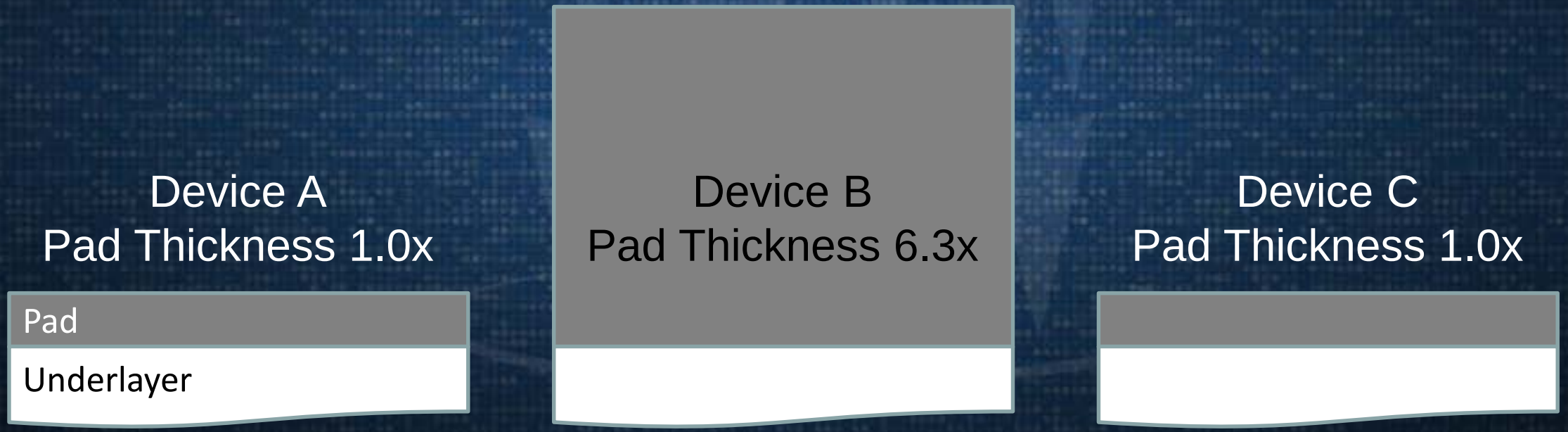
Conditions and Factors

- **Four different probe tips were evaluated on three different devices**

Item	Value
Wafers	Device A, B, C
Prober	300mm Wafer Prober
Temperature	Room Temperature
Probe Tip Type	1: Baseline 2: +70% Tip Area 3: +13% Probe Force 4: +13% Probe Force, +70% Tip Area

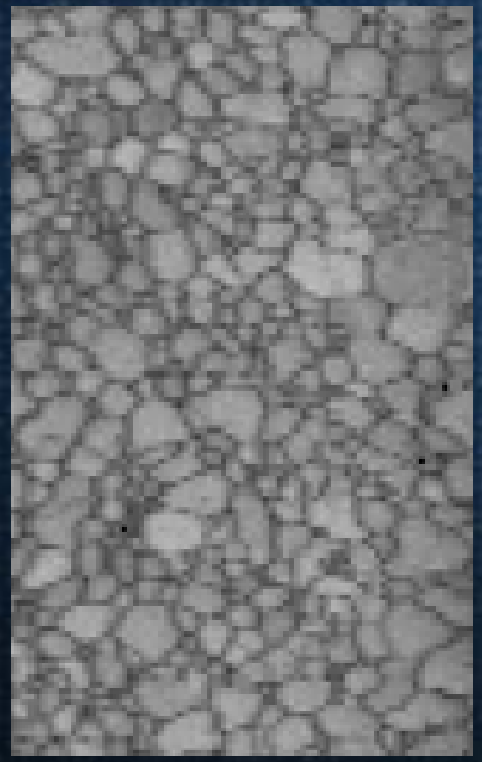
Device Probe Pad Characteristics

- **Pad Thickness Comparison**
  - Other properties (Pad Material, Surface Oxide, Hardness, Modulus) do not differ significantly

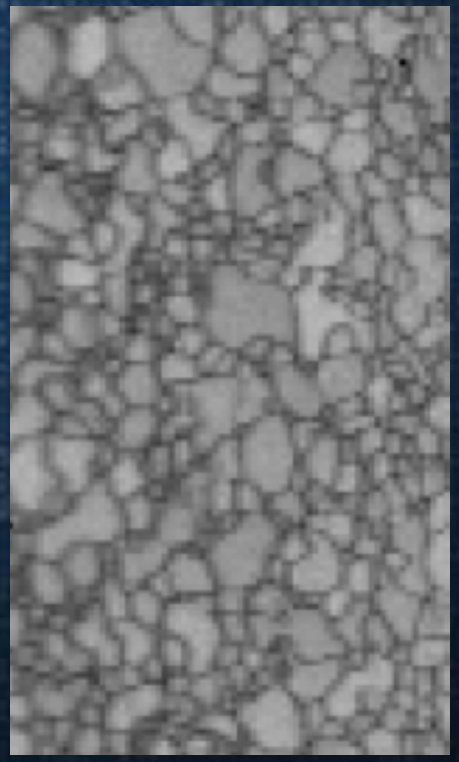


Device Probe Pad Microstructure Comparison

Device A	Device B	Device C
Grain Size: 1.0x	Grain Size: 4.6x	Grain Size: 1.3x
%GB > 15°: 50.0x	%GB > 15°: 29.0x	%GB > 15°: 1.0x

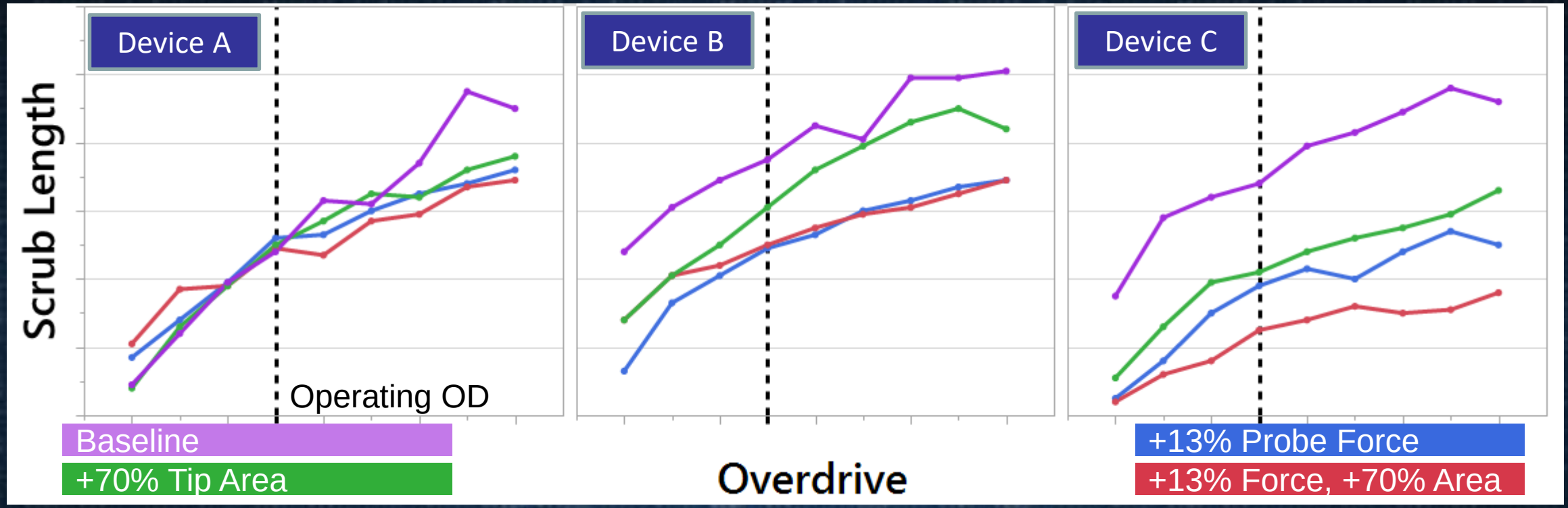






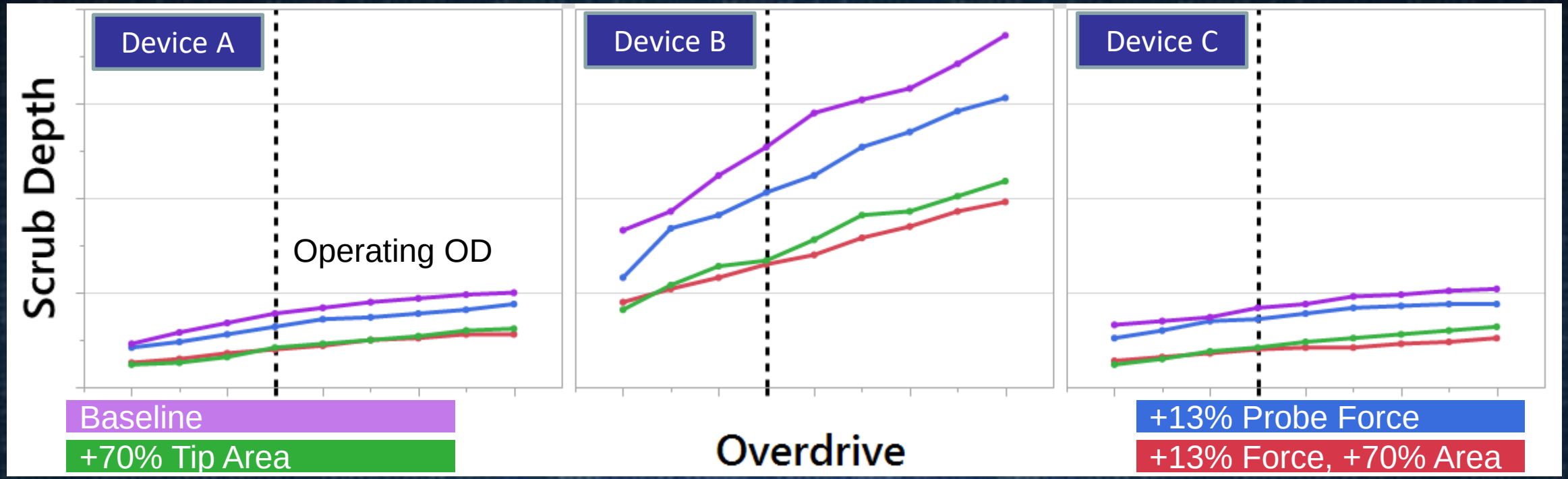
Results

Char Results – Scrub Length, Single Contact



- **Scrub Ratio characterization to determine AOT/POT is device-dependent**
- **Unpredictable effect on scrub length of changing tip characteristics**

Char Results – Scrub Depth, Single Contact

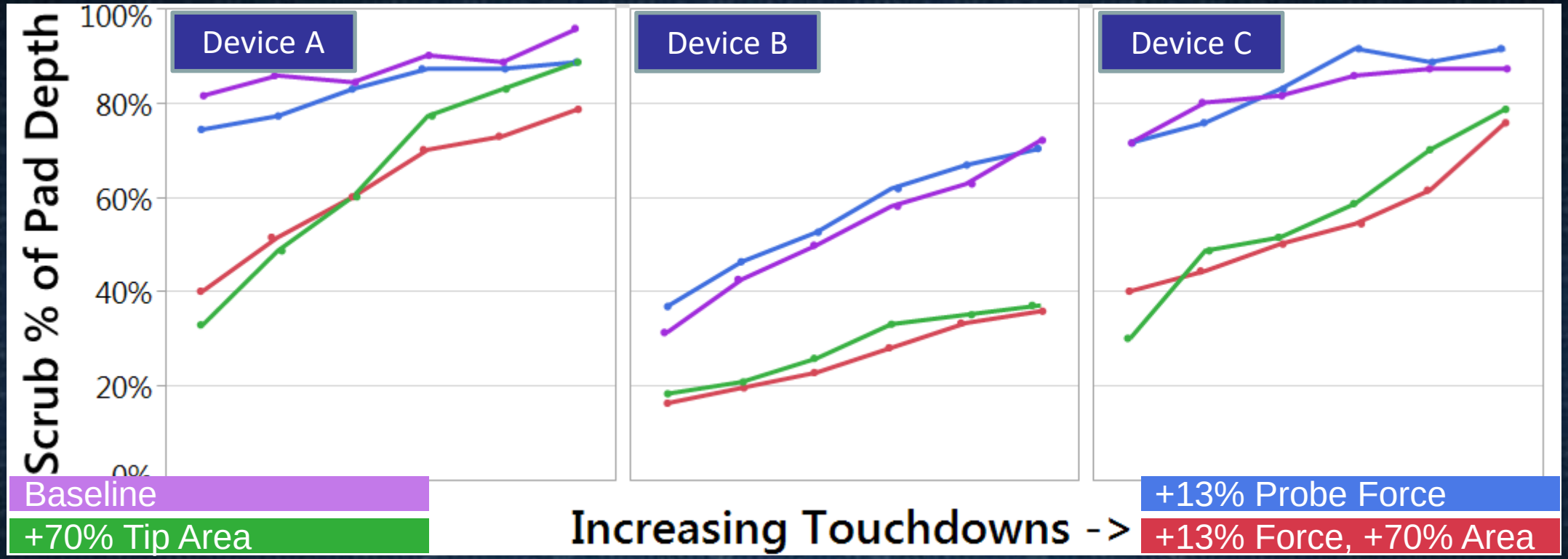


- Scrub depth response of a given probe tip varies by pad thickness
- Tip size is the dominant factor in determining scrub depth

Scrub Mark Images @ Operating Overdrive

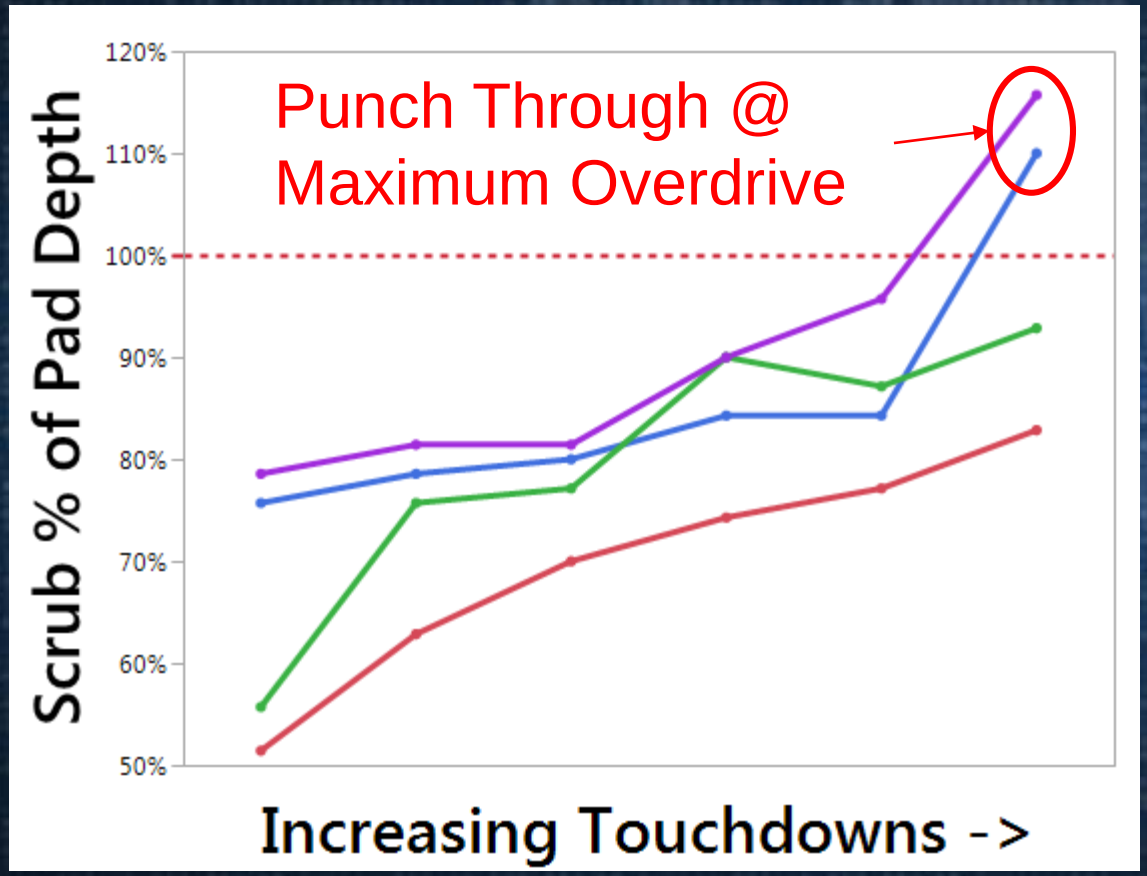
	Baseline	+70% Tip Area	+13% Force	+13% F, +70% A
Device A				
Device B “The Bulldozer” 				
Device C				

Char Results – Punch Through, Multiple Contacts



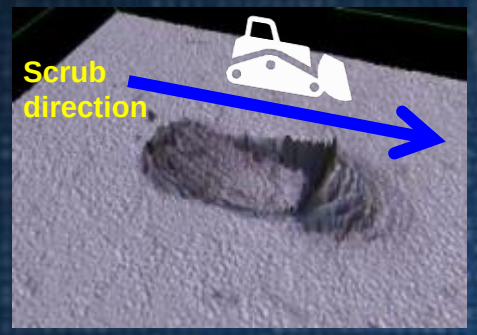
- Scrub depth approaches a limit at ~80-90% of pad depth
- Force characteristic has little to no impact on scrub depth.

Punch Through Observed on Device A

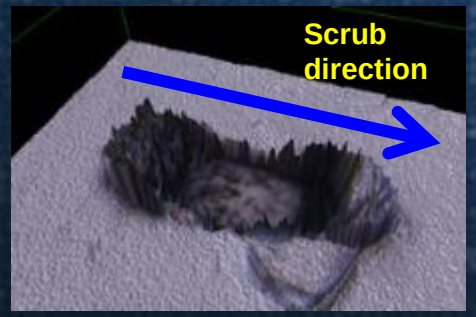


Scrub Depth Images – MJC Confocal Scope

Device B, Baseline Probe Tip



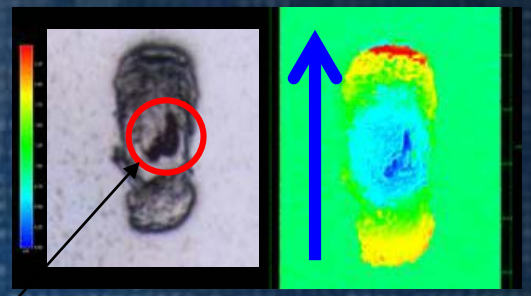
Single Contact



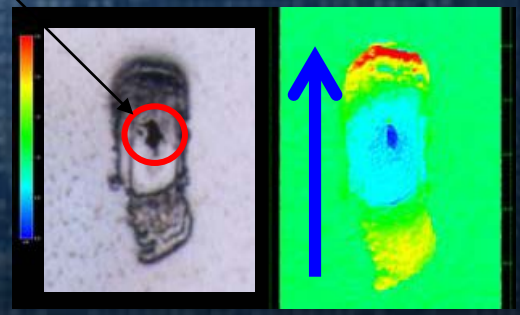
Multi-Contact

Punch Through

Device A, Baseline Probe Tip



Multi-Contact

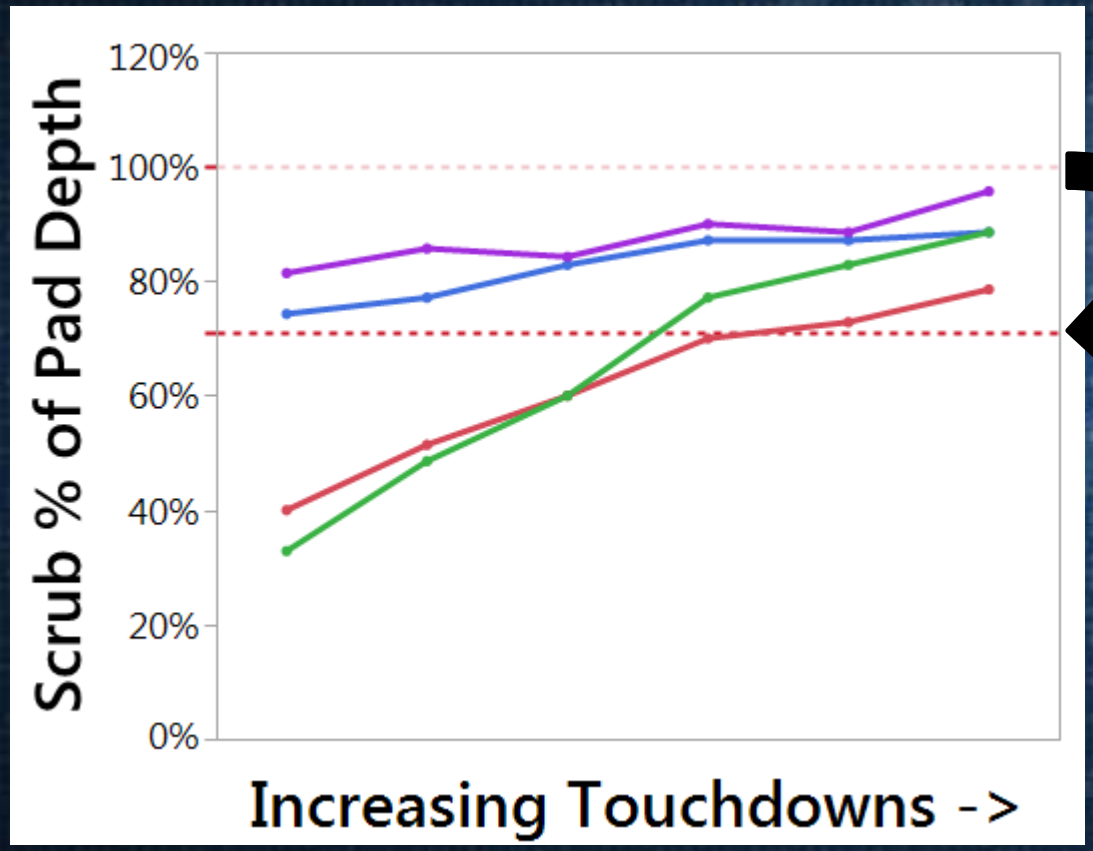


Multi-Contact +

Additional Considerations

What If…Pad Metal Becomes Thinner?

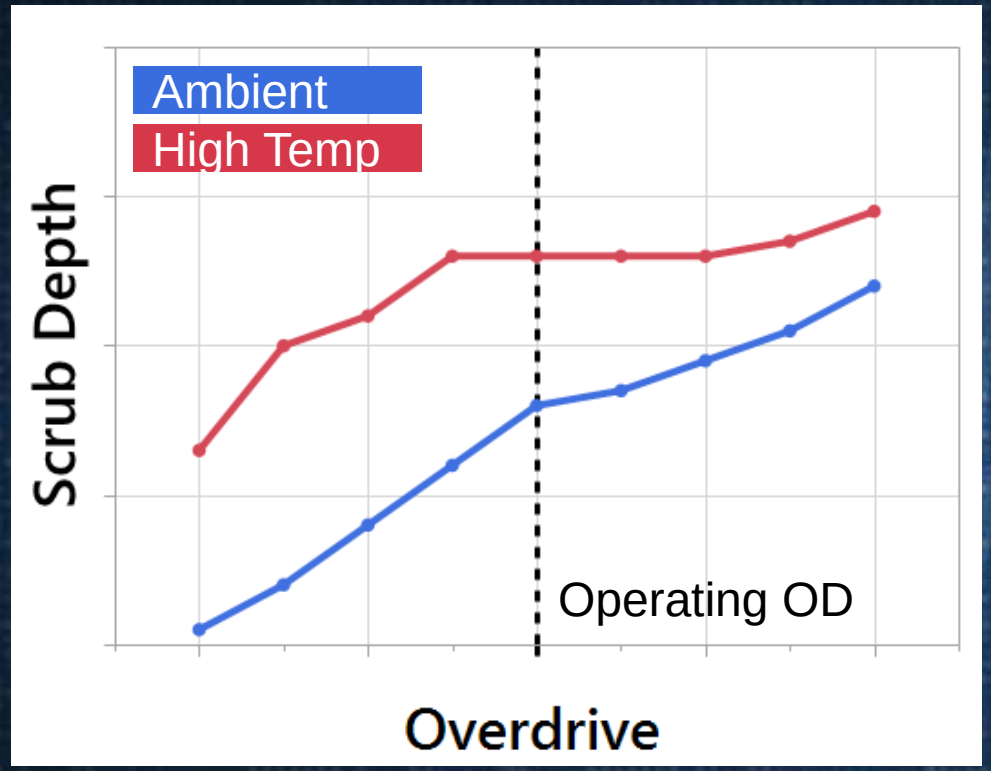
Device A @ Operating OD

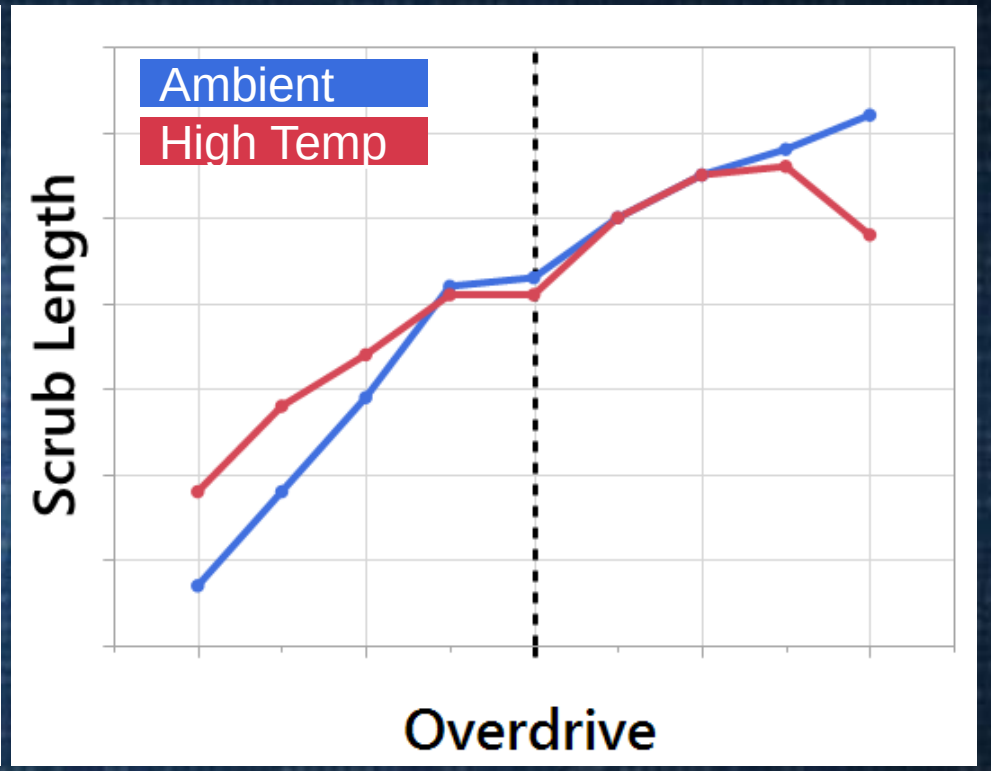


- **Potentially punch through on the first contact with small tips**
- **Large tips may not punch through (assuming pad hardening occurs); marginal at best**

What If…Testing Temperature Increases?

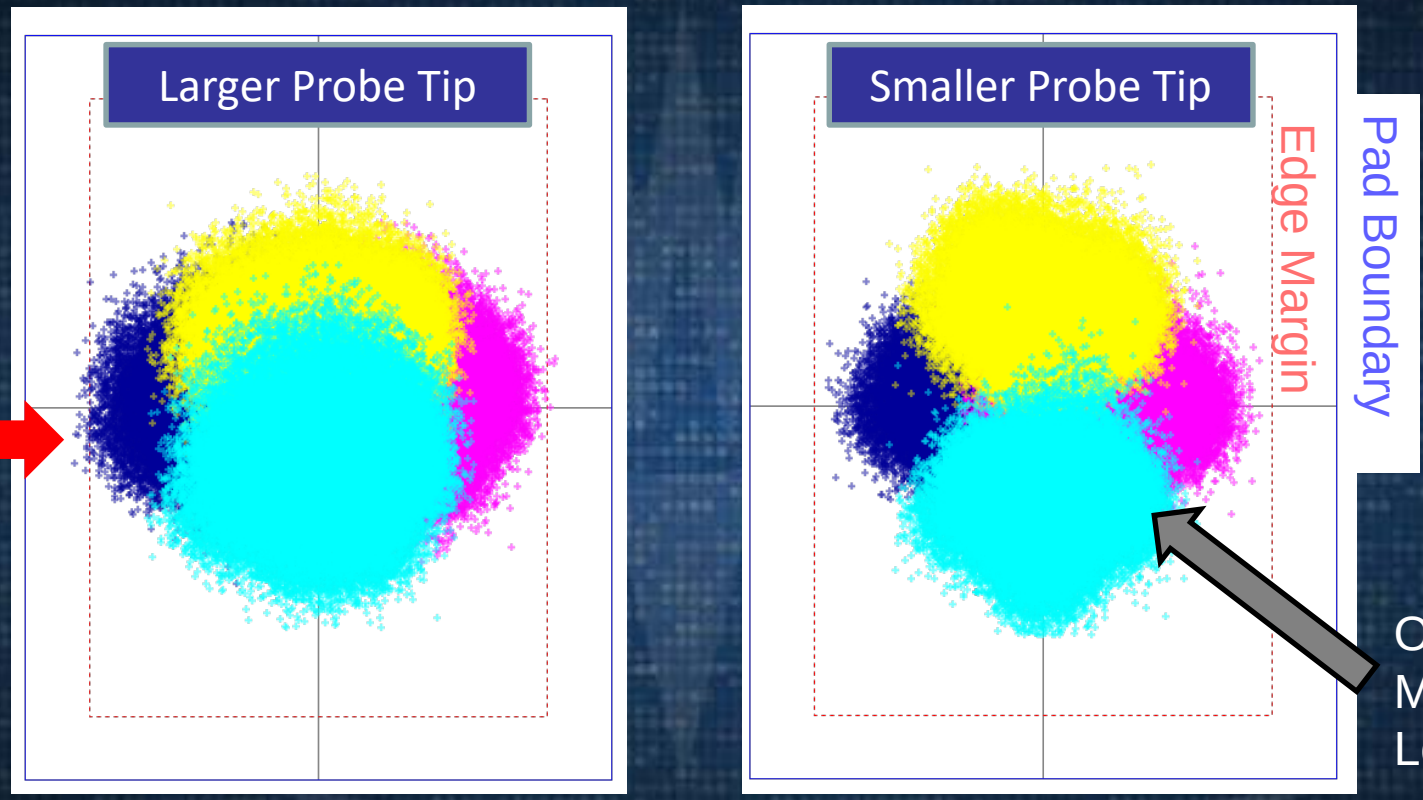
Device A, Probe Tip: +13% Force, Baseline Area





- **Scrub depth shows high temperature dependence; length does not**
- **Scrub depth rate of increase slows at high overdrive**

What If….Pad Size Shrinks?



- **Larger tip area = reduced scrub depth, but edge margin is strained**

Summary

Summary

- **Scrub characterization of probe types is critical to understanding advanced probing processes**
  - Depth and length can vary significantly across a breadth of similar devices

- **To meet the challenge of reduced pad dimensions, an array of probe tip offerings from probe card suppliers is necessary**
  - Varying tip area for optimized scrub depth
  - Varying tip size for optimized pad edge margin
  - The “right” balance of tip area vs. tip size

The Gap

- **Innovation Required:**
  - Can the probe card industry develop a one-size-fits-all probe tip for tomorrow's device requirements?
  - Or, can probe card suppliers cost-effectively produce an array of probes tailored for specific device properties?

Final Thoughts

- **Cooperative partnerships are critical in developing solutions for next-generation probing processes**
  - "Thank You" from Micron to MJC and MEC for partnering in this study

- **Acknowledgements**
  - Micron Technology: Kurt Guthzeit, Alistair Laing
  - MJC: Miho Kitayama, Yuma Tanaka
  - MEC: Dick Duncan

SW Test Workshop

Semiconductor Wafer Test Workshop

Probing solutions and inherent customization to enable advanced copper-based 3D integration schemes

Dong-pill Yang, SEC

Jung-woo Sung, SEC

Emanuele Bertarelli, Technoprobe

Raffaele Vallauri, Technoprobe

Dong-Hun Lee, Technoprobe Korea

Marco Prea, Technoprobe





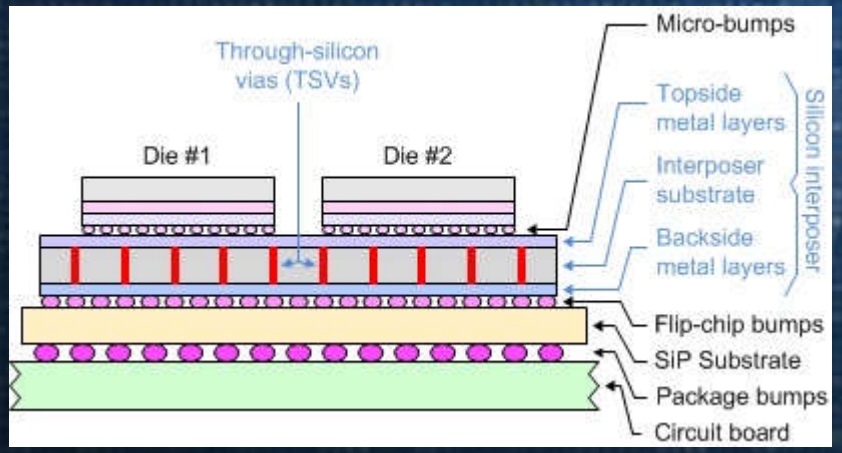
June 3-6, 2018

Overview

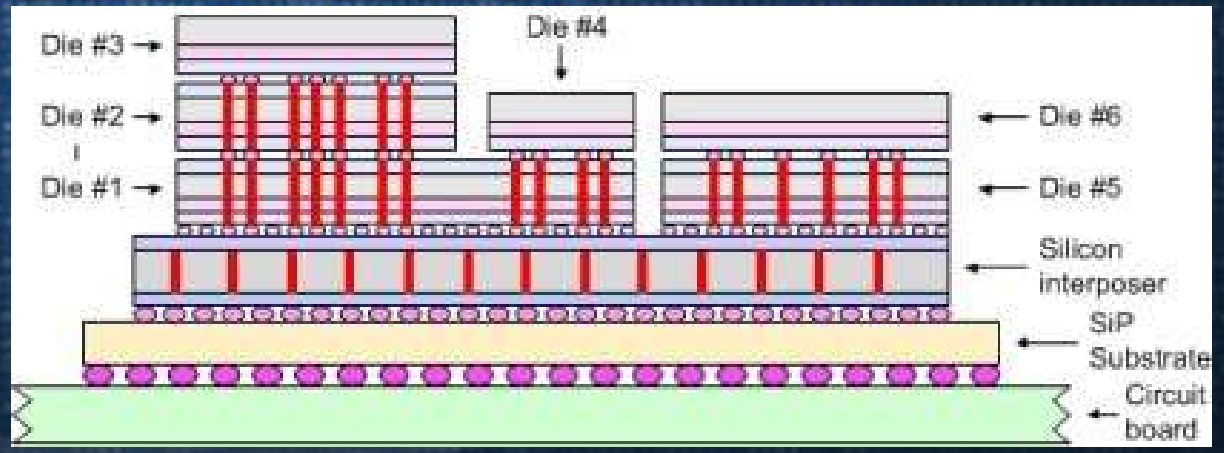
- **Background: Cu probing & Fan-Out Panel-Level Packaging (FOPLP) trends**
- **Probing technology path finding and know-how acquisition on Cu-based applications**
  1) Cu probing: early studies
  2) Processors probing
     - Customer A case study
     - Customer B case study
  3) Wide I/O memories probing
     - IMEC case study
- **Moving to FOPLP, RDL Cu pad probing: SEC case study**
  1) Technology customization
  2) Results of qualification at Customer
- **Lessons learned and future work**

Cu probing trend

- **A general trend can be identified in EWS towards Cu probing**
- **This is one of the key ingredients to allow semiconductor manufacturers to exploit 3D packing architectures with high interconnection density**
  - Main drivers are recent mobile processors and high performance memories



2.5D IC / System in Package using a Si interposer and through-silicon vias (TSVs)



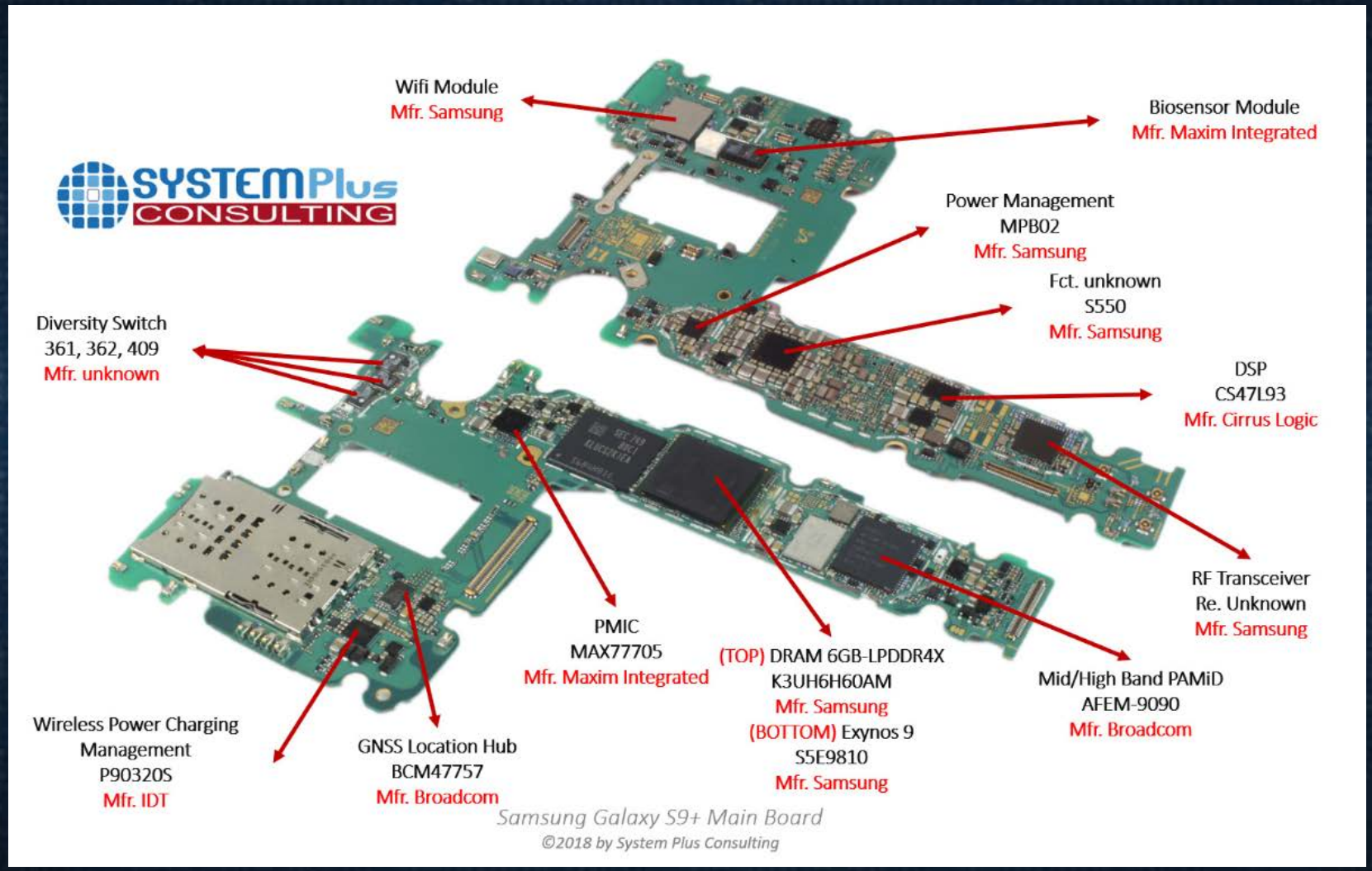
3D IC / System in Package example:
Memory dies stacked and attached to logic die and/or analog/RF die attached to a digital logic die, …

Ref. [1]

3D IC benefits versus 2D IC

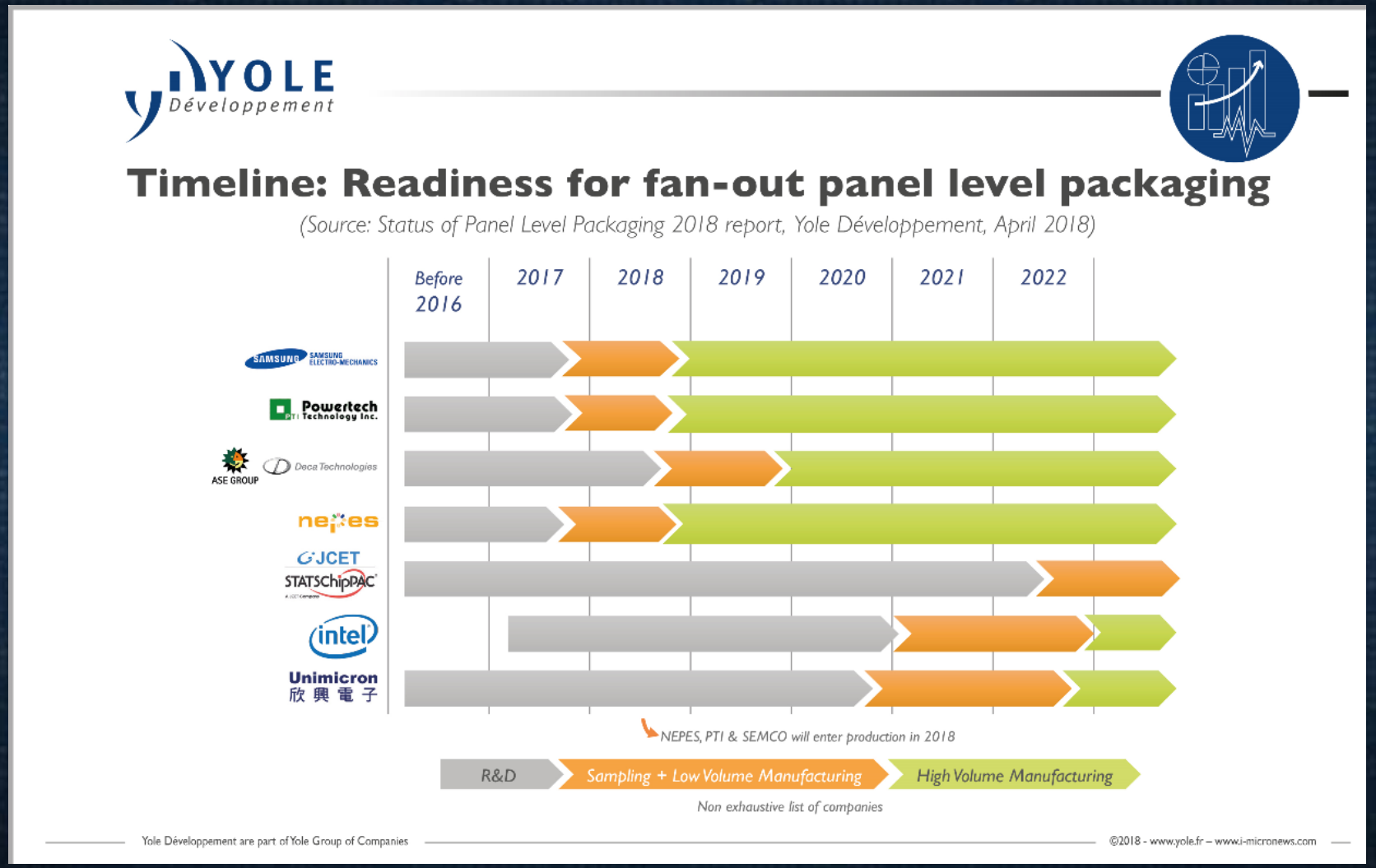
- **Smaller footprint**
  - More functionalities into a small space
- **Shorter interconnect length**
  - Decrease power consumption and power budget
  - Increase bandwidth = high bandwidth memories, parallel access
- **Design freedom**
  - Higher order of connectivity vs. 2D architecture
  - Heterogeneous components can be integrated
- **Cost improvements**
  - Partitioning of large chips into smaller dies for improved yield and testability

Packaging trend in mobile applications



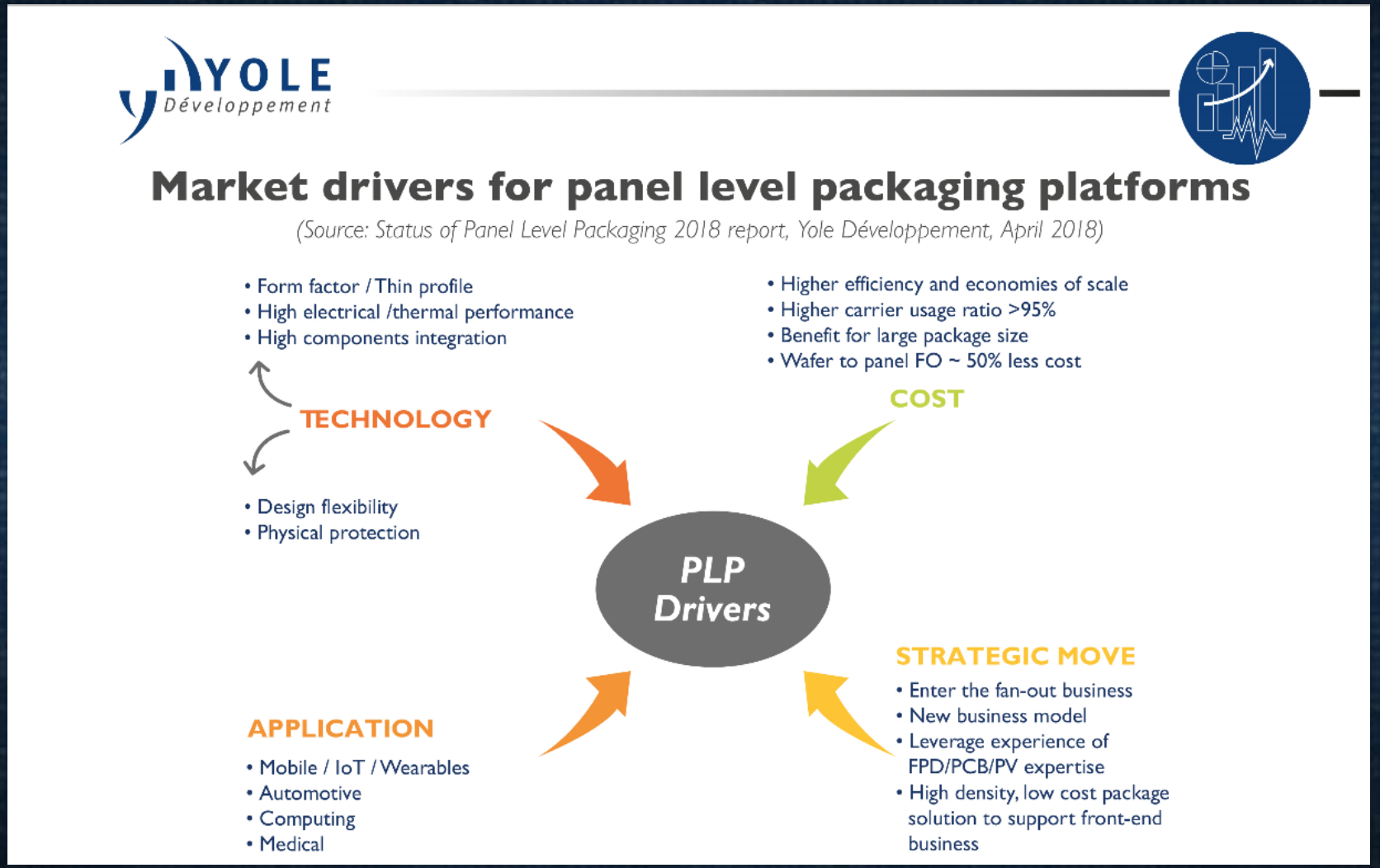
Ref. [2]

Readiness for fan-out panel level packaging



Ref. [3]

Panel level packaging technology drivers

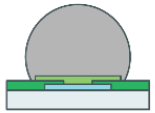
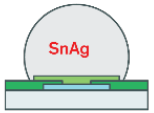
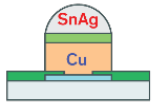
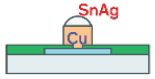


Ref. [3]

Cu-based interconnects

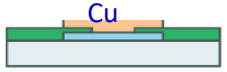
- Reducing solder amounts (finally to zero), Cu-based bumped interconnects gain lower pitch capability and higher current carrying capability
- Cu pad is an interesting option for RDL layer testing

Bumping technology generations:

	SnPb C4 Bump	Pb-Free C4 Bump	Cu Pillar + Pb-free Cap	Cu µ-Pillar + Pb-free Cap
Structure				
Diameter	75 – 200 µm	75 – 150 µm	50 – 100 µm	10 – 30 µm

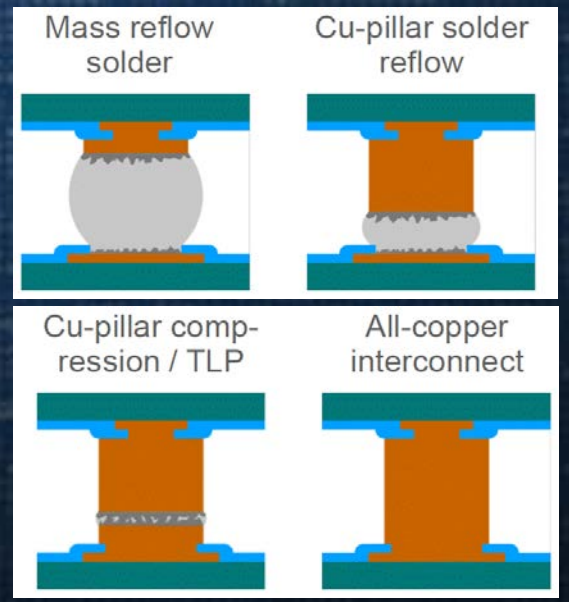
Old Technology → Current Technology → Next-Generation Technology

Pad option:

Cu Pad

50 – 100 µm

Ref. [4]

Roadmap from solder to all-copper interconnects:



Ref. [5]

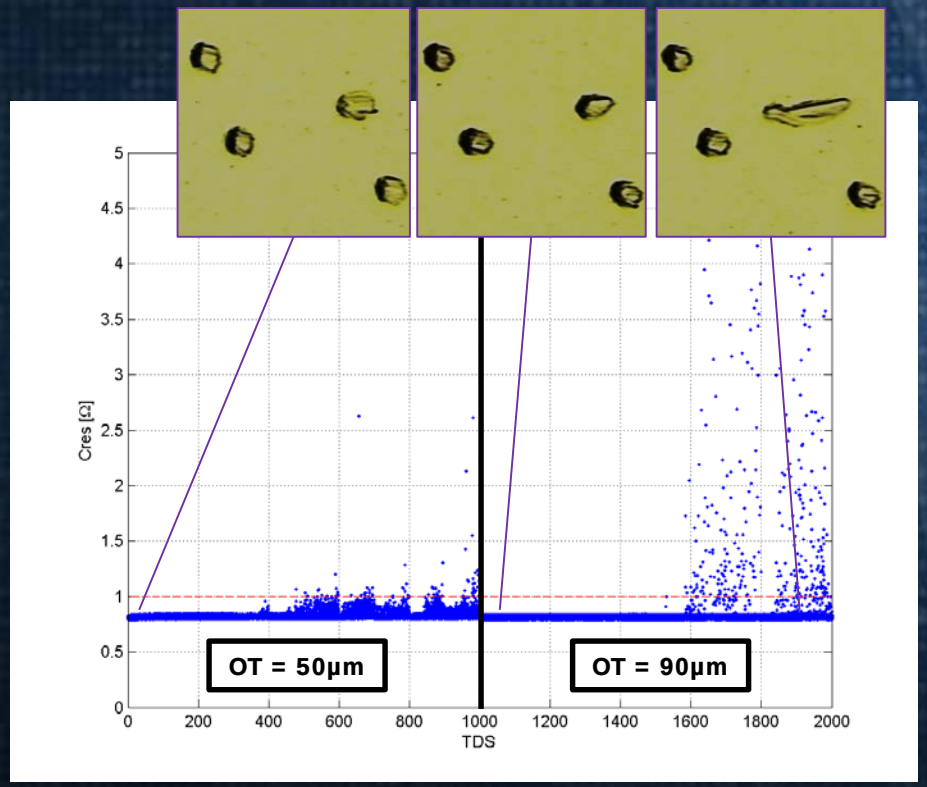
Probing technology requirements

- **Processors probing requires…**
  - High current carrying capability
  - Probing at both RT and Hot
  - Minimum pitch is not critical (≥ 90 µm FA)

- **Wide I/O memories probing requires…**
  - Ultra fine pitch (≤ 50 µm FA)
  - Current carrying capability is not critical

Early studies

- From the beginning, explorative studies on Cu blank wafers showed the importance of tip material and scrub control to guarantee contact stability

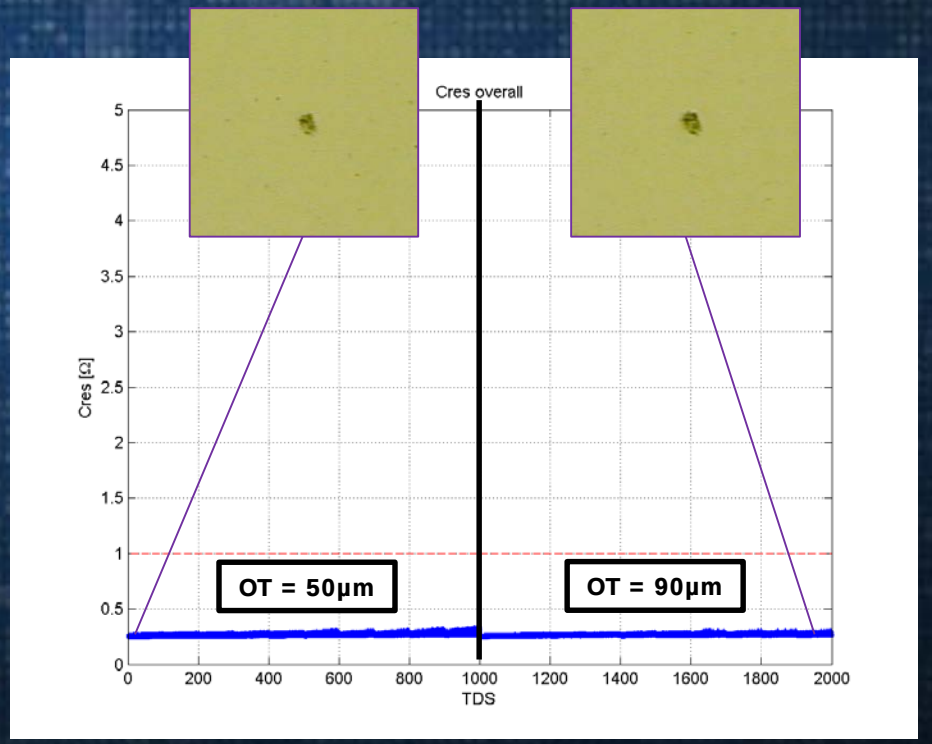


TPEG™
T3 LCR2

Standard mechanics

Pointed tip
LCR2 alloy

Cleaning Frequency = 100



Arianna™
A3 HC

Improved mechanics

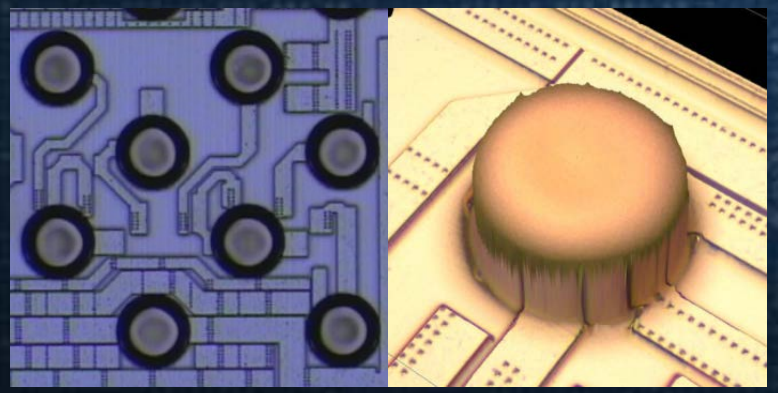
Pointed tip
Customized alloy

Cleaning Frequency = 100

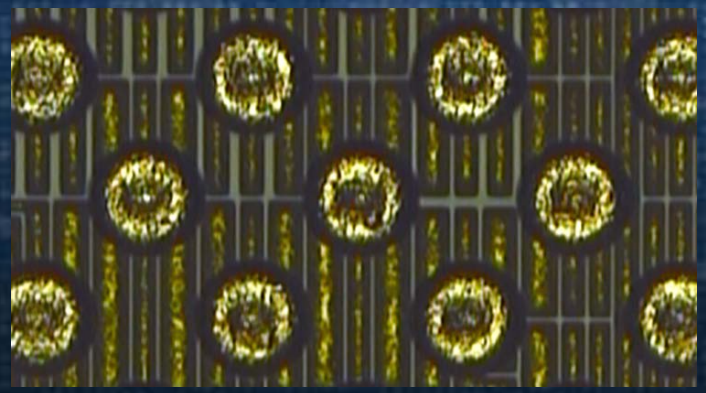
Early studies

- **Looking at Cu surface:**
  - Surface morphology and metallurgy differ largely from Customer to Customer, requiring dedicated customization studies
  - Cu surface (pads, pillars) are more prone to oxidation – or at least the oxide layer is impacting more contact resistance – than Al surface (pads)

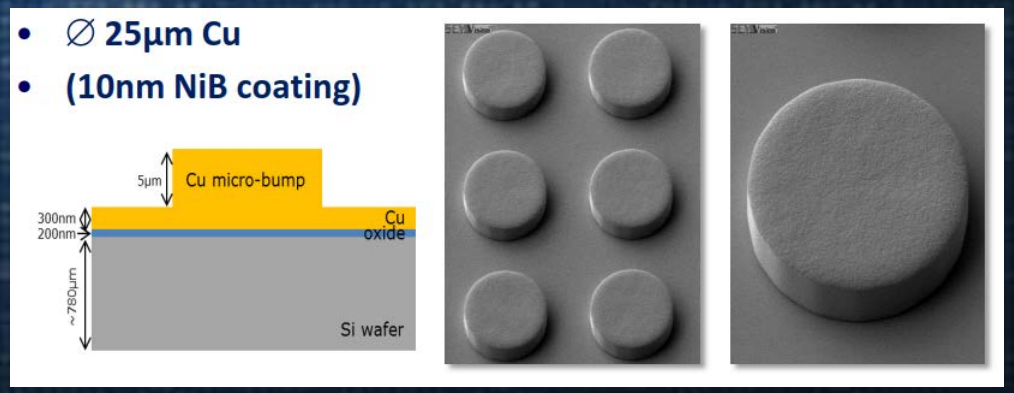
Customer A



Customer B



Customer IMEC (see paper)



Refs. [6,7]

Processor probing

- **Technology development through**
  - Probing technology path finding
  - Customer A case study
  - Customer B case study

Processor probing

Probing technology development

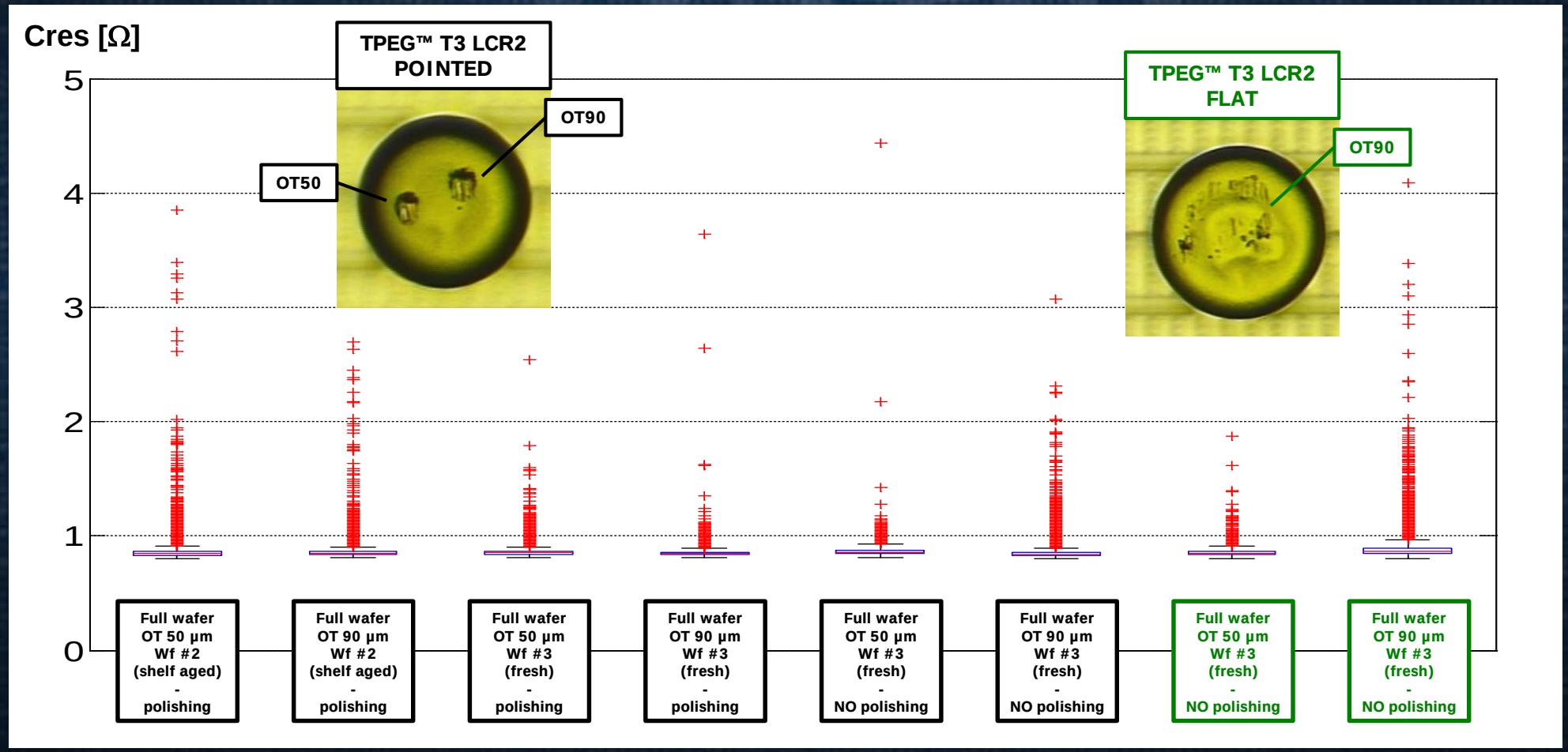
- **TP reference technology is TPEG™ T3 LCR2**
- **Arianna™ A3 HC & Arianna™ AS90 HC are proposed for this application to**
  - Improve contact resistance stability
  - Improve current carrying capability

PARAMETER	TPEG™ T3 LCR2	Arianna™ A3 HC	Arianna™ AS90 HC
Needle diameter	2 mils equivalent	2 mils equivalent	2.4 mils equivalent
X/Y Alignment	±10 µm	±10 µm	±10 µm
Z planarity	Δ 20 µm	Δ 20 µm	Δ 20 µm
Min pitch FA	90 µm	90 µm	90 µm
CCC	500mA	1200 mA	1500 mA

Processor probing

Customer A case study

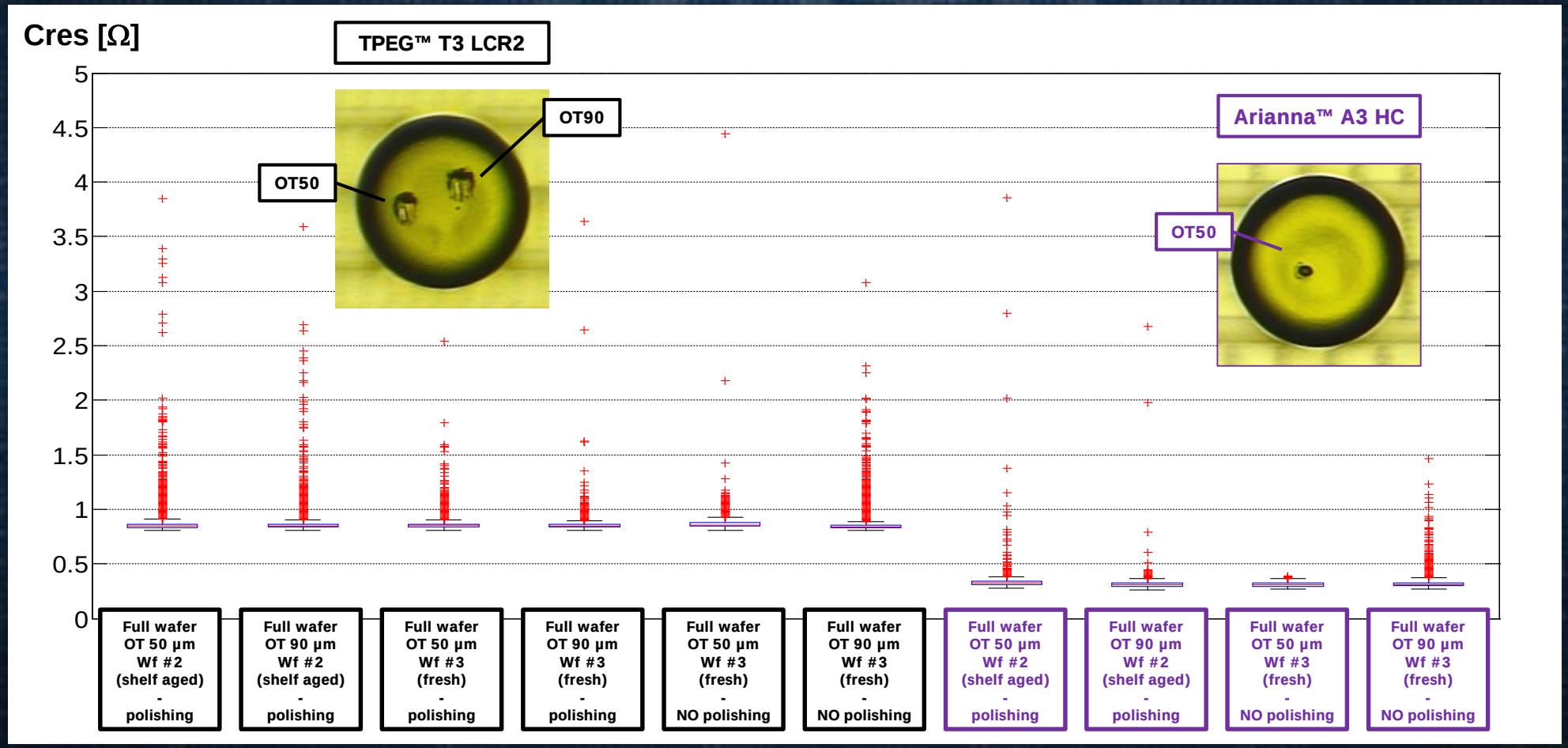
- **TPEG™ T3 LCR2: comparing pointed vs flat tip**



Processor probing

Customer A case study

- **Moving to Customized Tip solution: TPEG™ T3 LCR2 vs Arianna™ A3 HC**



Processor probing

Customer B case study – 1st run

- **Customer required to emulate Cu bump wafer testing as follow:**
  - 3x full wafers with polishing frequency 100, OD = 75µm electrical
  - 4x full wafers no polishing (tot. 1800 PTDs), OD = 75µm electrical
  - Success criterion: maximum Cres Probe Std Dev < 250 mΩ

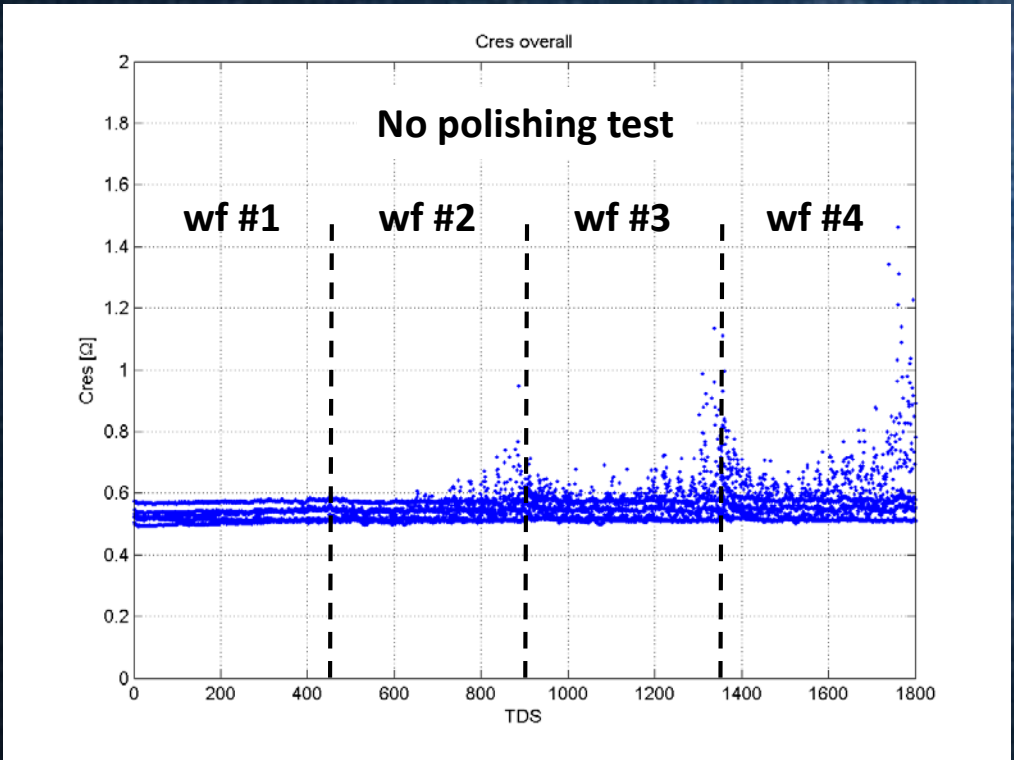
Technology	Tip Option	Scrub Option	Probe count	Max Probe SD polishing	Max Probe SD NO polishing
TPEG™ T3 LCR2	Pointed	Controlled	48	13 mΩ	13 mΩ
TPEG™ T3 LCR2	Flat	Controlled	48	4 mΩ	19 mΩ
Arianna™ A3 HC	Customized	Controlled	48	8 mΩ	6 mΩ
Arianna™ A3 HC	Customized	Standard	48	20 mΩ	87 mΩ

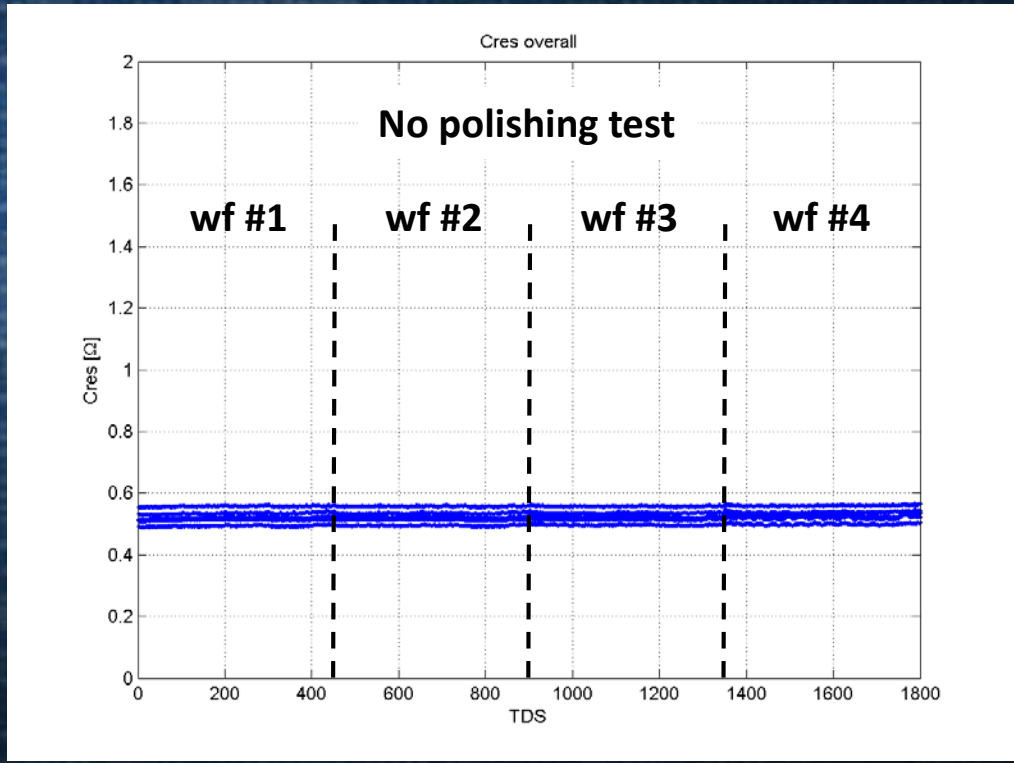
- **Stable electrical contact stability is found for all technologies**
  - Superior performances are confirmed for TP Customized Tip solution with controlled scrub
  - Controlled scrub mechanics is providing a measurable advantage

Processor probing

Customer B case study – 1st run

- **Arianna™ A3 HC, standard scrub**
  - Max Probe SD = 87 mΩ
  - Slight, progressive contact instability
- **Arianna™ A3 HC, controlled scrub**
  - Max Probe SD = 6 mΩ
  - Contact stability maintained



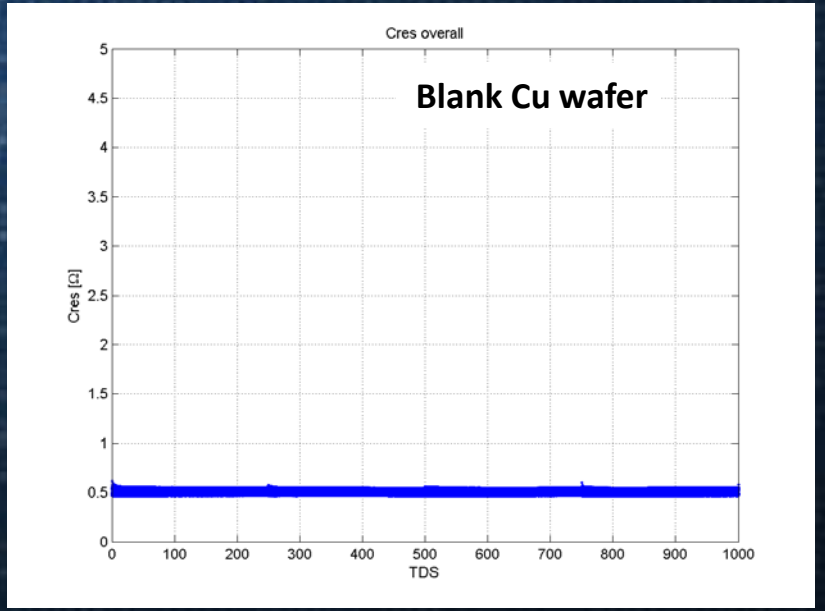


Processor probing

Customer B case study – 2nd run

- **Based on positive results with Arianna™ A3 HC technology, the Customer required to**
  - Further improve current carrying capability
  - Assess stability of electrical performances over entire life span → new evaluation procedure
  - Improve HF performances

- **Technoprobe proposed to move to Arianna™ AS90 HC**
  - Customized tip evaluated on Cu blank, showing high Cres stability
    - Cres ~ 0.5 Ω (including interconnection)
    - Maximum Cres Probe Std Dev = 5 mΩ
    - Total standard deviation (on 48 probes) = 27 mΩ
  - Dedicated tip designs to probe on Customer wafer are developed: Geometry 1 & Geometry 2

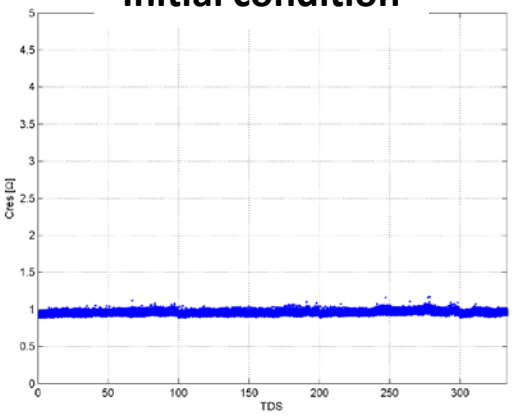
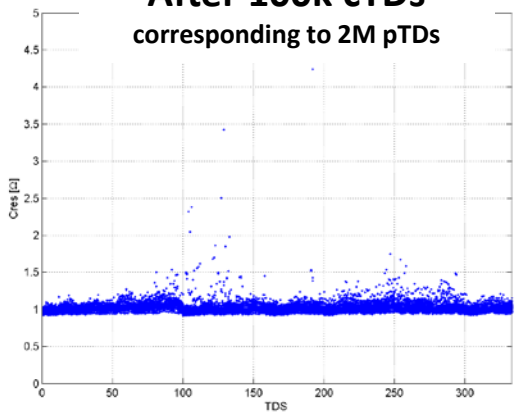
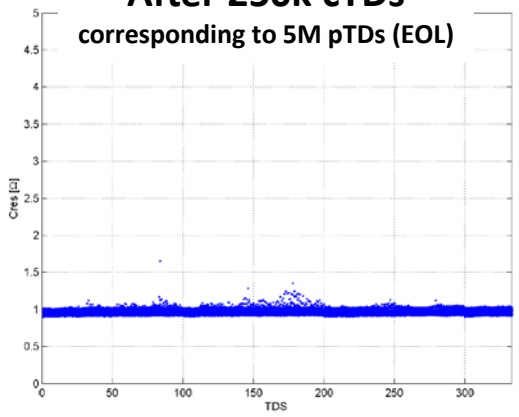
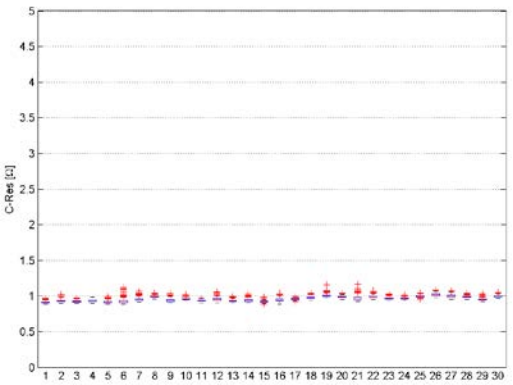
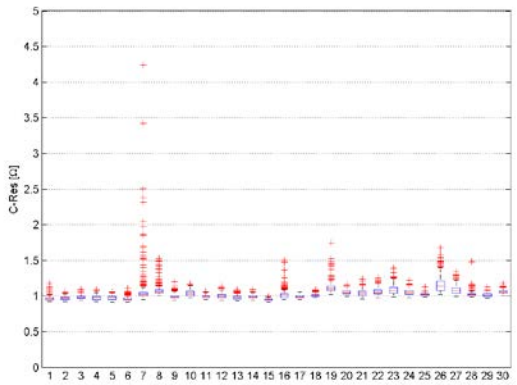
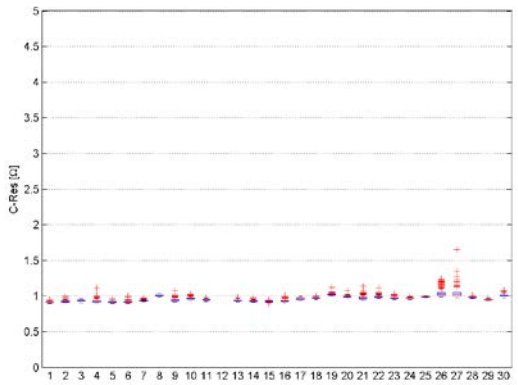


Overall Cres (1000 TDs, cleaning freq 100)

Processor probing

Customer B case study – 2nd run

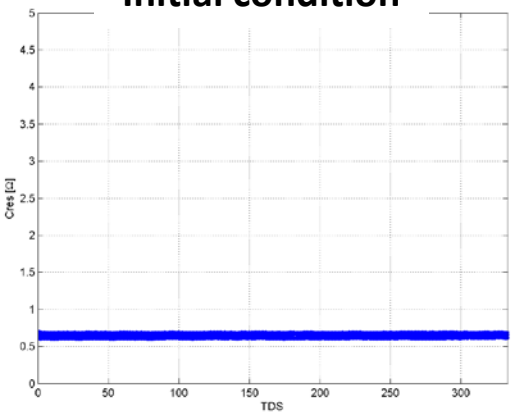
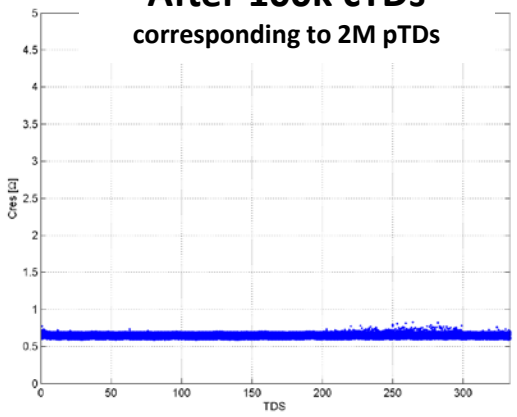
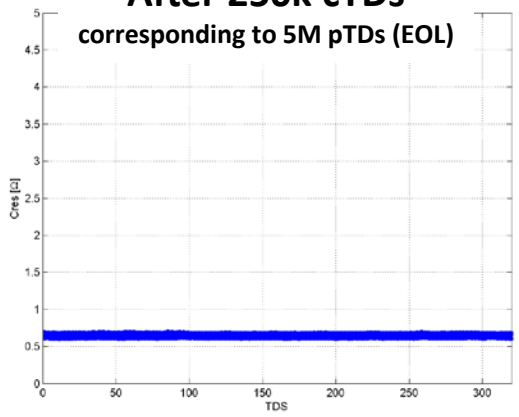
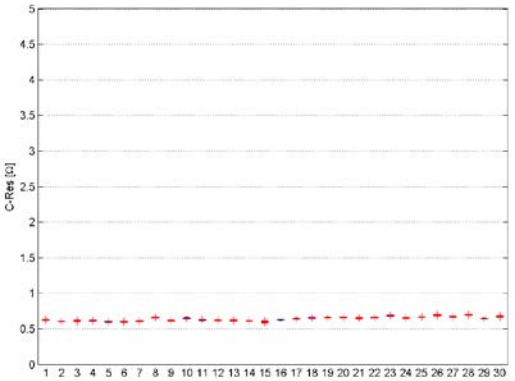
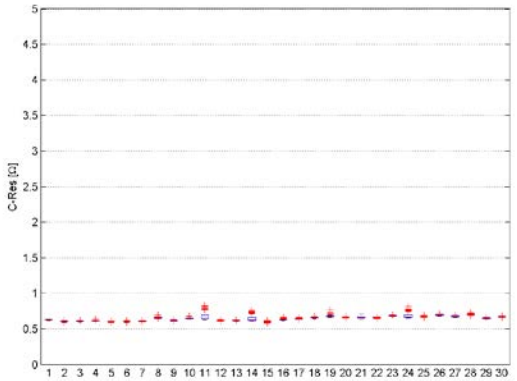
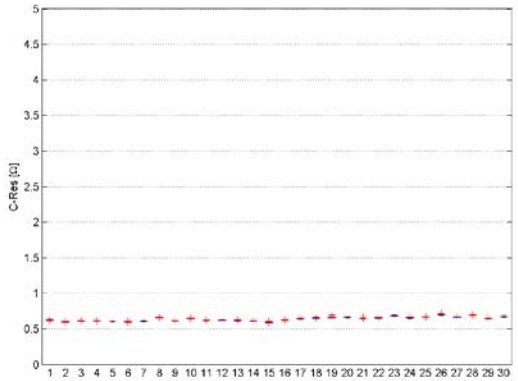
- **Arianna™ AS90 HC with Geometry 1 – cleaning ageing test**

	Initial condition	After 100k cTDs corresponding to 2M pTDs	After 250k cTDs corresponding to 5M pTDs (EOL)
Overall Cres (full wafer, cln freq 100)			
Single channel Cres boxplot (full wafer, cln freq 100)			

Processor probing

Customer B case study – 2nd run

- **Arianna™ AS90 HC with Geometry 2 – cleaning ageing test**

	Initial condition	After 100k cTDs corresponding to 2M pTDs	After 250k cTDs corresponding to 5M pTDs (EOL)
Overall Cres (full wafer, cln freq 100)			
Single channel Cres boxplot (full wafer, cln freq 100)			

Wide I/O memories probing

- **Technology development through**
  - Probing technology path finding
  - IMEC case study (ref.[8] dedicated paper at SWTW 2018 presented by IMEC "Leading-Edge Wide-I/O2 Memory Probing Challenges: TPEG™ MEMS Solution")

Wide I/O memories probing

Probing technology path finding

- **TSV/µ-bump memory dies probing needs ultra-fine pitch FA technologies**
  - TP first solution to address 40µm FA is dated 2010 to provide an engineering level solution (FT 1.0, mechanical manufacturing)
  - As further step, TP applied TPEG™ MEMS concept also to ultra-fine pitch

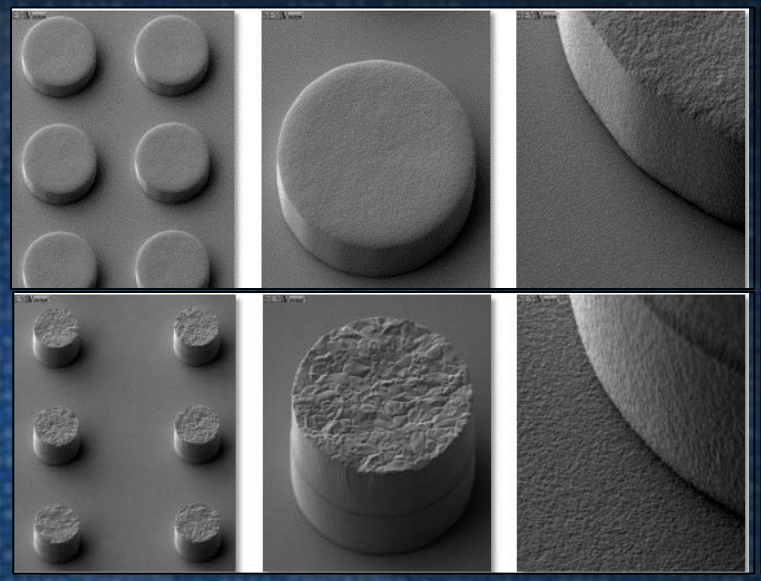
- **TPEG™ MEMS Tx0 probe family was developed**
  - Target application is 60-50-40µm FA probing over Al pads or µ-bumps

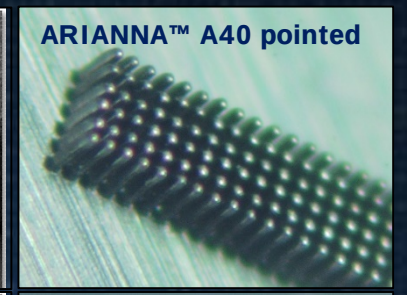
- **Now the respective Arianna™ Ax0 solutions are being introduced**
  - Target application is 60-50-40µm FA probing over Cu pads or µ-pillars

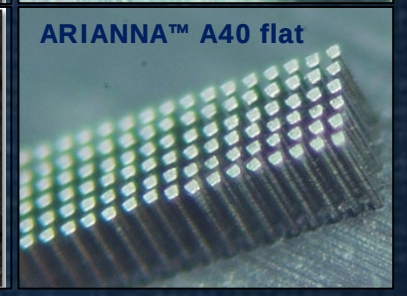
Wide I/O memories probing

Customer IMEC case study

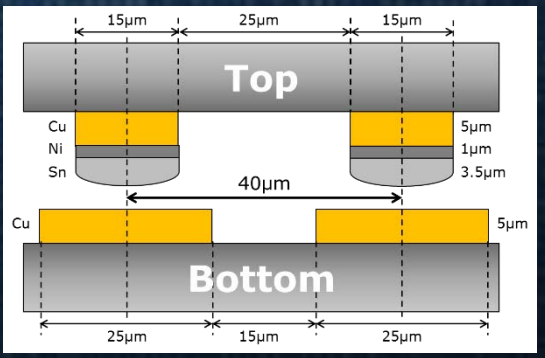
- **IMEC Blanket Micro-Bump wafer**
  - JEDEC Wide I/O 2 (JESD-229/2)
  - Top side: Cu/Ni/Sn ∅ = 15µm
  - Bottom side: Cu (+NiB) ∅ = 25µm
  - Micro-bumps shorted by blanket Cu







- **TP probe card**
  - 73 x 6 probes at 40µm pitch FA
  - Micro-wired space transformer
  - Arianna™ A40 flat probe head for Top side
  - Arianna™ A40 pointed probe head for Bottom side



See Refs. [6,7,9] for details.

SEC case study

Moving to FOPLP, RDL Cu pad probing

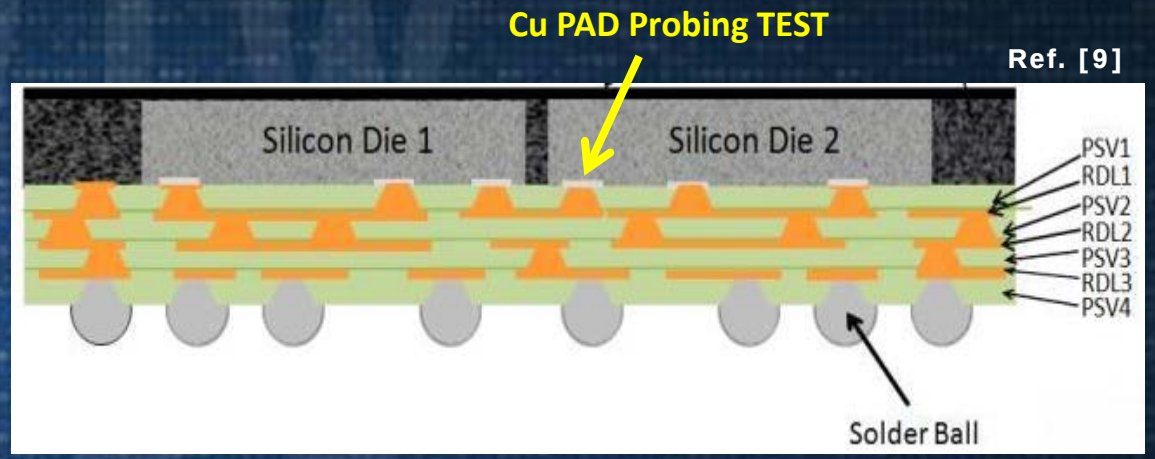
- **All path finding and know-how acquisition efforts allowed Technoprobe to conceive a solution to cope with requirements of FOPLP, Cu pad probing**

- **Specific SEC challenges and requirements drove us to develop a probing technology capable of:**
  - Small pad opening
  - Thin Cu metallization layer
  - Possible irregular pad topography

SEC case study

Technoprobe Technology customization

- **Requirement from SEC is to probe on Cu pads on RDL**
- **Main targets for evaluation:**
  - Same or better electrical contact performances vs. Al pad reference
  - Minimal pad damage to allow safe multiple testing (RT, Cold, Hot)

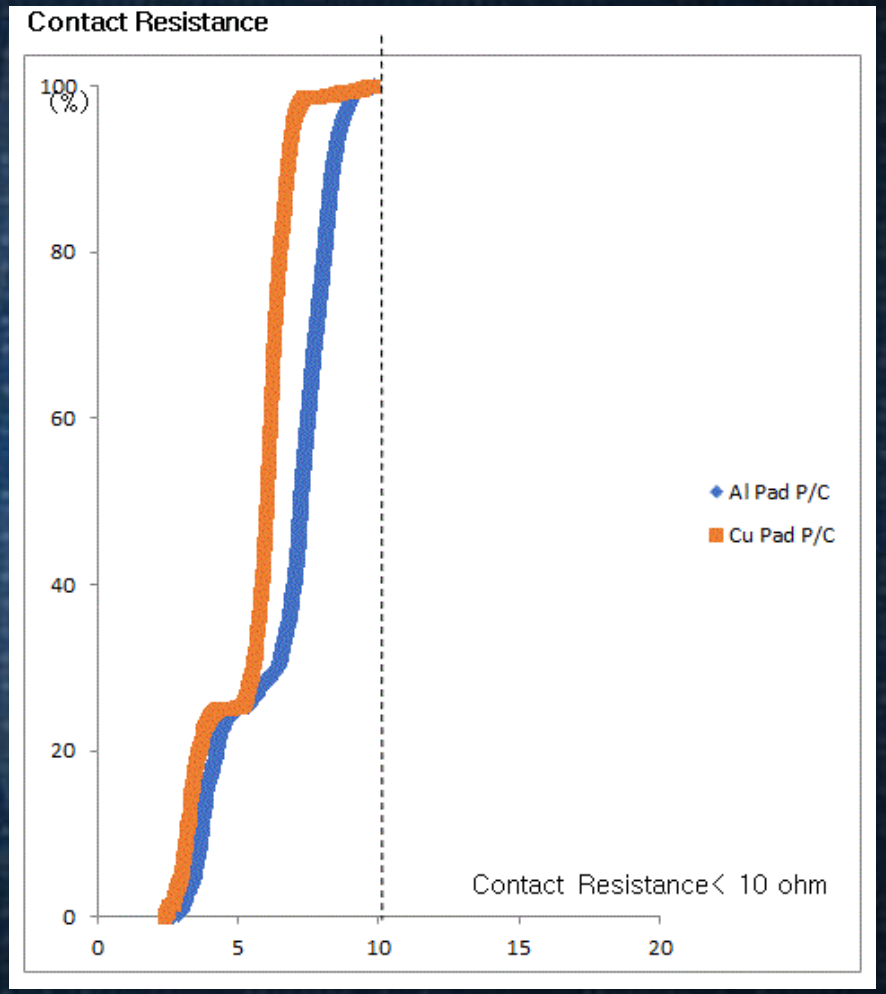


- **Arianna™ AS90 technology with further customized tip geometry and material is selected**
  - Tip Geometry 3 is selected
  - A novel alloy “Type 2” is specifically developed for this application

SEC case study

Results of qualification at Customer

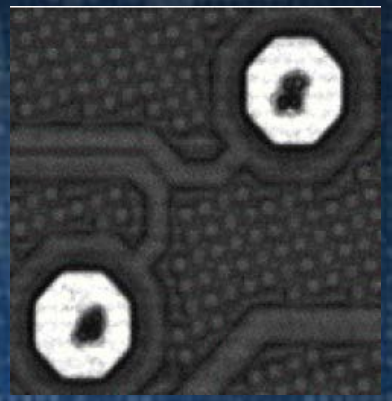
- **Stable Cres is found**
  - Results reported are for full wafer trial run
- **Probing electrical performances are exceeding Al Pad benchmark in terms of**
  - LVCC Margin test
  - DC test
  - DFT(Scan) test
  - Function test
  - Analog test



SEC case study

Results of qualification at Customer

- **Cu pad damage is very limited**
  - Scrub depth is not exceeding 300 nm
  - No delamination issues found



Al pad



Cu pad

- **Based on wear out data from the field, expected lifetime with current cleaning recipe is exceeding 1M probing TDs for RT testing**

SEC case study

Results of qualification at Customer

- **Arianna™ AS90 technology has been qualified by SEC for RT & HT testing and released to mass production**
  - Stable Cres is found with requested scrub mark depth and size
  - This result is achieved by a dedicated customization of probe tip (alloy and geometry)

Lessons learned

- **Cu probing on diverse target structures (pads, pillars, µ-pillars) is gaining momentum driven by processors and high performance memories testing requirements in the evolving 3D packing architectures scenario**

- **Key ingredients implemented by Technoprobe to successfully probe on different Cu structures are**
  - Tip : customized geometry and alloys
  - Scrub control to guarantee contact stability during probing process
  - … and a joint development path between probe card vendors and customers, allowing Technoprobe to verify and further customize probing solution for unprecedented electrical and mechanical performances

Thank you for your attention!

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The work done by technical team members at Technoprobe R&D & Process Engineering Department is gratefully acknowledged.

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[1] M. Maxfield, 2D vs. 2.5D vs. 3D ICs 101 – EE Times Website

[2] System Plus Consulting Website (http://www.systemplus.fr/)

[3] Yole Développement Website (http://www.yole.fr/2014-galery-3D.aspx#I0002f5d1)

[4] M. Lapedus, *Electroplating IC Packages* – Semiconductor Engineering Website

[5] L. Del Carro et al., *Functional electronic packaging* – IBM Research Zurich Website

[6] R. Vallauri et al., *Challenges probing next generation full array products with 60 µm pitch and below* – Proceedings of SWTW2015 (S01_03)

[7] R. Vallauri et al., *Ultra-Fine Pitch Probing Challenges and Solutions* – 1st IEEE European Test Symposium (2016)

[8] F. Fodor et al., *Leading-Edge Wide-I/O2 Memory Probing Challenges: TPEG™ MEMS Solution* – Proceedings of SWTW2018 (S02_03)

[9] W.K. Choi et al., *Ultra-Fine Pitch RDL Development in Multi-layer eWLB (embedded Wafer Level BGA) Packages* - IMAPS 2015 Orlando



SW Test Workshop

Semiconductor Wafer Test Workshop

LEADING-EDGE WIDE-I/O2 MEMORY PROBING CHALLENGES: TPEG™ MEMS SOLUTION

Ferenc Fodor

Erik Jan Marinissen

imec

Leuven, Belgium

Raffaele Vallauri

Daniele Acconcia

TECHNOPROBE

Wafer Probing Technologies

Cernusco Lombardone, Italy

June 3-6, 2018

1. INTRODUCTION
MOTIVATION

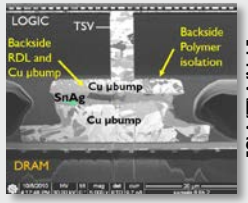
- Unique test system at imec for direct probing of fine-pitch large micro-bumps arrays
  - Advanced probe card characterization
  - Regular pre-/post-bond probing of wafers with micro-bumps
- Four-phase evaluation of Technoprobe probe cards:
  - Phase 1 : Wide-I/O2 **1bank** probe card with TPEG™ T40 tips
  - Phase 2 : Wide-I/O2 **1bank** probe card with ARIANNA™ A40 tips

  Same card
  Different probe heads
  - Phase 3 : Wide-I/O2 **4bank** probe card with TPEG™ T40 tips
  - Phase 4 : Wide-I/O2 **4bank** probe card with ARIANNA™ A40 tips

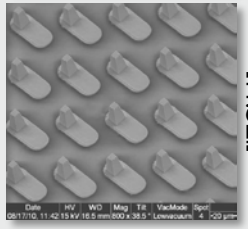
  Same card
  Different probe heads
- Completed so far: phases 1 and 2

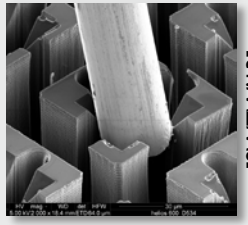
1. INTRODUCTION
RELATED PRIOR WORK

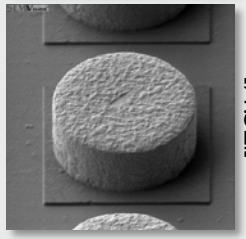
- **SWTW'11**: Marinissen et al. *(imec + Cascade Microtech)*
  - Imec and Cascade started collaboration, defined probe targets
- **ITC'11**: Smith et al. *(Cascade Microtech + imec)*
  - First collaboration results, mainly on probe technology
- **SWTW'13**: Böhm et al. *(Feinmetall + Team Nanotec + imec + FH + CM)*
  - Silicon crown tips, embedded in vertical probe card with TSVs
- **ITC'14**: Marinissen et al. *(imec + Cascade Microtech + TU Delft)*
  - WIO1-1Bank: good R_C; no impact on bond yield; cost-effective
  - But... (i) only 1 Bank and (ii) only daisy-chains of 30 micro-bumps
- **SWTW'17**: Marinissen et al. (*imec + Cascade Microtech*)
- **ITC-Asia'17**: Marinissen et al. (*imec + Cascade Microtech GmbH + FormFactor*)
  - Fully automatic test system for advanced probe card characterization



[SWTW'11]


[ITC'11]


[SWTW'13]


[ITC'14]

OUTLINE

1. Introduction
2. Test Infrastructure
3. imec Test Chips with Micro-Bumps
4. Design of Experiments
5. Probing on Sn Micro-Bumps
6. Probing on Cu Micro-Bumps
7. Conclusion

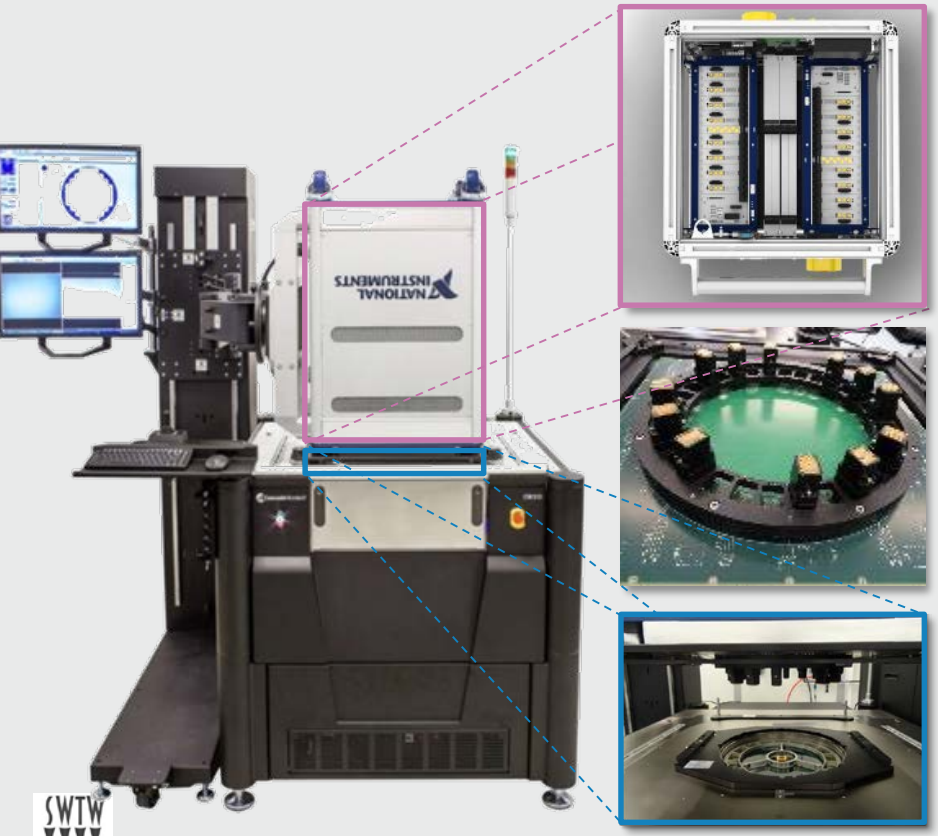
2. TEST INFRASTRUCTURE

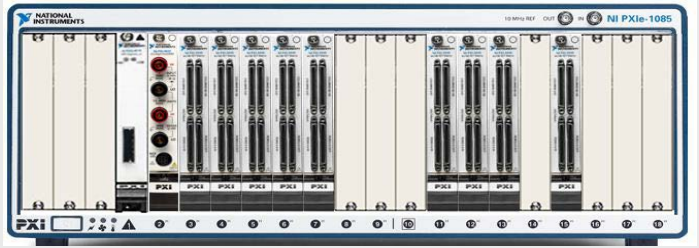
2. TEST INFRASTRUCTURE

VORTEX 2.2 TEST SYSTEM FOR MICRO-BUMP PROBING

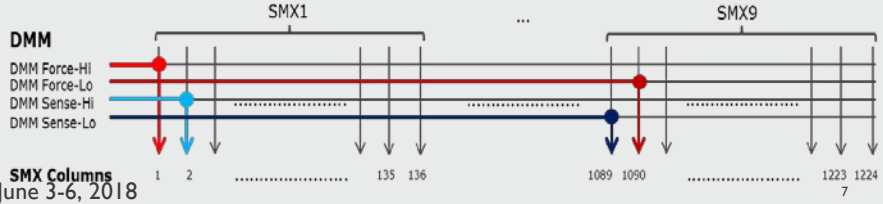


VORTEX 2.2 TEST SYSTEM FOR MICRO-BUMP PROBING





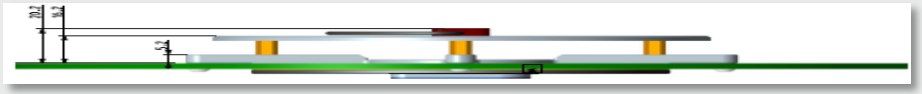
- PXI Rack: programmable Switch Matrix
  - 4 input rows driven by DMM
  - 9×136 = 1,224 output columns
- Two- and four-point *R* measurements
  - R_{max} = 1,000 Ω @100 meas/second
  - $R_{meas} > R_{max}$ ➔ 'NaN' (=open)



TECHNOPROBE WIDE-I/O2 MEMS PROBE CARDS



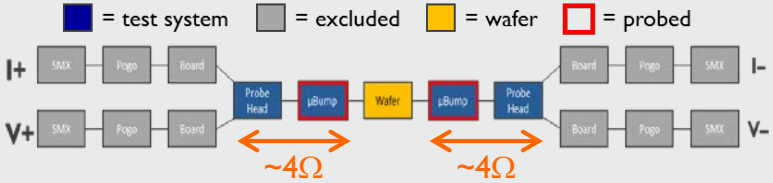






Technoprobe Specification

Parameter	TPEG™ T40	ARIANNA™ A40
Needle diameter	1 mil equiv.	1 mil equiv.
Tip shape	Flat (Sn)	Flat (Cu)
Z planarity	Δ10μm*	Δ10μm*
Minimum pitch	40μm full array	40μm full array
Force/tip (at 75μm OT)	1.2 gf/tip	1.2 gf/tip
Pin current (CCC)	250 mA	250 mA



Pseudo four-point measurements

- Two tester channels per probe tip, connected at jumper interface

3. IMEC TEST CHIPS WITH MICRO-BUMPS

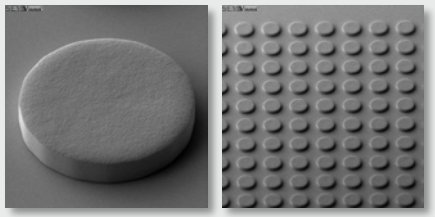
3. IMEC TEST CHIPS WITH MICRO-BUMPS
PROBE CARD CHARACTERIZATION WAFERS

Blanket Micro-Bump Wafer (BMB)

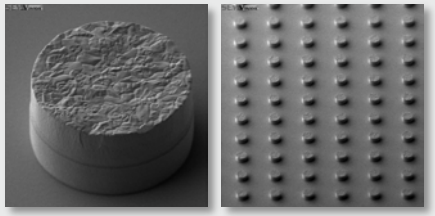
- Only micro-bumps, all shorted

Probe interface:

- Three fine-pitch micro-bump arrays
- Different metallurgies
  - Ø25µm Cu μbumps : 5µm height
  - Ø15µm Cu/Ni/Sn μbumps : 9.5µm height



Ø25µm Cu



Ø15µm Cu/Ni/Sn



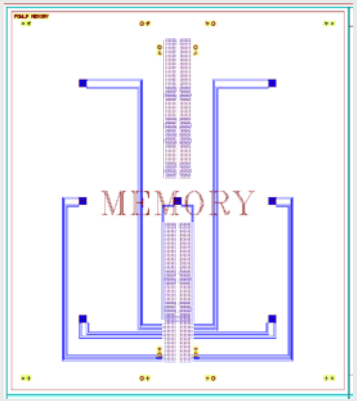
WIO2
@40/40µm
27 arrays

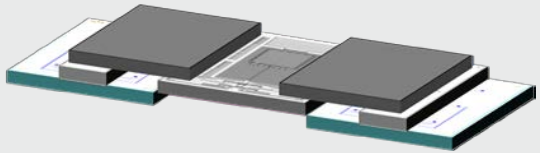
WIO1
@40/50µm
27 arrays

WIO1
@50/50µm
18 arrays

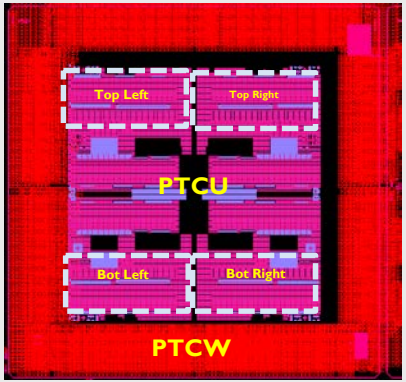
3. IMEC TEST CHIPS WITH MICRO-BUMPS
DEVICE WAFERS

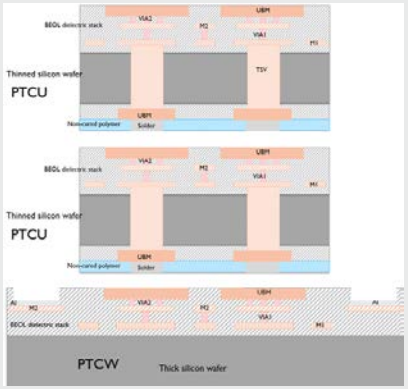
FOWLP Memory





Processing Test Chips 'U' and 'W'





Probe interface:

- WIO2-4banks with Ø15µm Sn micro-bumps
  - Micro-bump height: **9.5µm**
- Technoprobe TPEG™ T40 probe card

Probe interface:

- 4 × WIO2-1bank with Ø30µm Cu micro-bumps
  - Micro-bump height: **0µm** (embedded)
- Technoprobe ARIANNA™ A40 probe card

4. DESIGN OF EXPERIMENTS

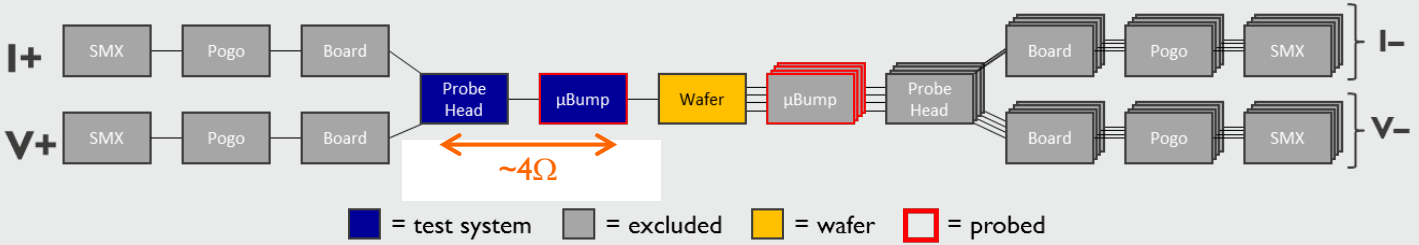
PROBE CARD QUALIFICATION TESTS (1/2)

1. Incoming Inspection on BMB

- Electrical characterization of probe card
- Probe-check measurements at varying over-travels
- Determine first-to-last and long-term suitable over-travel
  - Based on electrical measurements and probe marks

Probe-check routine

- Individually characterizes probe tips
- Measurements include up to 4Ω parasitics
- Measure one probe vs. others ganged
  - Repeat for all probes



PROBE CARD QUALIFICATION TESTS

2. Run-in of Probe Card and Probe Tip Cleaning on BMB

- Creating mileage on the probe card
- Probe-check measurements at selected over-travel
- Determine optimal cleaning interval

Recommended cleaning recipe

- Substrate : 3M / 3µm pink
- Interval : 100 – 500 touch-downs
- Over-travel : 35-50 µm

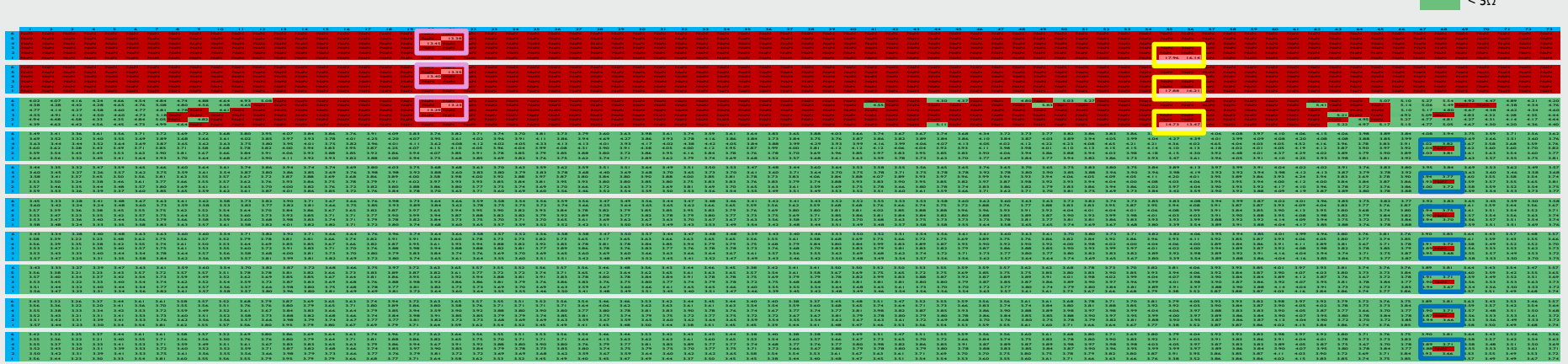
3. Device Wafer Tests

- Use probe card for pre/post-bond testing of device wafers

5. PROBING ON SN MICRO-BUMPS

5. PROBING ON SN MICRO-BUMPS

INCOMING INSPECTION



Over-travel	NaNs	Rmin	Rmax	Rmean
0	434	13.38	17.96	15.11
10	434	13.35	17.88	15.09
20	319	4.02	14.73	4.85
30	1	3.28	4.69	3.87
40	1	3.24	4.40	3.75
50	1	3.23	4.25	3.72
60	1	3.21	4.17	3.71
70	1	3.21	4.16	3.70
80	1	3.20	4.15	3.69
90	1	3.20	4.15	3.69

Identified anomalies:

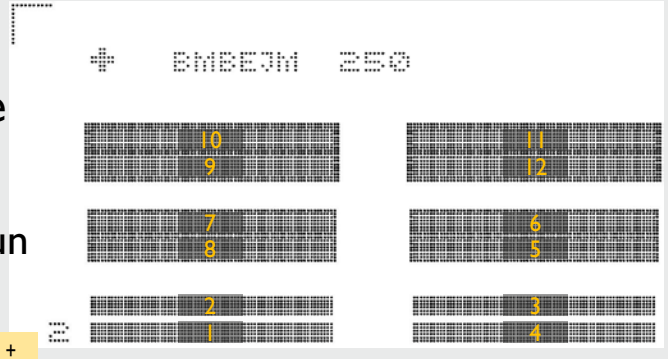
- Permanent SHORT : Probes 239-313
- Temporary SHORT : Probes 55-56
- Permanent OPEN : Probe 214

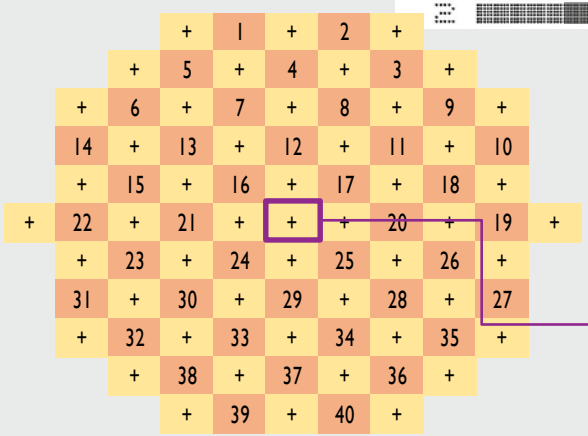
Minimum over-travel: 50µm

RUN-IN OF PROBE CARD

On BMB Wafer

- Check consistency of electrical measurements per probe
- Automatic probing on batches of dies
  - One batch: 40 dies × 12 arrays = 480 touch-downs per run
  - Probing neighboring arrays per die
  - Meandering from North to South





Legend

N — Nth probed die

\+ — Non-probed die

Training die – used for:
- Calibrating PTPA
- Incoming Inspection

Excluded from checkerboard

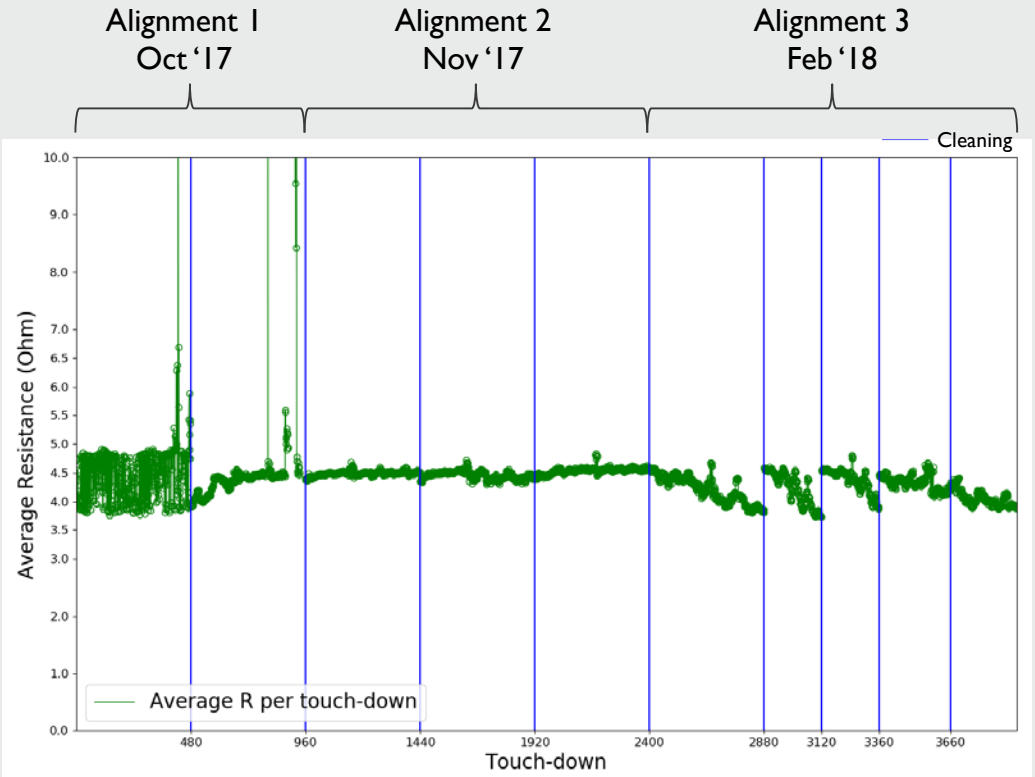
Tip Cleaning

- At varying intervals
  - First after every 480 touch-downs
  - Later after 240 or 300 touch-downs

5. PROBING ON SN MICRO-BUMPS

RUN-IN OF PROBE CARD: ELECTRICAL RESULTS

- Alignment 1
  - Fine-tuning of the test setup
  - Accuracy adjustments
- Alignment 2
  - Normal operating conditions
- Alignment 3
  - Influenced by chuck tilt and low over-travel



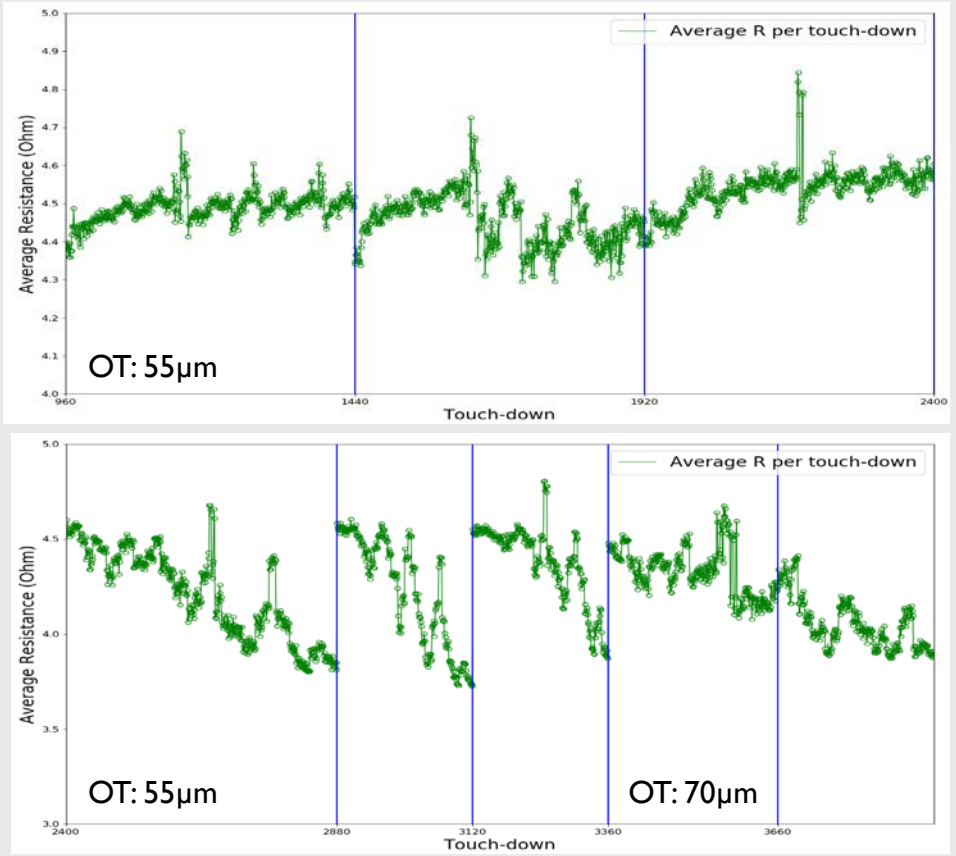
RUN-IN OF PROBE CARD: ALIGNMENTS 2 AND 3

Alignment 2

- Outliers in *R* due to wafer anomalies
- Probe tip cleaning not effective
  - Probes do not get dirty

Alignment 3

- Weaker contact at lower over-travel due to chuck tilt
- Increasing the over-travel flattens *R*-curve



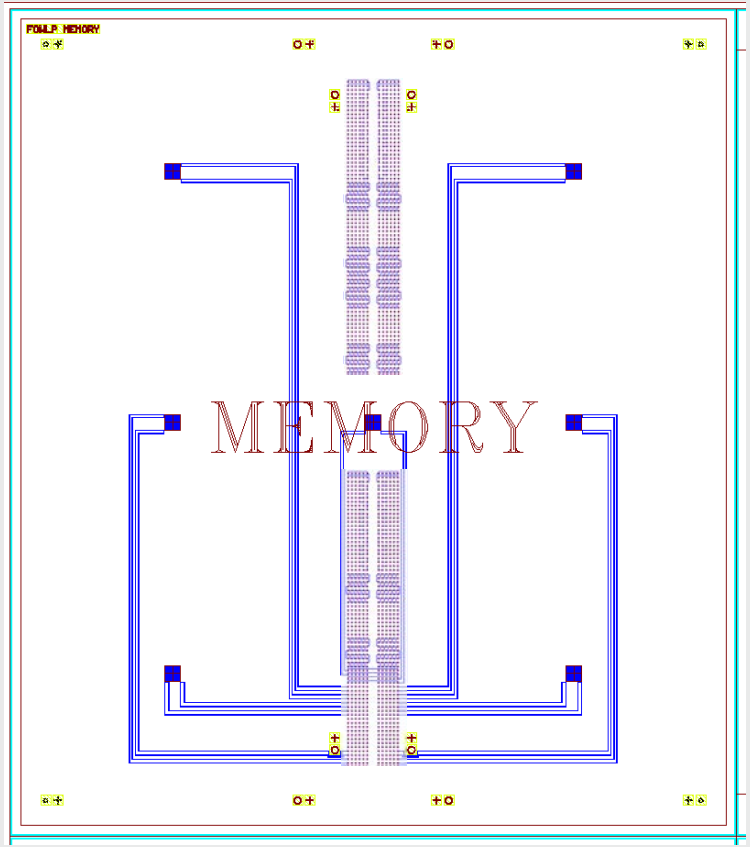
5. PROBING ON SN MICRO-BUMPS
FOWLP MEMORY: DIE DESIGN

Material:

- Fully processed ø300mm wafer, thinned, on tape frame
- 149 Memory dies

Test:

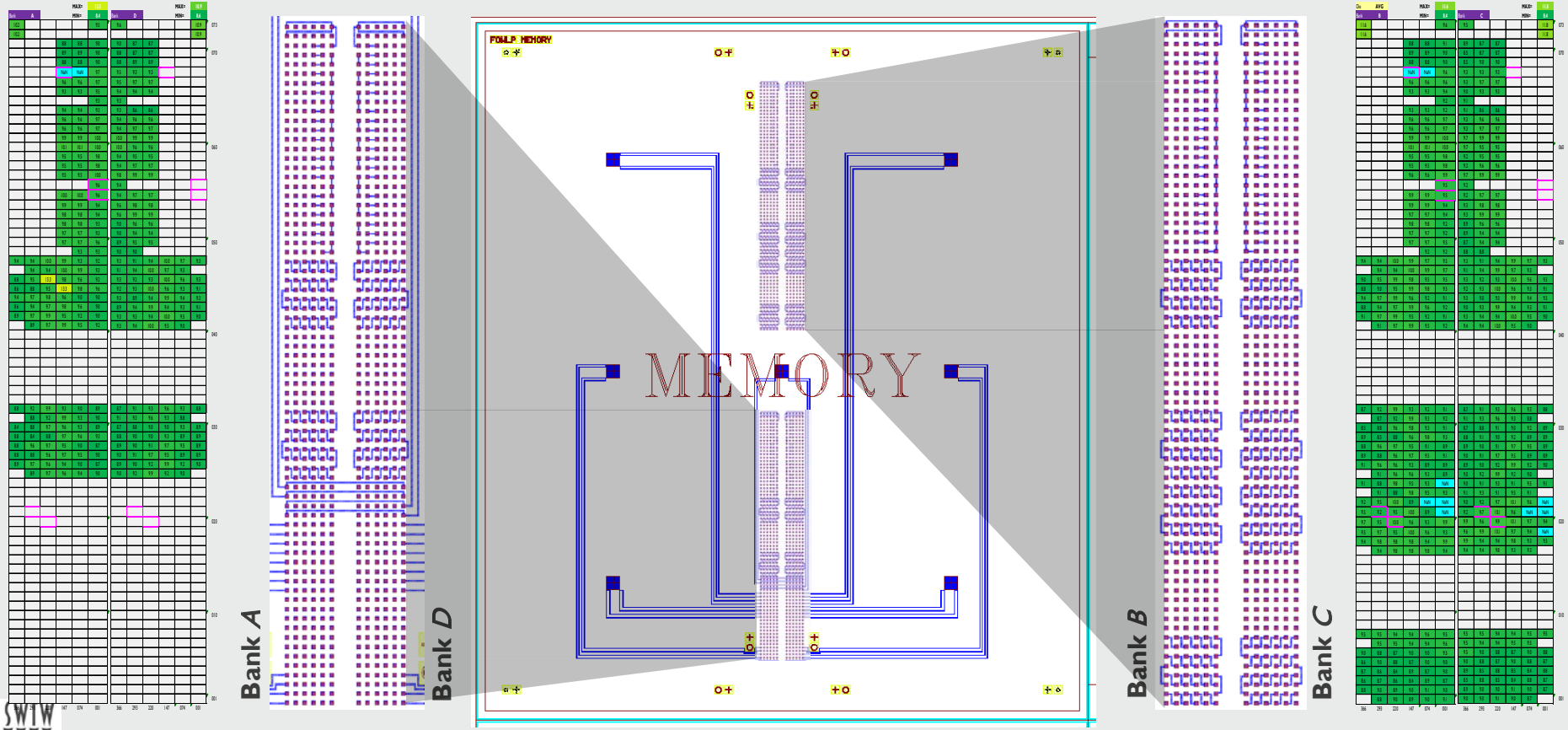
- Pair-wise connected micro-bumps
- 452 measurements / die → 67,348 / wafer
- ~50 minutes test time / wafer
- Measurements include up to 8Ω parasitics



5. PROBING ON SN MICRO-BUMPS

FOWLP MEMORY: DIE DESIGN

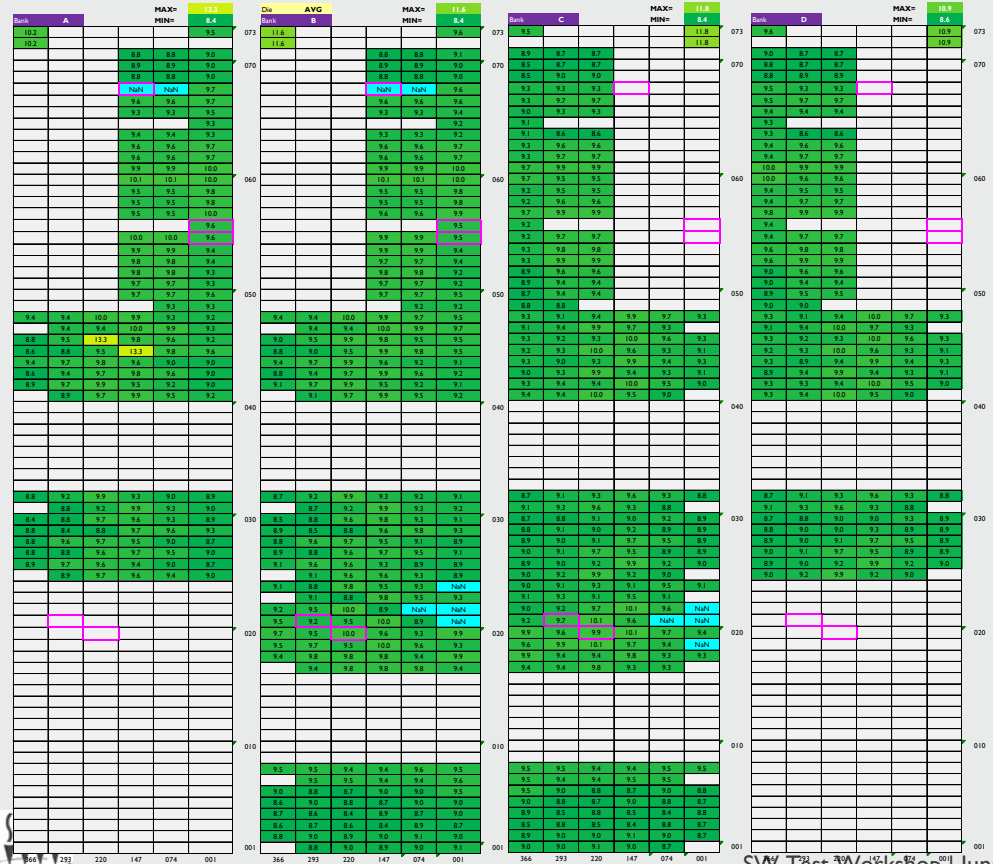
Legend
- = SHORT to neighbor
- = Not connected



5. PROBING ON SN MICRO-BUMPS

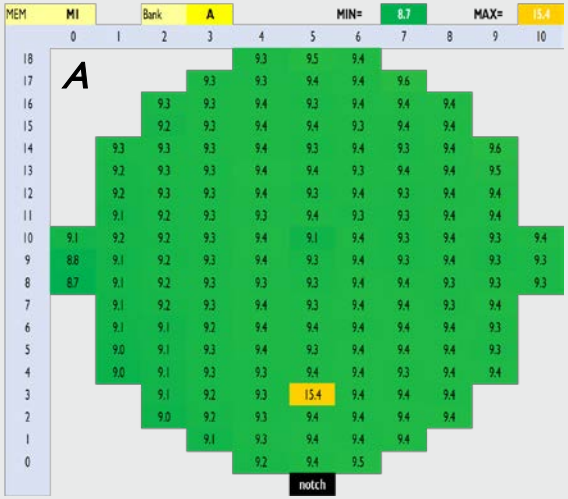
FOWLP 'MEMORY': ELECTRICAL RESULTS

NaN =	NaN	Ohm
MAX Color =	20.0	Ohm
MIN Color =	8.7	Ohm



- Average of all measurements per probe
- Measured resistance as expected!
- Identified one high-ohmic die

➔ exclude from further processing



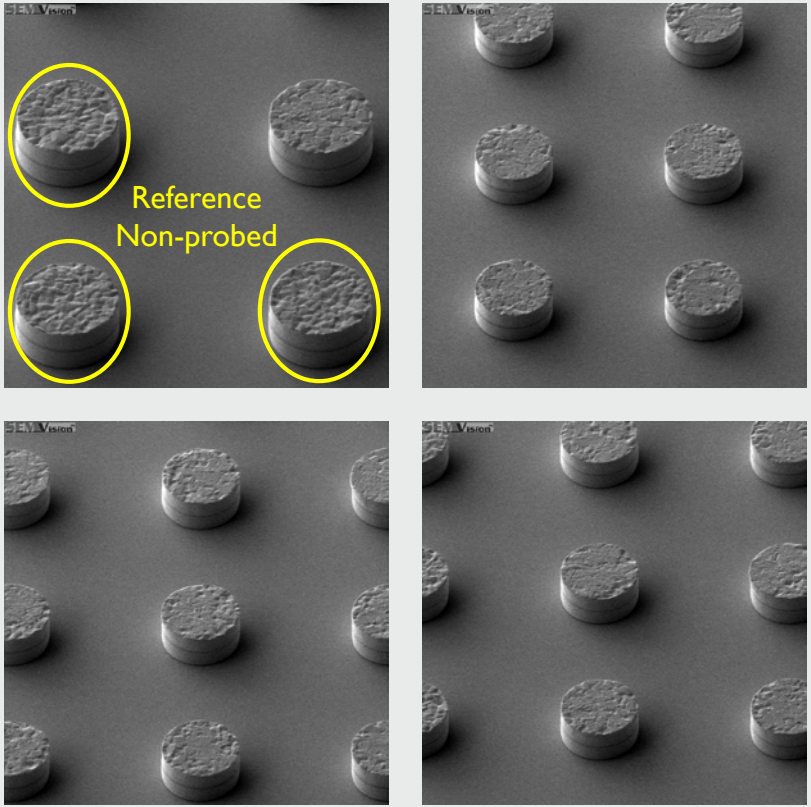
5. PROBING ON SN MICRO-BUMPS

TYPICAL PROBE MARKS

BMB : 9.5µm tall Sn micro-bumps

- Probe diameter : Ø25 µm
- Bump diameter : Ø15 µm

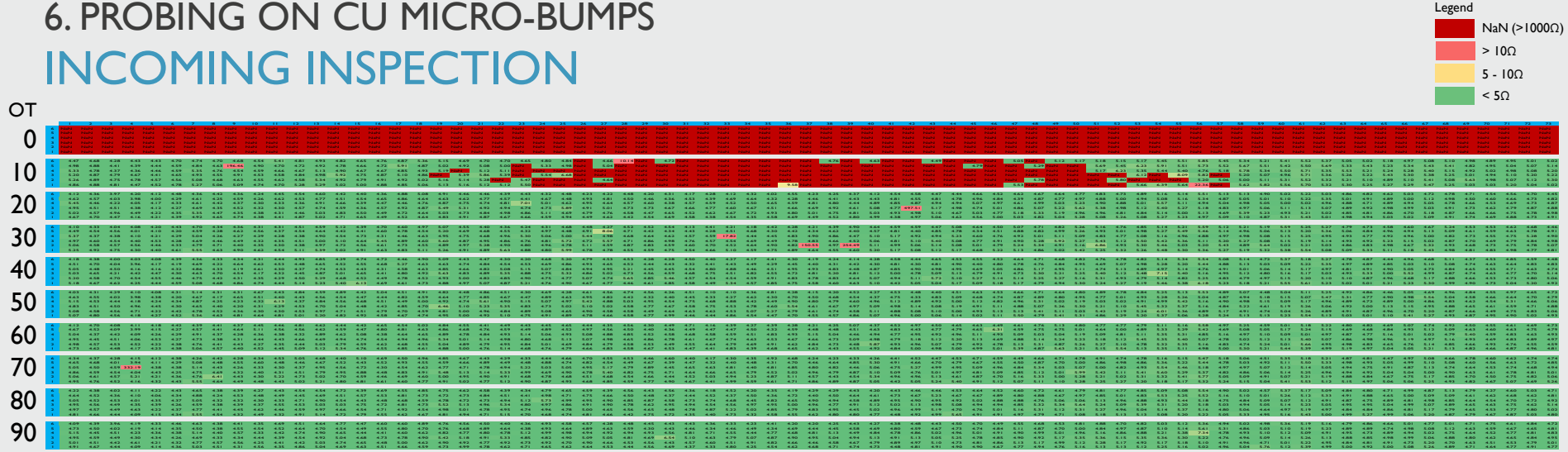
- Probe marks nicely centered
- Uniform marks across whole wafer
- Very light imprints



6. PROBING ON CU MICRO-BUMPS

6. PROBING ON CU MICRO-BUMPS

INCOMING INSPECTION



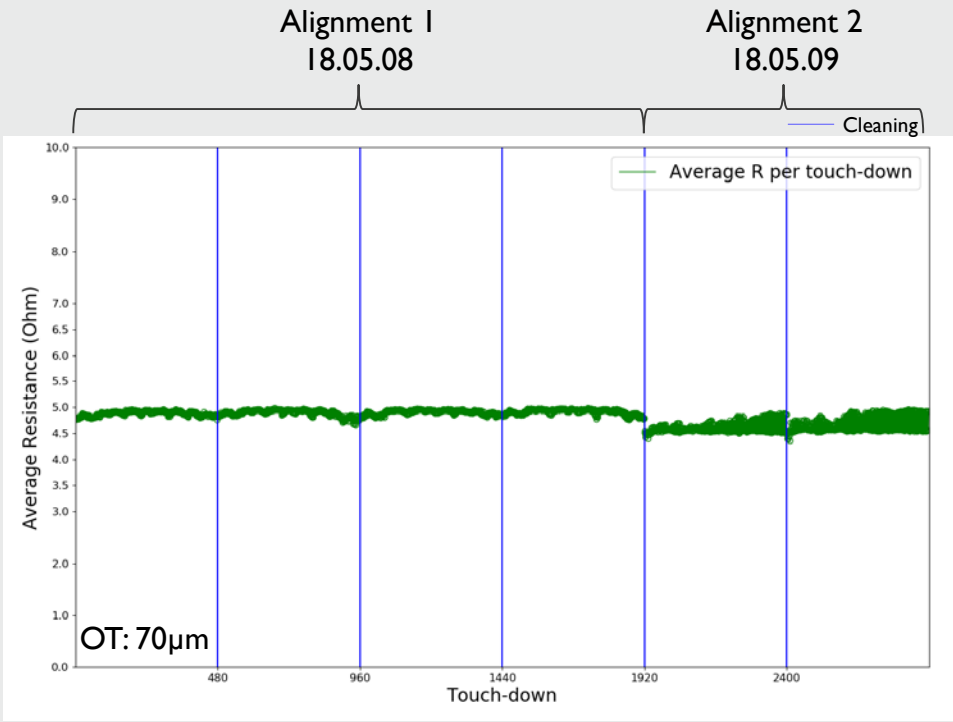
Over-travel	NaNs	Rmin	Rmax	Rmean
0	438	-	-	-
10	157	4.28	196.46	5.20
20	0	3.97	497.51	4.79
30	0	4.01	254.49	4.92
40	0	3.96	7.15	4.79
50	0	3.98	6.46	4.80
60	0	3.99	6.31	4.78
70	0	3.94	332.19	4.85
80	0	4.01	5.73	4.77
90	0	3.96	7.34	4.76

No shorts or opens!

Minimum over-travel: 60µm

RUN-IN OF PROBE CARD: ELECTRICAL RESULTS

- Alignment 1
  - Normal operating conditions
- Alignment 2
  - Measurements influenced by chuck tilt
- Probe tip cleaning not effective
  - Probes do not get dirty



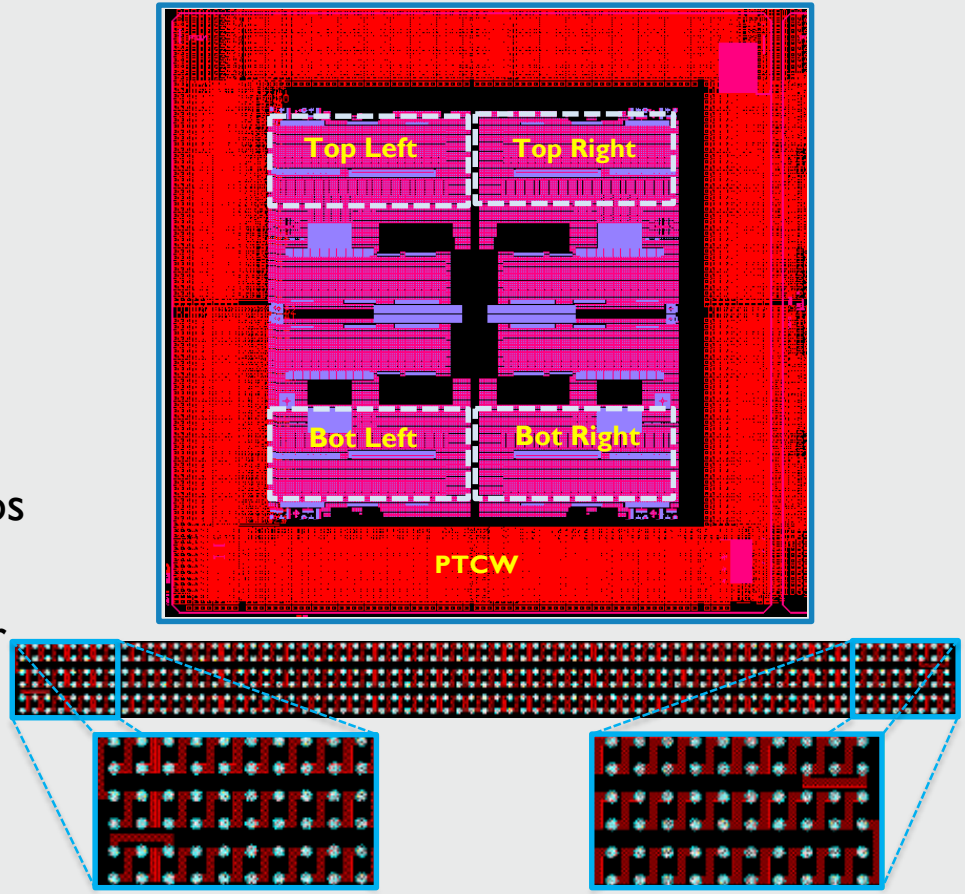
PTCW: DIE DESIGN

Material:

- Fully processed ø300mm wafer
- 275 PTCW dies

Test:

- Pair-wise diagonally-connected micro-bumps
  - Exceptions at corners
- 872 measurements / die → 239,800 / wafer
- ~50 minutes test time / wafer



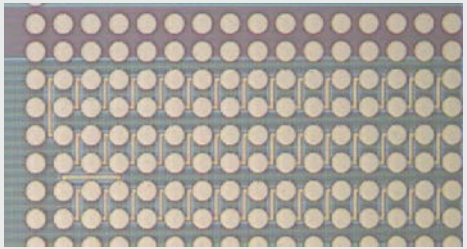
6. PROBING ON CU MICRO-BUMPS
PTCW: ELECTRICAL RESULTS

- Four measurements per probe / die ➔ 1100 measurements per probe / wafer
- Measurements include up to 8Ω parasitics

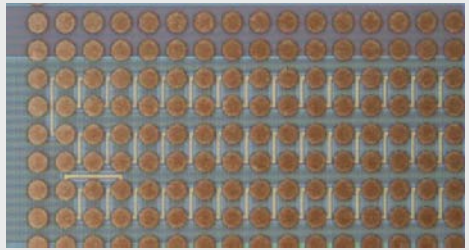
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64	65	66	67	68	69	70	71	72	73
6	11.0	10.5	10.3	11.0	11.3	11.8	12.2	12.7	12.4	13.3	13.2	12.7	13.3	11.0	12.9	11.7	13.3	12.5	14.5	13.3	13.8	11.6	11.2	11.4	10.6	11.5	11.2	10.5	12.3	11.0	12.1	10.8	10.1	10.3	10.1	10.6	10.2	10.5	9.9	10.4	10.7	10.6	10.6	10.5	10.3	10.4	10.5	11.5	10.5	11.1	10.8	10.9	11.2	11.1	11.4	11.8	11.6	11.7	11.4	11.6	11.8	11.5	11.5	12.4	11.3	11.7	11.5	11.7	11.8	11.3	11.1	10.2	10.9
5	11.3	10.5	11.4	10.5	10.6	12.5	13.3	11.3	12.2	13.2	14.0	14.5	11.3	11.4	11.2	14.2	11.6	12.9	13.9	15.8	12.7	11.6	10.2	10.9	12.6	10.5	10.4	12.3	10.8	12.2	11.2	10.9	10.3	9.8	10.3	10.4	10.7	9.9	10.5	10.1	10.5	11.1	10.7	10.1	10.3	10.6	10.7	10.5	11.4	10.6	11.2	10.9	10.8	11.2	11.5	12.0	11.8	11.0	11.7	11.4	11.4	12.4	11.9	10.8	12.8	11.3	10.8	11.9	12.0	11.1	10.9	11.6	10.6
4	12.5	13.5	13.6	11.1	11.6	11.7	13.1	12.2	12.1	12.6	12.2	12.4	13.1	11.9	13.0	10.7	12.1	13.0	12.8	15.5	15.8	15.0	16.2	15.1	14.8	14.7	13.8	13.0	12.4	11.9	12.8	12.6	12.5	13.4	13.1	13.2	12.5	13.4	12.2	12.8	12.5	13.6	12.5	12.7	12.4	12.9	13.6	12.0	14.2	12.7	14.2	13.1	12.0	11.8	11.8	12.2	11.8	12.2	11.9	11.9	13.0	11.5	13.3	12.4	13.1	12.7	13.4	13.6	12.1	11.2	11.1	11.0	10.5
3	15.0	14.5	11.5	12.1	11.4	11.1	12.6	13.6	12.0	12.4	12.6	11.6	12.6	14.4	10.8	12.2	10.7	11.5	15.7	14.7	15.0	17.1	14.8	15.0	15.2	14.2	14.3	13.0	11.5	12.1	12.3	13.1	12.8	12.7	14.0	13.1	12.6	11.8	13.4	12.6	13.1	12.4	13.3	12.5	13.0	12.7	12.4	14.6	11.7	14.5	13.8	12.5	12.1	12.0	12.0	11.5	12.5	12.3	11.8	12.1	12.1	13.2	10.9	13.2	13.0	13.1	14.1	13.3	11.2	11.5	11.9	10.8	12.7
2	15.5	17.2	16.9	14.1	15.8	15.8	16.7	15.3	16.5	14.9	15.3	16.0	17.0	15.6	16.5	15.2	17.4	15.6	22.8	15.6	18.3	14.8	16.6	14.0	18.8	14.4	18.1	15.5	16.1	19.7	15.5	16.2	16.2	15.2	14.8	15.0	13.8	15.0	13.7	13.7	12.3	13.1	12.0	13.8	12.6	13.5	13.0	13.9	13.9	12.9	13.4	11.8	13.4	12.6	13.8	13.1	13.6	13.5	13.6	13.8	14.4	13.6	14.6	12.4	14.6	13.2	14.3	12.6	13.7	14.2	13.1	16.5	11.2
1	20.6	19.7	13.1	18.0	14.7	14.2	15.9	19.8	15.6	13.1	14.8	17.8	16.6	15.4	14.7	17.4	16.0	18.5	15.3	22.6	15.6	17.2	14.1	18.3	14.0	18.8	14.6	16.7	16.6	15.0	20.4	16.2	15.3	15.8	15.1	14.6	14.7	12.7	14.7	14.0	13.0	11.6	13.3	12.2	14.0	13.0	13.4	13.2	13.7	14.0	12.3	13.5	11.7	13.2	13.0	13.3	13.3	14.2	13.9	13.4	13.9	14.8	12.6	15.3	12.4	14.2	13.8	13.1	11.9	14.9	15.4	12.2	19.0

Average *R* per tip across full wafer

- Measured resistance higher than expected
  - Oxidation of Cu micro-bumps



Reference



Heavily oxidized micro-bumps

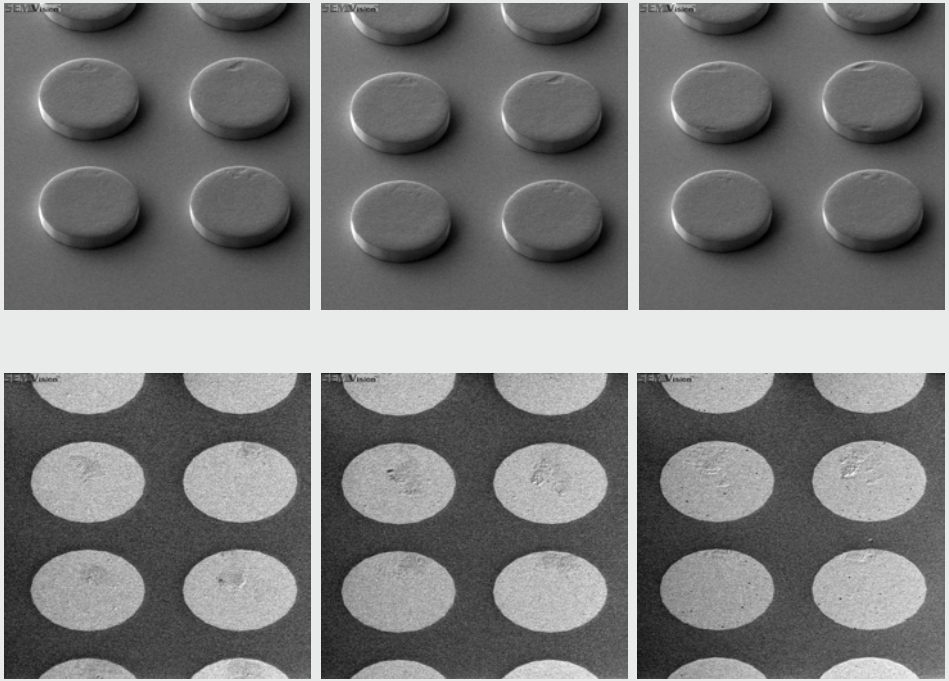
TYPICAL PROBE MARKS

BMB : 5µm tall Cu micro-bumps

- Probe marks on North of *µ*bump
- Uniform marks across whole wafer
- Light imprints

PTCW : Embedded Cu micro-bumps

- Corrected alignment → centered marks
- Light probe imprints



7. CONCLUSION

SUMMARY

- Successfully evaluated two WIO2-1bank probe cards from Technoprobe
  - Stable electrical results
  - Light probe marks
  - No effect of probe tip cleaning, as probes did not get dirty

Probing on Sn micro-bumps

- Technoprobe's TPEG™ T40 probes
- Well-suited for Sn probing
- Probe card to be routinely used in imec

Probing on Cu micro-bumps

- Technoprobe's ARIANNA™ A40 probes
- Well-suited for Cu probing

Future Work

- Continue evaluation with Wide-I/O2-4bank probe cards



SW Test Workshop

Semiconductor Wafer Test Workshop

TPEG™ Mantis: a new solution for multiple advanced applications





Davide Sangiorgio — *STMicroelectronics*
Marco Sciurba — *STMicroelectronics*

Tommaso Masi — *Technoprobe*
Riccardo Vettori — *Technoprobe*

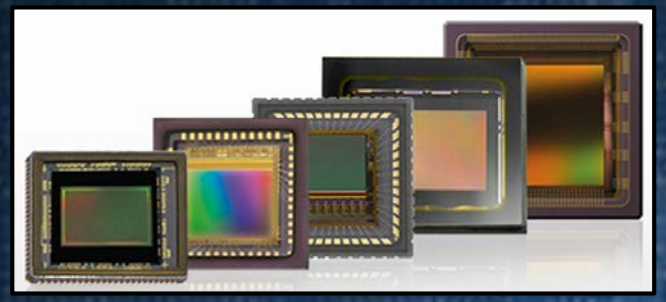
June 3-6, 2018

Overview

- Applications requirements
- TPEG™ Mantis concept
- TPEG™ Mantis general characteristics
- STM experience on field
- Summary

Applications Requirements

- **Customer device applications for TPEG™ MEMS MANTIS**



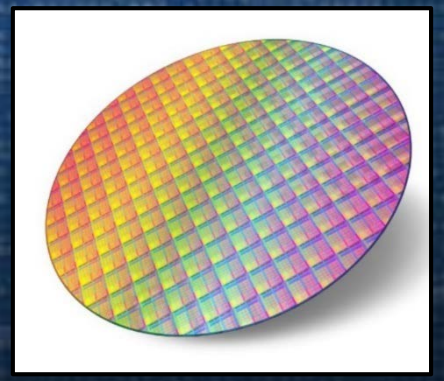
CMOS Image **Sensors**



NOR and NAND **Memories**



Consumer, Industrial and Auto
µControllers & **LCD Drivers**



Parametric Test (WAT, eTest, T84, ...)

Applications Requirements

- **General characteristics requested for CIS and Parametric Tests**
  - Mechanical solution that allows the passage of light through the probe card for the Imaging Sensor stimulation
  - Possibility to mount lens or diffusers in the Probe Card
  - Small scrub marks and low PAD damage
  - Controlled production of debris
  - Direct Attach solutions to minimize Probe Card cost
  - Low Signal attenuation up to 1.2 GHz
  - Good probe to probe insulation

TPEG Mantis Concept

- **Mantis probe concept**
  - Mantis is a µCantilever needle using Technoprobe TPEG™ MEMS Technology. It merges the benefits of both technologies: Vertical and Cantilever.
  - The inspiration came from…

…Nature



TPEG Mantis Concept

- **Mantis probe concept**
  - Mantis is a µCantilever needle using Technoprobe TPEG™ MEMS Technology. It merges the benefits of both technologies
  - The inspiration came from…

…Nature



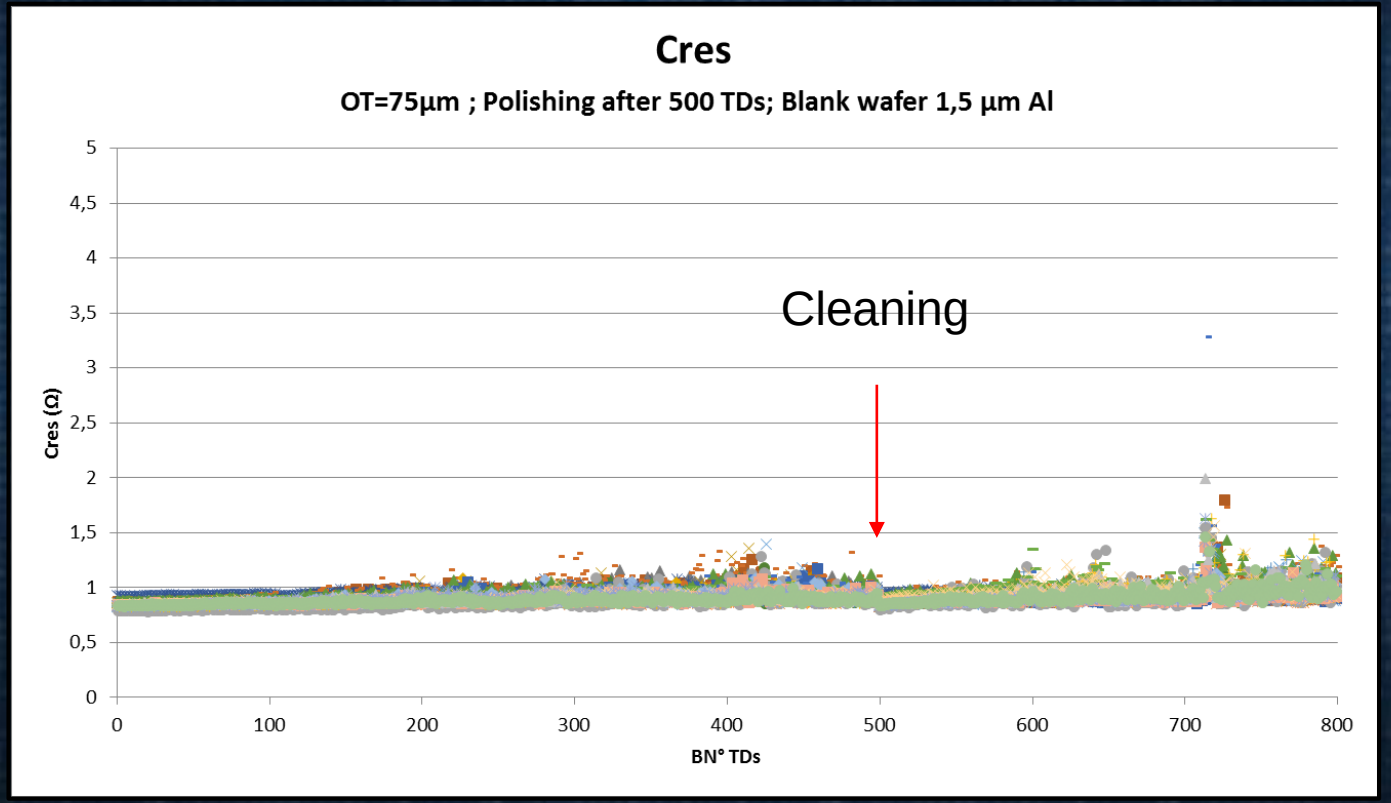
TPEG™ Mantis Internal qualification

- **Tests performed for the internal qualification**
  - Mechanical Test:
    Resistance to fatigue with 1M TDs at 120 µm Overdrive and 100K TDs on wafer edge
  - Cres Test on Blank wafer.
  - Scrub Analysis
  - Probe Current Capability
  - RF Simulation

  - Test on Customer Field:
    Pad damage analyses, Testing Yield evaluation, Life on field evaluation, etc…

Cres Test

- Cres Test performed at OT=75µm on Al Blank wafer (Al thickness 1,5 µm)
- Cleaning done after 500 TDs



Scrub analyses Vs. Temperature

- **TPEG™ Mantis scrub marks on Al Pad at different temperatures**
  - TPEG™ Mantis scrub mark highlighted with the red circle.



OT=75 µm T= -40°C

OT=75 µm T= 60°C

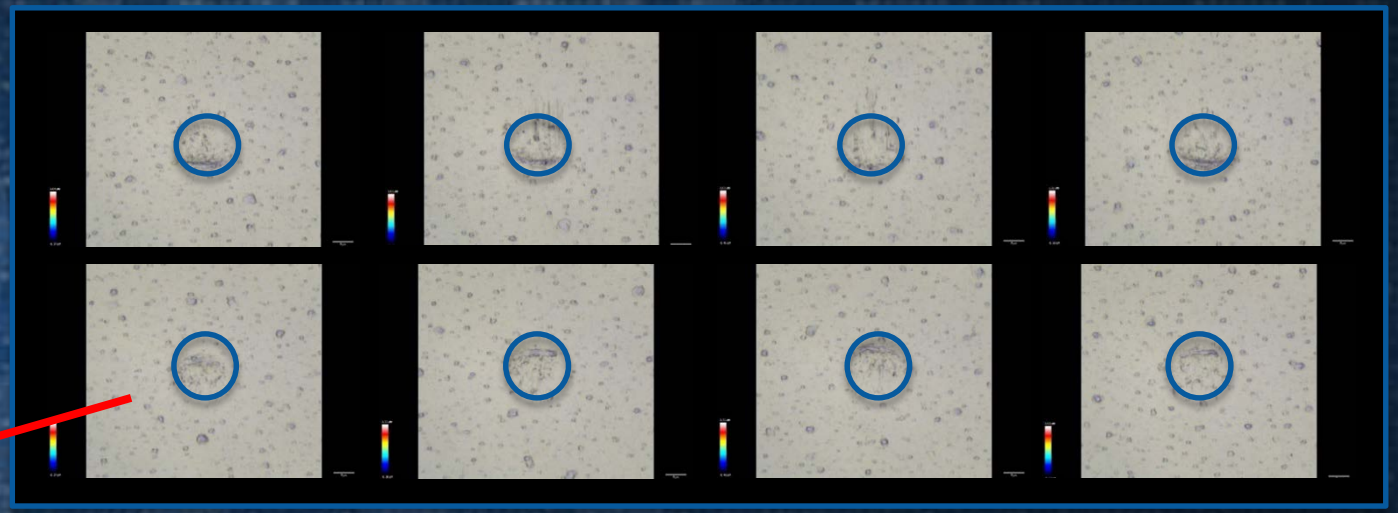
OT=75 µm T= 105°C

Scrub analyses

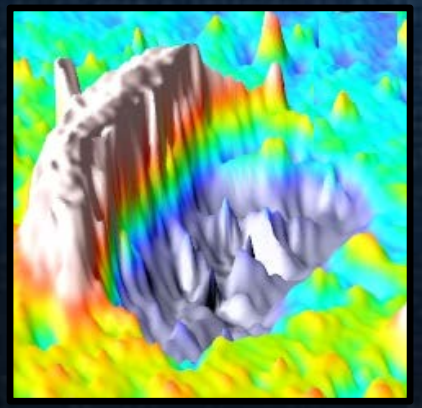
- **Statistical scrub marks collected on Al blank wafer with thickness of 1.5µm at 50 and 100µm OD**

OT=50µm

OT=100µm



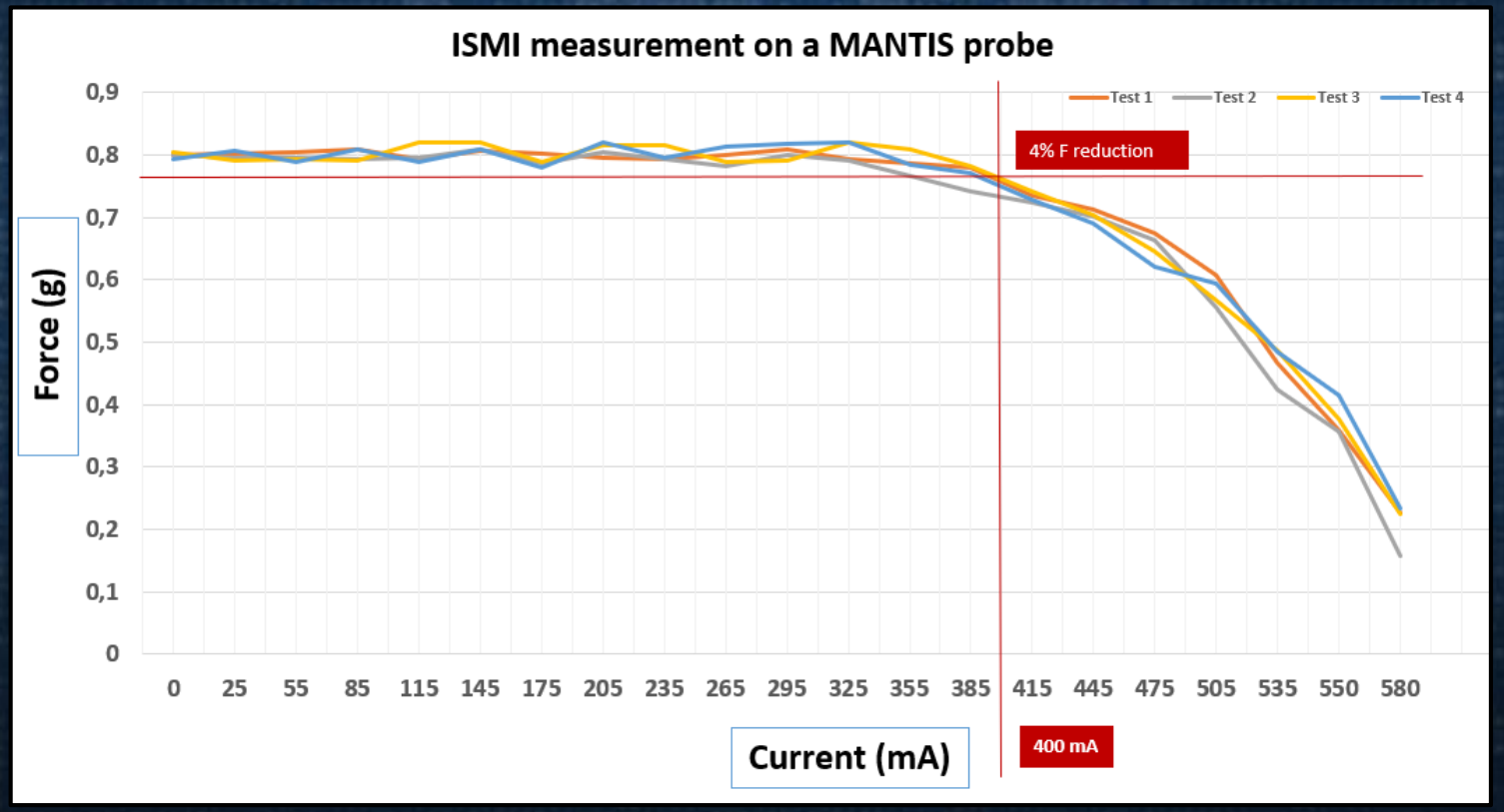
- **Results:**



- At OT = 50um: Scrub length max = 16 µm, Scrub depth max = 290nm
- At OT = 100um: Scrub length max = 22 µm, Scrub depth max = 390nm

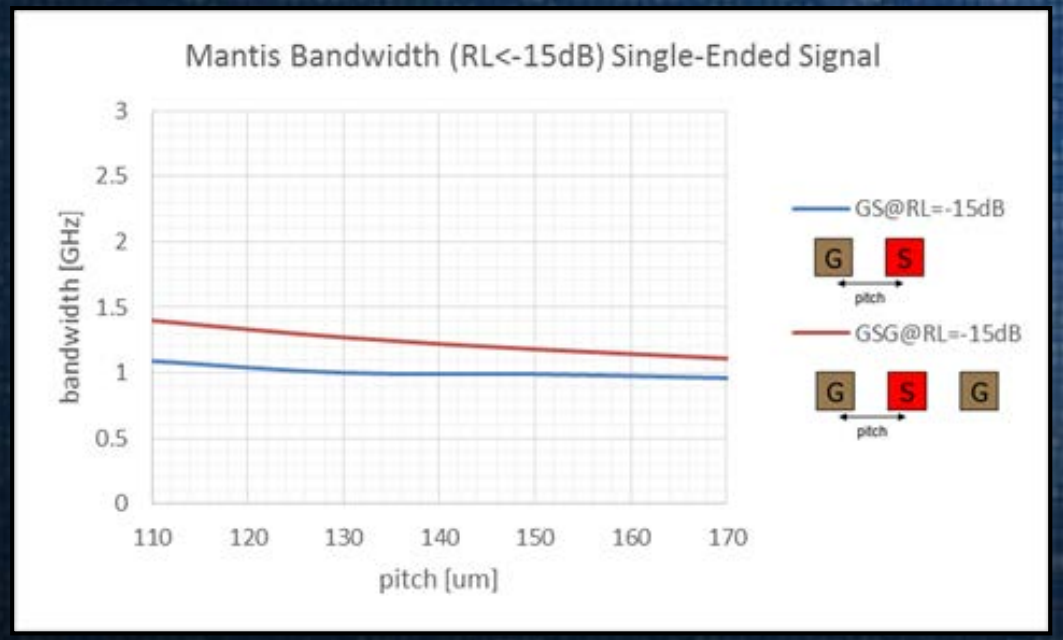
CCC analyses

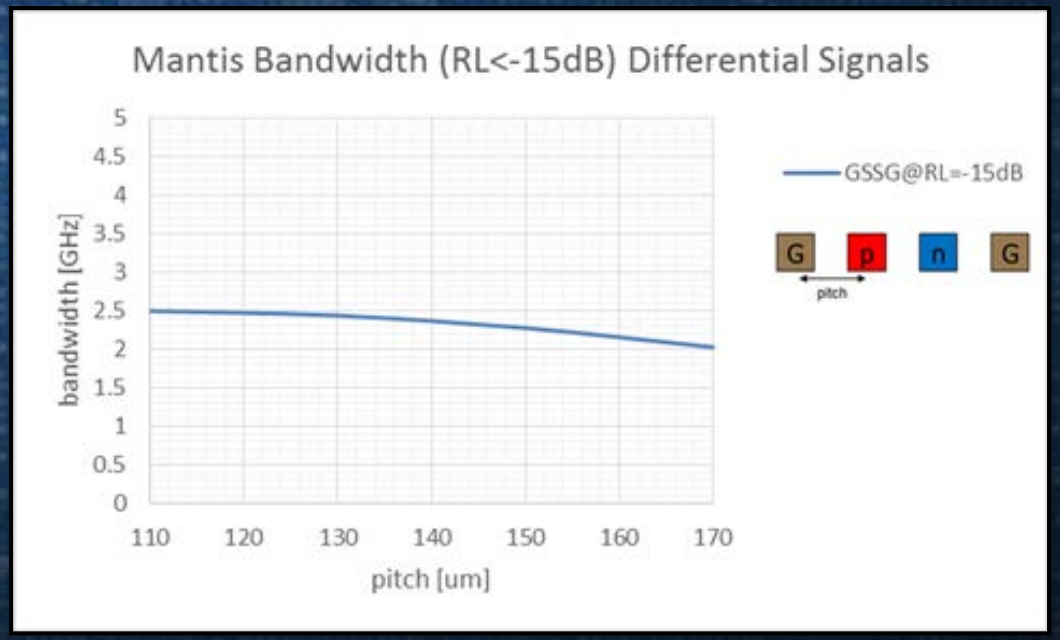
- **CCC performed with the ISMI 09 method**
  - The current TPEG™ Mantis probe, has a 20% force reduction at 500 mA
  - Max CCC limit at 4% of force reduction is 400 mA. This is the limit for TPEG™ Mantis probe
  - The CCC can be increased customizing the probe.



RF Simulations (Return Loss ≤ 15dB)

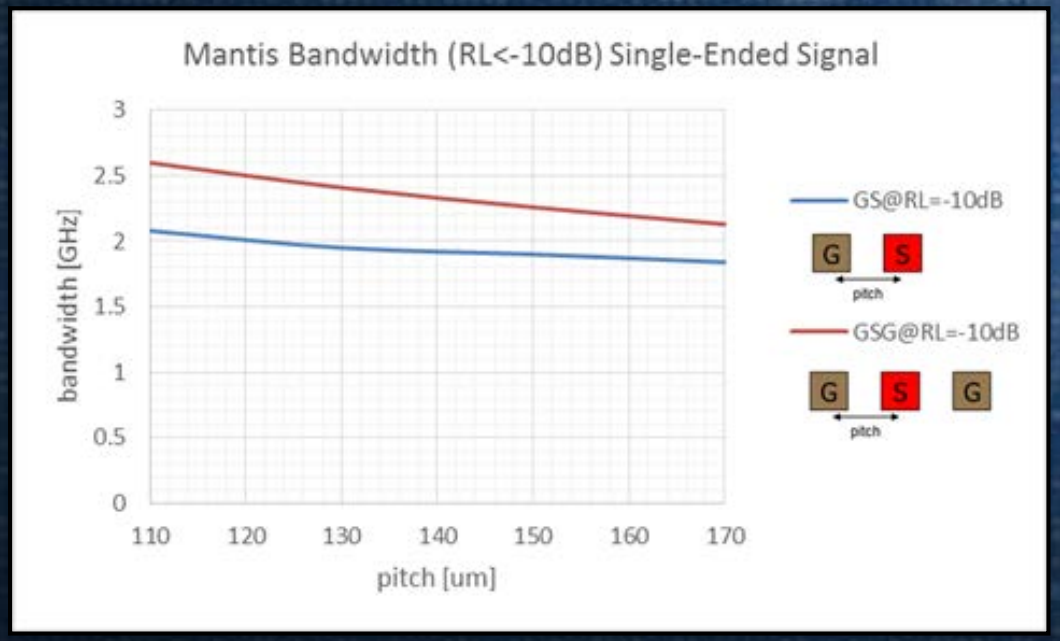
- **Technoprobe performed RF simulations with different kind pitches and Signal modes.**
  - TPEG Mantis bandwidth has been simulated with different configurations.
  - The RL is maintained under 15 dB at 1 GHz for a large pitch window with Single Ended Signals and 2 GHz with Differential Signals.

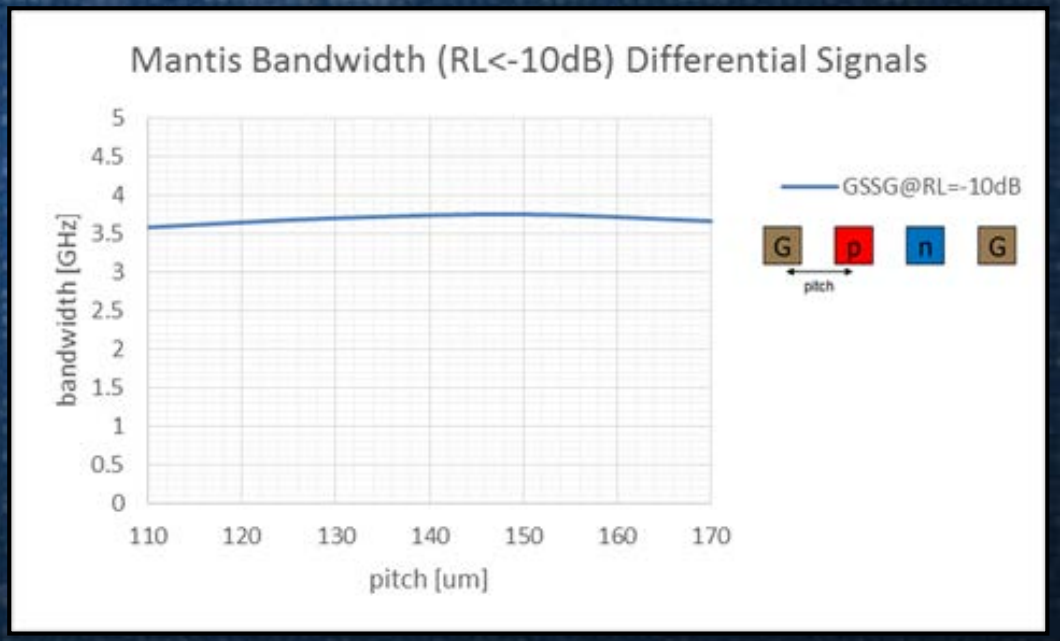




RF Simulations (Return Loss ≤ 15dB)

- **Technoprobe performed RF simulations with different kind pitches and Signal modes.**
  - TPEG Mantis bandwidth has been simulated with different configurations.
  - The RL is maintained under 10 dB at 1,8 GHz for a large pitch window with Single Ended Signals and 3.5 GHz with Differenzial Signals.





TPEG Mantis Description

- **Target Key Values**
  - Low Force
  - Low Pad Damage with controlled and limited scrub mark in all the OD range
  - X and Y alignment comparable to Vertical MEMS Needle
  - Good Z planarity comparable to high end Vertical MEMS Needle
  - Possible to use Direct Attach PCB or Interposer (no need of complex and high costs MLOs or MLCs)
  - Low constrains in layout capability
  - Same tip size during entire lifetime
  - Good Current Carrying Capability that can be customized.
  - High parallelism

TPEG Mantis Specs

PARAMETER	TPEG™ MEMS MANTIS
Contact Diameter	16±4 µm
Usable Tip Length	> 200µm
Max pin count	> 20.000 pins
X, Y alignment accuracy and Z planarity	X,Y ± 10 µm; Z electrical plan Δ 20 µm
Min pitch and configuration	50µm linear configuration(Probes from 2 directions)
Pin Current (CCC ISMI 2009)	400 mA
Force (at 75µm OD)	3.0 g
Working OD / Max OD	75µm / 100 µm

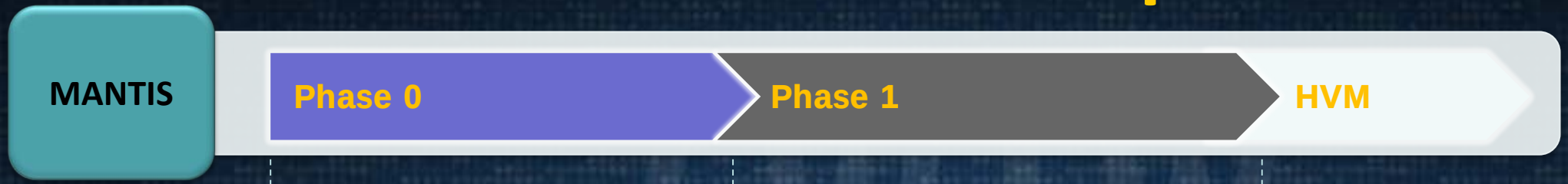
STMicroelectronics Experience



STMicroelectronics qualification criteria

- **STM used a High Volume product for qualification and benchmark of Mantis technology vs. STM standard one. ST qualification conditions:**
  - No PAD damaged at maximum OT and maximum number of passes
  - No crack under PAD at maximum OT and maximum number of passes
  - Scrub marks size and position within spec
  - Yield aligned (or better) to standard production card
  - No “special requirement” for cleaning
  - The above conditions to be verified at 0-time and after production (150kTDs)

STM evaluation plan



T0 – Incoming:

- Probe card information summary and qualification data
- Electrical and mechanical analysis and qualification
- Probing DOE results
- Conclusion

T1 - 150kTDs:

- Probe card information summary and qualification data
- Electrical and mechanical analysis and qualification
- Probing DOE results
- Conclusion

TF – 1M TD:

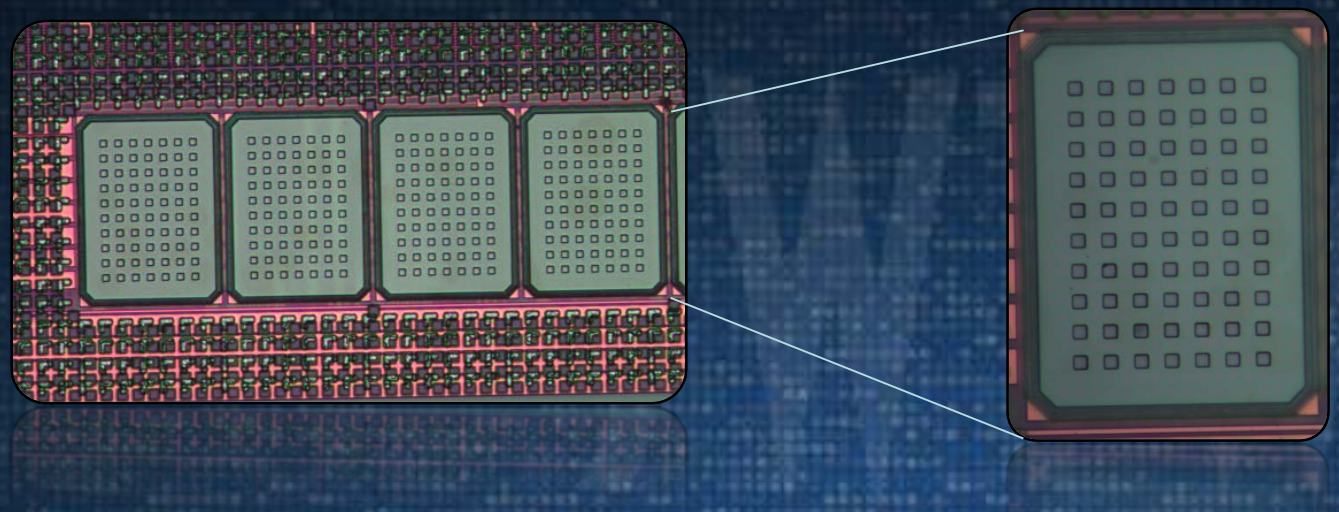
- Lifetime Evaluation
- Uptime Evaluation
- Conclusion

Before starting

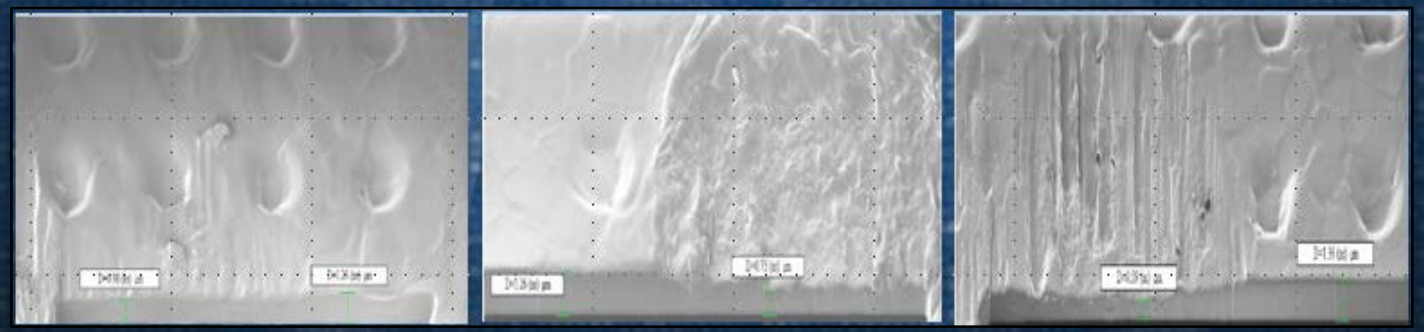
- **Probecard design**
  - X16 DUTs
  - 320 springs
- **Working overdrive**
  - 80µm
- **T0 and T1 probing DOE conditions**
  - Number of passes: 12
  - Overdrive from 60µm to 120µm
- **Cleaning material**
  - ITS PP150



PAD damage evaluation at T0



No crack under passivation under worst conditions OD=120µm (with 12passes)



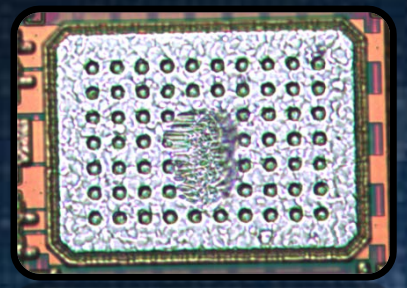
No crack under passivation under worst conditions

OD=80µm/12passes
Scrub depth 280nm

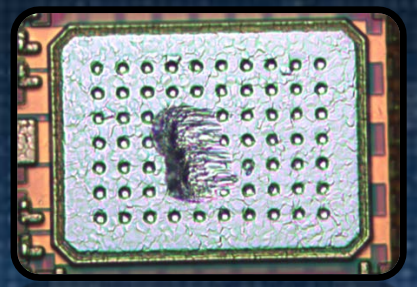
OD=100µm/12passes
Scrub depth 530nm

OD=120µm/12passes
Scrub depth 770nm

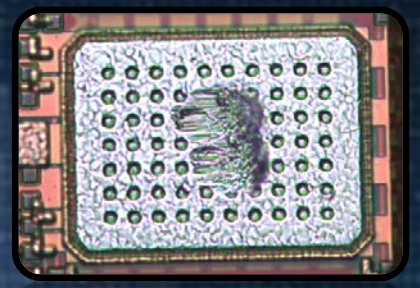
Scrub mark evaluation at T0



OD=80µm
12 passes



OD=100µm
12 passes

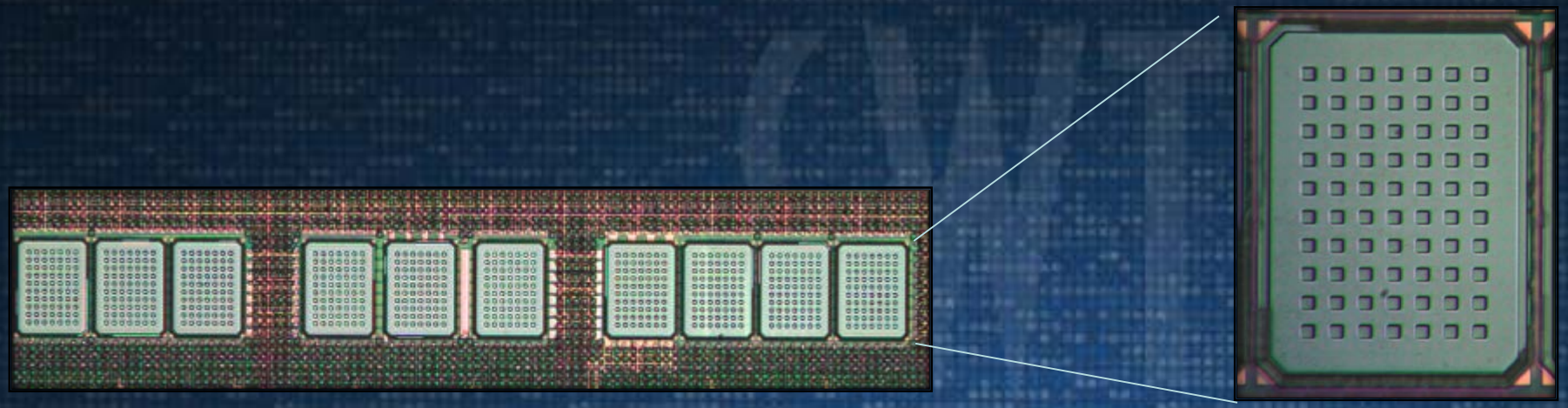


OD=120µm
12 passes

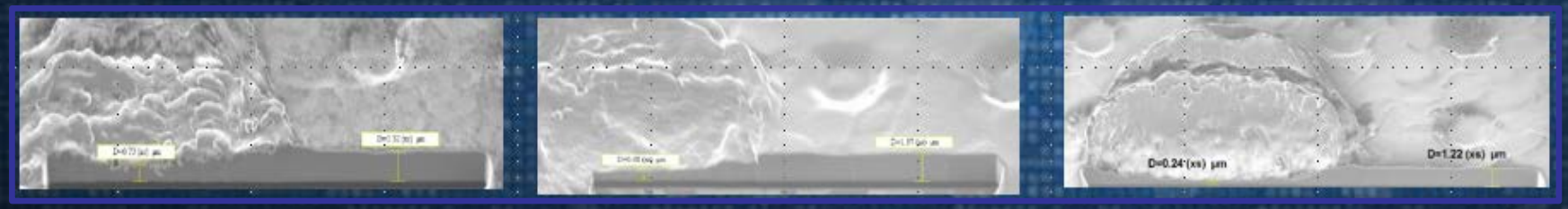
OD	PAD edge Y-margin Cpk	PAD edge X-margin Cpk	Scrub Length Cp	Scrub Width Cp
60µm	6.80	5.00	2.68	3.03
80µm	7.28	3.25	3.46	3.01
100µm	9.06	3.01	3.45	4.03
120µm	3.31	3.03	4.82	2.69

Scrub marks area under worst conditions within spec (<400µm2 vs. 3400µm2 Square Bonding PAD size)

PAD damage evaluation at T1=150kTDs



No damage under metal layer with the worst conditions OD=120µm (with 12passes)



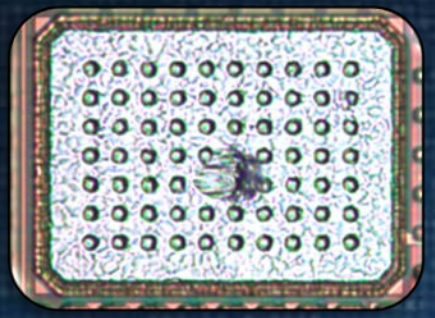
No damage under metal layer under worst conditions

OD=80µm/12passes
Scrub depth 580nm

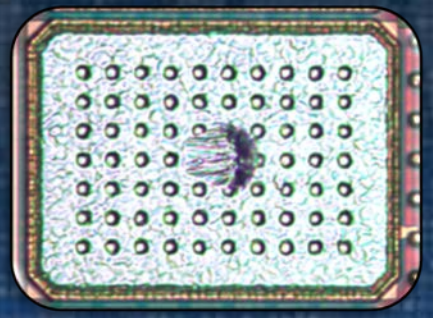
OD=100µm/12passes
Scrub depth 890nm

OD=120µm/12passes
Scrub depth 970nm

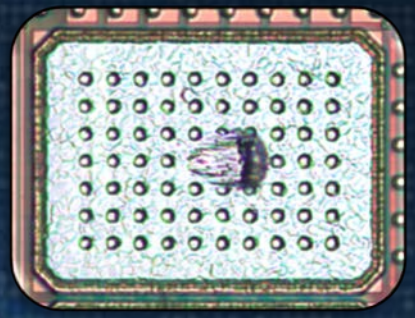
Scrub mark evaluation at T1=150kTDs



OD=80µm
12 passes



OD=100µm
12 passes



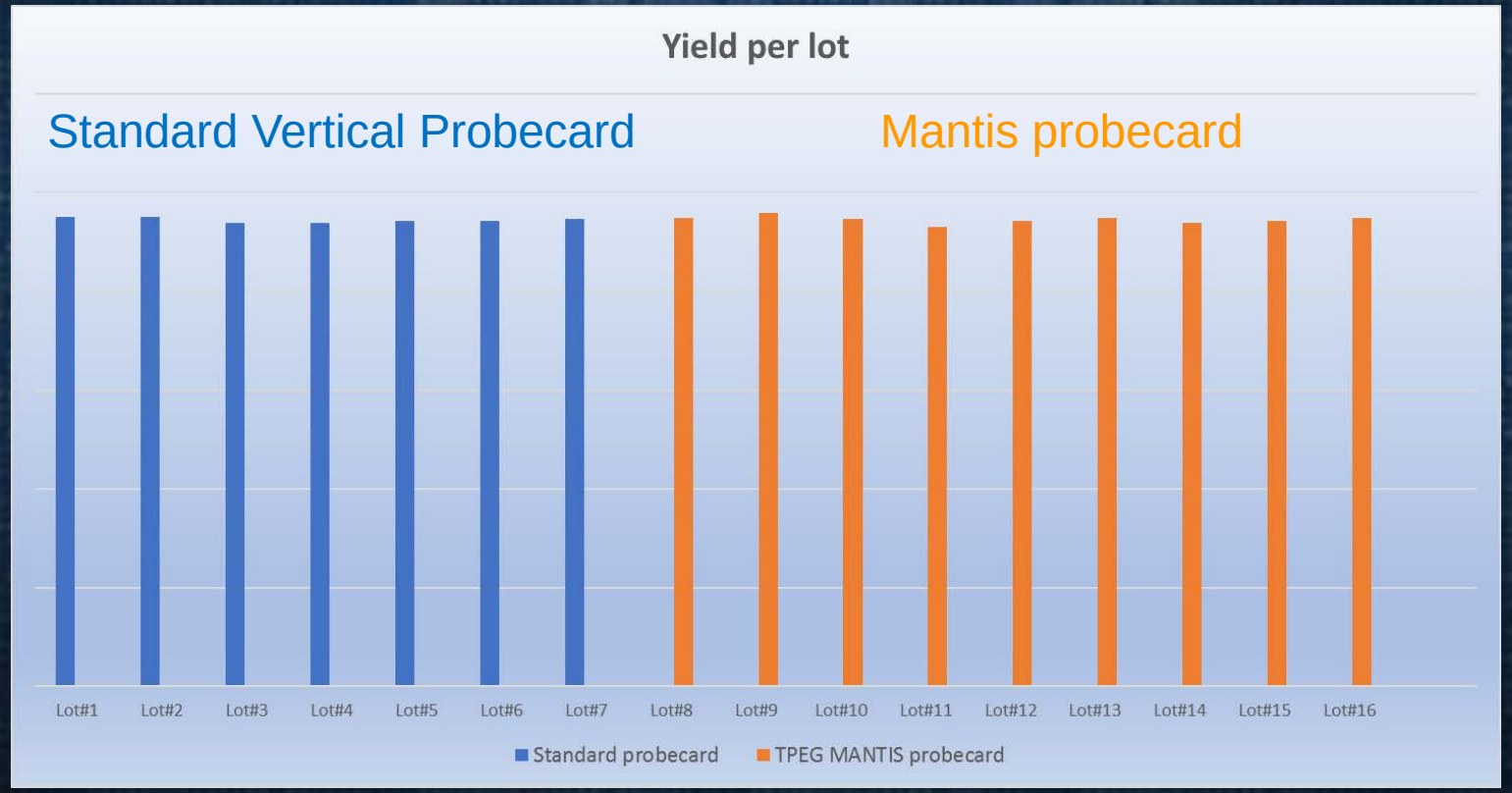
OD=120µm
12 passes

OD	PAD edge Y- margin Cpk	PAD edge X-margin Cpk	Scrub Length Cp	Scrub Width Cp
80µm	5.04	4.28	4.02	3.01
100µm	8.77	6.75	2.43	3.43
120µm	9.45	5.06	4.8	4.02

Scrub marks area under worst conditions within spec (<400µm2 vs. 3400µm2 Square Bonding PAD size)

Yield benchmark from T0 to T1 to today

- **The probecard is in production since end of 2017 with the same cleaning material as the reference probecard**



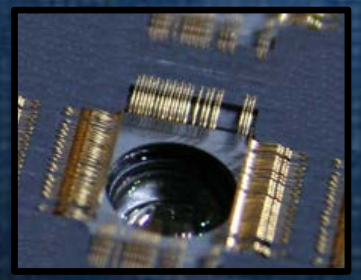
Yield aligned to standard production solution

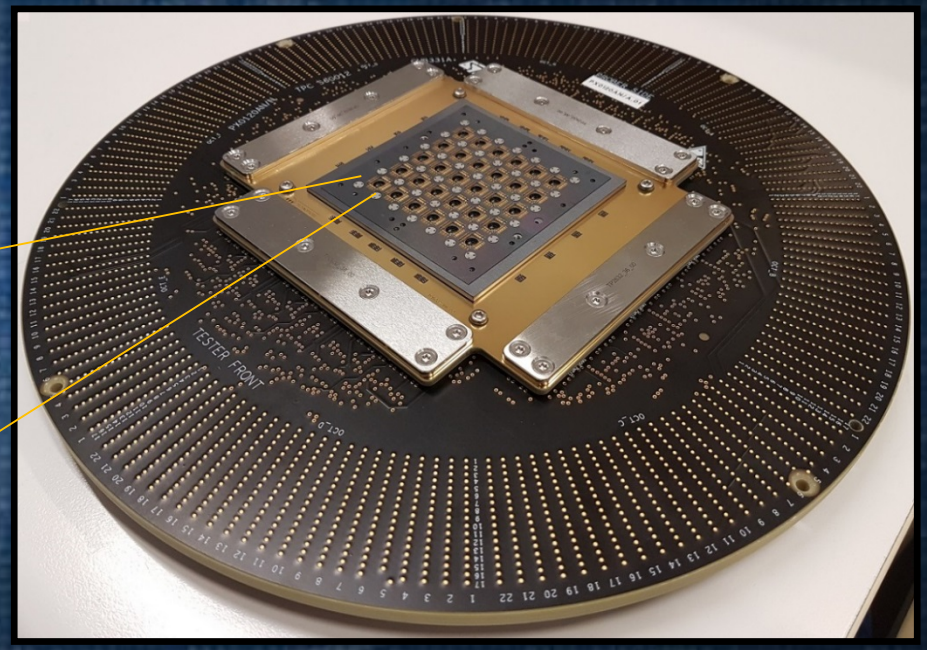
STM Conclusion

- **Qualification**
  - TPEG MEMS Mantis probecard passed all the qualification criteria
- **High Volume production**
  - TPEG MEMS Mantis probecard is in production since end of 2017
  - It reached 1.2MTDs without any issue so far
  - Uptime 99%
  - Tip consumption 30µm (on total 220µm usable tip)
  - We will keep monitoring it…

Next

- **CMOS Image Sensor probecard**
  - 3600 probes
  - x30
  - Status: in qualification





Thanks for your Support !

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SW Test Workshop

Semiconductor Wafer Test Workshop

2-0-1-8

New probe design and development for high current capacity using bi-furcated structure

Joonyeon Kim, Yugyeom Kim

Samsung Electronics

Taegyun Kim, Yongho Cho

Microfriend Inc.

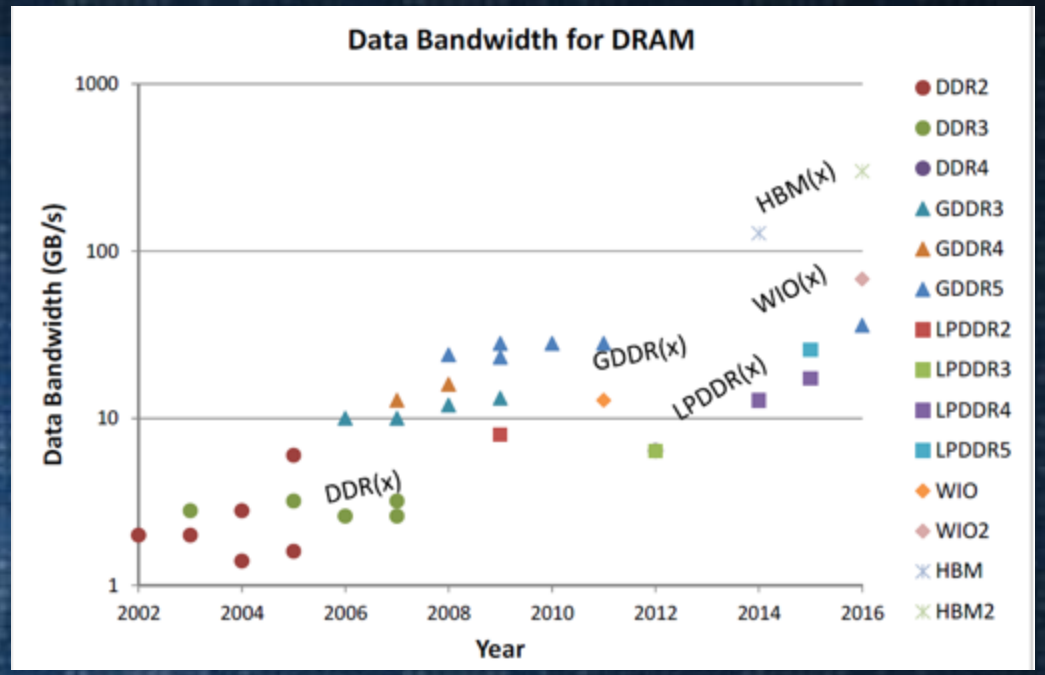
June 3-6, 2018

Overview

- Device Trend and Challenge
- Goal of study
- Design and realization for high current capacity
- Experiment and result in manufacturing field
- Summary

DRAM Device Trend

- **Higher performance device**
  - EDP : DDR3 → DDR4 → DDR5
  - Graphic : GDDR4 → GDDR5 → GDDR6
  - Mobile : LPDDR3 → LPDDR4 → LPDDR5
  - Density : 6G → 8G → 16G
- **Higher current consumption**
  - GDDR 6, High Bandwidth Memory (HBM)
  - Requiring high current test INFRA
- **Lower pin per DUT for maximum parallelism**
  - As test parallelism increases, number of pins for DUT decreases
  - It is connected a number of PWR/GND pins



What is probe burnt ?

- **Over current causes probe burnt**
  - Energies resulting from high current may result in high temperatures at probe
  - Probe burnt causes tip burnt and beam depress
- **Burning of the tip can be prevented by cleaning solutions**
  - Cleaning method
  - Cleaning period
  - Needle polishing materials
- **How to prevent probe beam depress?**
  - Current? / Voltage?
  - Device makers don’t want to change device test condition

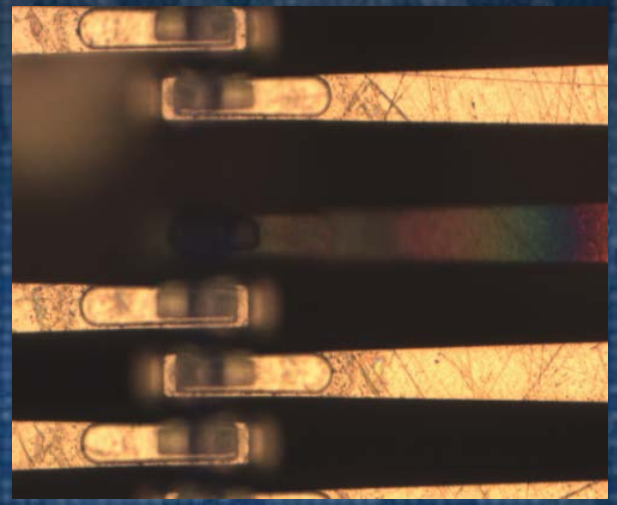
Side effects of beam depress

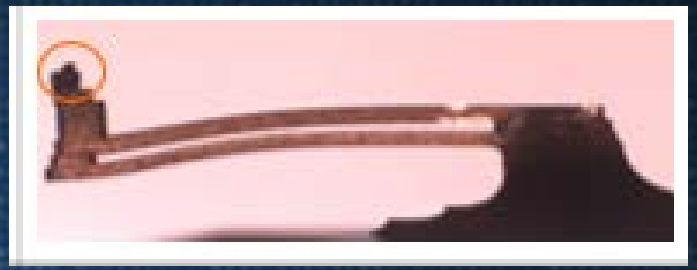
Current ↑

Temperature ↑

Strength
Yield point ↓

Plastic
Deformation

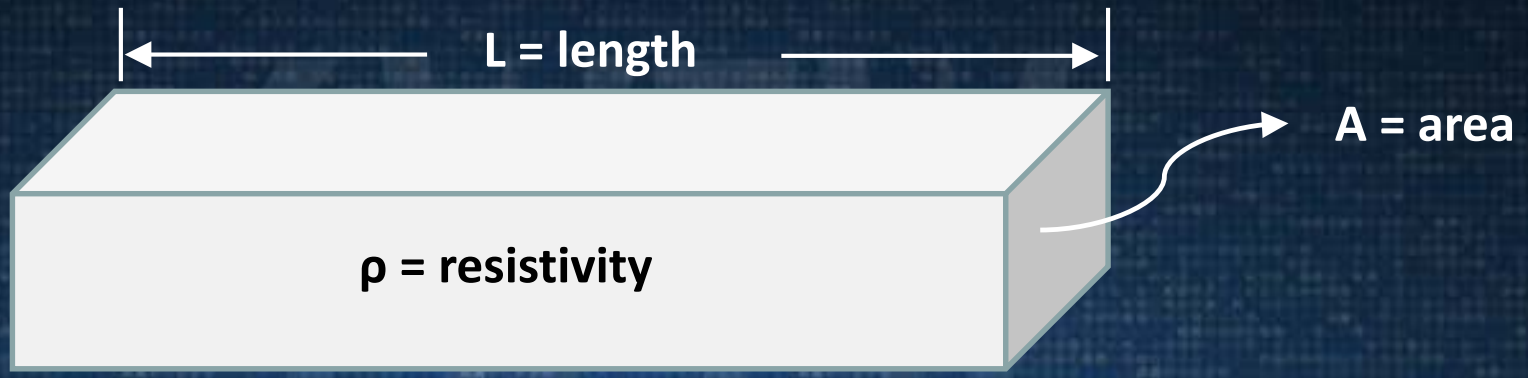




- **Depressed probes cause**
  - High contact resistance
  - Malposition of scrub marks
  - Yield loss

Current carrying capacity & Resistance

$$R = \rho \frac{L}{A}$$



- **For increasing C.C.C of probe**
  - Decreasing resistance of probe
- **For reducing resistance**
  - Low resistivity material → It requires material of probe is changed
  - Enlargement of A (Cross section)
  - Shorten length

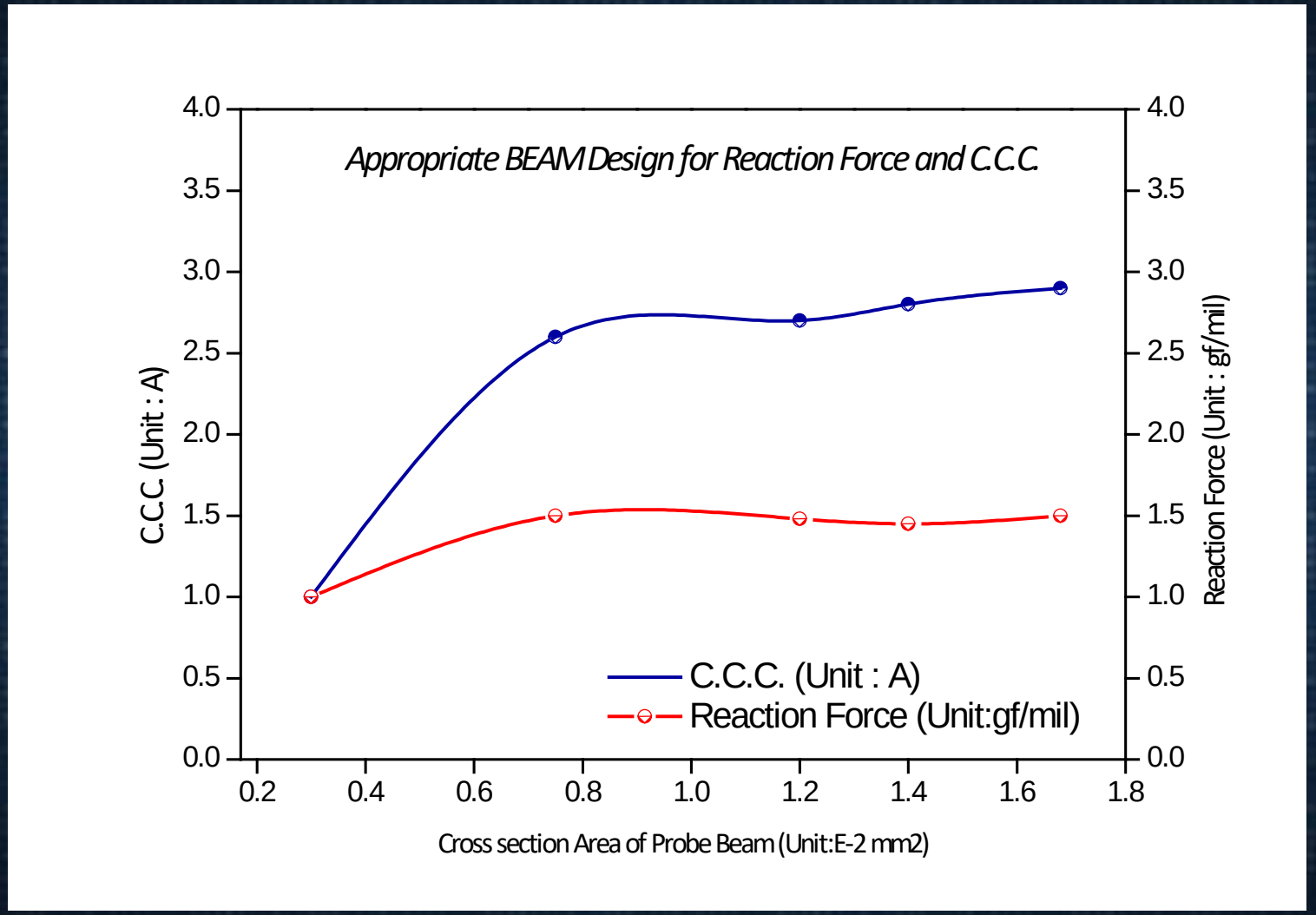
Bi-furcated structure

- **C.C.C Maximized Structure**

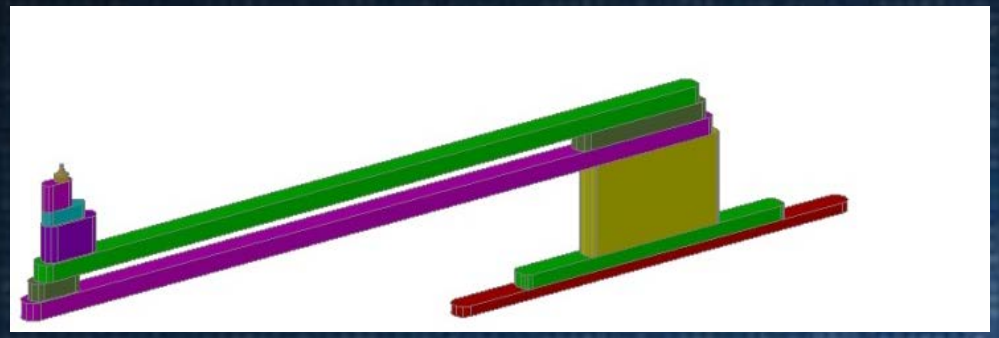


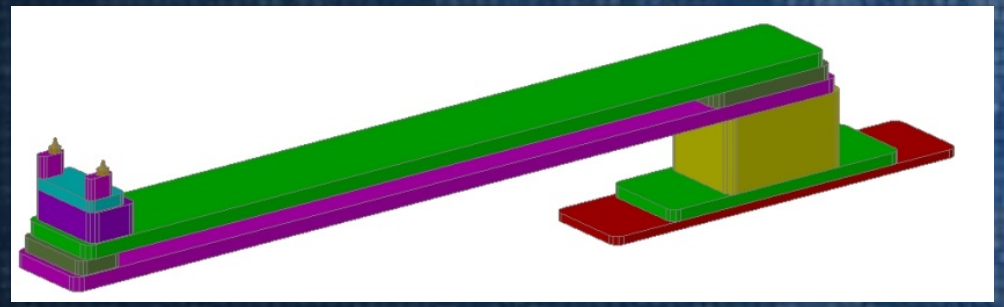
  - As section area widened, C.C.C increases
  - **But, it has side effects of increased reaction force**
- **Requirement**
  - **Correlation between C.C.C and reaction force**
  - ***In order to balance other probes, we have to adjust reaction force of the probe.***
  - ***When Pad lay out is designed, power pads must be designed to be adjacent.***

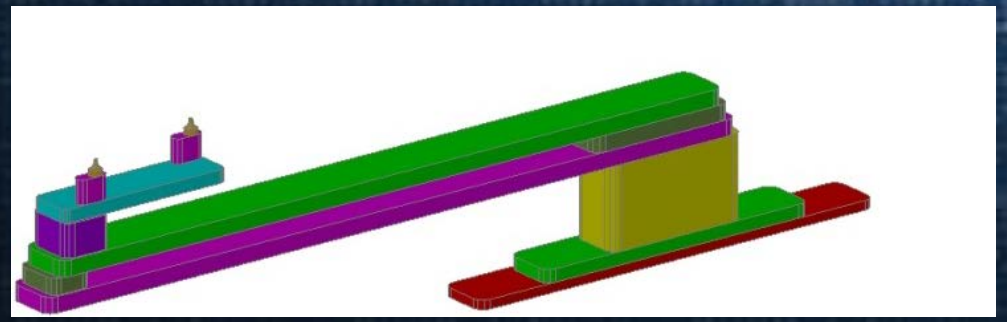
Correlation between C.C.C and Reaction force



Design & simulation probes





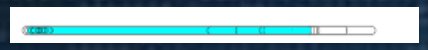
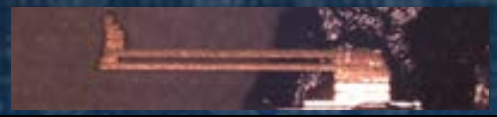
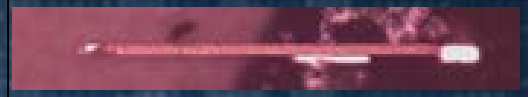
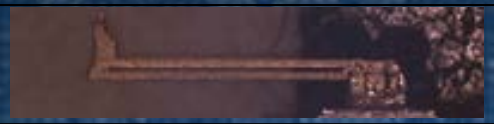
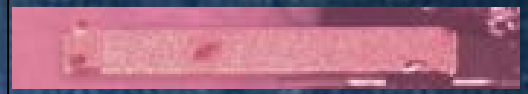
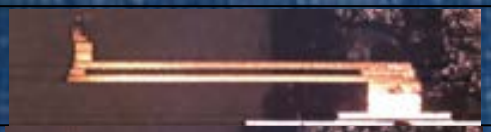
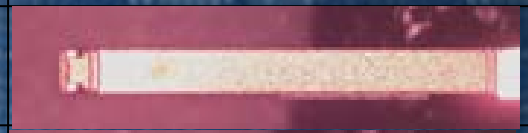
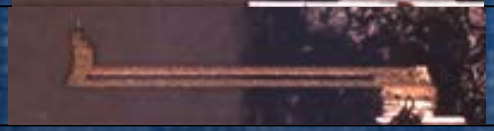
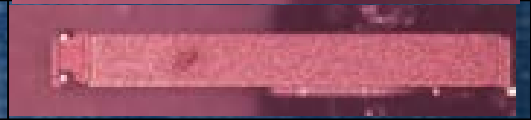
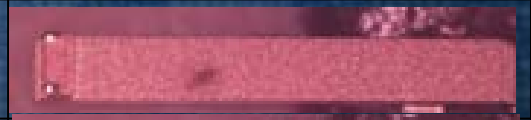
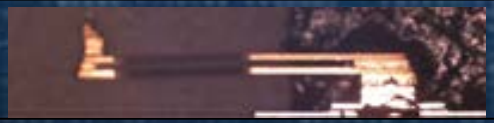
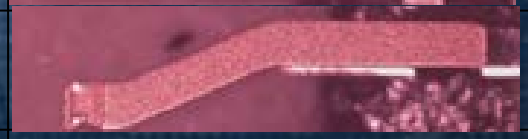
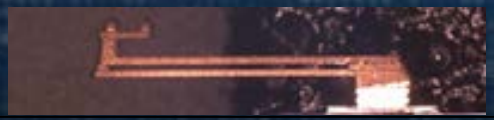
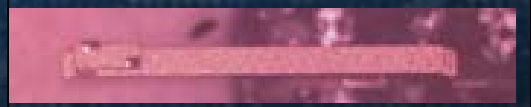
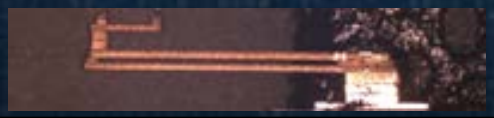
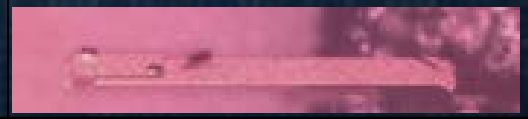


Normal MEMS Probe
Reaction force = F_n
C.C.C = I_n

Bi-furcated MEMS Probe 1
Reaction force = F_{b1} × 3.6
C.C.C = I_n × 3.3

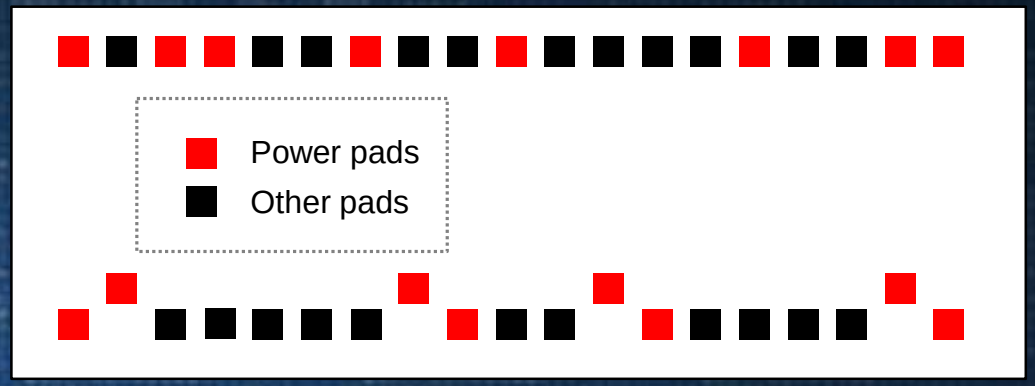
Bi-furcated MEMS Probe 2
Reaction force = F_{b2} × 2.6
C.C.C = I_n × 2.67

Design & simulation probes

	No.	Shape	Side View (실제 Image)	Top View (실제 Image)	BEAM Length (㎛)	BEAM Width (㎛)	Force (Sim)
Single PROBE	1				1961㎛	60㎛	1.08gf/mil
Bifurcated PROBE Type 1	2				2117㎛	240㎛	3.34gf/mil
	3				2370㎛	240㎛	2.13gf/mil
	4				2470㎛	280㎛	2.13gf/mil
	5				2590㎛	336㎛	2.13gf/mil
	6				2265㎛	240㎛	2.13gf/mil
2열 Bifurcated PROBE₩ Type 2	7				2117㎛	150㎛	2.15gf/mil
	8				2117㎛	150㎛	2.1gf/mil

Design pads lay-out

- **Power pads rearrange**
  - Rearrange power pads which require high current
    - One of power pad next to another power pad
  - Matching the number of top/bottom power pads



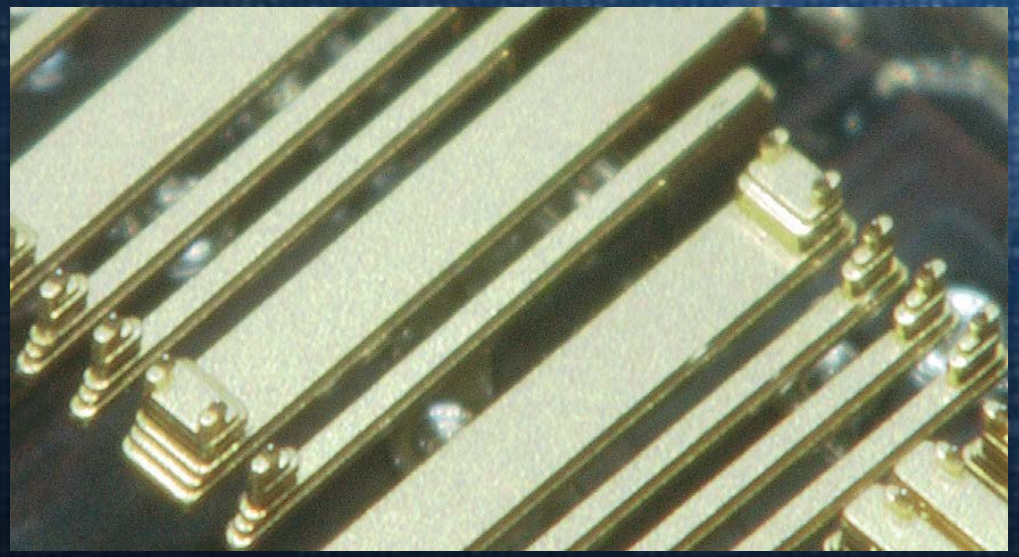
- **Total probe force balance**

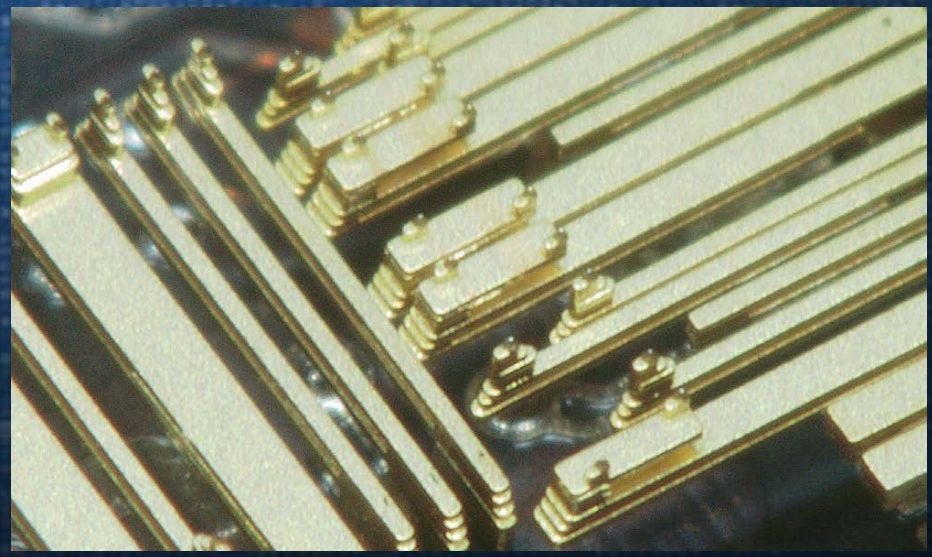
Σ Force of upward direction probes

Σ Force of downward direction probes

Probe fabrication

- **Bi furcated probe array realization using 3-D MEMS process**
  - Probe array realization for DRAM device
  - 31,000 pins per probe card
  - 3 types of bi furcated probes are mixed in 1 DUT



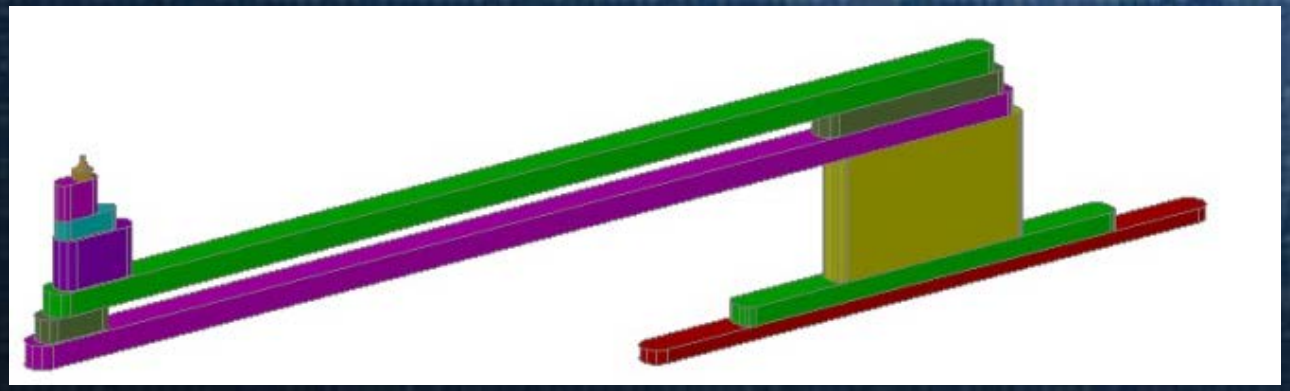


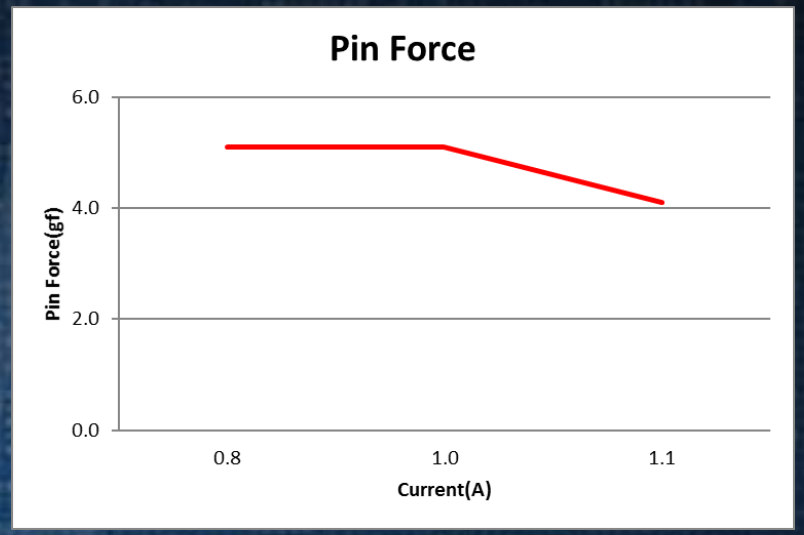
Performance evaluation

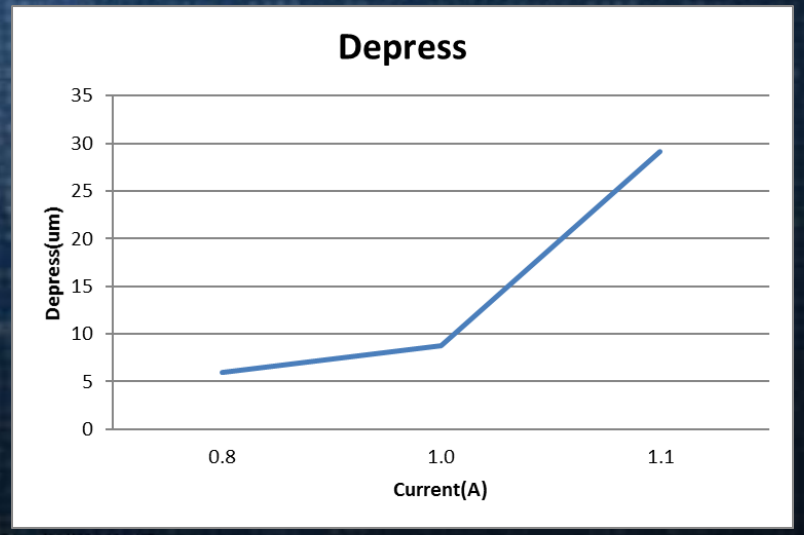
- **Measurement parameter**
  - C.C.C of probe
  - Reaction force of probe
  - Depress (㎛)
- **Test condition**
  - Temperature : 100 ℃
  - Current applied for 1 hour at contact condition
  - Increase the current by 200mA every 1 hour
  - Measure depress & reaction force
- **Failure condition**
  - When the probe depress over 25㎛
  - When reaction force is reduced more than 15%

Evaluation (Normal Probe)

Current	Depress	Pin Force(gf)		Reduction rate
		Before applying current	After applying current	
0.8	6	5.2	5.1	2%
1.0	9	5.2	5.1	2%
1.1	**29**	**5.2**	**4.1**	**21%**

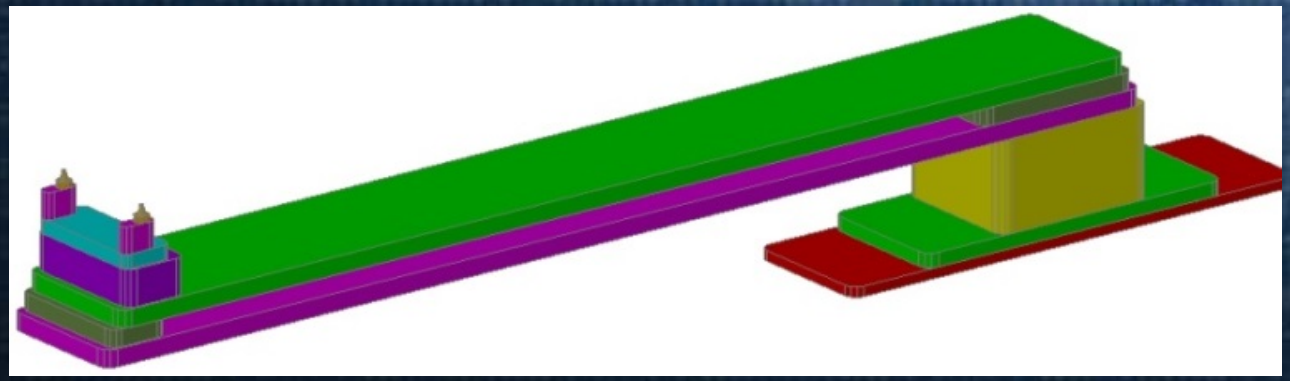


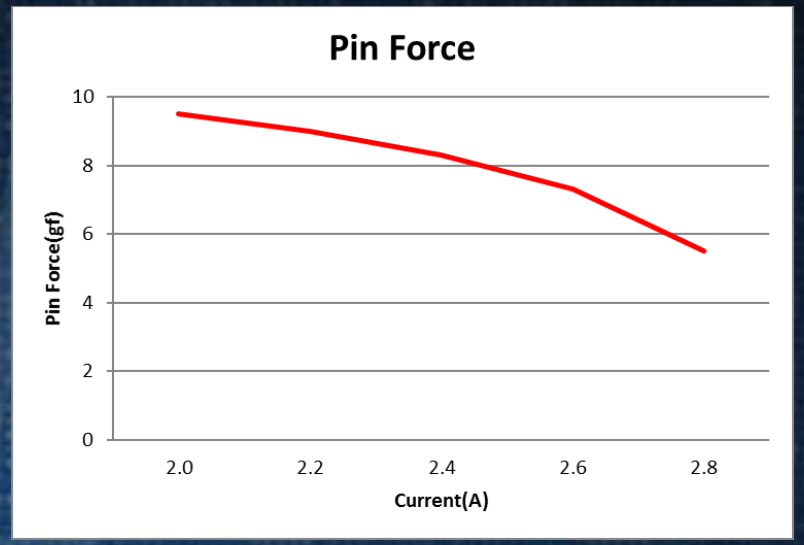


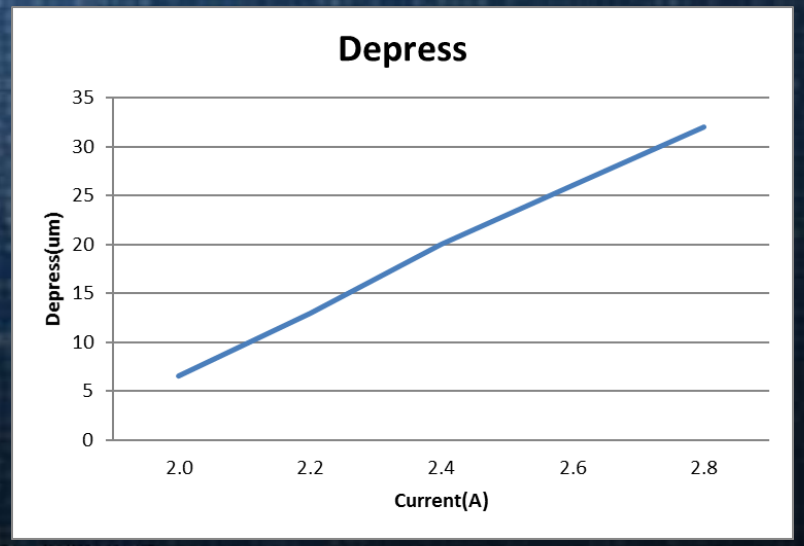


Evaluation (type 1)

Current	Depress	Pin Force(gf)		Reduction rate
		Before applying current	After applying current	
2.0	6.5	10	9.5	5%
2.2	13	10	9	10%
2.4	**20**	**10**	**8.3**	**17%**
2.6	26	10	7.3	27%
2.8	32	10	5.5	45%

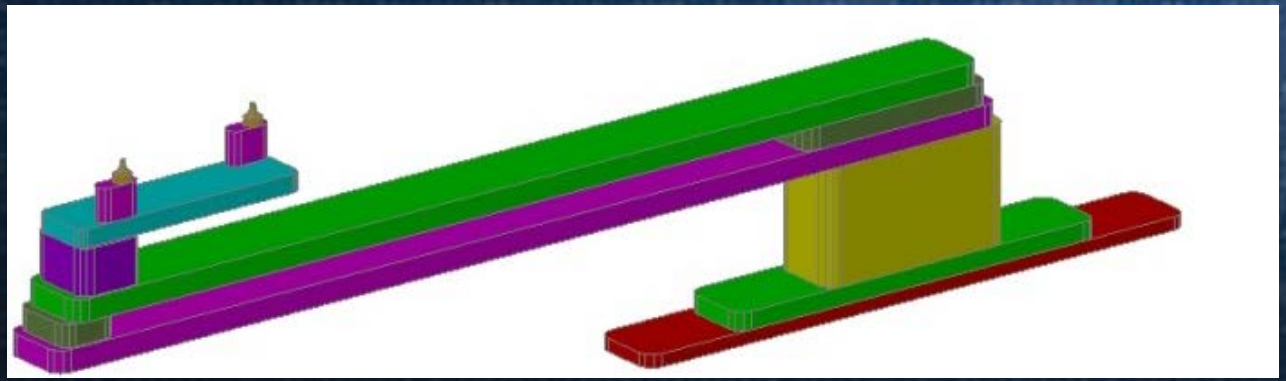


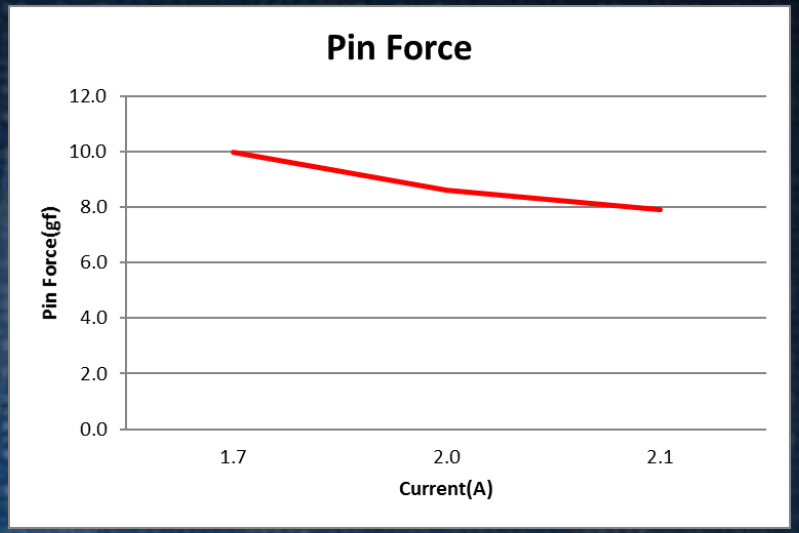


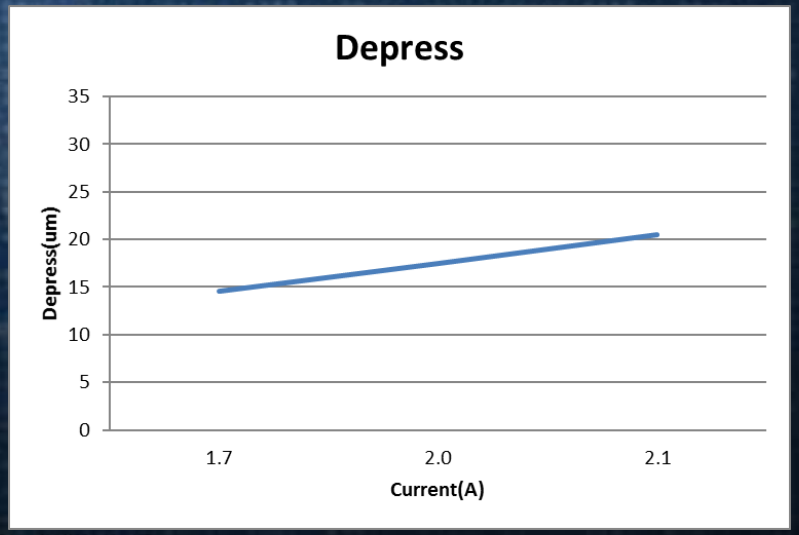


Evaluation (type 2)

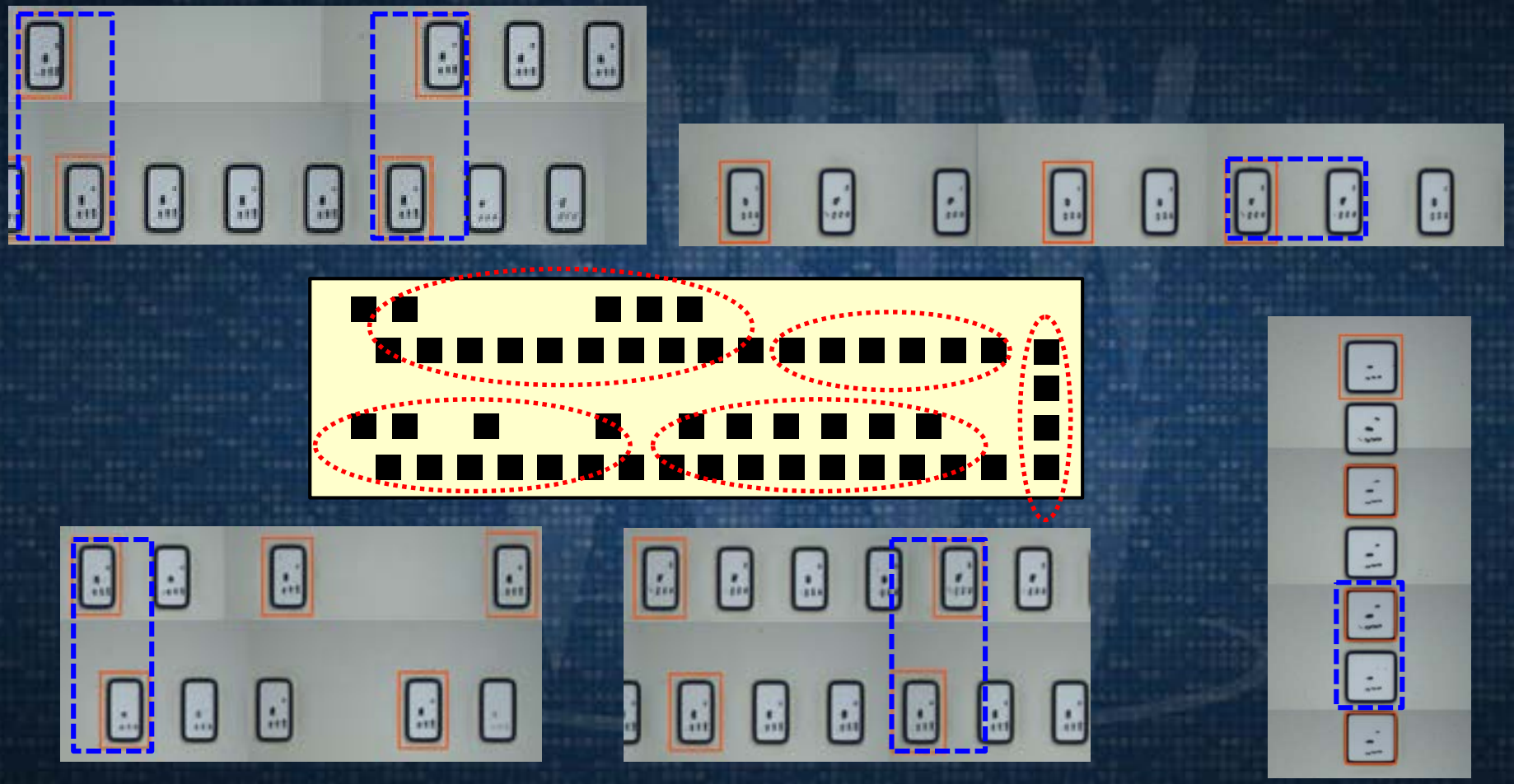
Current	Depress	Pin Force(gf)		Reduction rate
		Before applying current	After applying current	
1.7	15	10	10.0	0%
2.0	18	10	8.6	14%
2.1	**21**	**10**	**7.9**	**21%**



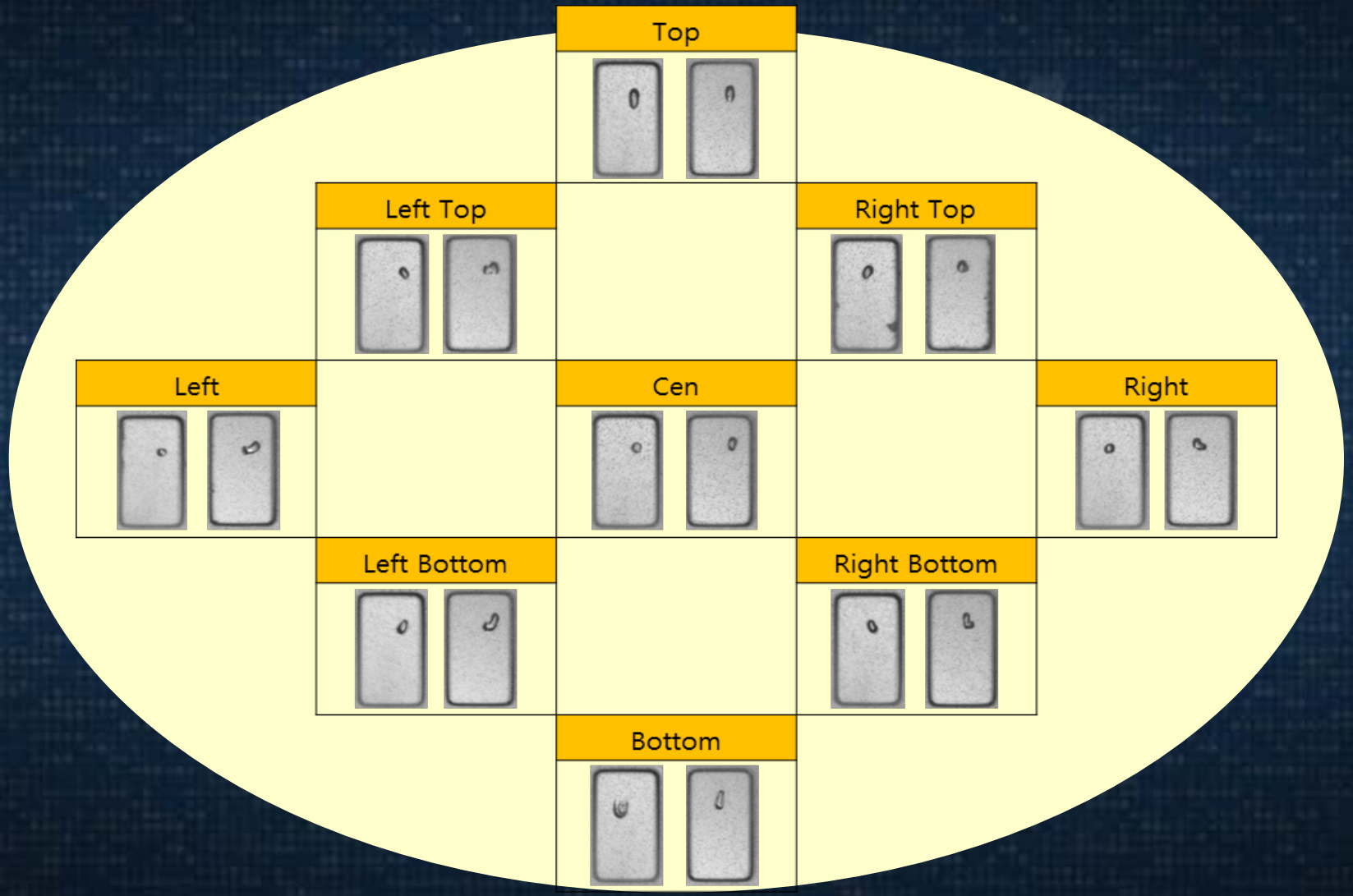




Field test (DUT)



Field test (Wafer)



Summary

- **Memory devices require high current INFRA for wafer testing**
- **New probe using bi furcated structure improves its C.C.C**
- **To balance contact force, it needs to optimize pad lay-out**
  (including pads position and number)
- **It is available to apply new probe for mass production line**

Thanks for your Support !



- Je-Young Park
- Sang-Kyu Yoo
- Yu-Gyeom Kim



- Yong-Ho Cho
- Tae-Kyun Kim

SW Test Workshop

Semiconductor Wafer Test Workshop

2-0-1-8

Advanced cantilever probes showing similar advantages as their vertical opponent

Franz Steger (TI)

June 3-6, 2018

SW Test Podium Presentation Flow

- Drive / Motivation
- Key Parameters
- Setup
- First results
- Long term study
- Summary / Conclusion
- Acknowledgement

Drive / Motivation

- Low Pin count products (<100 pins)
- Old testers (>20 years) using 2” probe card
- Low performance of available Cantilever technologies (lifetime, contact stability, probe mark size, Al swarf/stringers, …)
- High manual effort (maintain, set up, interruptions)
- Other available technologies not suiting
- Standardization

Key parameters of the probes

Standard Cantilever

- ~15 mil length
- Flat tip
  ➔ Large scrub mark
- 1.9 g per mil OT
- Tungsten (+ Rhenium)

JEM XP5

- ~25 mil length
- Round tip shape
  ➔ small scrub mark
- 1.1 g at max. OT (90um)
- Material ‘XP5’

Technoprobe Canti3

- ~25 mil length
- Round tip shape
  ➔ small scrub mark
- 0.9g at max. OT (80um)
- Material LCR2 (same as vertical)

Setup up

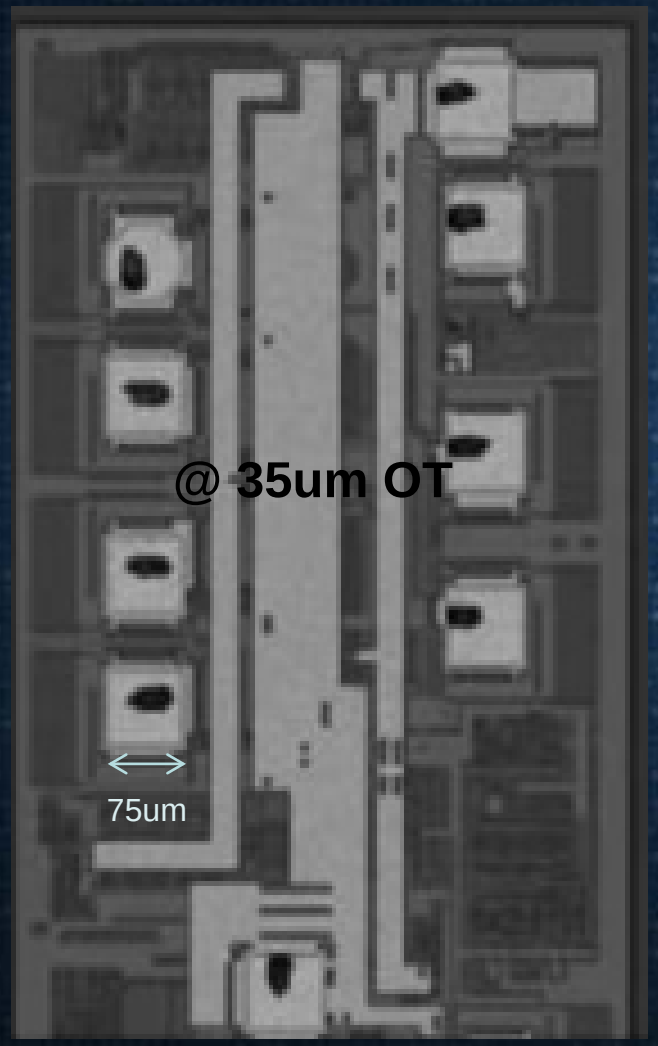
- **Prober: TSK UF200**
  - Standard 50mm cleaning block
- **Online Cleaning**
  - MIPOX WA6000 SWE
    (if you want your needle tips behave like a vertical, treat it like one)
- **Test**
  - Currents up to 200mA per pin

First results

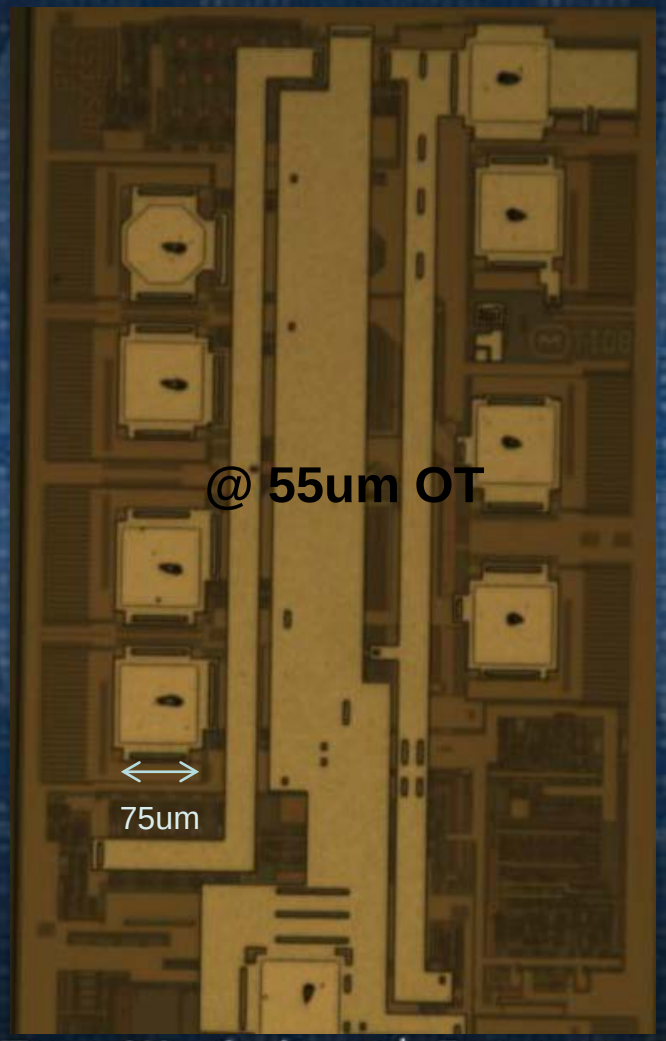
- Corresponding probe marks
- Cracks below bond pad
- Needle shapes
- Electrical Contact
- Probe yield comparison

Corresponding Probe Marks

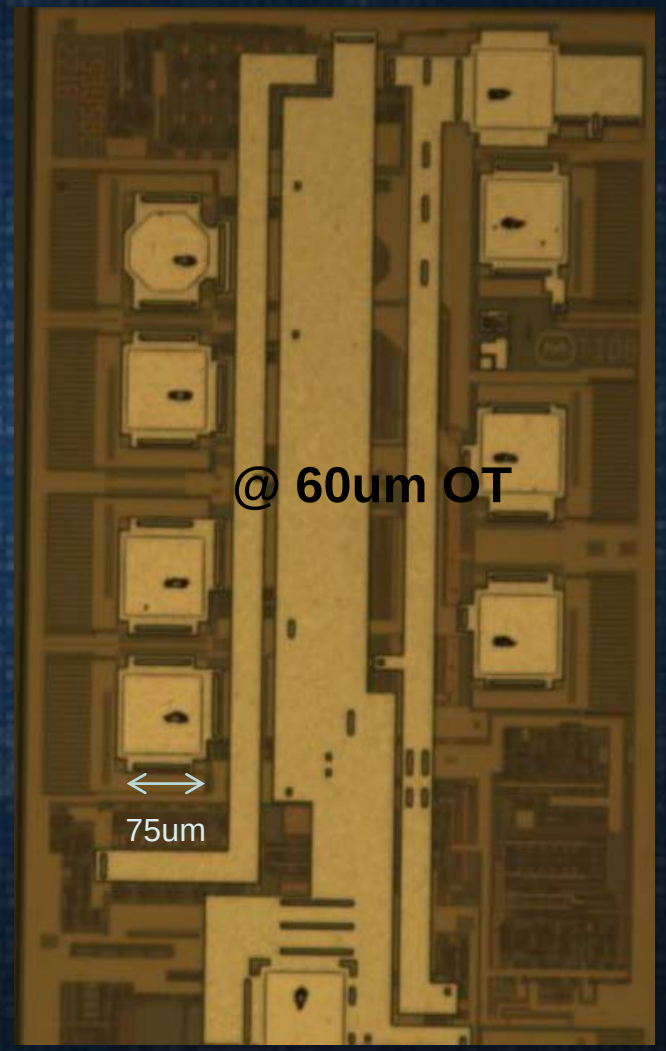
Std. Canti.



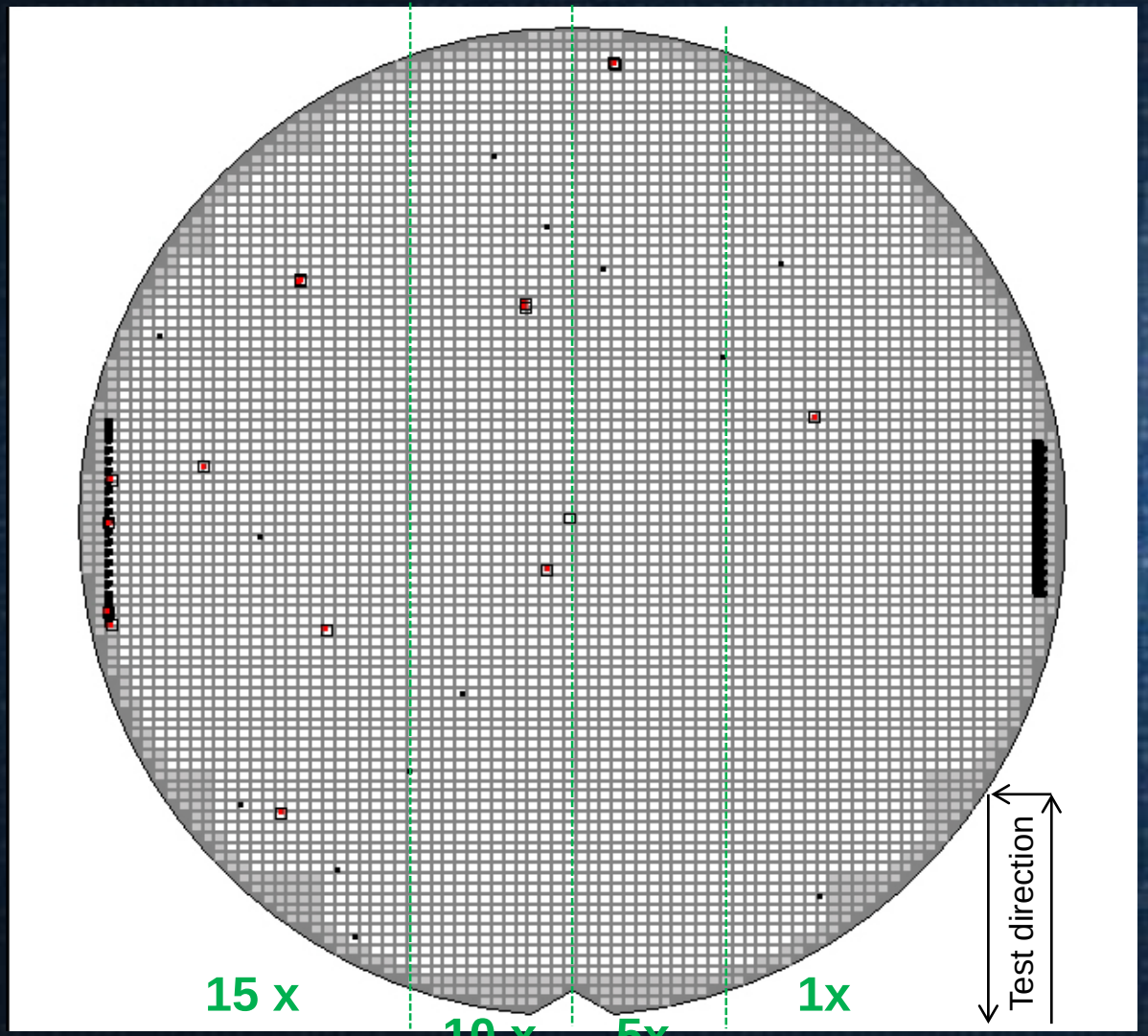
Canti 3

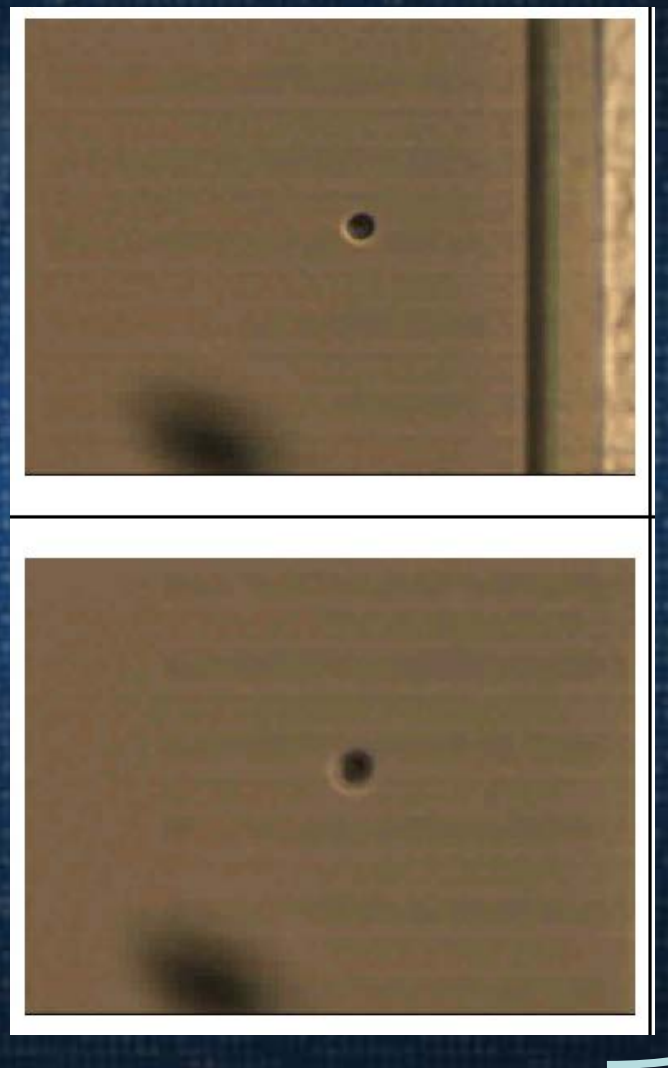


XP5



Cracks below bondpad



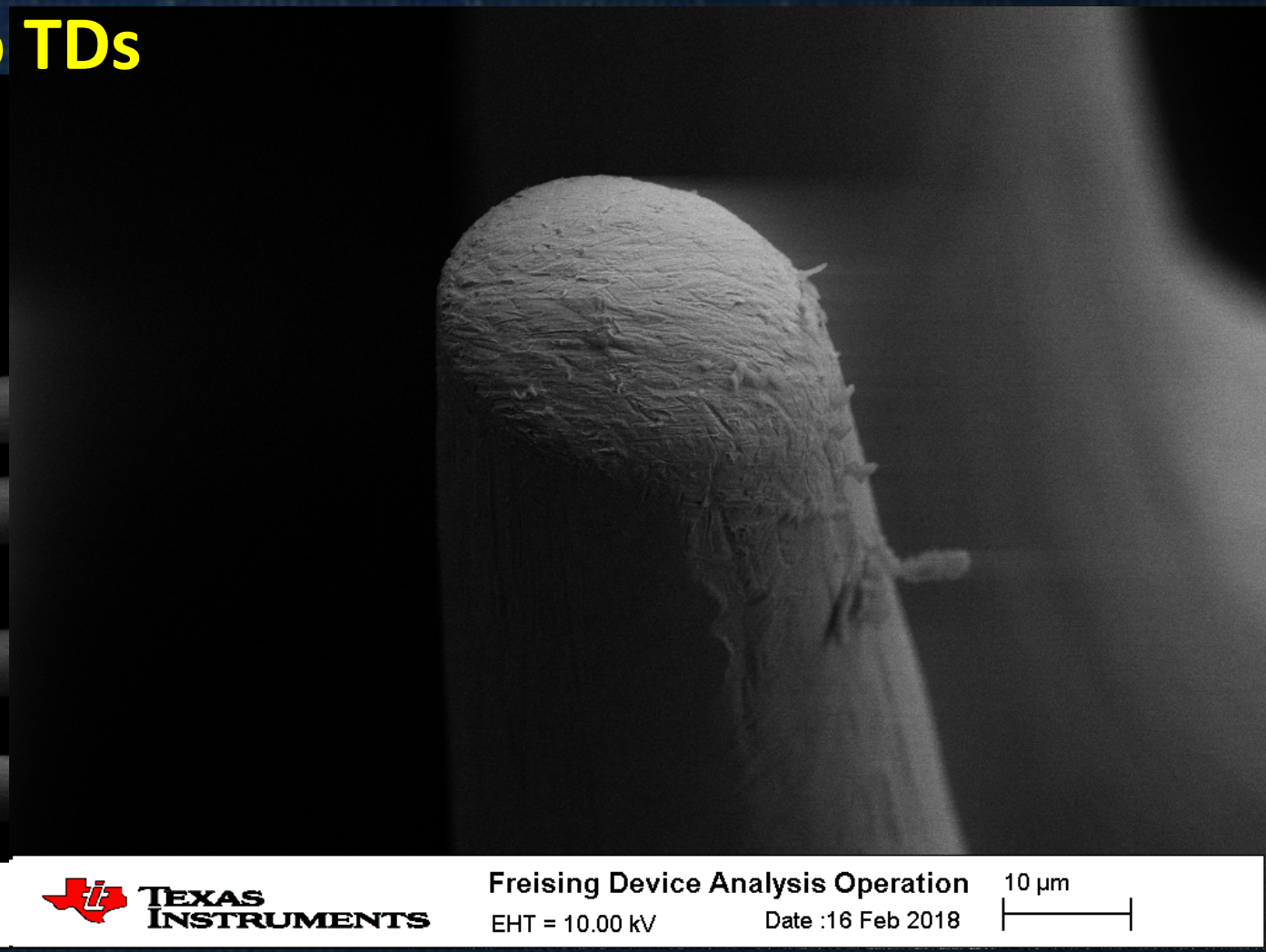


No Cracking found for both technologies

Needle Shape

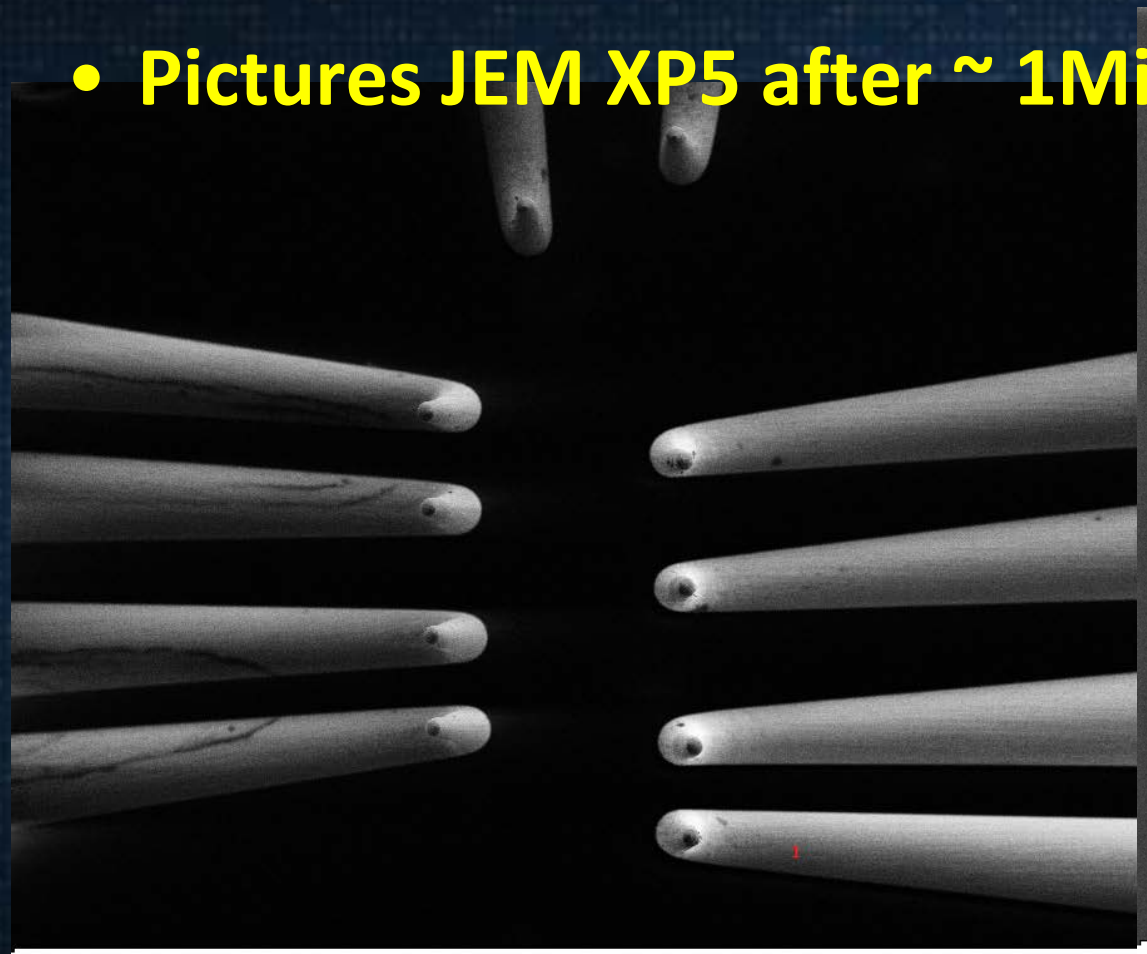
- Pictures Canti3 after ~ 1Mio TDs

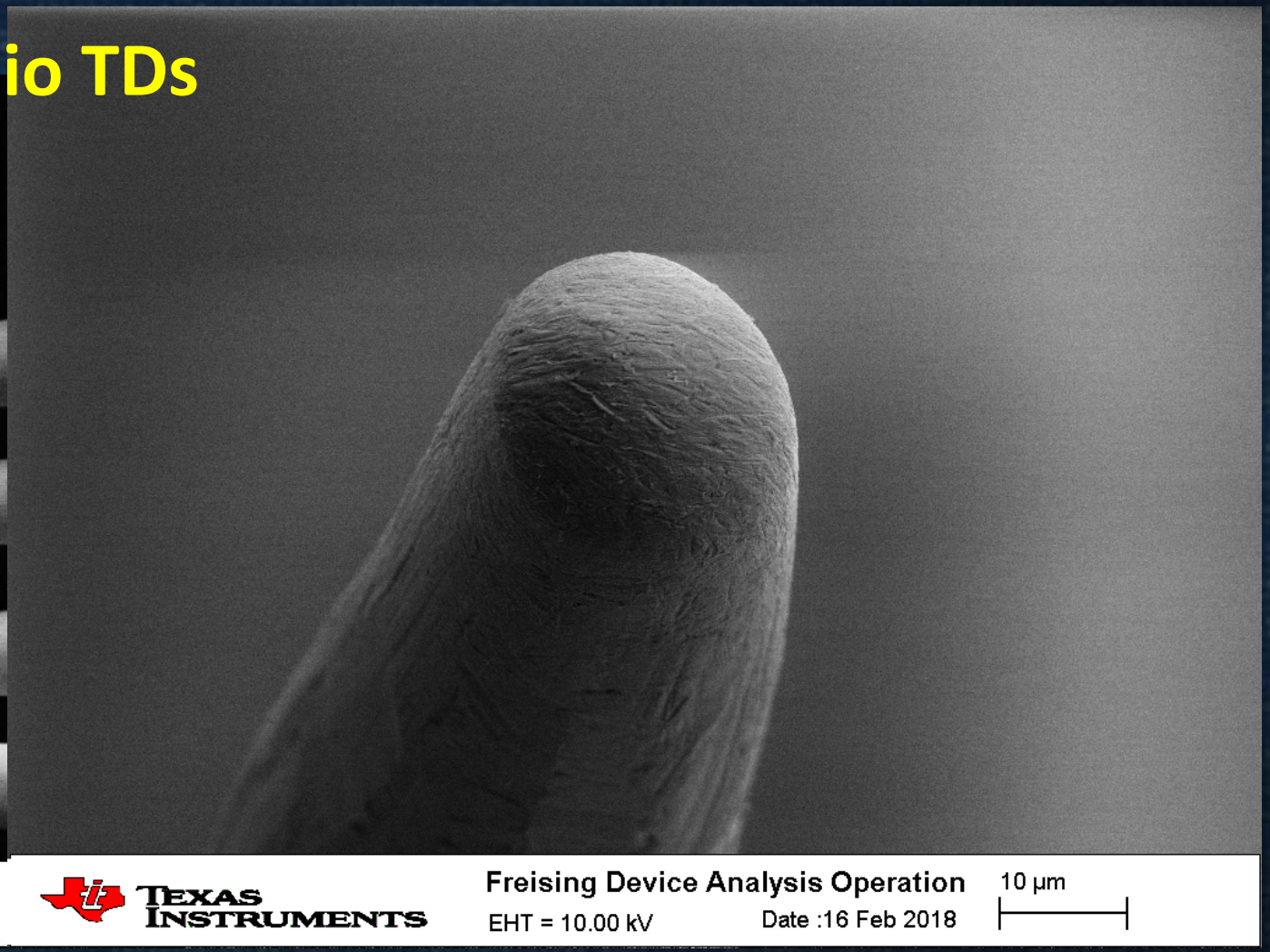




Needle Shape

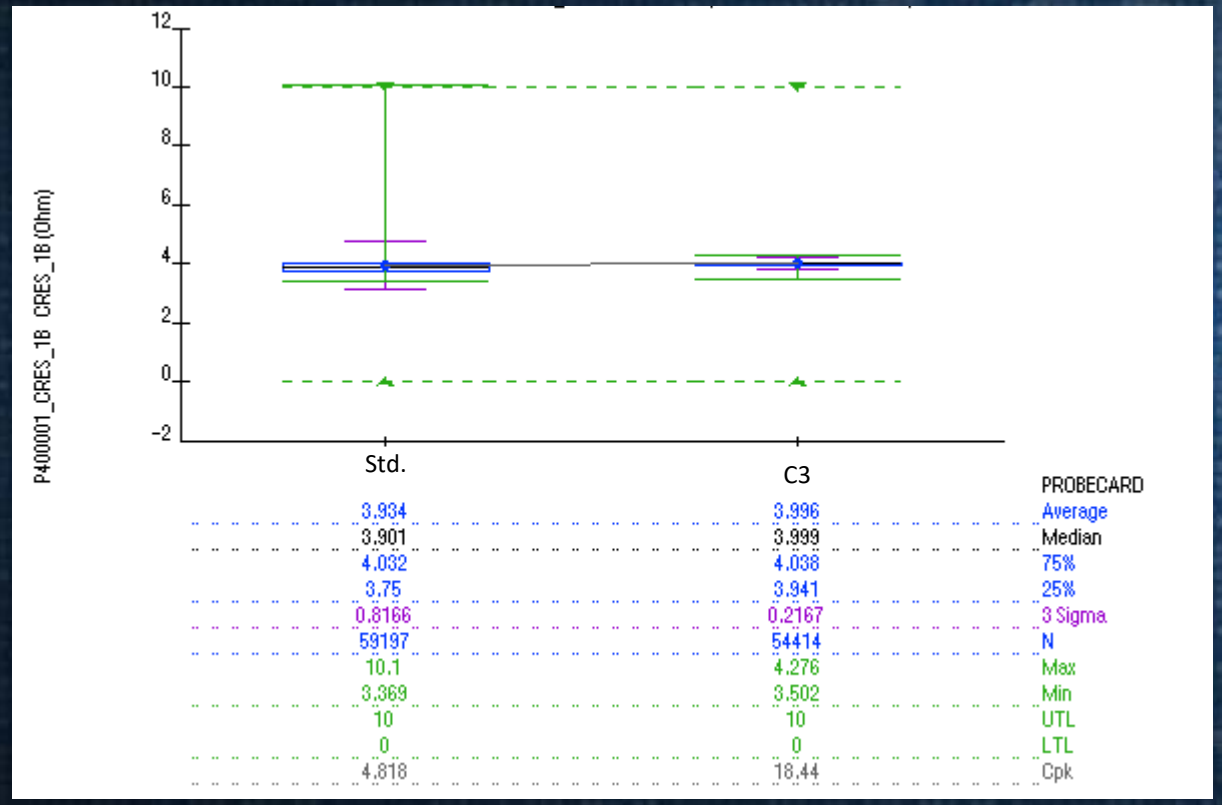
- Pictures JEM XP5 after ~ 1Mio TDs



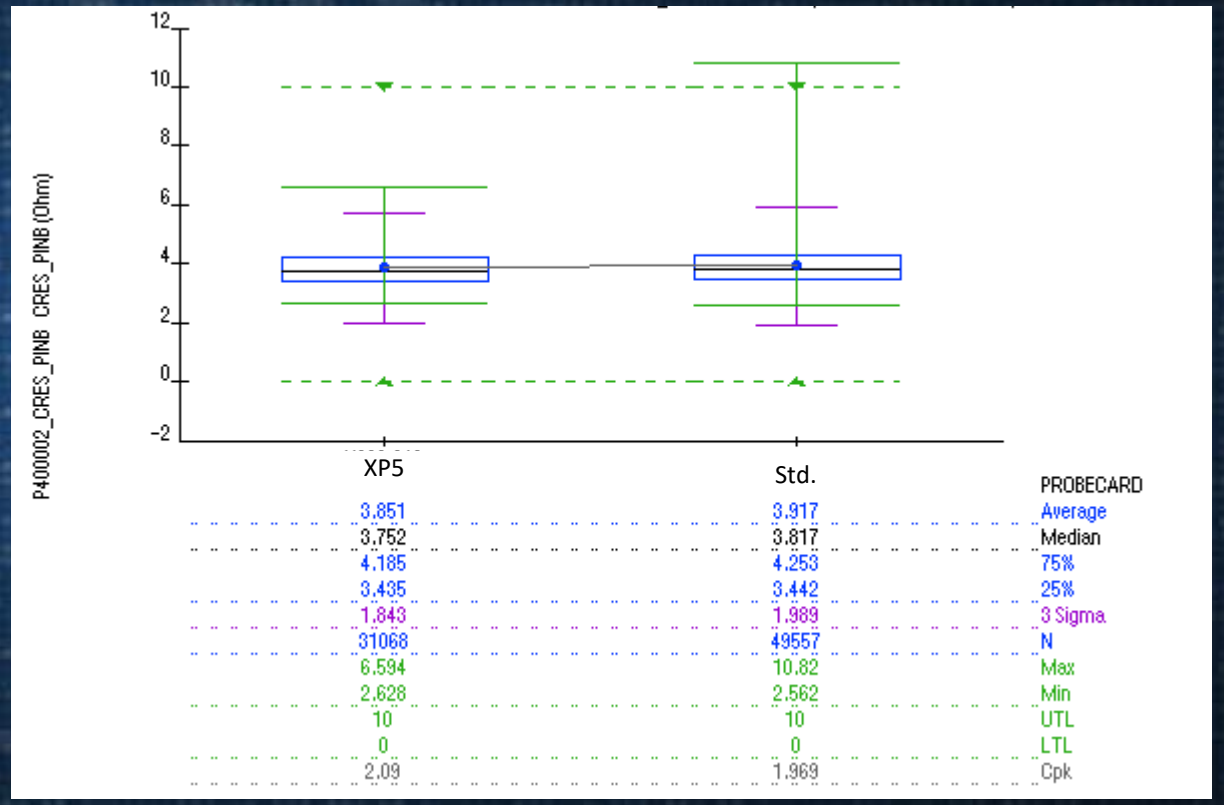


Electrical contact

Standard Cantilever vs. Canti3

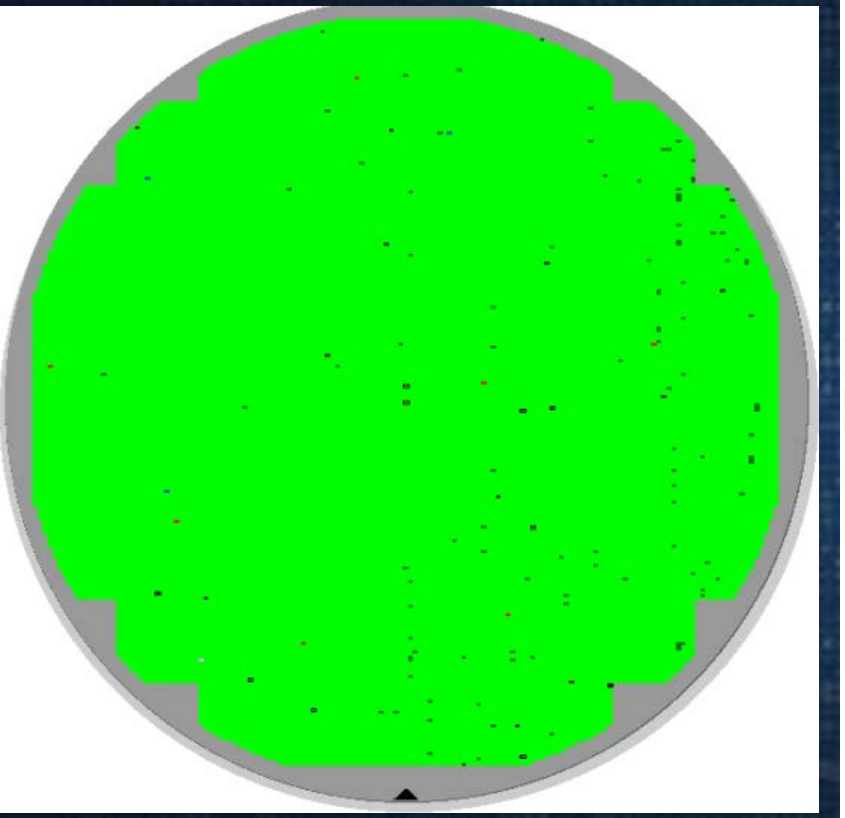


JEM XP5 vs. std. Cantilever



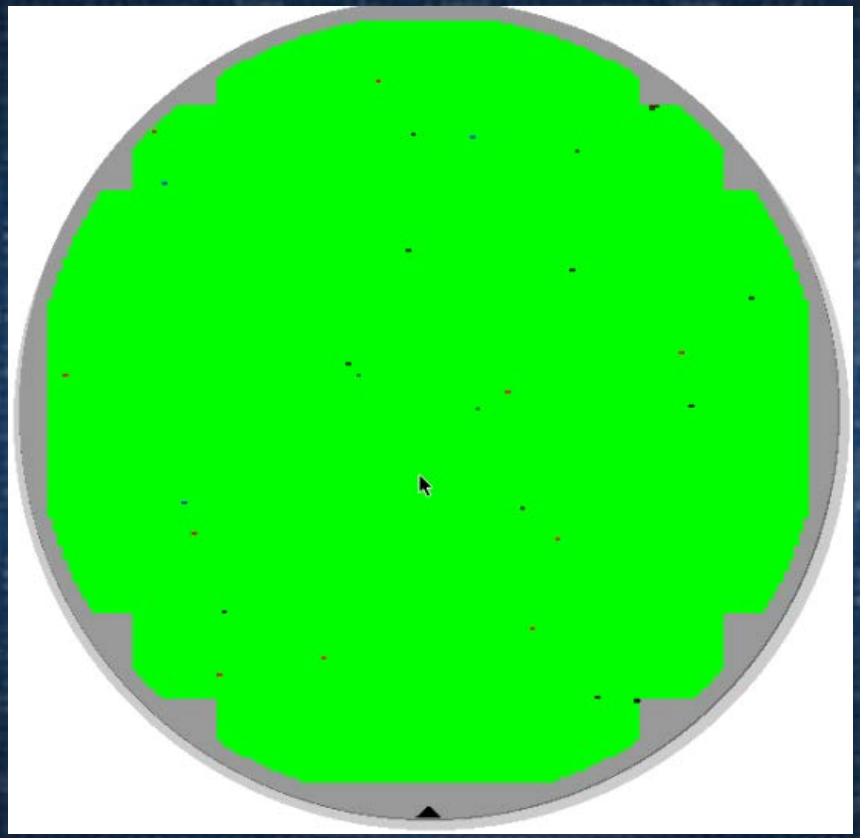
Probe Yield compare

Std. Canti
@45um OT



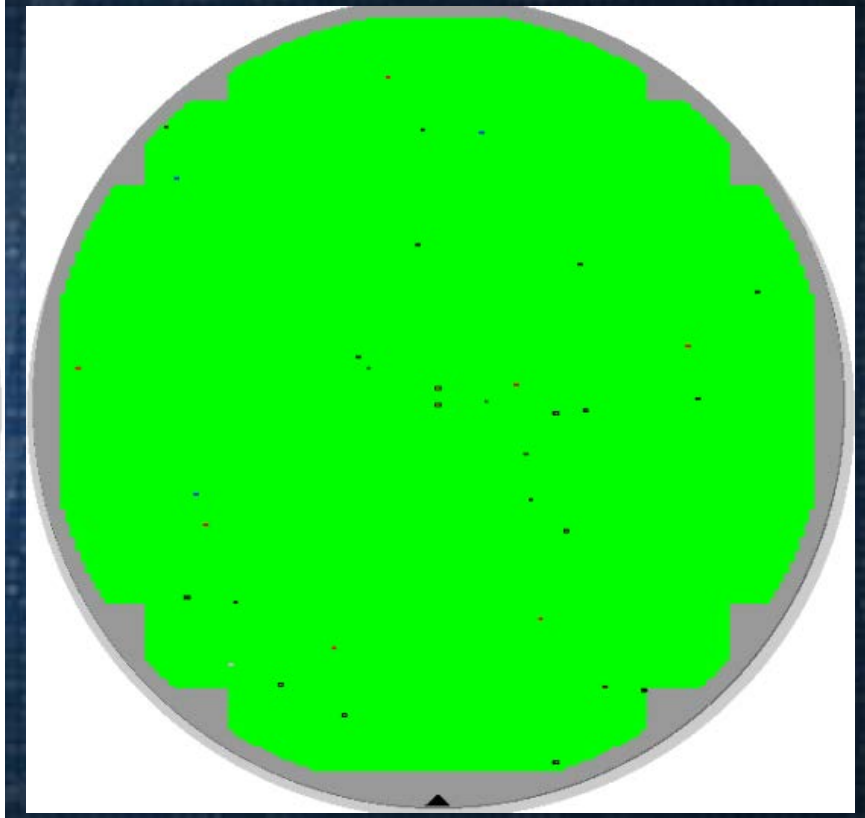
99.60%
Optical Loss: 400 units

CANTI3
@35um OT



99.92%
Optical Loss: 100 units

JEM XP5
@35um OT`

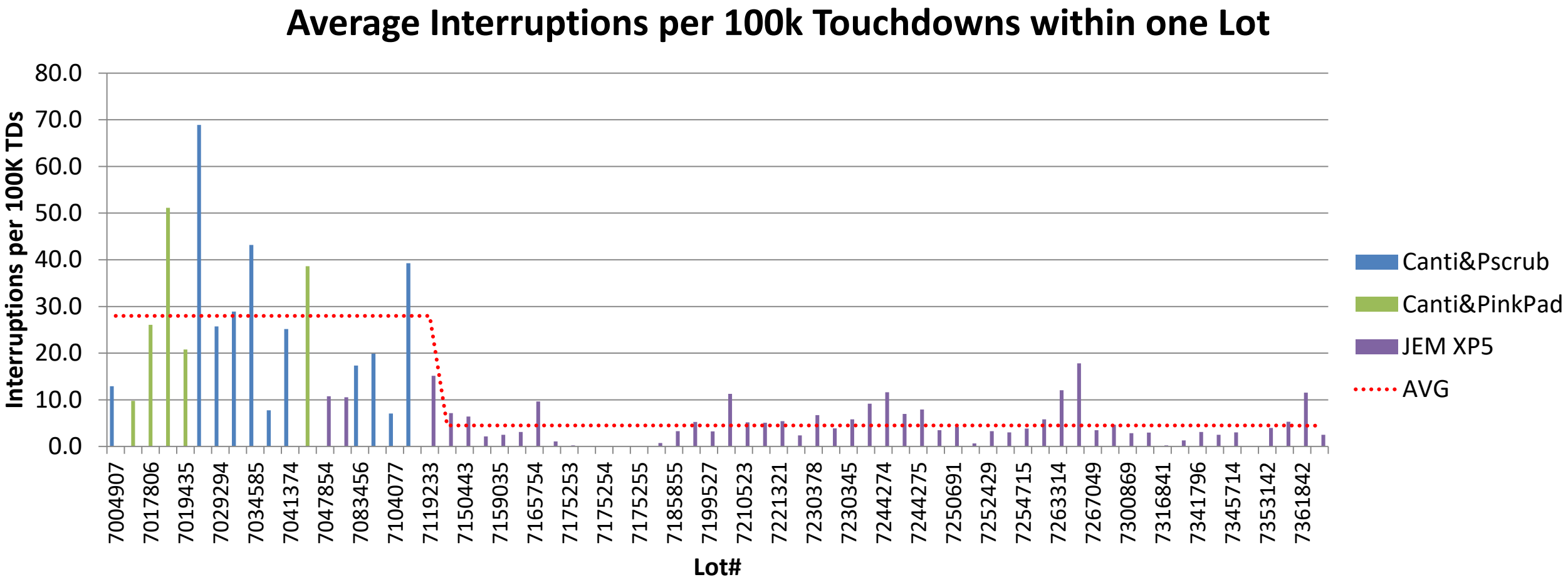


99.93%
Optical Loss: 120 units

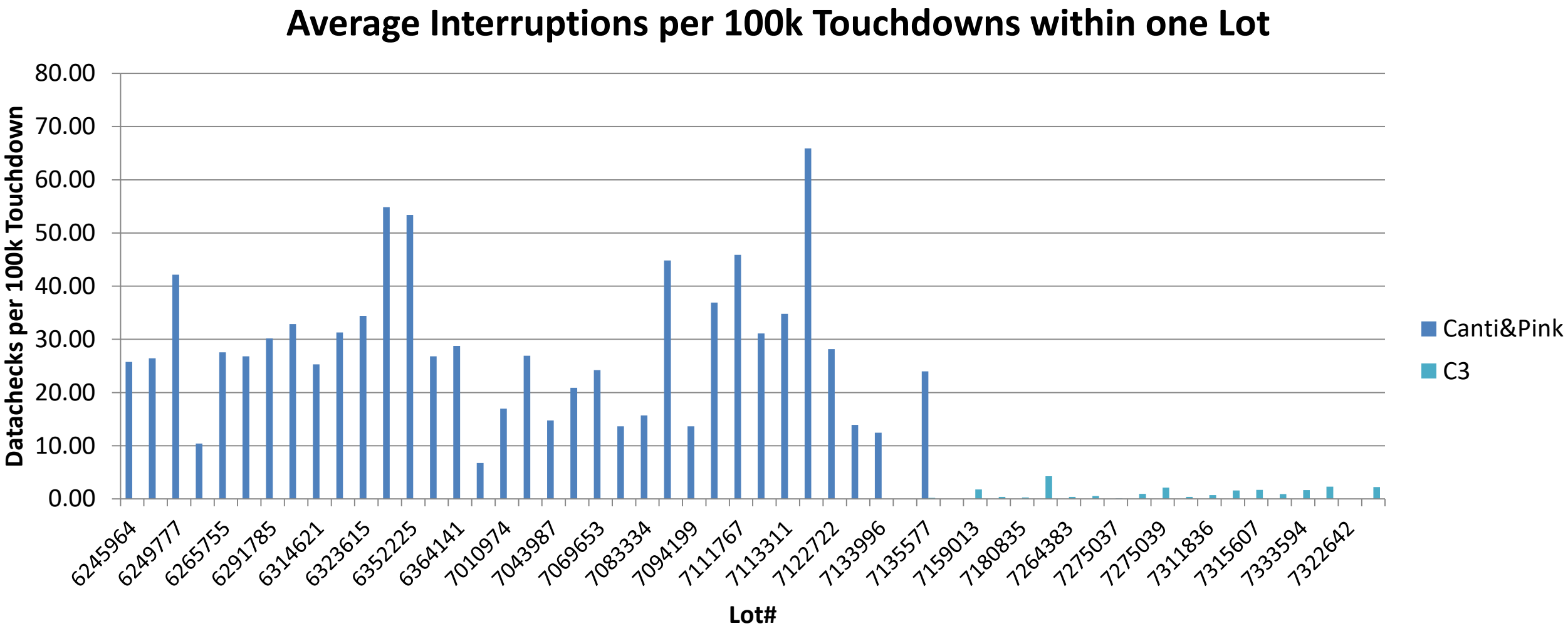
Long term study

- **Production Interruption**
  - Cantilever vs. JEM XP5
  - Cantilever vs. Techoprobe Canti 3
- **Life time**
  - JEM XP5
  - Techoprobe Canti 3

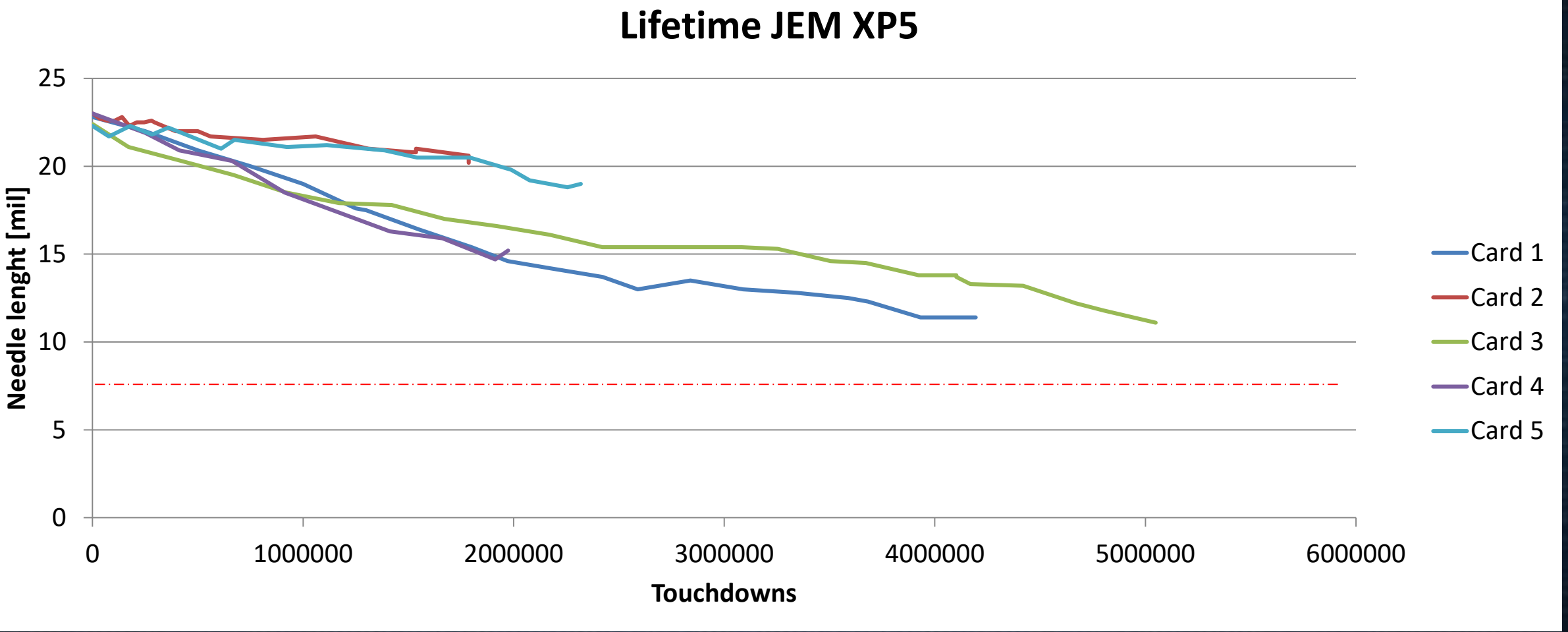
Production interruptions



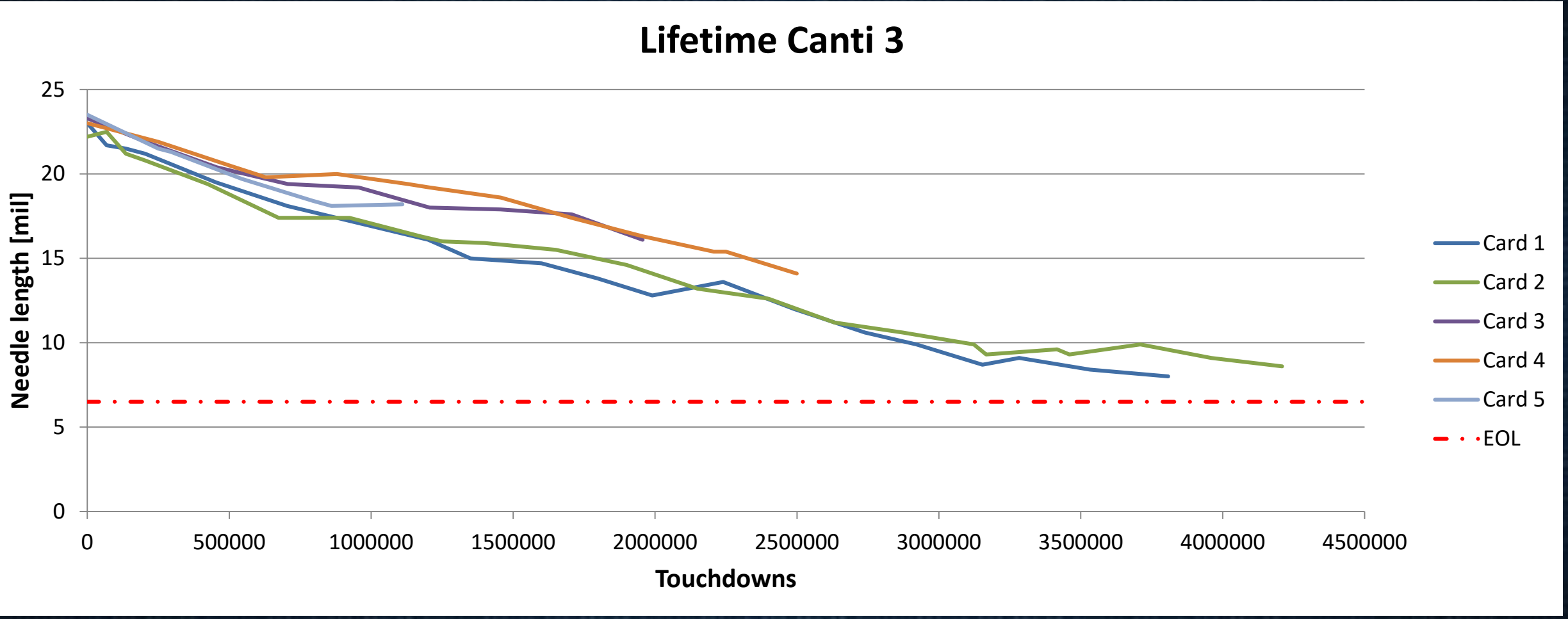
Production interruptions



Life time


Lifetime JEM XP5
Needle lenght [mil]
25
20
15
10
5
0
0
1000000
2000000
3000000
4000000
5000000
6000000
Touchdowns
Card 1
Card 2
Card 3
Card 4
Card 5

Life time


Lifetime Canti 3
Needle length [mil]
25
20
15
10
5
0
0
500000
1000000
1500000
2000000
2500000
3000000
3500000
4000000
4500000
Touchdowns
Card 1
Card 2
Card 3
Card 4
Card 5
EOL

Summary & Conclusion

- **Both solution superior to standard cantilever**

Category	Technoprobe Canti 3	JEM XP5
Mechanical stability	Slightly weaker	Slightly harder
Lifetime	~ 4 mio +	~6.5 mio +
Contact resistance	Most stable, slight offset	Lower and also very stable
Scrub mark	Close to vertical	
Cost (*)	2x	4x

Very contact sensitive products…

Very high volume products

(*) compared to std. cantilever. For >100 pins cost get even closer to cantilever std.

Acknowledgement

Special thanks to

- **JEM (Japan Electronic Material) Europe:**
  - Joe Mai
  - Sébastien Perino
  - Sabine Plousey
- **Technoprobe Italy**
  - Alessandro Antonioli
  - Sara Vergani
  - Riccardo Vettori
- **Texas Instruments Freising**
  - Andreas Meissner
  - Michael Janssen
  - Werner Huber
  - Fromund Metz
  - Helmut Rinck
  - Dr. Friedrich Taenzler

SW Test Workshop
Semiconductor Wafer Test Workshop
2-0-1-8

Probe Card Test Solution for 5th Generation Mobile Communications



Norman
Chunghwa Precision Test Tech

June 3-6, 2018

Outline

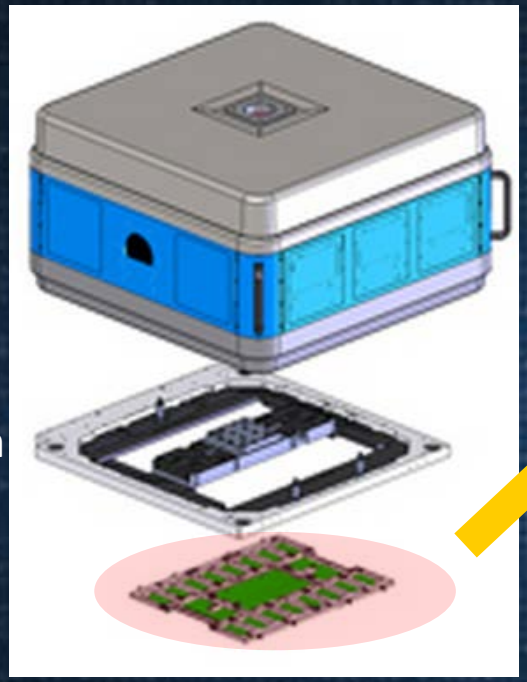
- Probe Card Test Solutions
- Pogo Pin Design for 28GHz Application
- The Loss Factors of T-Line & DK/DF Extraction
- Measurement and Simulation Correlation
- Conclusion

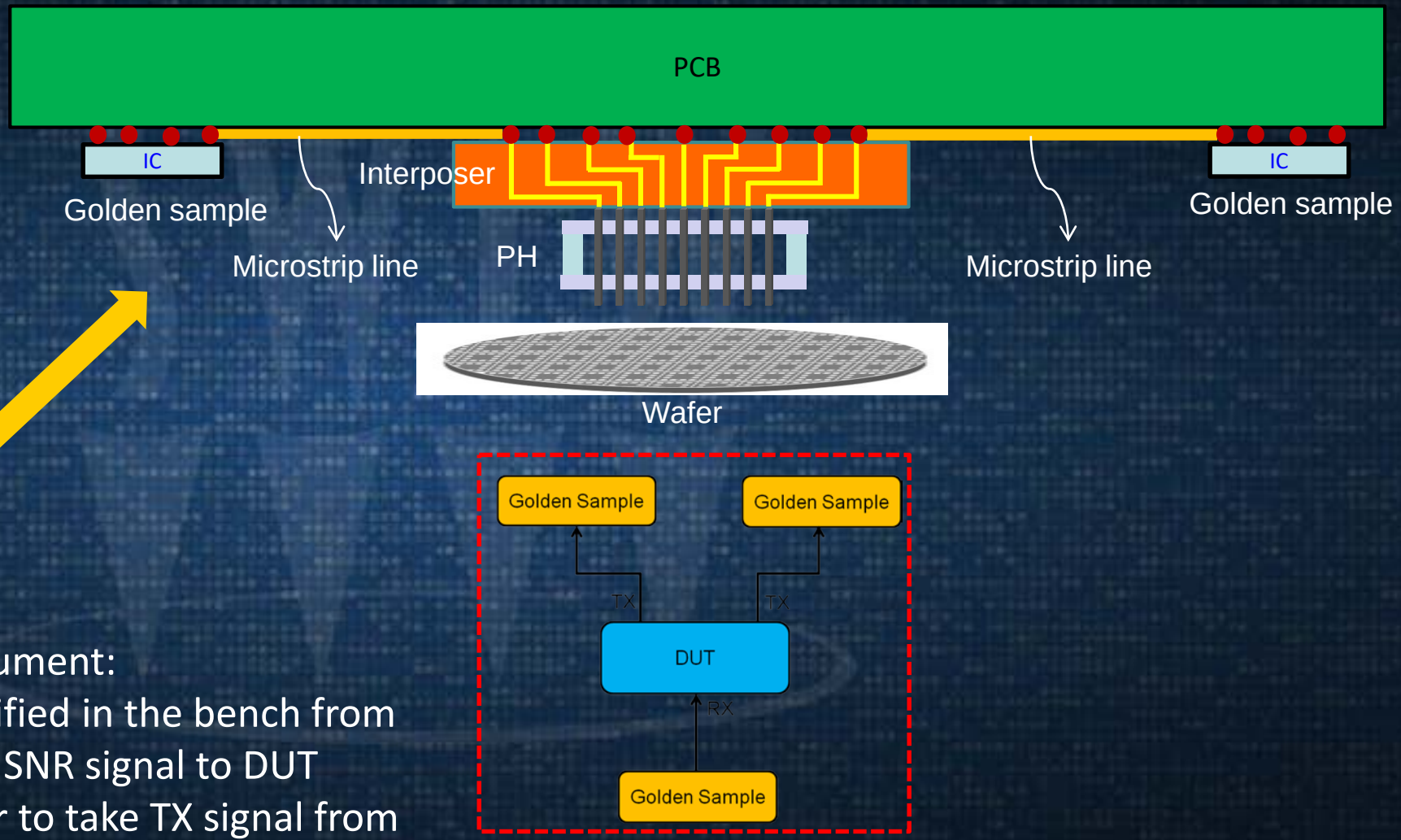
Probe Card Test Solution I

ATE

Bridge Beam

Probe Card





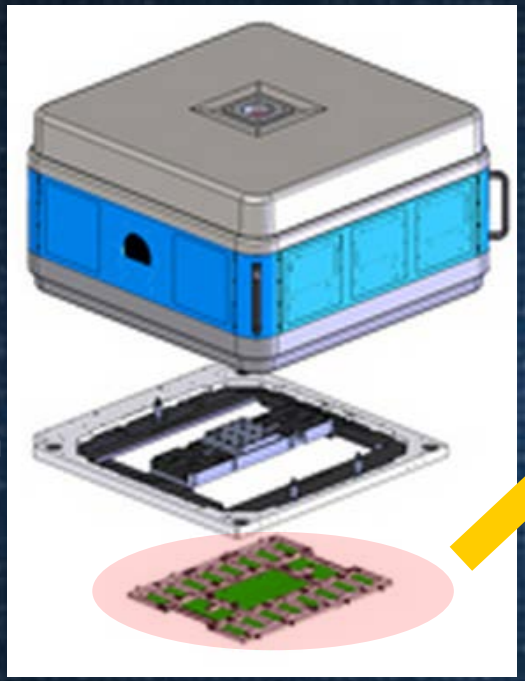
Golden Sample as an Ideal Instrument:
The best-performance chips verified in the bench from Socket which can transmit good SNR signal to DUT and also work as a good receiver to take TX signal from DUT.

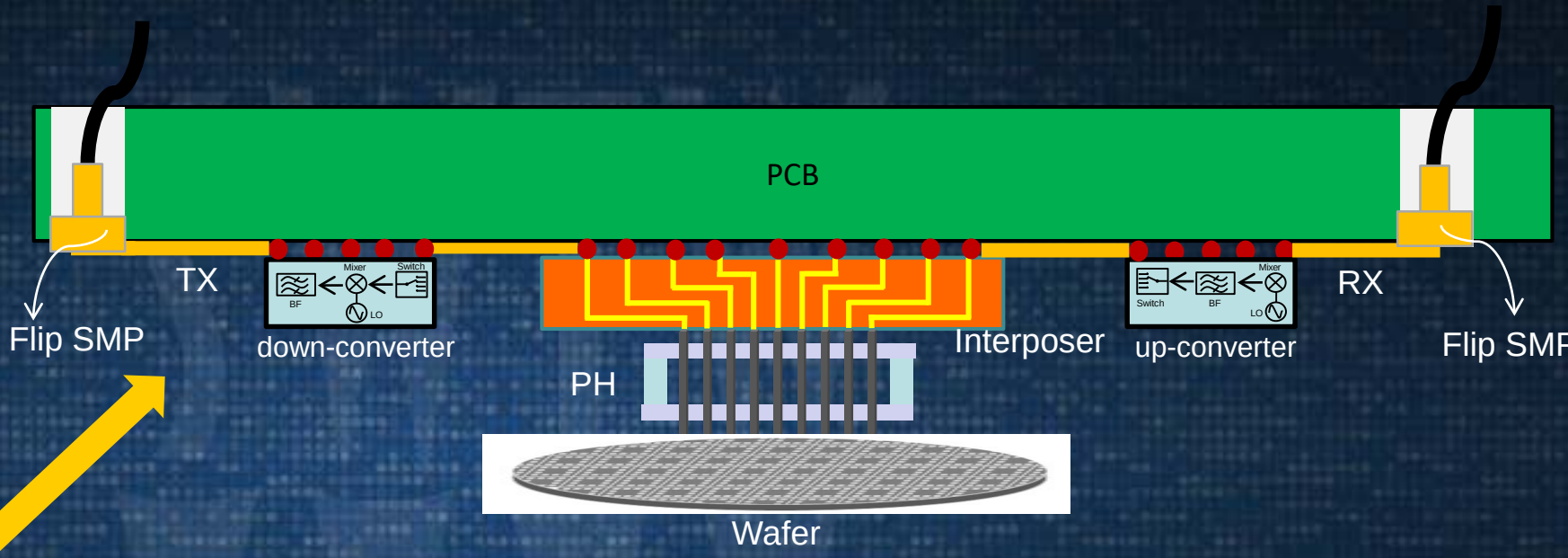
Probe Card Test Solution II

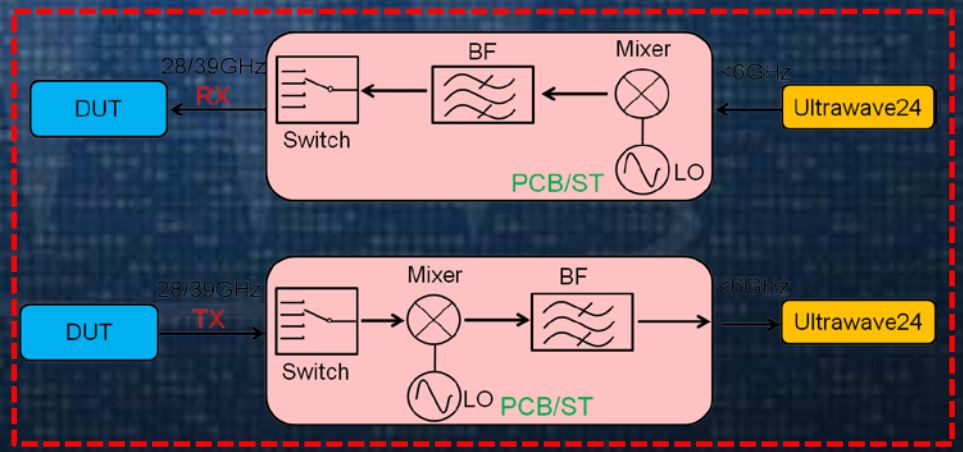
ATE

Bridge Beam

Probe Card





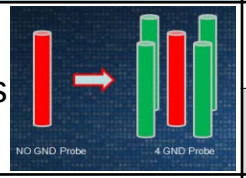
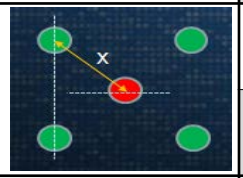
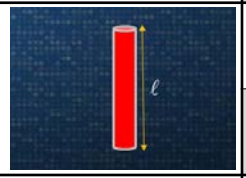
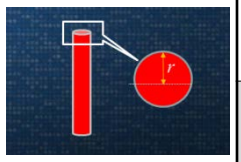


Up-Converter Components:
LPF ➔ Mixer ➔ Local Oscillator ➔ BPF ➔ Switch

Down-Converter Components:
Switch ➔ LNA ➔ BPF ➔ Mixer ➔ LPF

Impedance Control on Probe Pattern

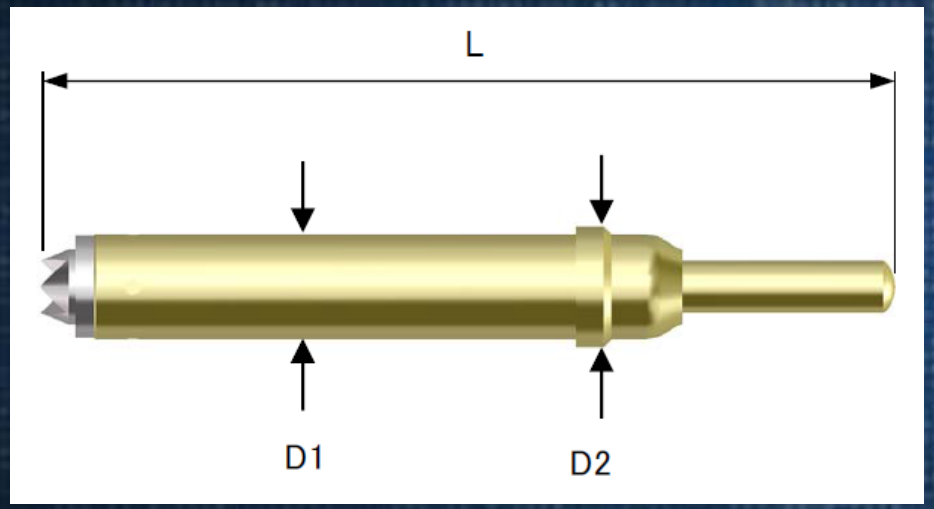
- DFT should take impedance continuity of probe pattern into consideration

Key Factors of Impedance Control	Variables of Probe Pattern		
	Bandwidth		
①GND Probe Quantities 	No GND Probe	2 GND Probe	4 GND Probe
	★	★★	★★★
②Probe Pitch 	X = 0.8mm	X = 0.5mm	X = 0.4mm
	★	★★	★★★
③Probe Length 	Length =3.5mm	Length = 3mm	Free Length = 2.4mm
	★	★★	★★★
④Probe Radius 	Type A(0.24mm)	Type B(0.26mm)	Type C(0.3mm)
	★	★★	★★★

Performance: ★ Bad ★★ Medium ★★★ Good

Refer to 2017 SWTW" Probe Pattern Design for Low-Cost and High-Speed Loopback Test"

28GHz Pogo Pin Specs



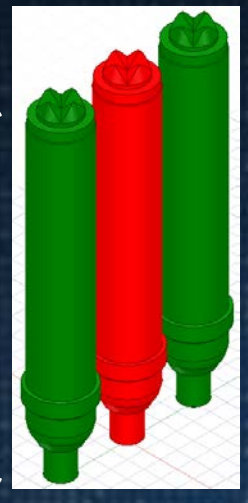
Mechanical Spec.	
Pitch	0.4 mm
Barrel Dia (D1/D2)	Φ0.3/0.34 mm
Free/Operating Length	2.4/2 mm
Operating Stroke	0.4 mm (0.25+0.15)
Spring Force	16±4 gf
Tip Style	Crown
Electrical Characteristics	
Resistance @ Initial	60mOhm(AVR)
Current Capacity	1.8A Max @ Room Temp.
Self-Inductance	0.31 nH

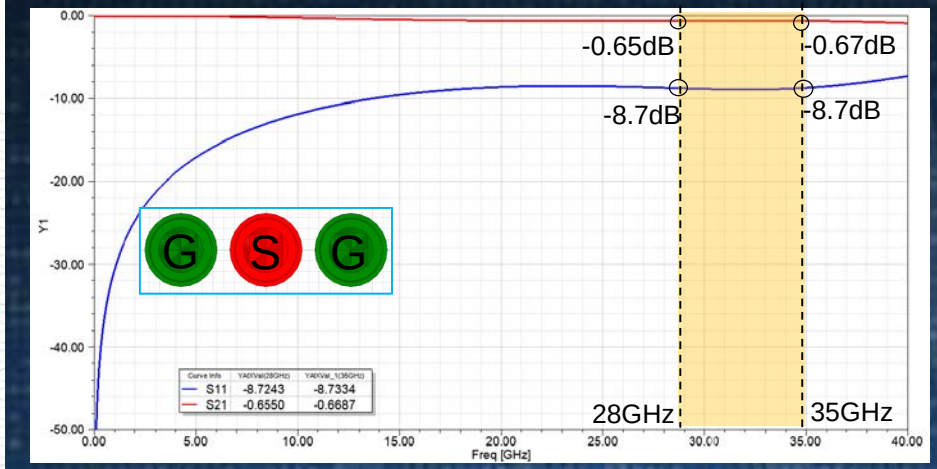
28GHz Pogo Pin Simulation

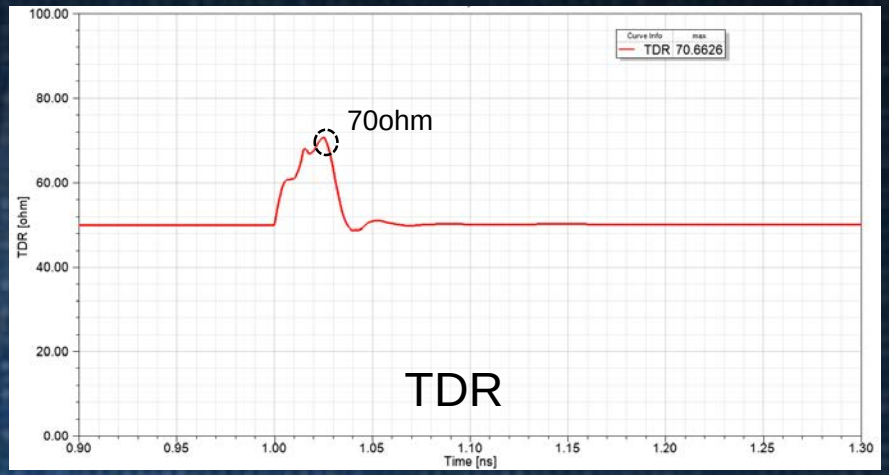
Pitch:0.4mm



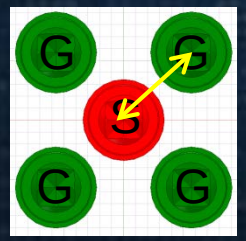
Length:2 mm
(After Preload)

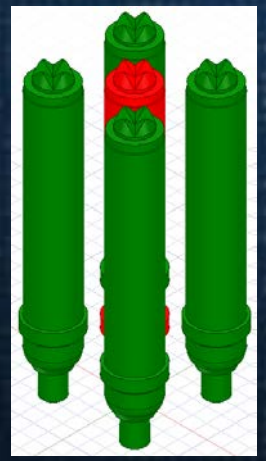


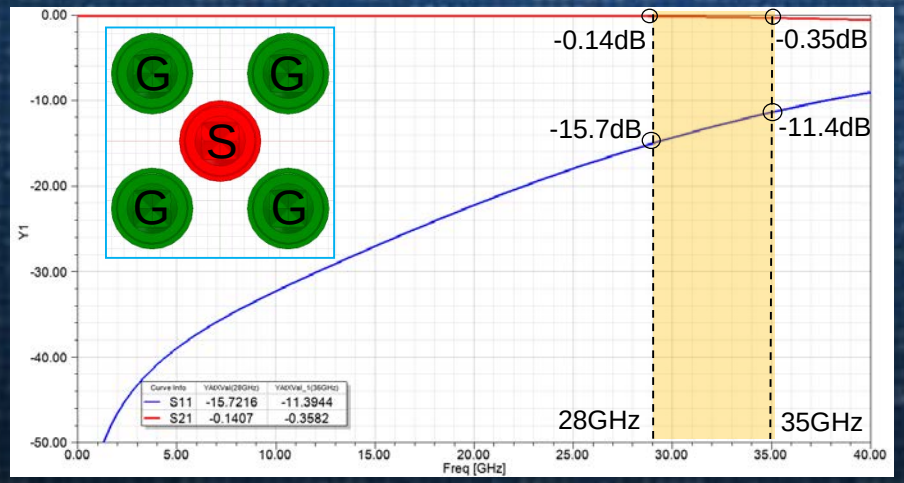


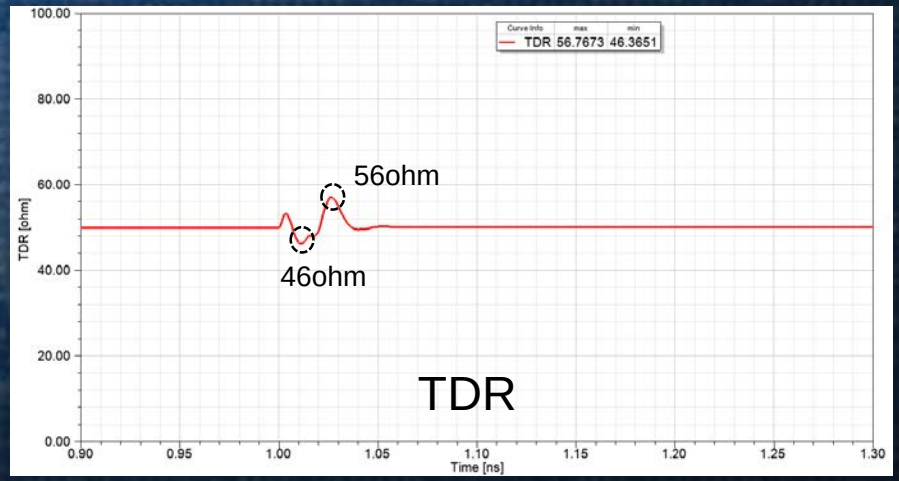


Pitch:0.4mm









The Loss Factors of the Transmission Line

T-Line Loss : $\alpha_{dB} = A_1\sqrt{f} + A_2 f \quad (dB/in)$

Conductive loss(α_c)

- Conductor loss refers to the T-Line series Resistance.
- T-Line Resistance is proportional to $\sqrt{f}$
- T-Line Resistance is inversely proportional to trace width.
- Metal Surface Roughness is also crucial.

Dielectric loss(α_d)

- Dielectric loss refers to the T-Line shunt Conductance.
- Dielectric loss is proportional to f_{req} & $\sqrt{\varepsilon_r}$ & $\tan\delta$.

$$\alpha_d = \frac{\pi \times f \times \tan\delta \times \sqrt{\varepsilon_r}}{3\times 10^8}$$

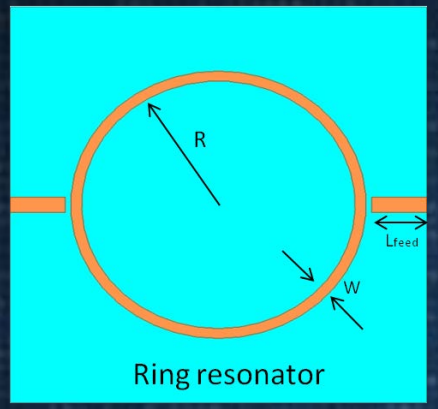
For 5G, we need low and flat DK/DF vs. Freq. due to 2 reasons:

1. 28GHz is a very high Freq., a big weighting in this loss formula.
2. DK/DF are Freq. dependent & 850 MHz Channel BW in 5G.

➔ Keep channel power flatness & Avoid wideband signal dispersion due to different Vp.

PCB DK/DF Extraction

- M-Line Ring Resonator: Two-port gap-coupled Ring method to extract the PCB material's DK and DF.



DK Extraction

$\lambda_o = \frac{c}{fr}$ (1)

$\lambda_g = \frac{\lambda_o}{\sqrt{\varepsilon_{eff}}}$ (2)

$\ell_F = n\lambda_g$ (3)

From (1), (2), and (3)

$\varepsilon_{eff} = (\frac{nc}{\ell_F fr})^2$

$\varepsilon_{eff} = \frac{\varepsilon_r + 1}{2} + \frac{\varepsilon_r - 1}{2\sqrt{(\frac{1+12h}{w})}}$

λ_o : Wavelength of the wave with fr in free space

λ_g : Wavelength of the wave with fr in straight line

fr : Resonant frequency

n : Order of the resonant frequency

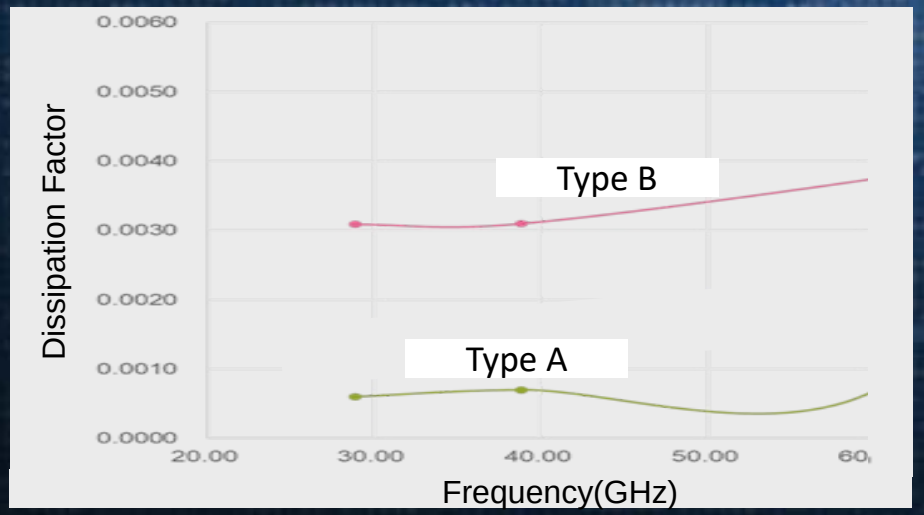
DF Extraction

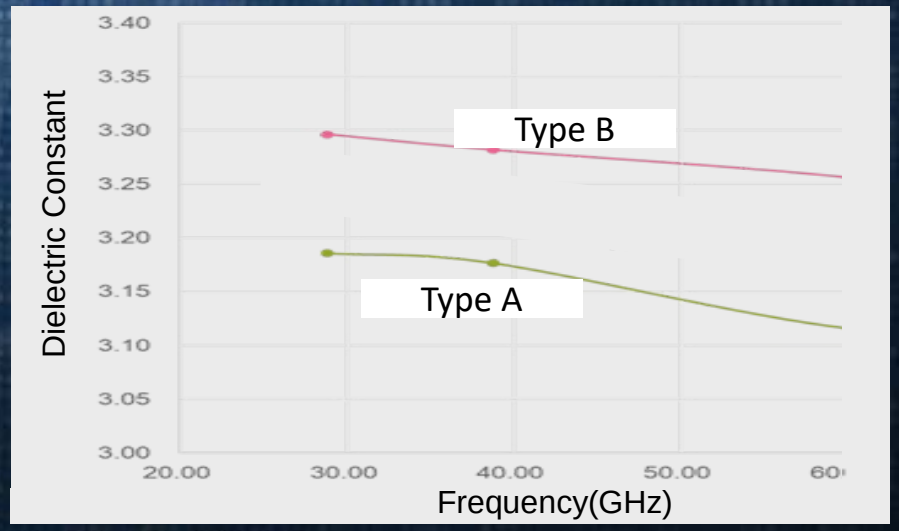
$Q = \omega \frac{Stored\ \ energy}{Disspated\ \ power} = \frac{f_r}{BW_{3dB}} = \frac{f_r}{f_2 - f_1}$

$\frac{1}{Q} = \frac{1}{Q_c} + \frac{1}{Q_d}$

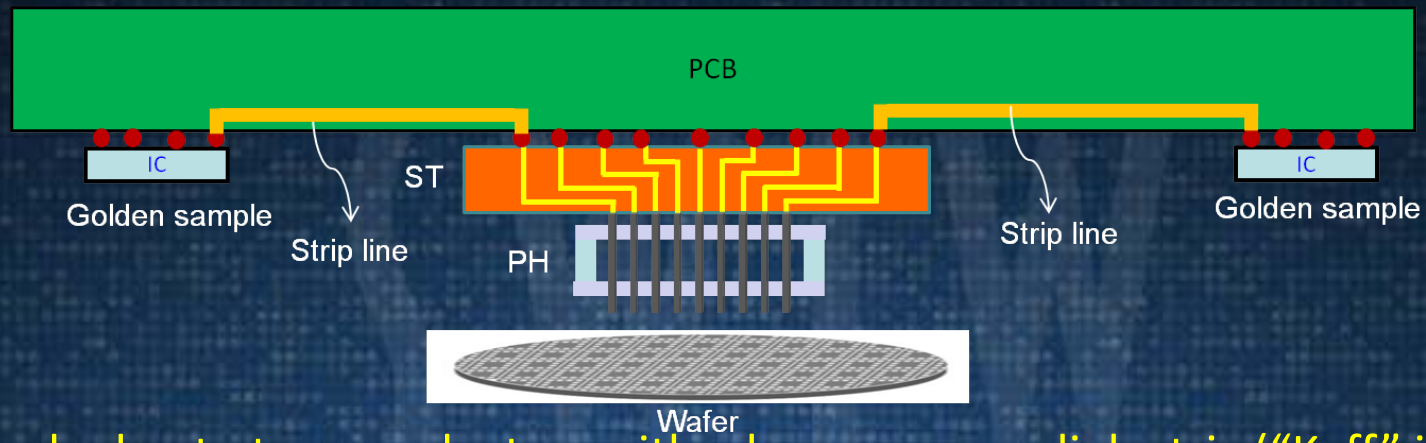
Dissipation factor(DF)

$DF = \tan\delta = \frac{1}{Q_d} = \frac{1}{Q} - \frac{1}{Q_c}$

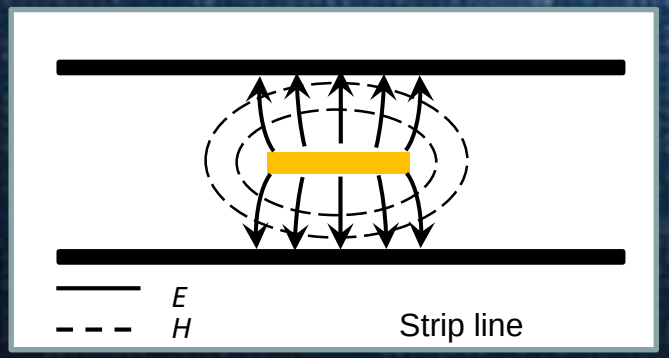


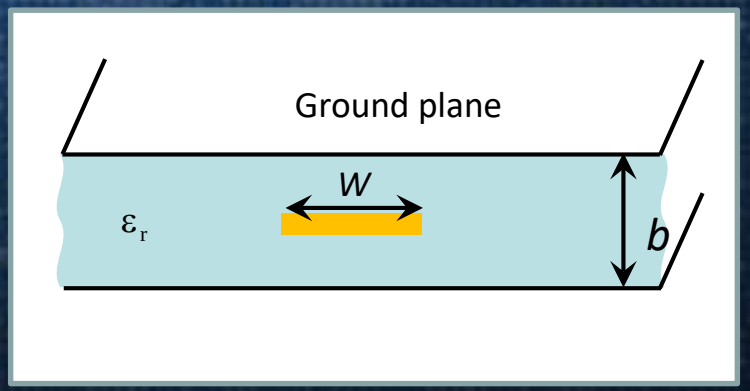


Transmission Line Structure-Strip line

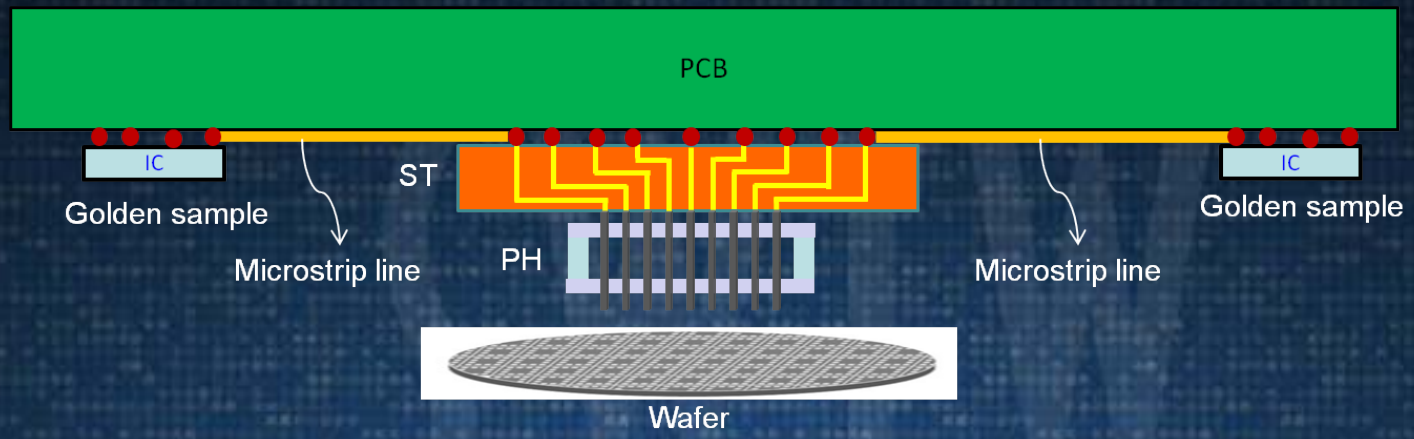


- Usual Mode: TEM mode due to two conductors with a homogenous dielectric (“Keff” is equal to εr.).
- High Order TE/TM Modes: Asymmetry is introduced between two GND planes, particularly in mmWave Freq.
- GND Stitch Via: Used to eliminate high order mode, an over-moded phenomenon.

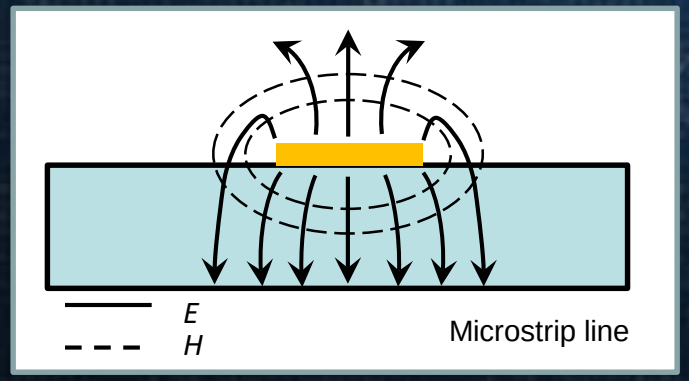


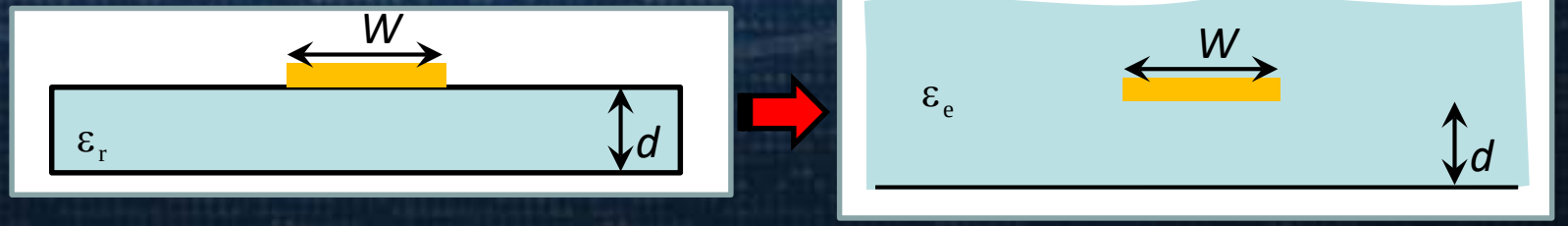


Transmission Line Structure-Microstrip line

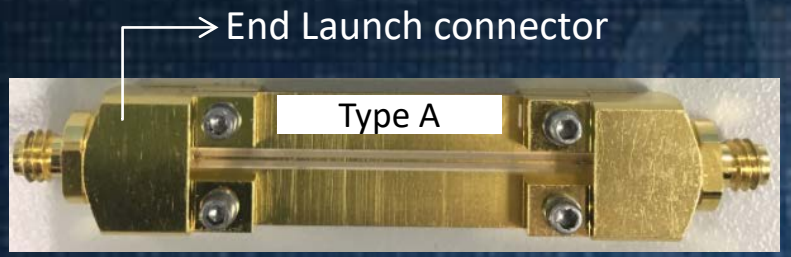


- Usual Mode: Complicated interface results in different Vp in the air and inside the dielectric.
  Quasi-TEM mode due to very thin dielectric, just like static case.
- Above the signal is air, effective dielectric constant :1<εe< εr.
- High Order Mode: Eliminate it by avoiding trace transverse discontinuity (bends, junction 、 return path and step trace width change).

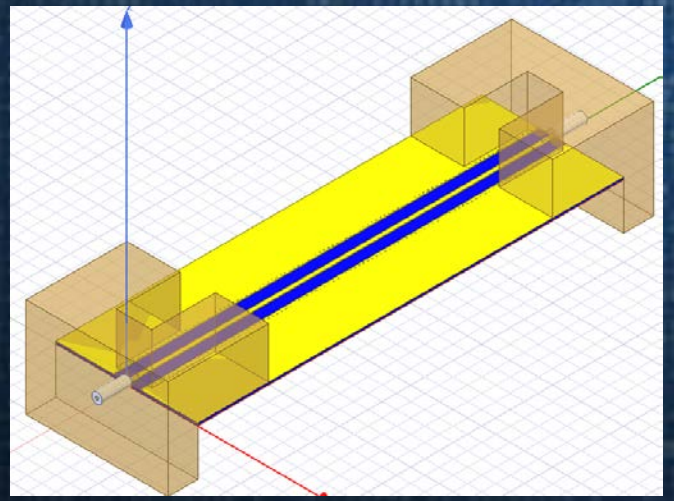




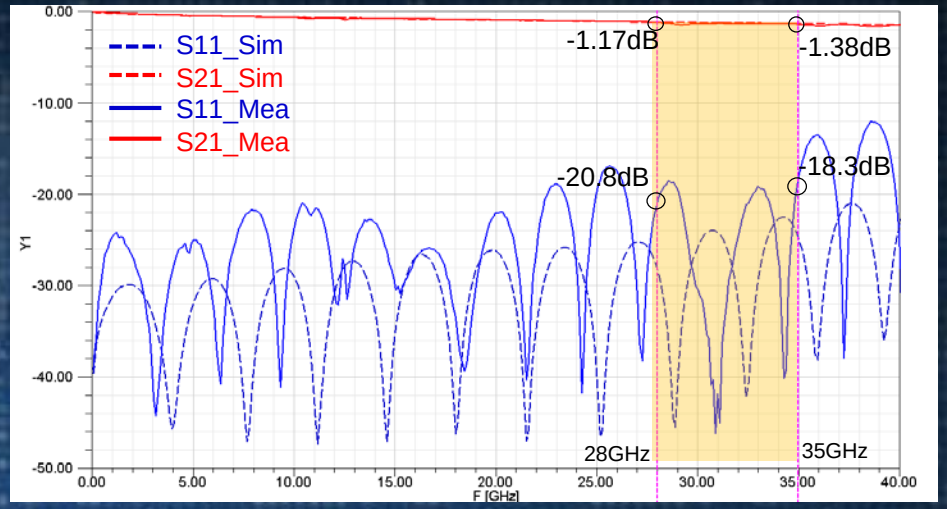
MS Line Simulation and Measurement (Type A)

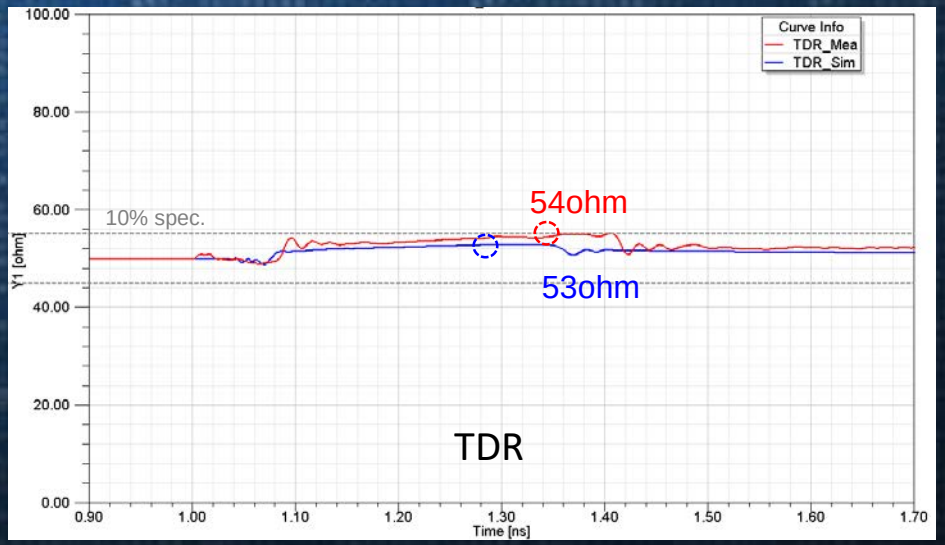


30mm, Type A microstrip line with 5mil CORE
Stitch via spacing:8mil

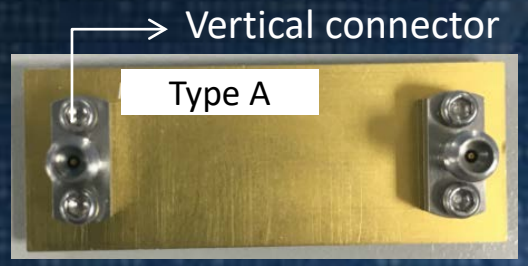


HFSS simulation

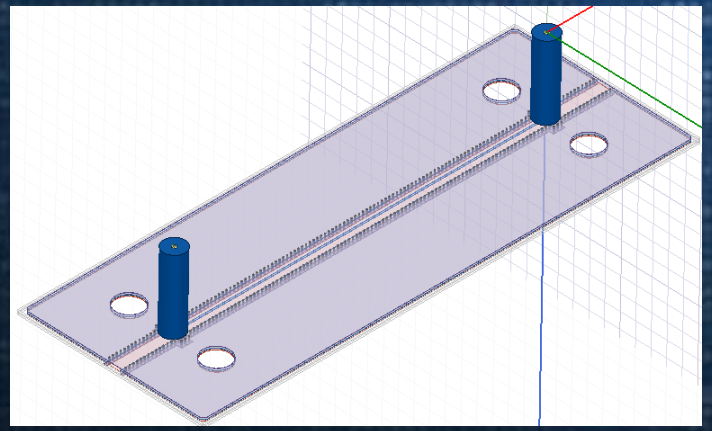




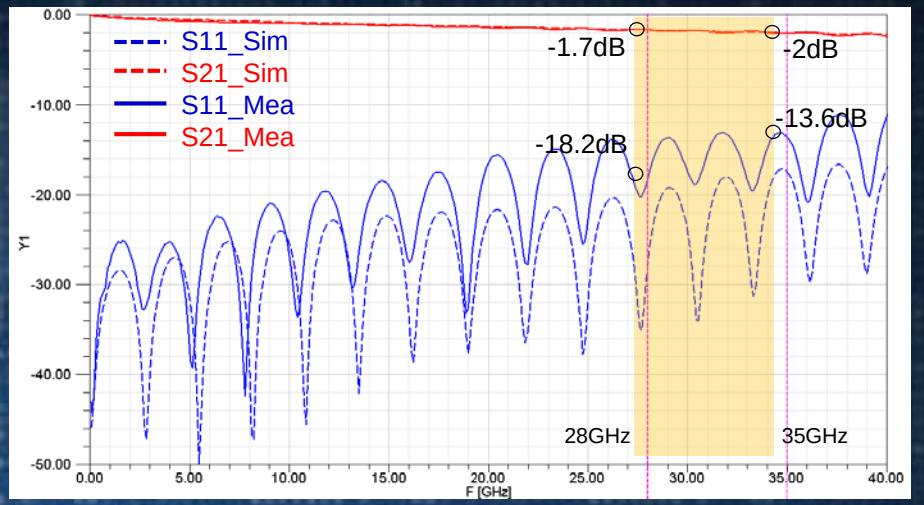
Strip line Simulation and Measurement (Type A)

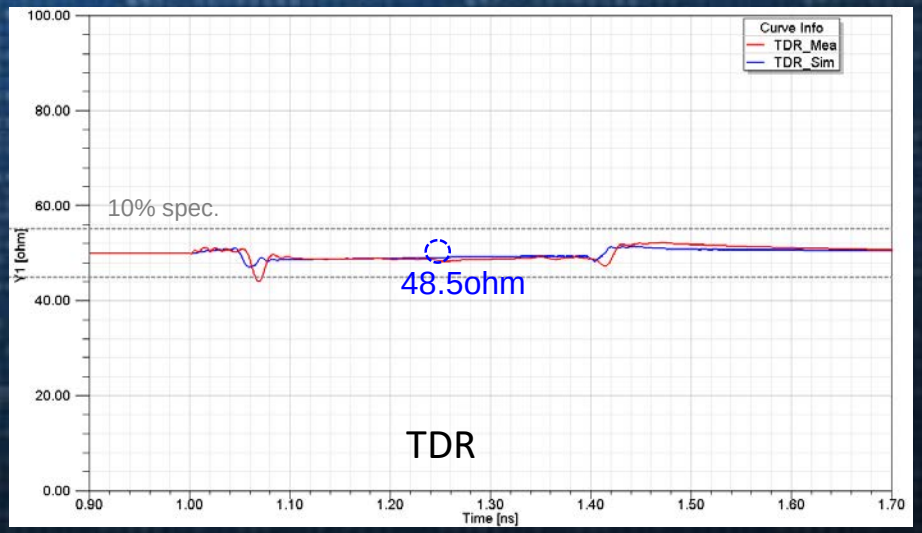


30mm, Type A strip line with 5mil CORE & 5mil PP
Stitch via spacing:8mil

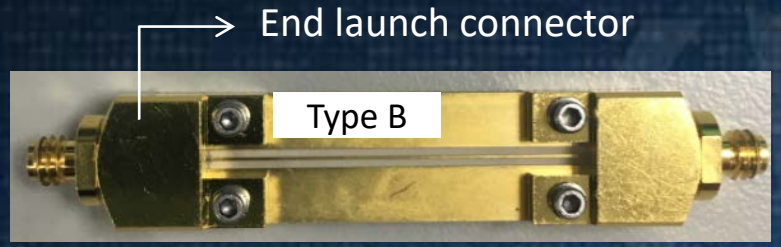


HFSS simulation

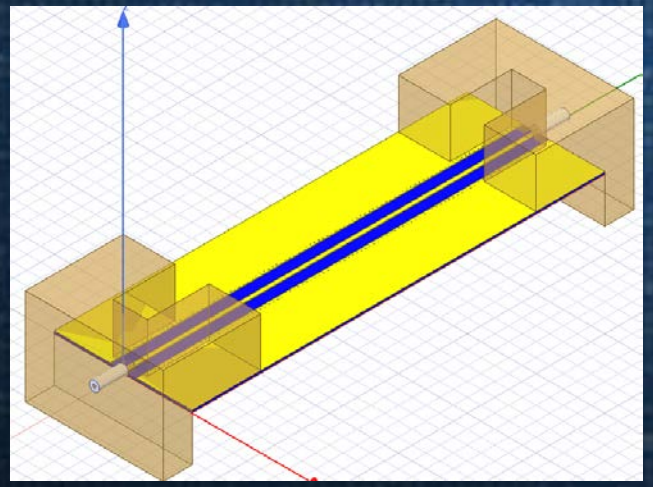




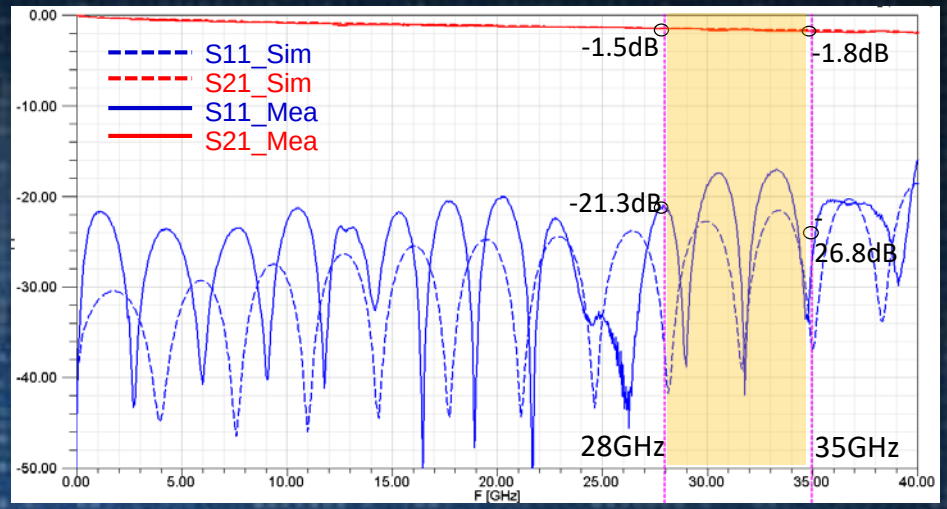
MS Line Simulation and Measurement (Type B)

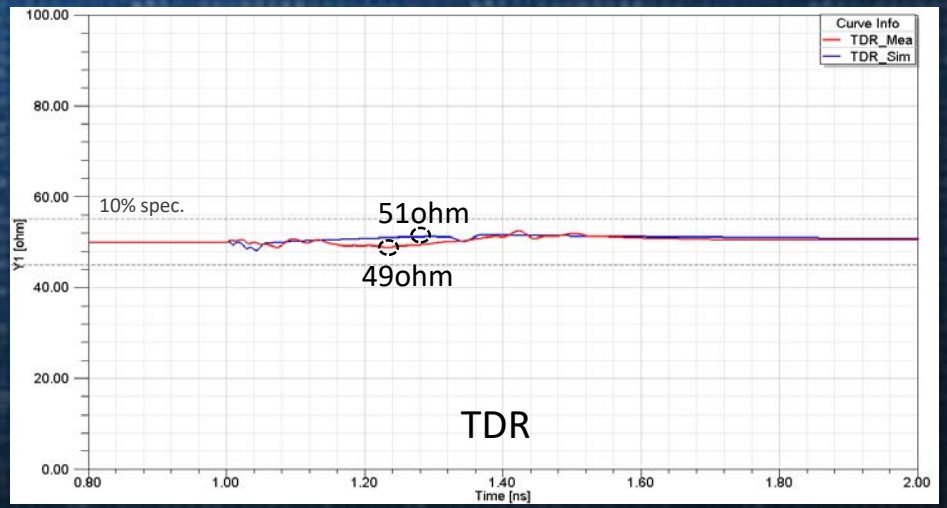


30mm, Type B microstrip line with 4mil CORE
Stitch via spacing:8mil

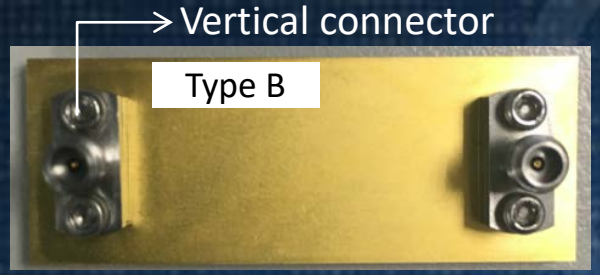


HFSS simulation

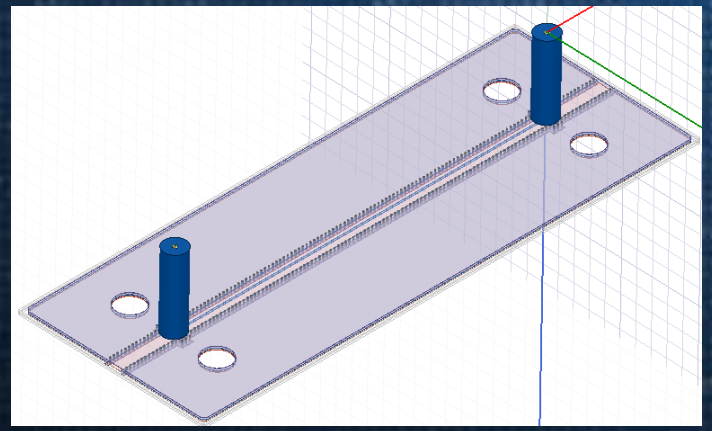




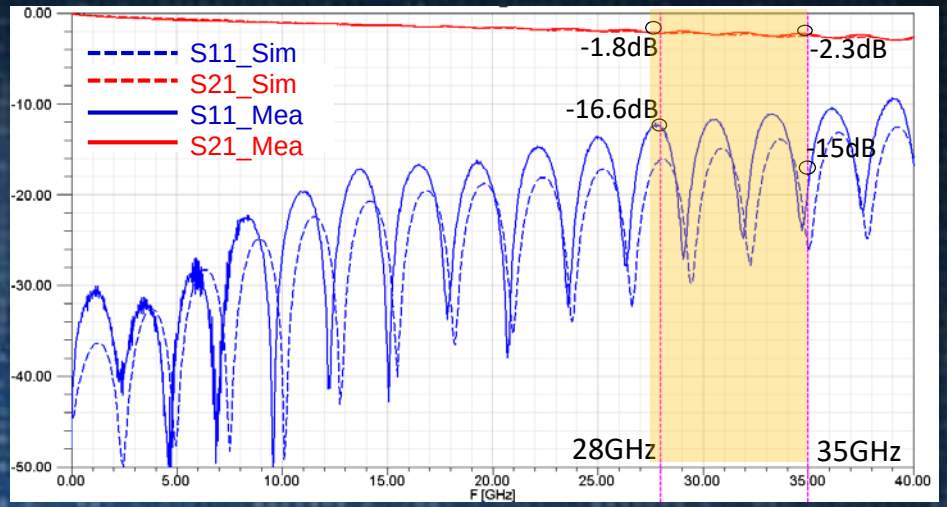
MS Line Simulation and Measurement (Type B)

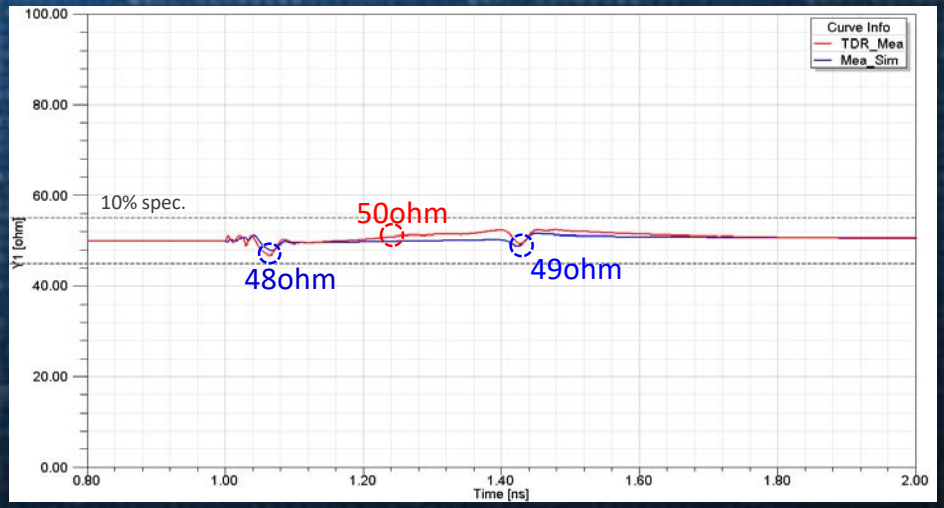


30mm, Type B strip line with 4mil CORE & 3.5mil PP
Stitch via spacing:8mil



HFSS simulation





Correlation Summary

Structure	MS Line (30mm)		Strip Line (30mm)	
Material	TypeA	TypeB	TypeA	TypeB
S21@ 28GHz	-1.2dB	-1.5dB	-1.7dB	-2.2dB
S11@ 28GHz	-20.8dB	-21.3dB	-18.2dB	-16.6dB
Performance	★★	★	★★	★

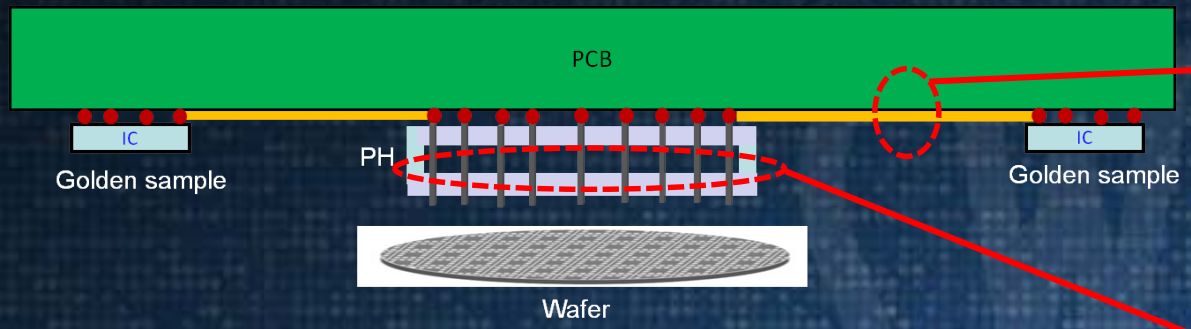
- For the same material, Microstrip line has lower loss than Stripline:

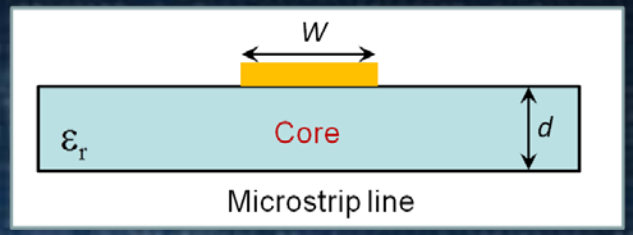
① At 28GHz, dielectric loss dominates the total power loss.

② Microstrip line has part of the electromagnetic field line in the air with lower loss.

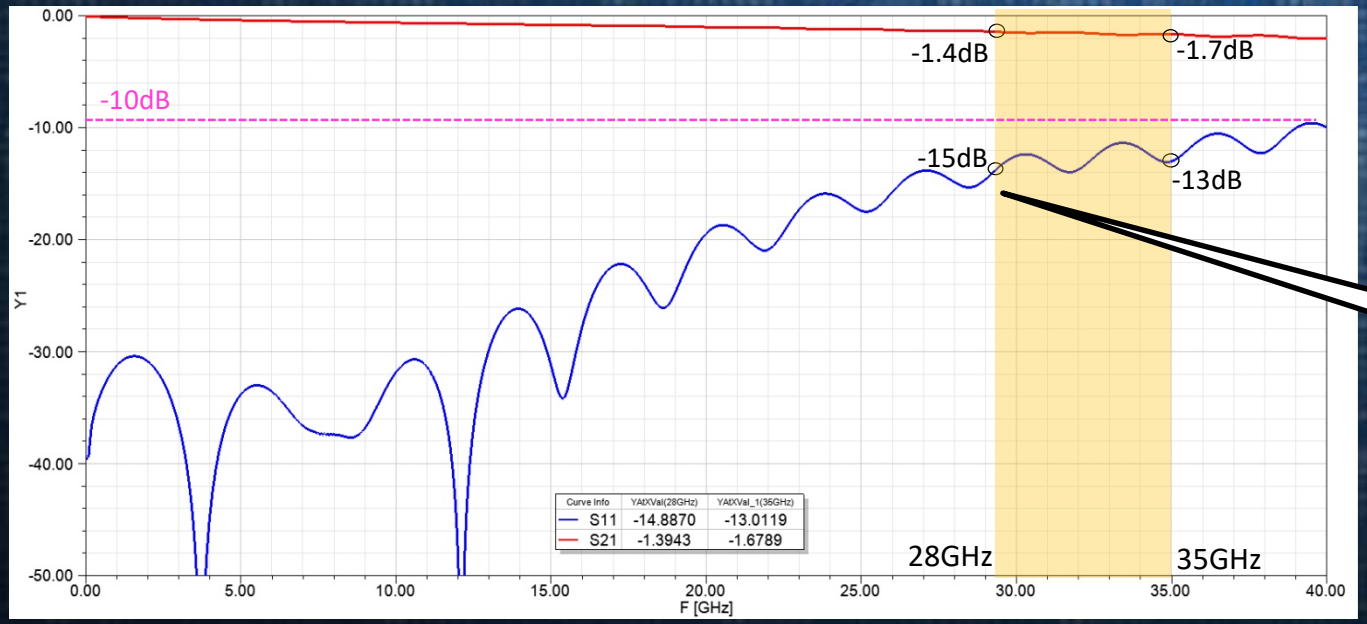
- Same transmission line structure in different materials:
  Low DF indeed has lower power loss.

28GHz Probe with PCB simulation

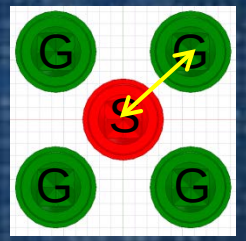


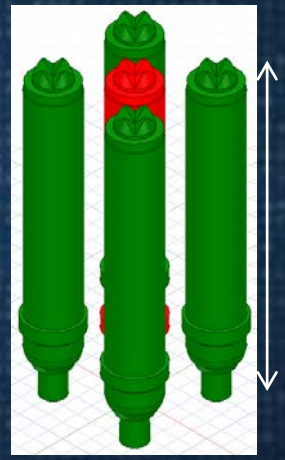


30mm, Type A Microstrip line with 4mil CORE



Pitch:0.4mm





Length:2mm

The loss is only -1.4dB at 28GHz and the return loss is below -15dB.

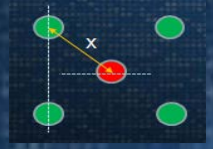
Conclusion

- Probe Design

— For 28GHz probe design, there are 4 key factors to optimize the probe pattern for high performance, and we proposed a best design for 28GHz.

①GND Probe Quantities ②Probe Pitch ③Probe Length ④Probe Diameter









- PCB T-Line Correlation

— After we put extracted DK/DF back to simulation, the correlation results are very close for both Microstrip line and Stripline.

— For the same material, Microstrip line has lower loss than Stripline.

— For the same trace structure on different material, low DF has lower power loss.

- 28GHz Probe Card Solution

— After the performance optimization and carefully correlation, we provide the best Probe Card Test Solution of the cascaded Pogo pin + Microstrip Line + Type A lower DK/DF material.

SW Test Workshop
Semiconductor Wafer Test Workshop

WLCSP xWave for high frequency wafer probe applications

Jason Mroczkowski
Xcerra Corporation

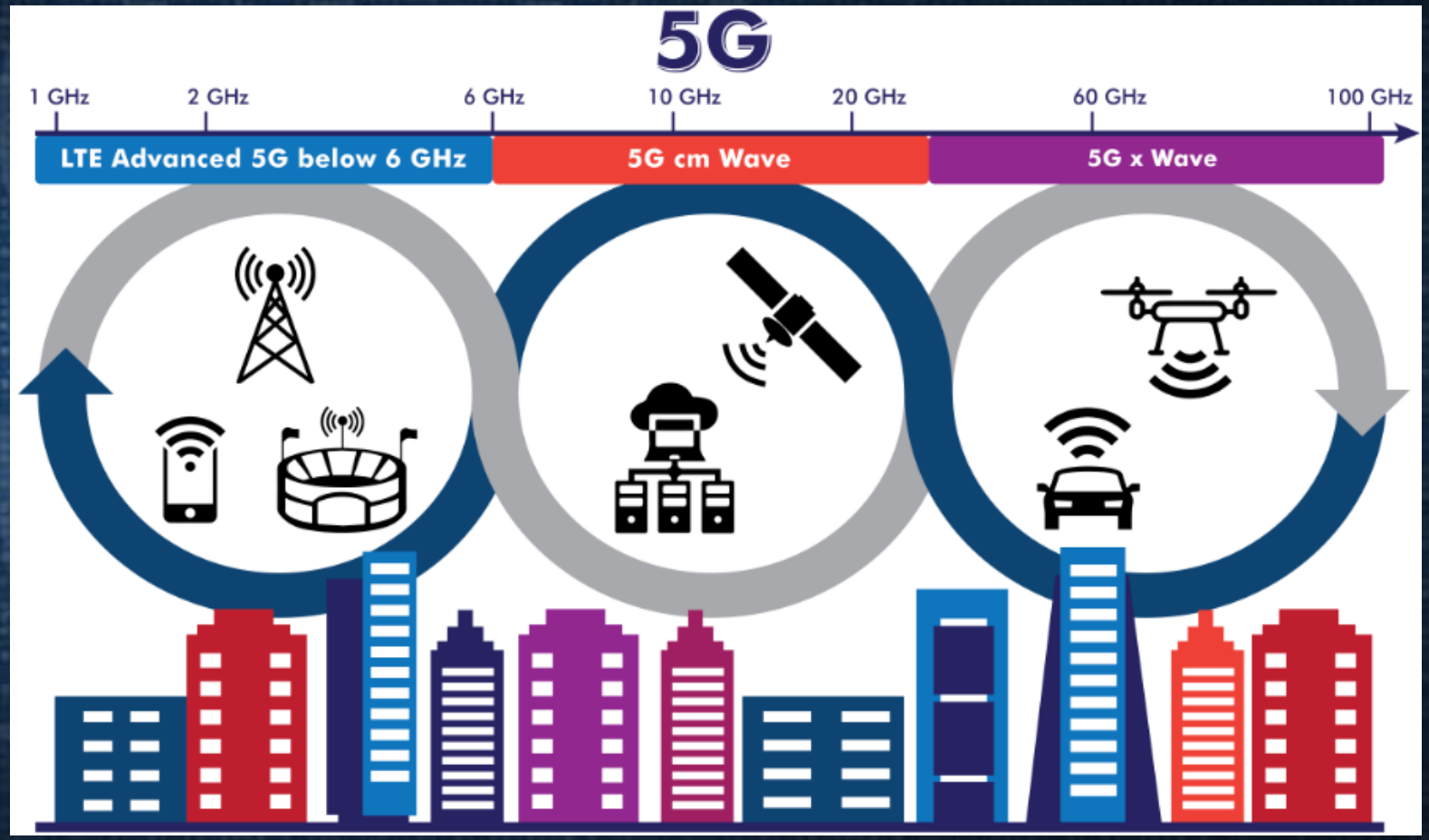
June 3-6, 2018

Overview

- Introduction / Background – cmWave and mmWave Market/applications and xWave
- Objectives / Goals – Move from package test to wafer test
- Methods / Materials / Procedures – design considerations, mechanical simulation, electrical simulation, characterization
- Results / Relevant Findings / Key Data – tip design, force, insertion loss, impedance
- Discussion of Results / Strengths / Weaknesses, etc. – minimum pitch, multisite
- Summary / Conclusion - viable cmWave and mmWave wafer level test solution
- Follow-On Work – Beta sites

RF Market Summary

- **The RF market has pull**
  - RF Component Market Growing to $22B by 2022
    - cmWave (3GHz – 30GHz) = $18.2B,
    - mmWave (30GHz-100GHz) = $4.6B
  - Rapid growth in mmWave applications
    - ADAS, 5G telecom UltraGig, WiGig, and Satellite devices
    - **up to 40% CAGR through 2022.**



mmWave Market

- **ADAS**
  - Advanced Driver Assistance System (Automotive Radar)
  - Short Range 24GHz and Short and Long Range 80GHz versions
  - CMOS – Low cost, High integration, catching up with SiGe
  - SiGe – High power/frequency performance ,High cost ,Low integration
  - GaN – Highest frequency performance, high cost, low integration, being oboseted by SiGe
- **5G telecom**
  - 5G Backhaul – routers behind the tower
  - 5G End Node – Handheld phones/tablets/devices
  - Contacted test – external antenna arrays
  - AIP – Antenna In Package – Over the air test
  - 28GHz and 39GHz bands popular
  - Eband/Vband expected as next generation





mmWave Market

- **UltraGig/WiGig**
  - Fixed Wireless applications
  - Local area networks
  - Short range line of sight
  - beamforming
  - 57-64 GHz extended to 71 GHz



- **Satellite Internet**
  - Low orbit satellite internet systems
  - Global aircraft high speed internet connection
  - Terrestrial and orbiting devices
  - Ku (12-18 GHz) and Ka (26.5-40 GHz) bands
- **High Speed Cloud Networks**
  - SERDES - 54GBPS NRZ, 112GBPS PAM4
  - 3rd Harmonics reach 80GHz
  - RF theory applies to Digital applications



xWave Technology - Broadband Production Solution to 100 GHz

Best Signal Integrity

- New paradigm eliminates board and Pogo pins from RF path
- Shortest possible, coplanar waveguide
- Compatible with single-ended and differential signals
- Minimum number of transitions between Tester and DUT

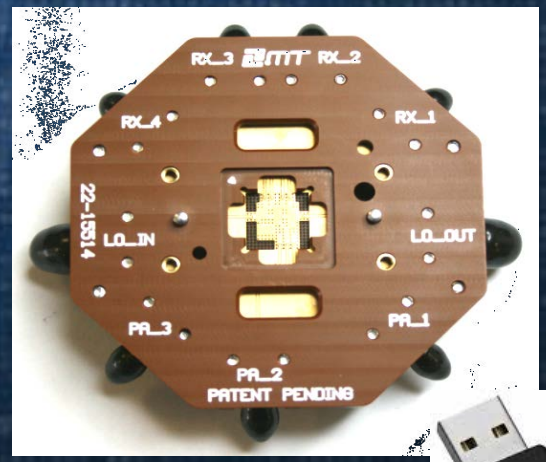
Highly Integrated Solution

- Contactor includes entire path from tester to DUT
- Only power and control signals use board and Pogo pins

High-Volume Production Package Test Solution

- *Not just a lab bench science kit!*
- 1.5 M+ cycles on original hardware
- Field-maintainable mechanical assembly
- Includes calibration kit
- Tri Temp Capable (-55 to 155°C)

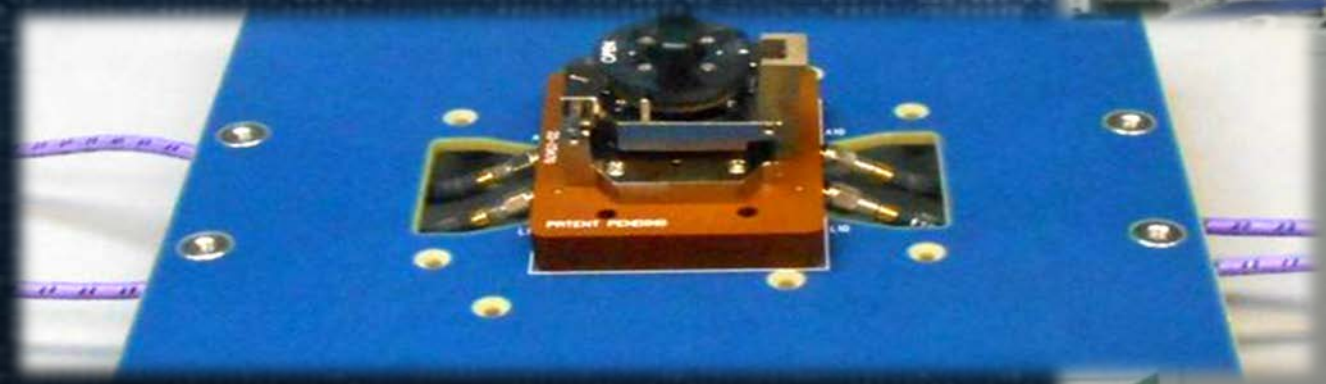


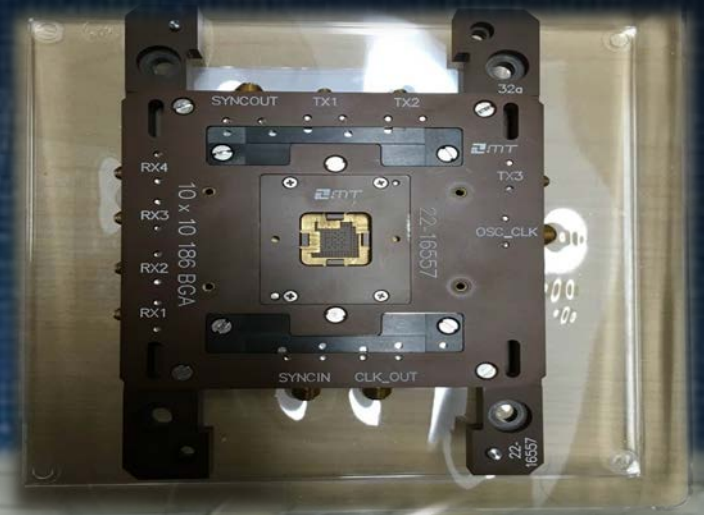




xWave Contactor Field Results

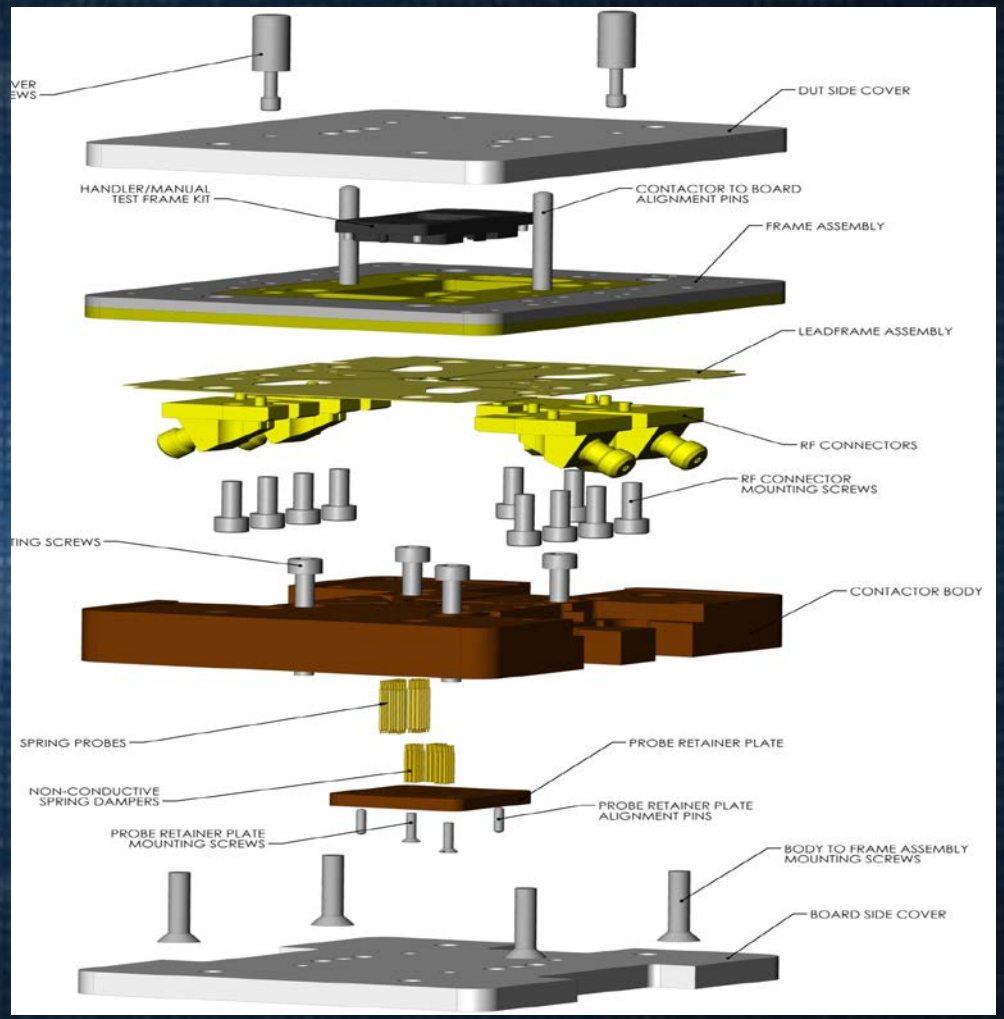
- Millions of cycles on original hardware
- Soldered-down device performance @ 80 GHz
- 100% Correlation between Lab and Production
- 80%+ Automotive Radar applications use xWave Contactors
- xWave used in production 5G, SERDES, Radar, and WiGig



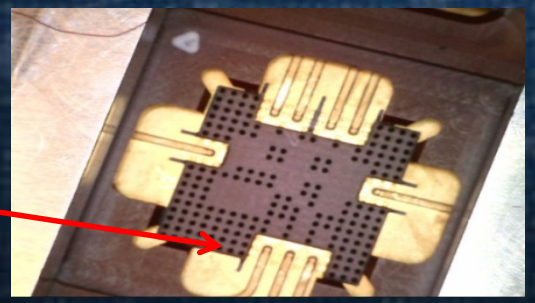


xWave: Designed for cmWave/mmWave RF Performance

- Minimized number of interfaces
- Best signal quality
- Highly reliable and robust
- Best suited for production environments
- Patent # 9842793
- Additional Patents Pending

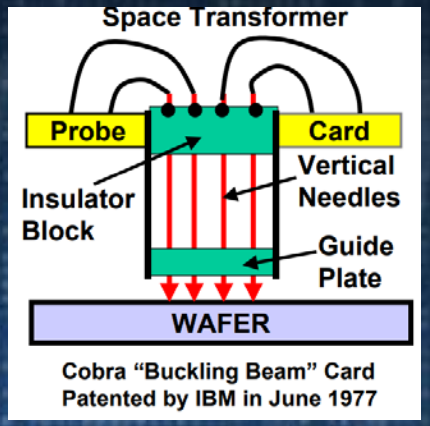


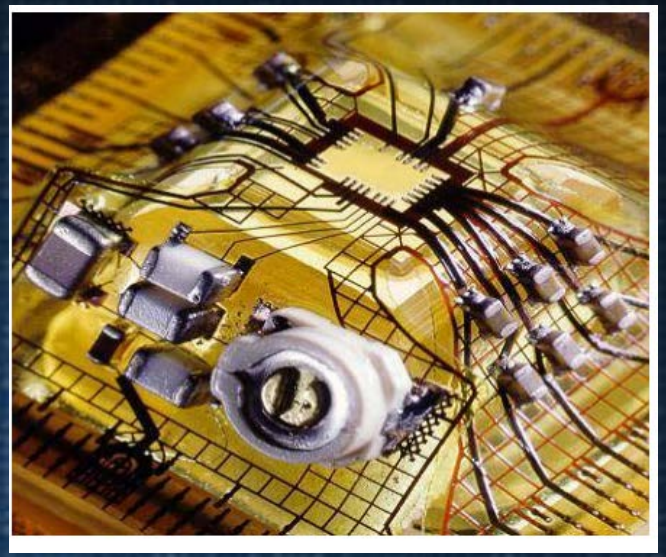
DUT Interface

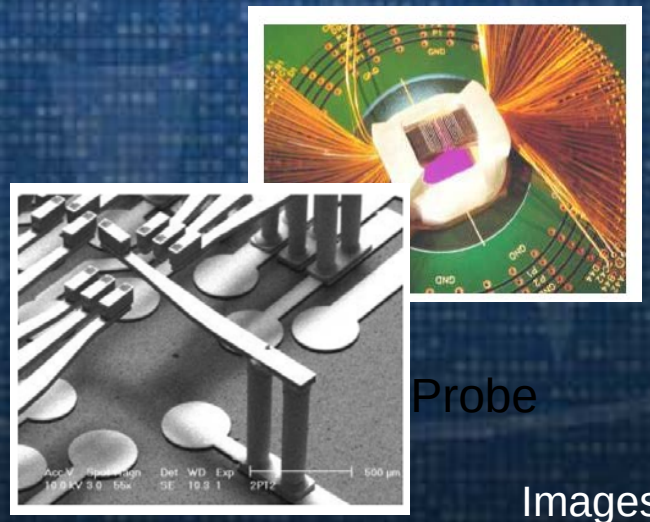


Current RF Probe Limitations

- **Cantilever**
  - No impedance control
  - Extremely High inductance
  - Limited to <2GHz
  - Decoupling components far from DUT
- **Vertical Probe**
  - Shorter uncontrolled impedance path
  - Lower inductance than cantilever
  - Limited to <6GHz
  - Decoupling components ~1-2cm from DUT
  - Individually replaceable probes
- **Membrane**
  - Impedance controlled to DUT
  - No additional inductance
  - Decoupling caps ~1-5mm from DUT
  - Limited compliance (~50um)
  - Fragile
  - Not field replaceable







Probe



Images provided by William Mann Chair, Southwest Test Workshop

xWave: Wafer Level Final Test

Shortest signal path from die to tester

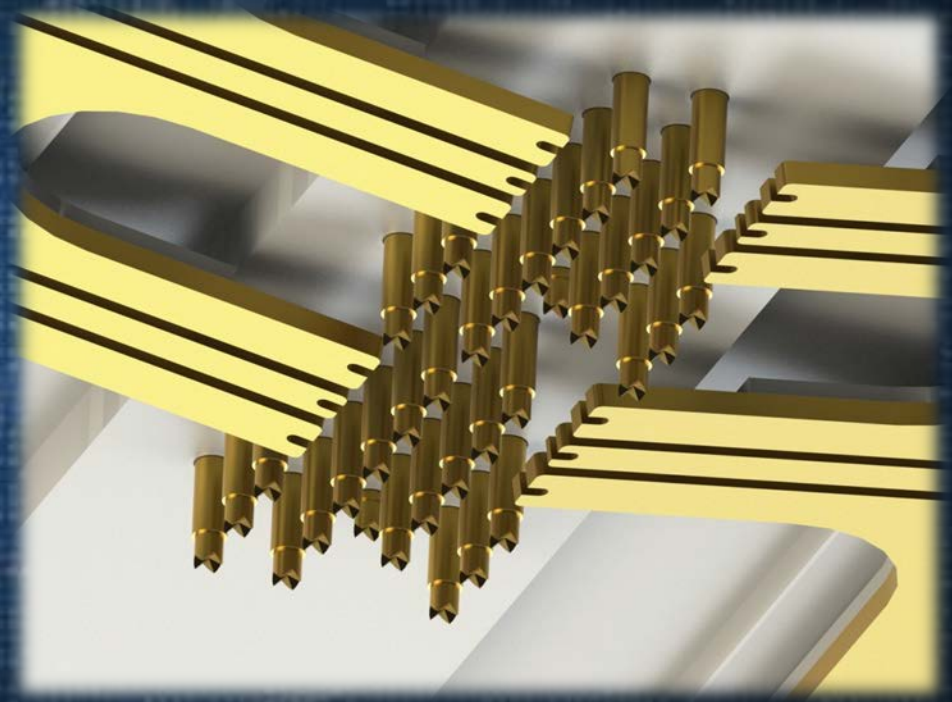
- Direct Tester to DUT connection
- High speed signals bypass PCB
- Impedance controlled signal path

Same core technology as standard xWave

- Robust Leadframe technology
- Hybrid Pogos for Power and control signals

Made for Production Environments

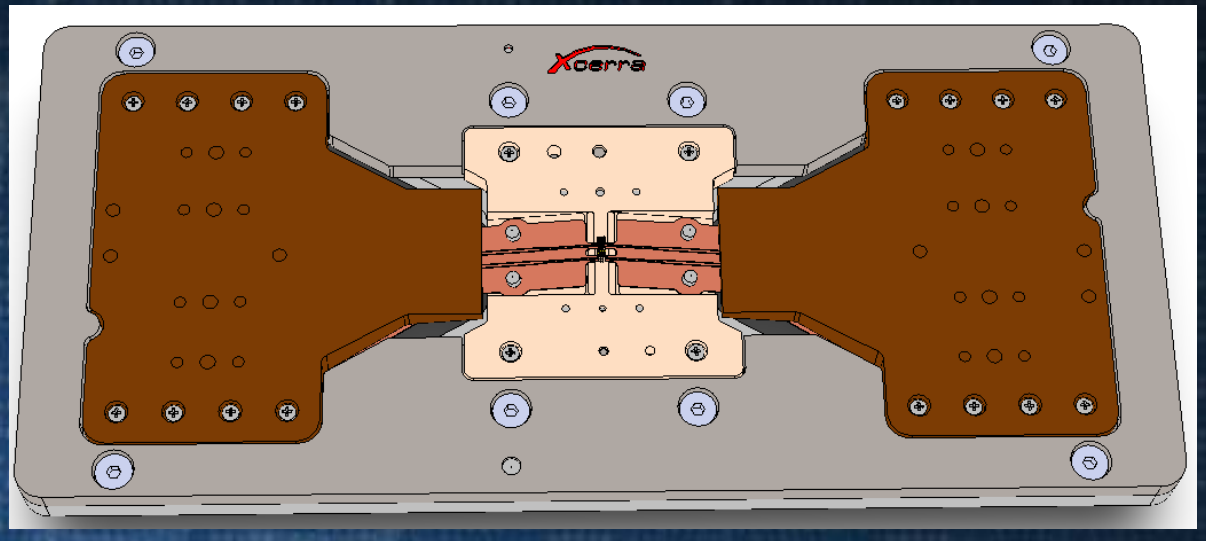
- *Field replacable spring probes, leadframes, connectors/waveguides*
- 200um overdrive

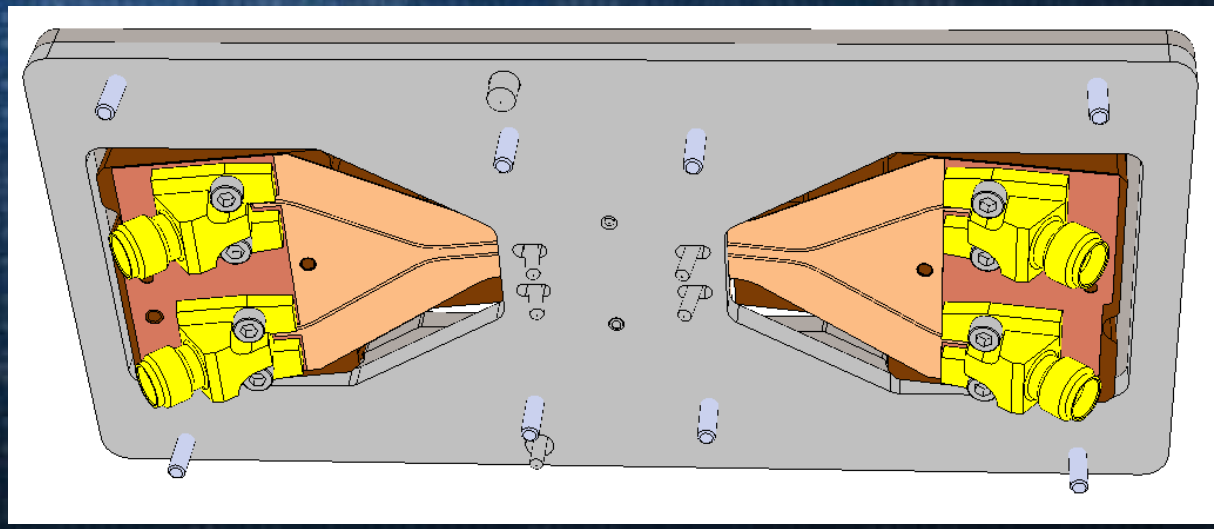


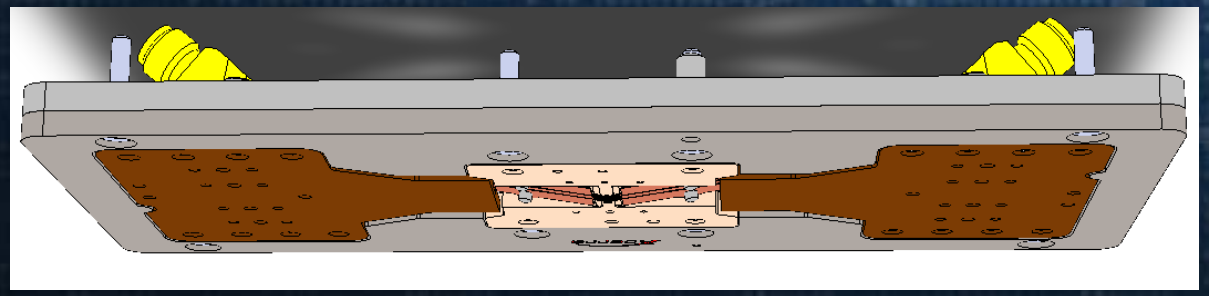
Wafer level probe solution up to 100GHz and pitches down to 100um

WLCSP xWave Design Goals

- **Maintain as much as possible from package test xWave technology**
  - mmWave Signal integrity
  - High compliance
  - Field maintainability
  - Robustness and longevity
  - Tri-Temp capability

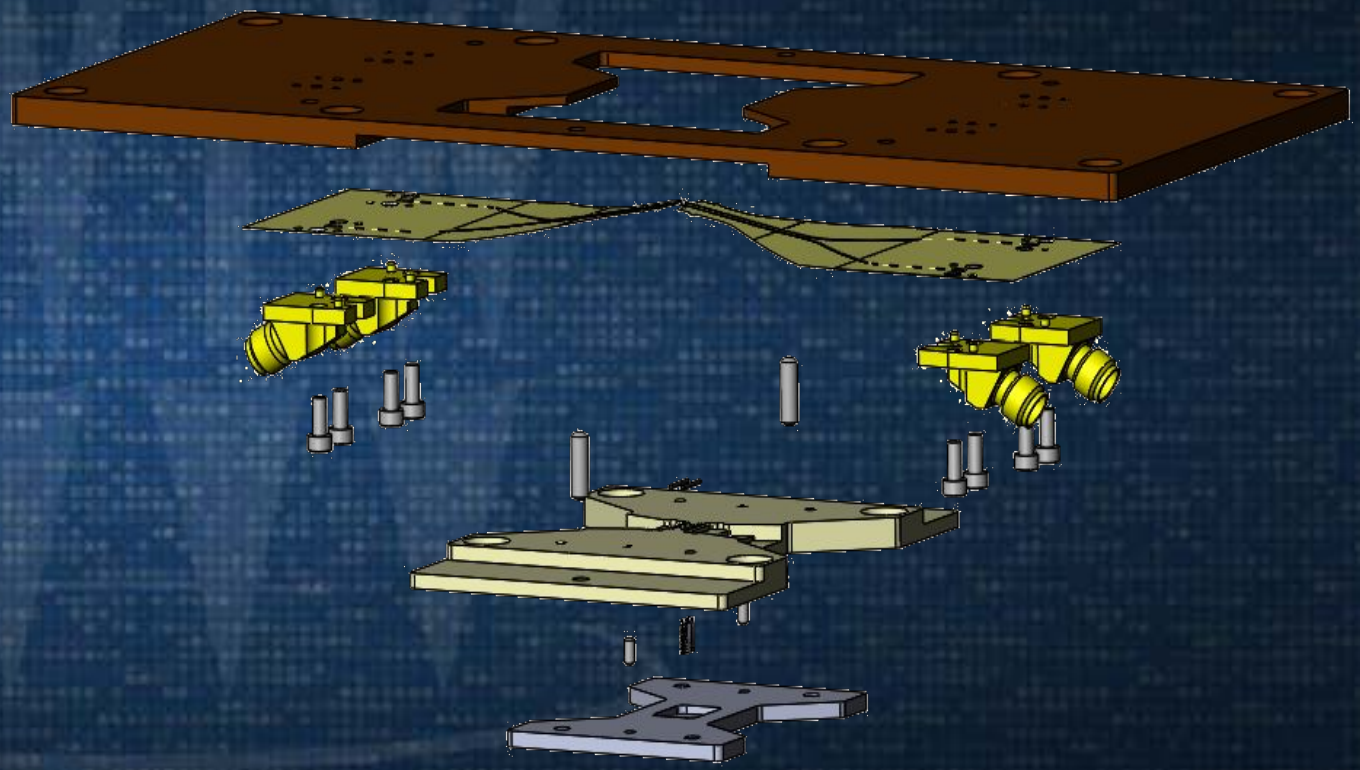






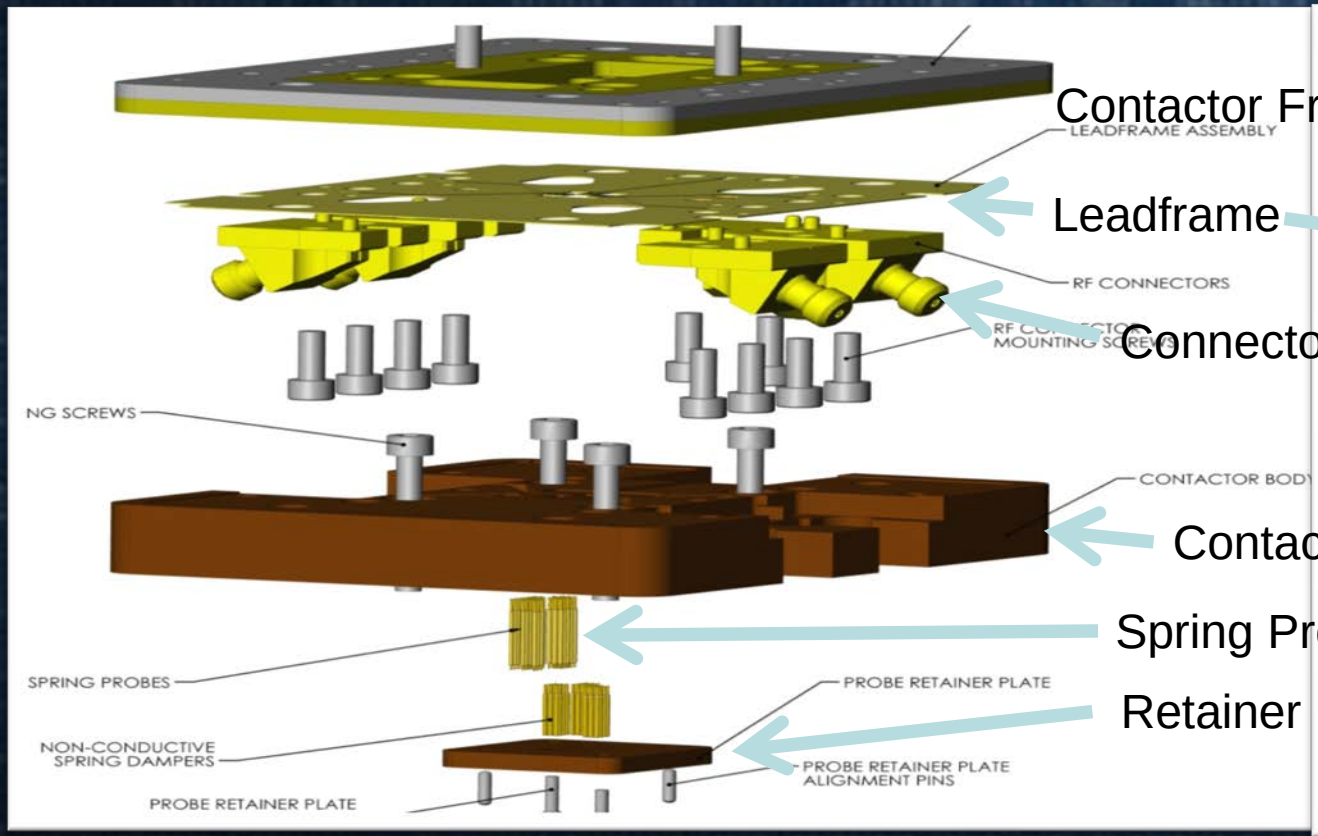
Objectives/Goals

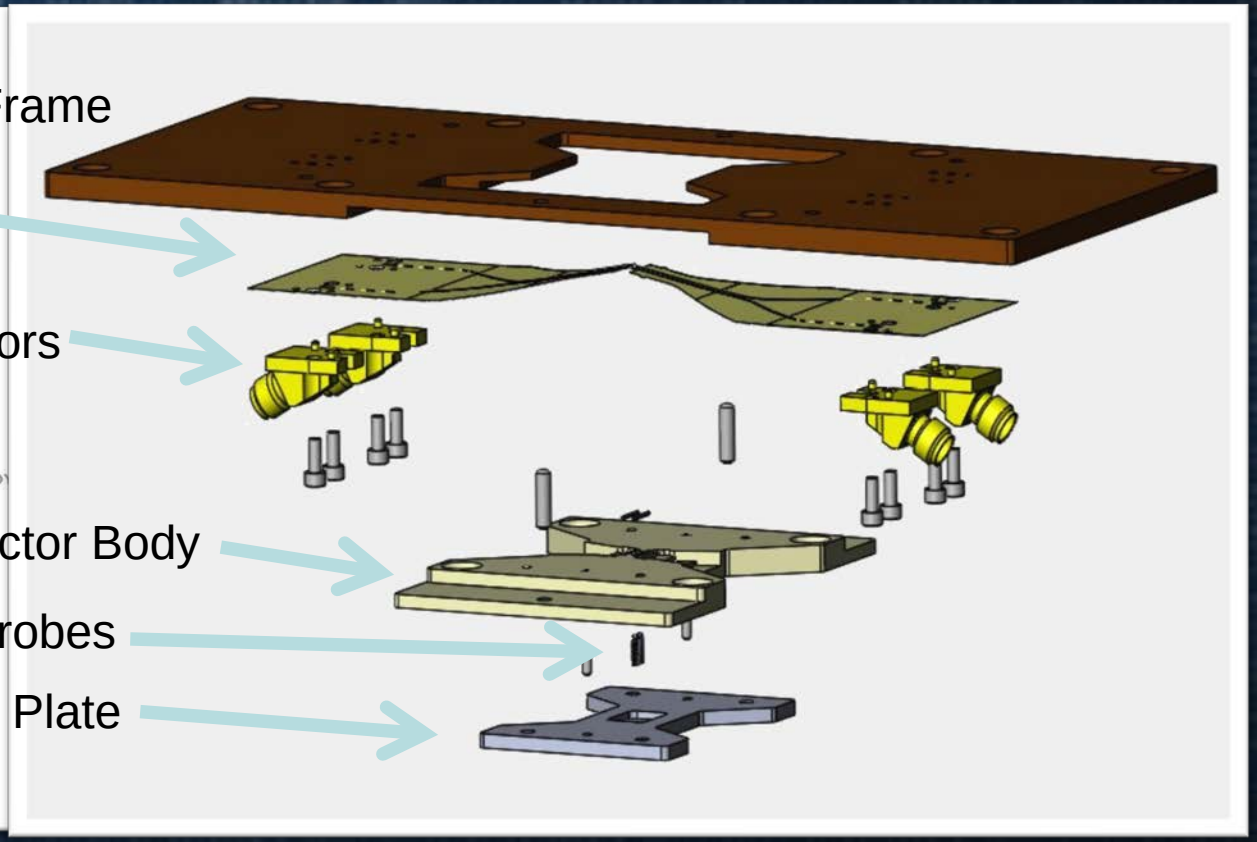
- **Move xWave Technology from package test to wafer probe**
  - Move contact point of leadframe to infinite plane
  - Combine leadframe with fine pitch pogo technology
  - Reduce leadframe features to match bump pitch
  - Reduce leadframe force to limit contact marking on wafer bumps
  - Limit scrub to ensure no ball shear



Package Test vs. Wafer Level Test xWave Comparison

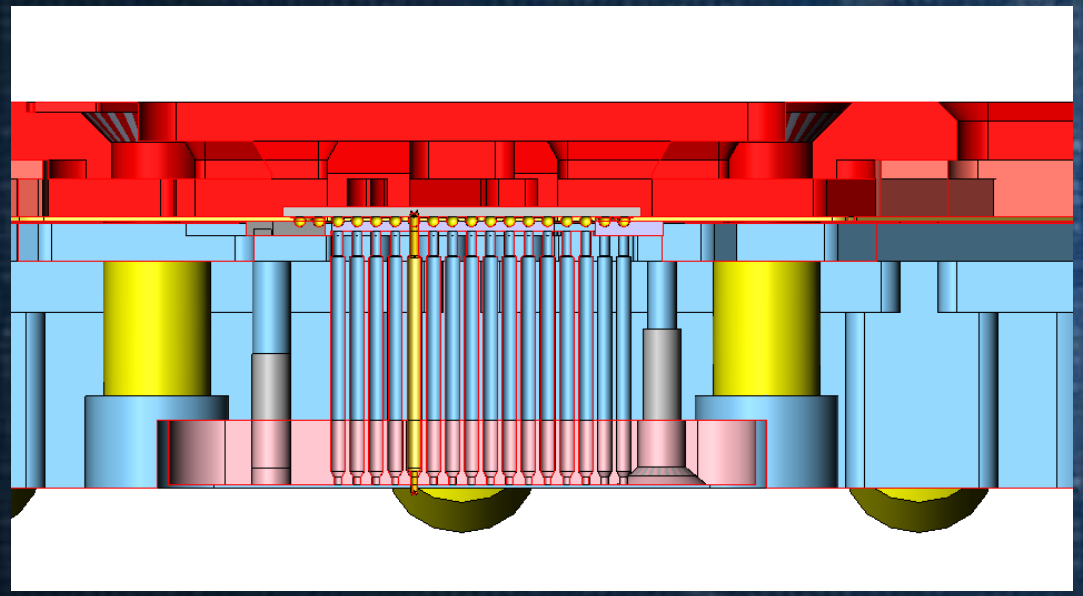
- **Package Test xWave**
- **WLCSP test xWave**

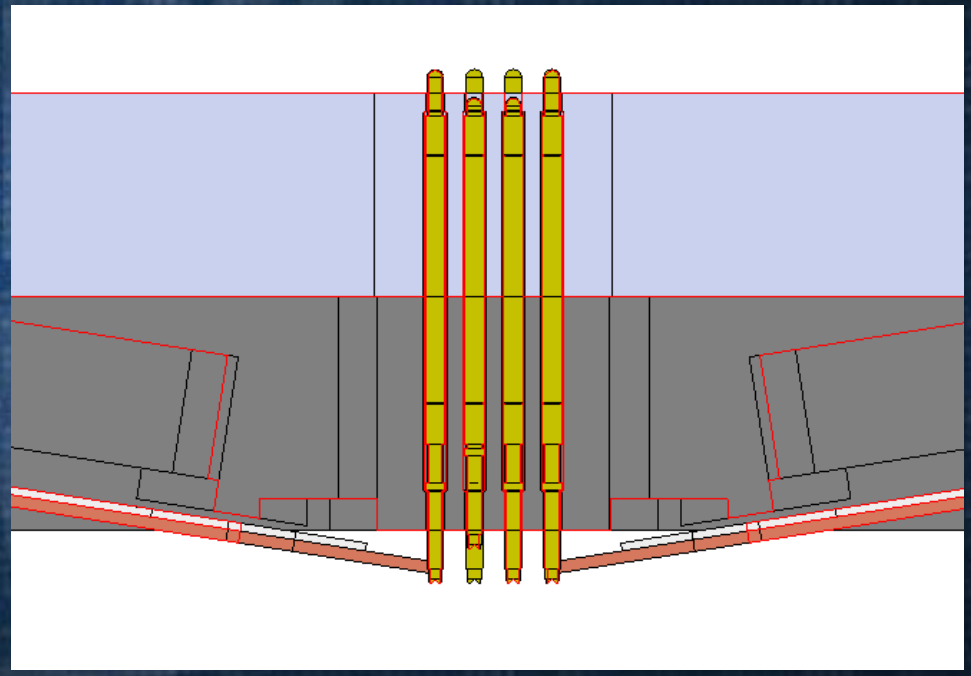




Move contact plane to infinite plane

- From Flat leadframe in DUT pocket to Angled leadframe at infinite plane





- From CSP5 probe to CSP015 probe

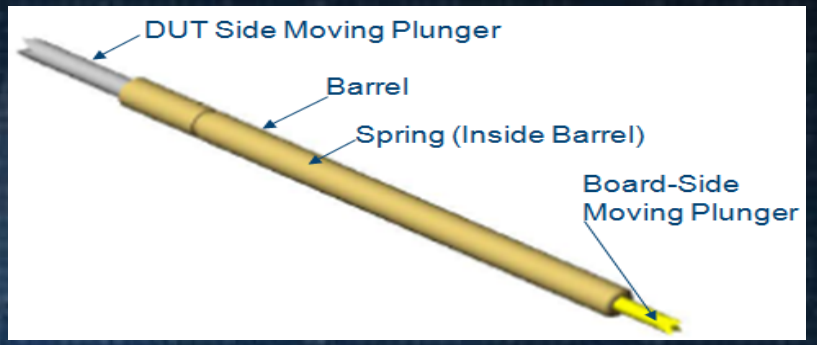
CSP Family of High Performance Tough Probes

Designed for Rugged High Performance

High Reliability, corrects connection between uneven surfaces and satisfies high throughput in mechanically demanding high volume test applications

- Increased durability for heavy duty applications
- Highly customizable size, stroke, and pin count
  - Uneven mating surfaces
  - High tolerance stack-ups
- Easily Integrated
- High current/power device test

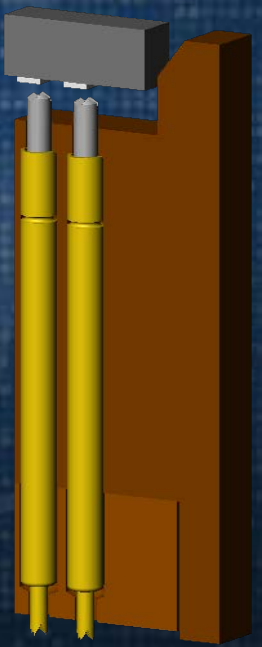




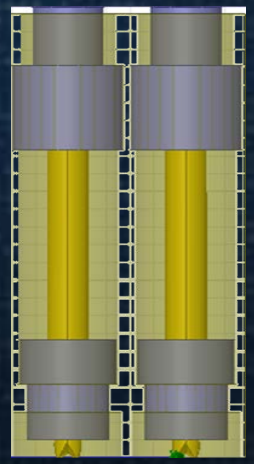
Large compliance window ensures consistent contact

- Large compliance window compensates for less-than-perfect device co-planarity
- Reduced or eliminated false failures due to package warp, interface board bowing, etc

CSP Singulated and Strip Test



ICON - CSP Coaxial

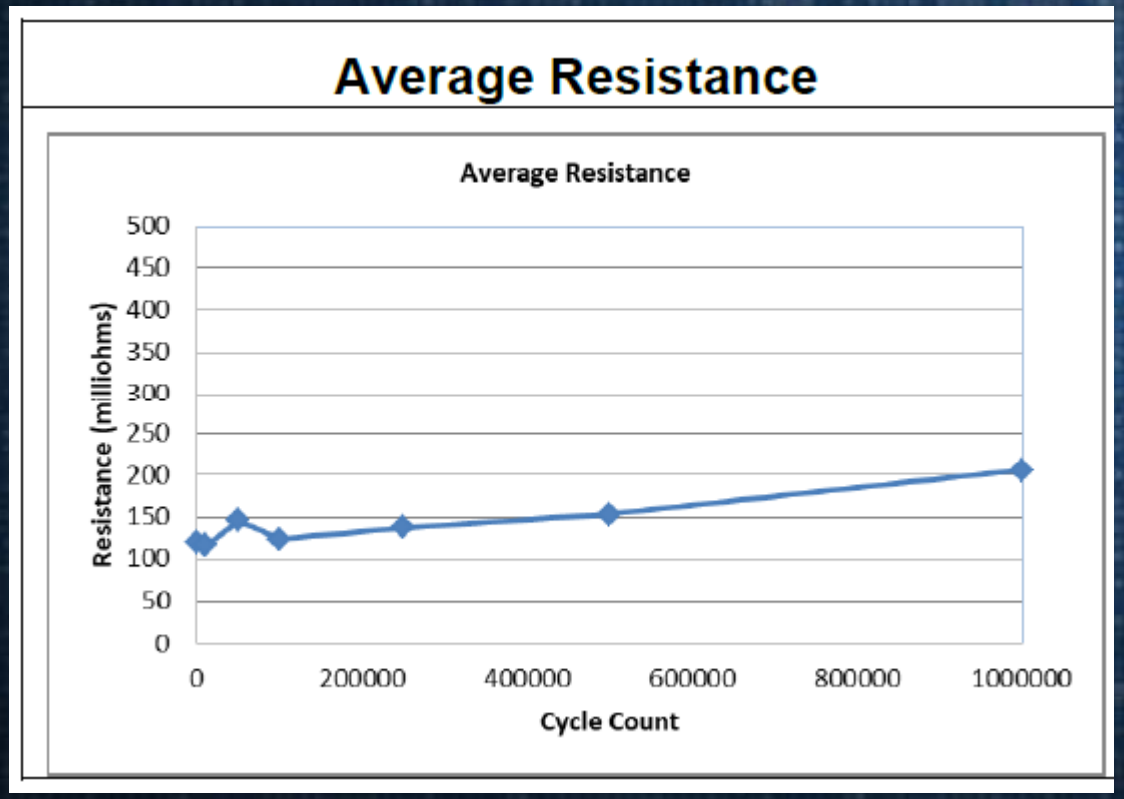


One probe test floor standard

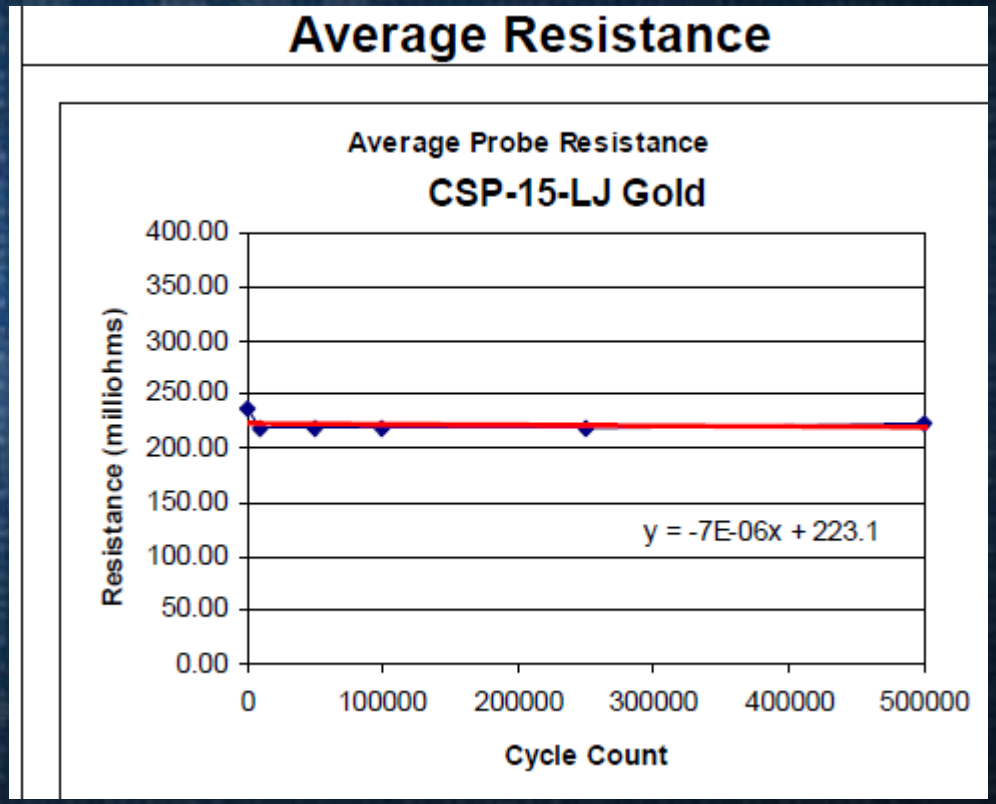
- 0.15 mm, 0.4 mm, 0.5 mm and 0.8 mm pitch

Probe comparison

- CSP5

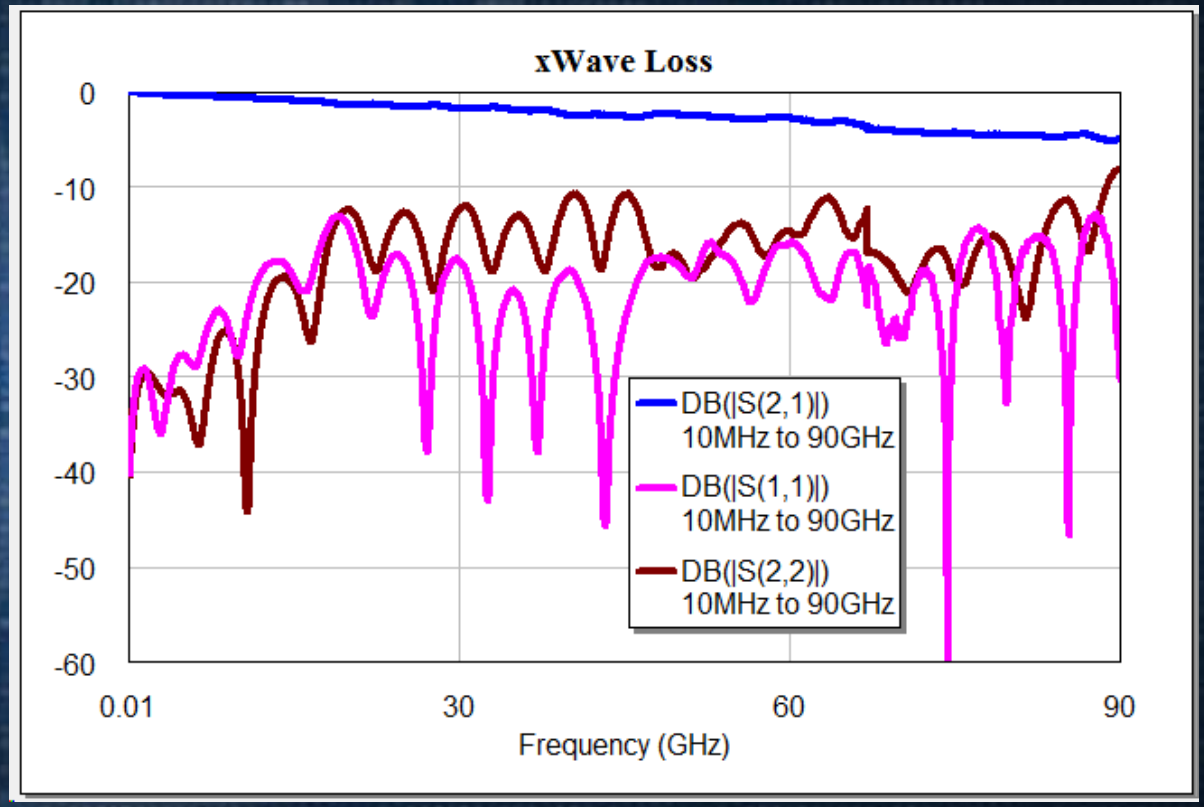


CSP015



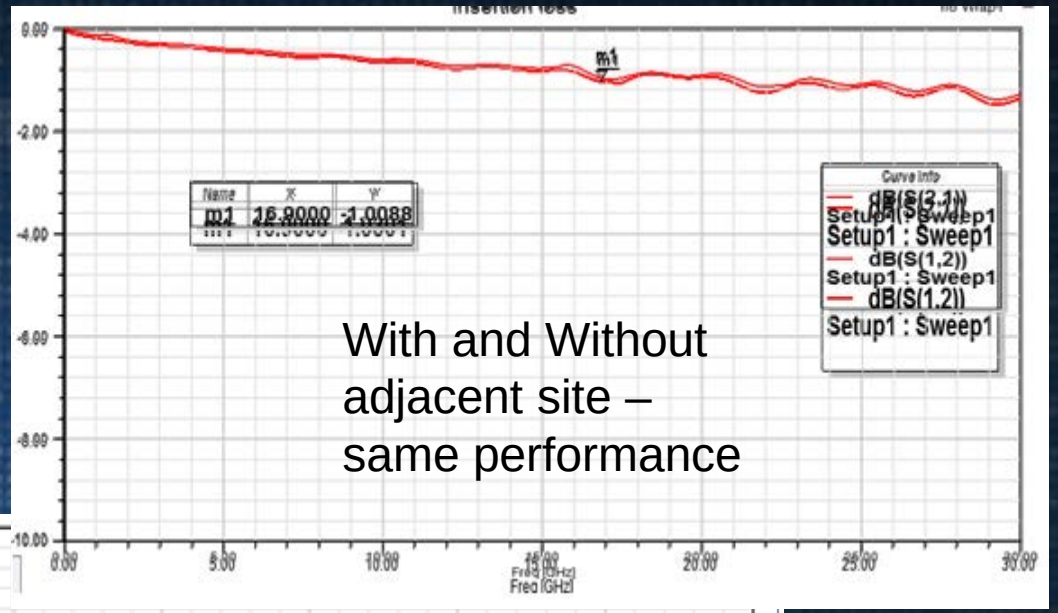
WLCSP xWave Signal Integrity

- **Same Coplanar Waveguide Leadframe structure as package test version except:**
  - Thinner metal
  - Finer pitch
  - Narrower RF leads
  - Smaller ground signal gap
  - Adjacent site solder ball proximity
  - With and without ground wrap

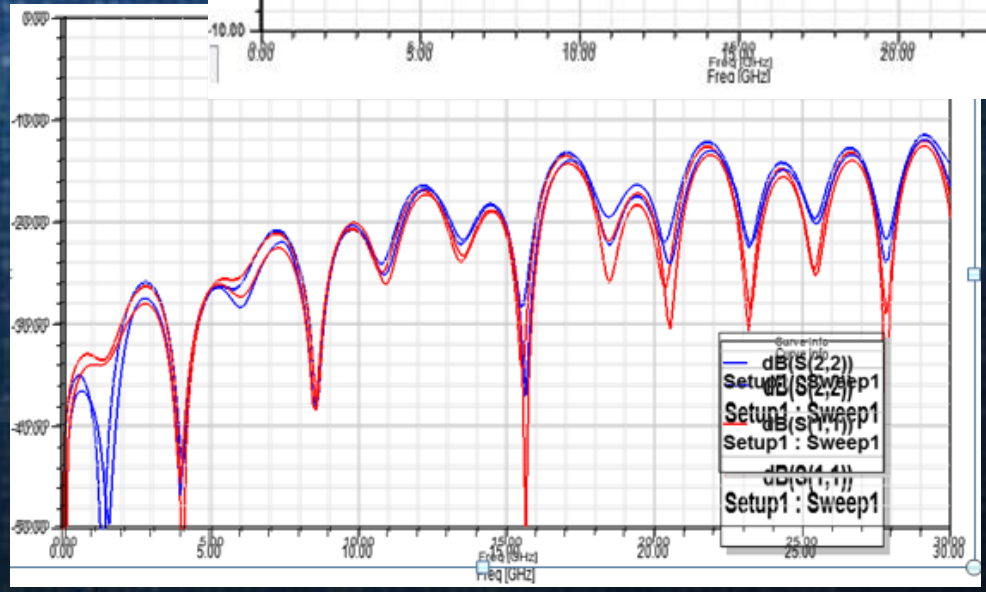


WLCSP xWave Signal Integrity

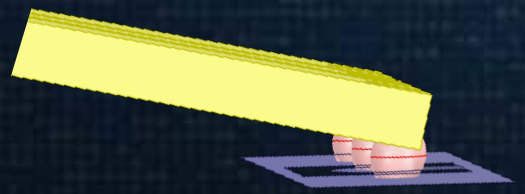
- **Impact of Adjacent site**
  - 15deg angle at free height
  - 5deg angle at test height
  - Proximity of adjacent site to test site
  - Same performance with and without adjacent site



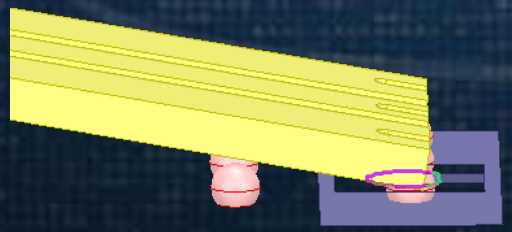
With and Without adjacent site – same performance



No adjacent site

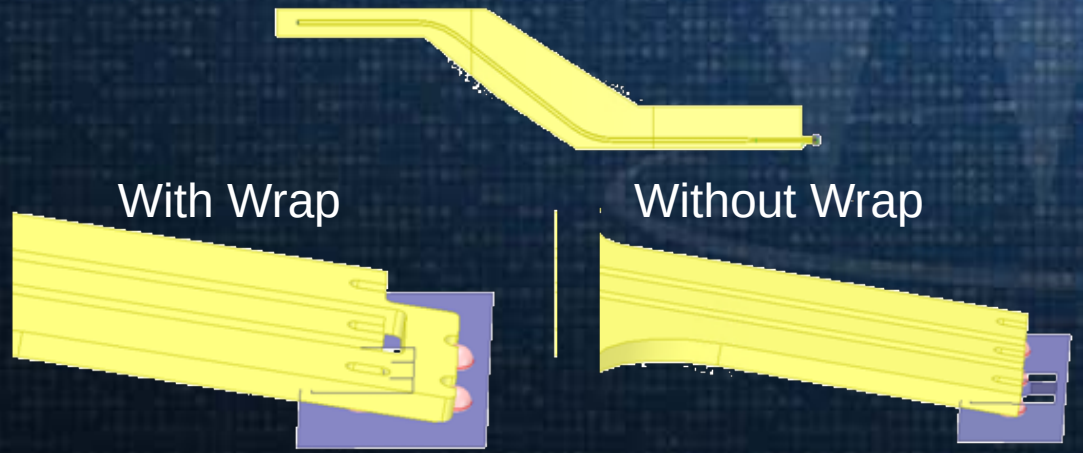


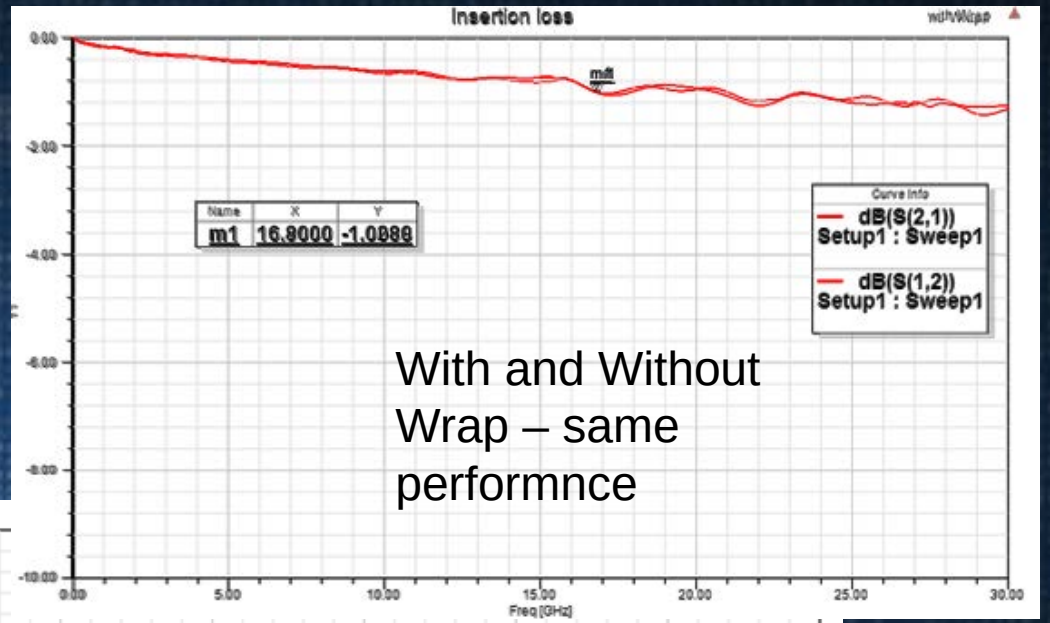
with adjacent site



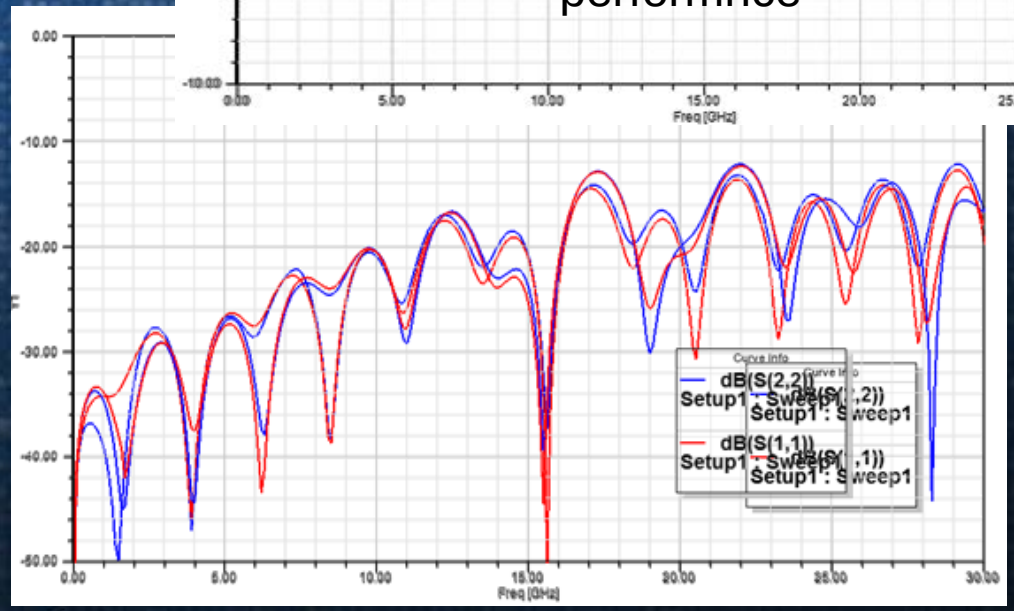
WLCSP xWave Signal Integrity

- **Eliminated CPW ground wrap**
  - Relies on DUT to maintain ground potential on either side of signal lead
  - Same performance with and without ground wrap



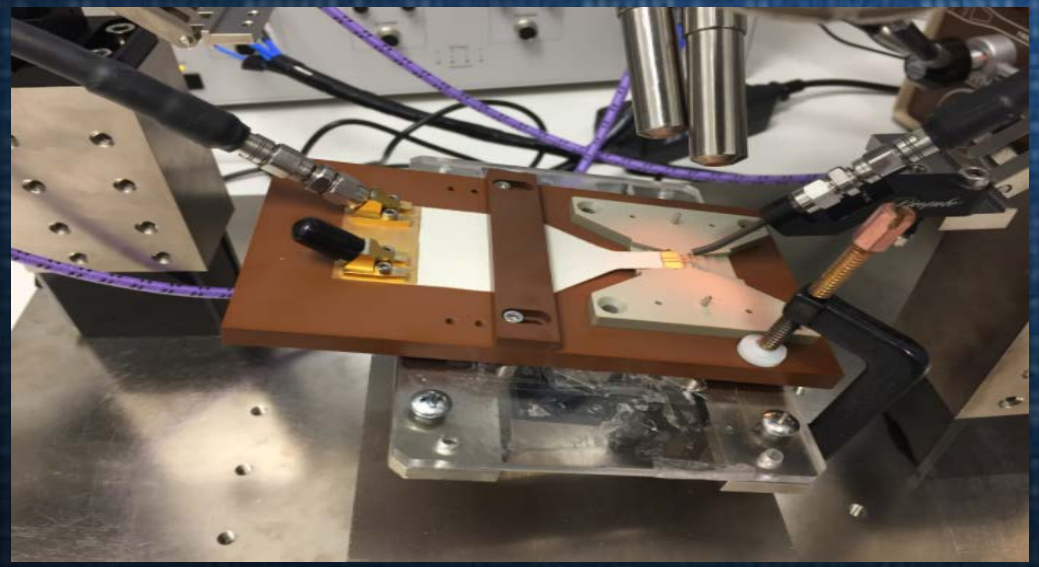


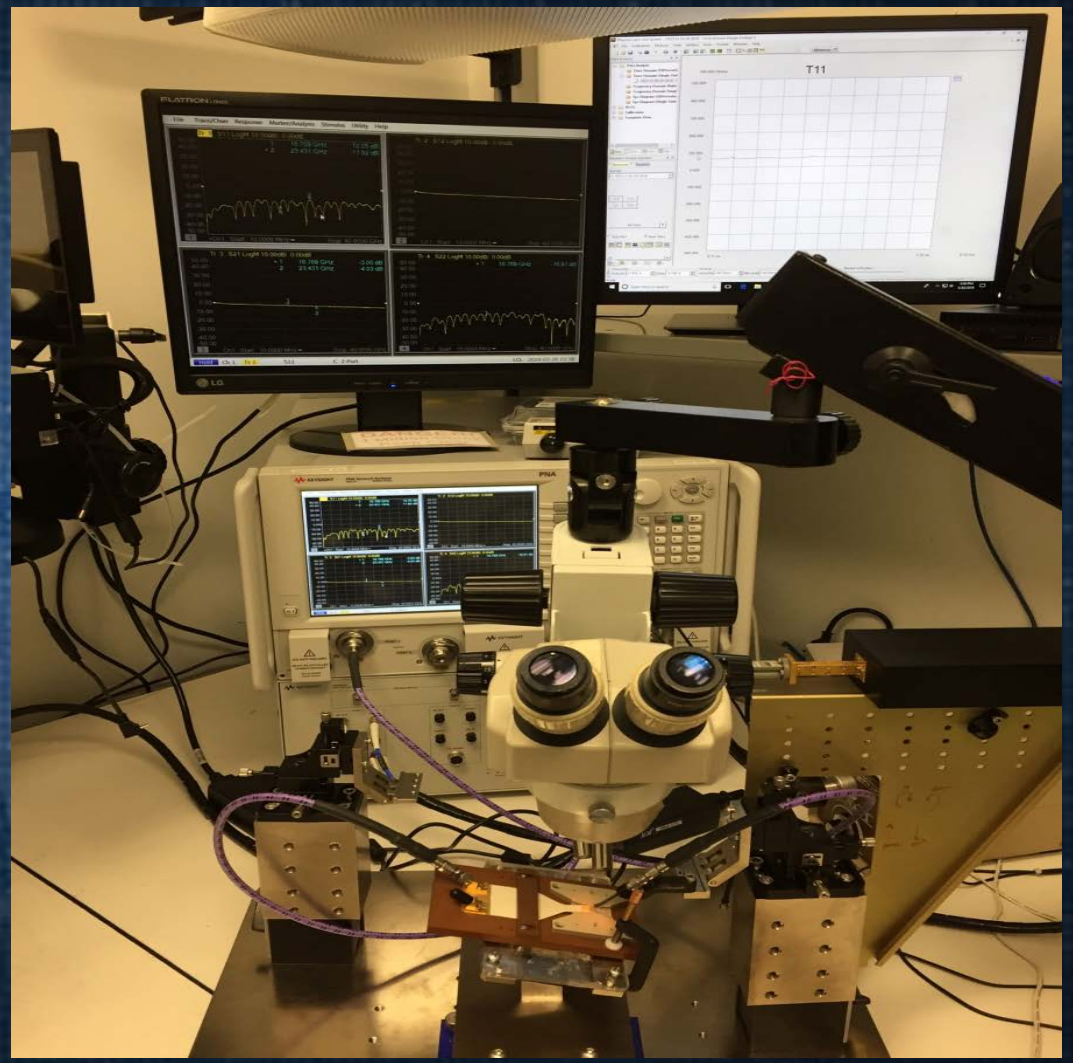
With and Without Wrap – same performnce



xWave Dual Site Probe Card Prototype RF Lab Measurement

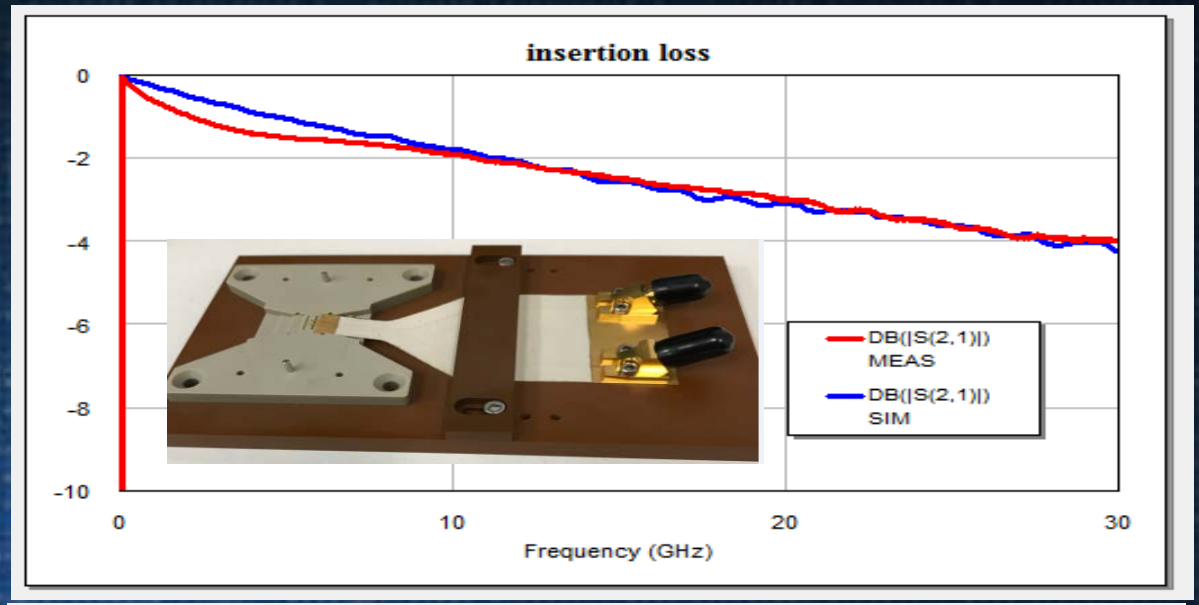


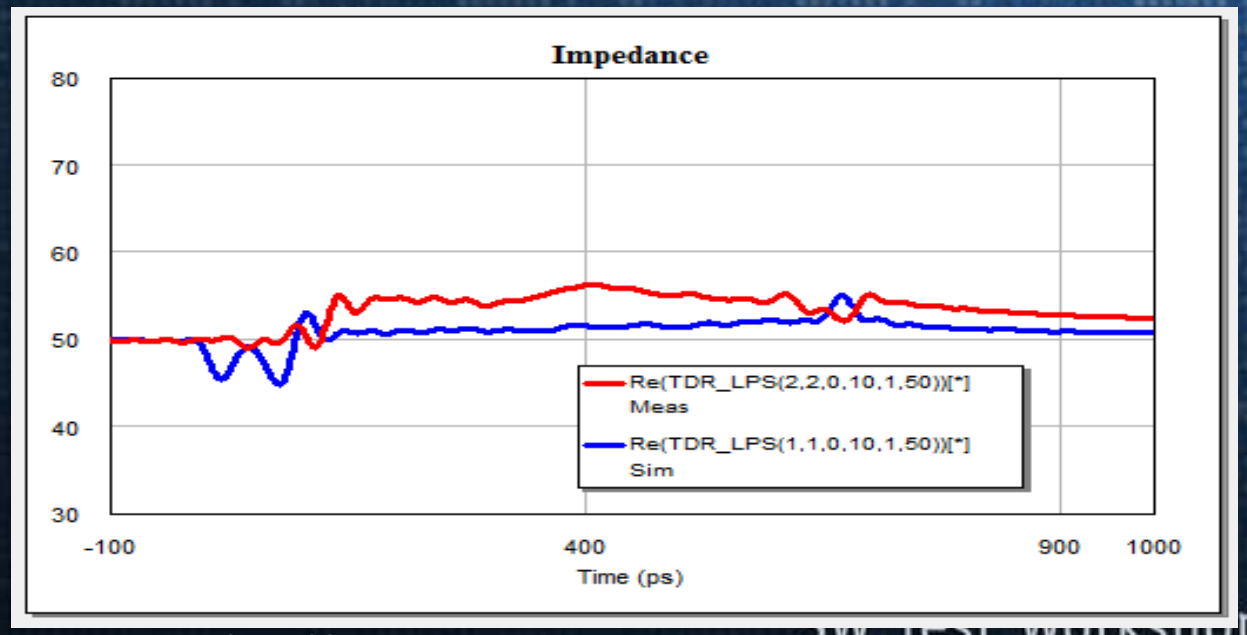


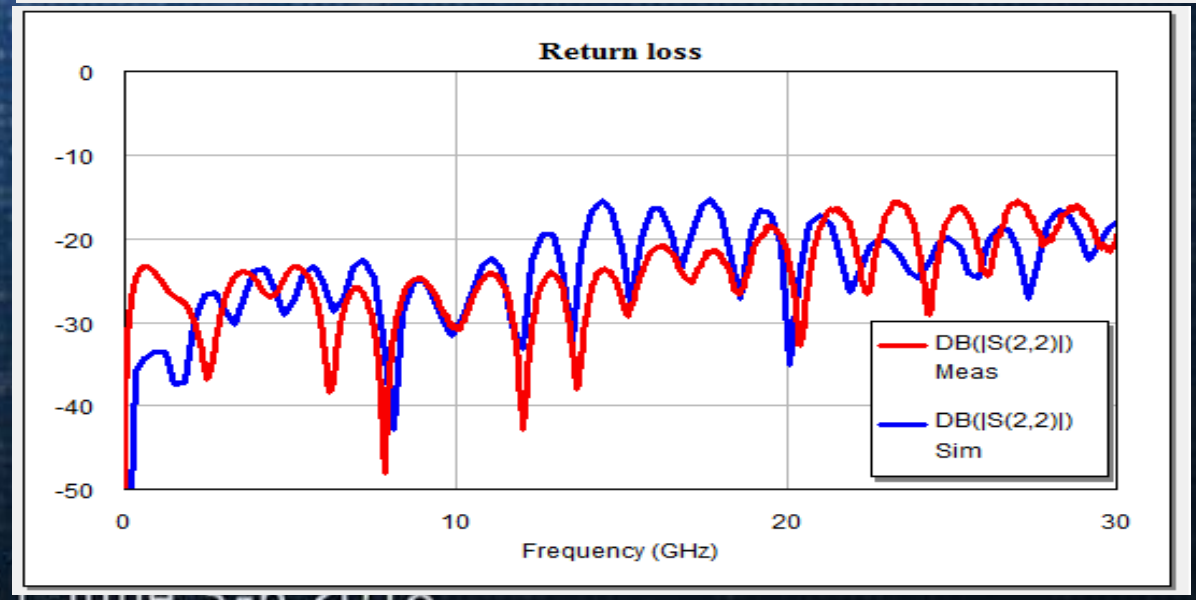


Simulation – xWave Dual-Site Probehead

- Linear Insertion loss linear through 40 GHz
- Return loss less than 15dB
- Impedance Matched within 10%
- Application optimized for 30GHz max frequency
- Technology applicable to 80GHz

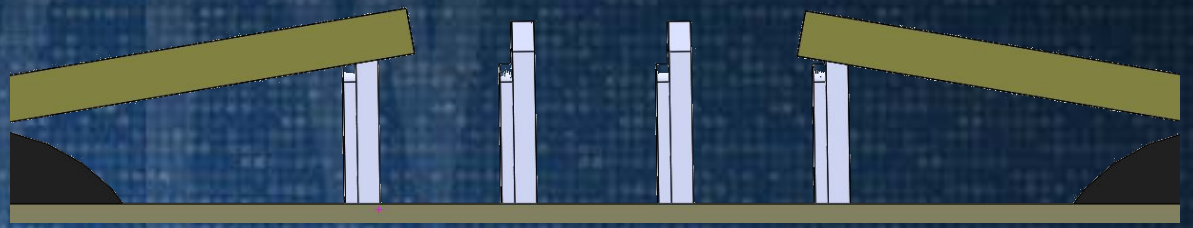


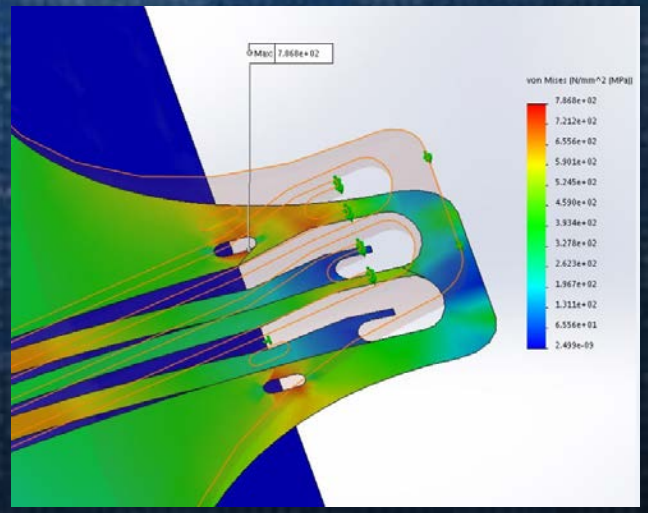




WLCSP xWave Mechanical Design

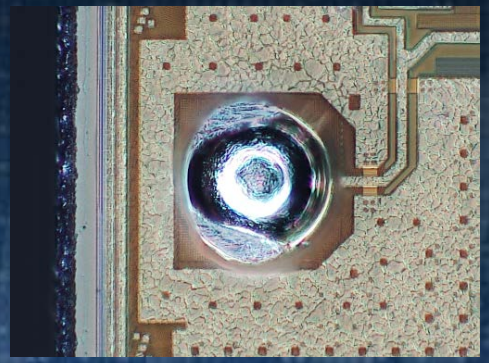
- **Force**
  - Leadframe – 14g @ 150um overtravel
  - Adjustable based on leadframe cross section and cantilever anchor
  - Sufficient force without spring damper
- **Thermal**
  - Designed for Tri-Temp
  - Same materials as standard xWave
  - All materials match CTE

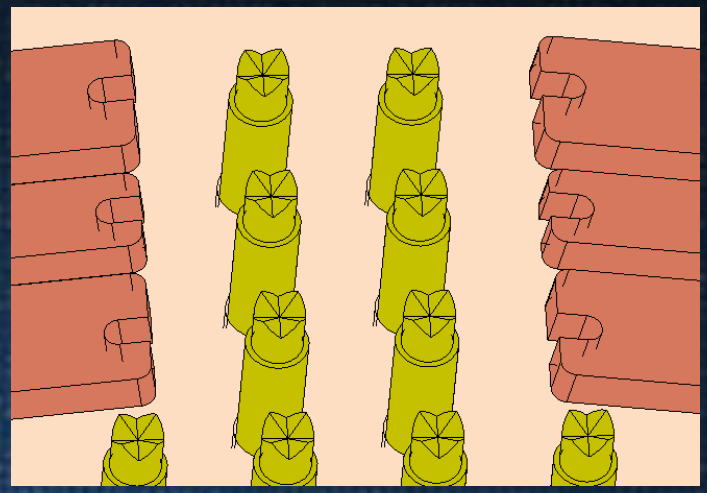


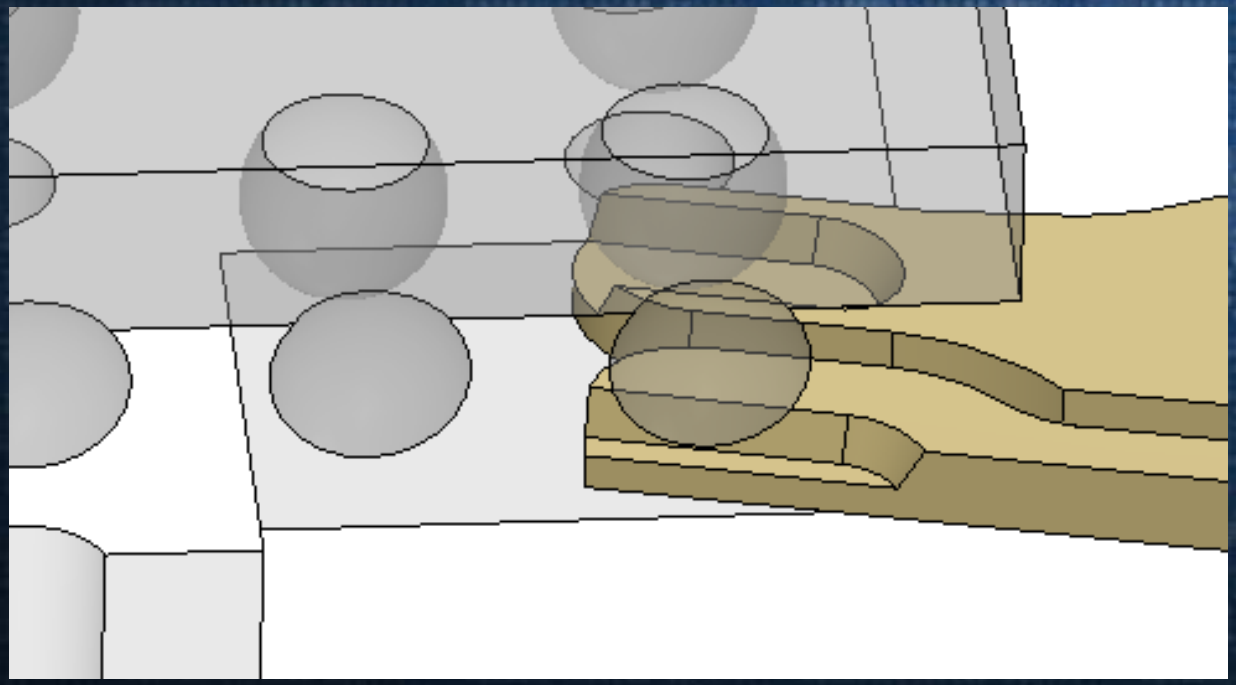


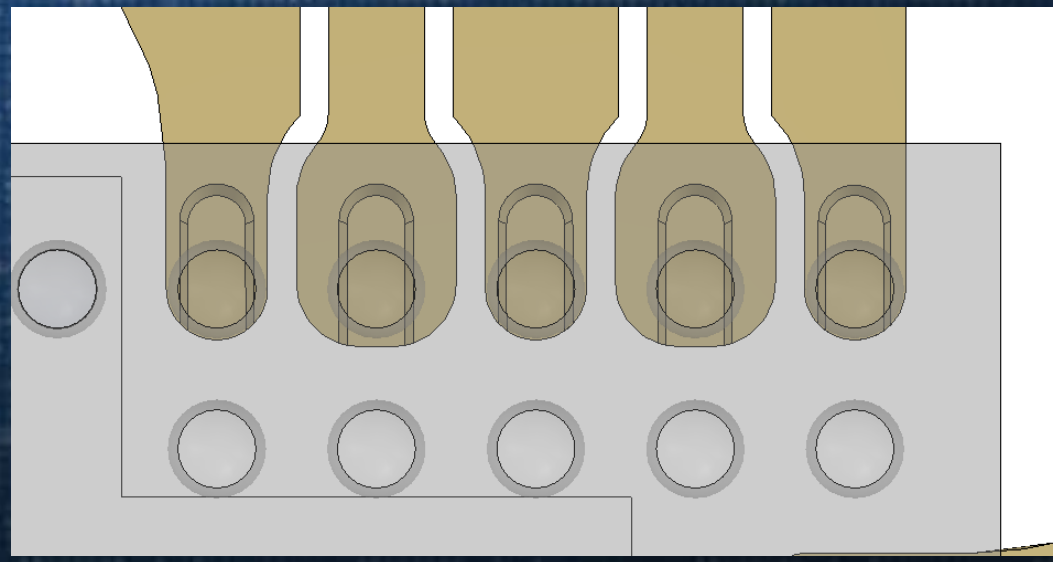
WLCSP xWave Mechanical Design

- **BGA Contact feature**
  - Leadframe - U shape edge contact to ball
  - ~10um knife edge scrub
  - Pogo – 4 point crown



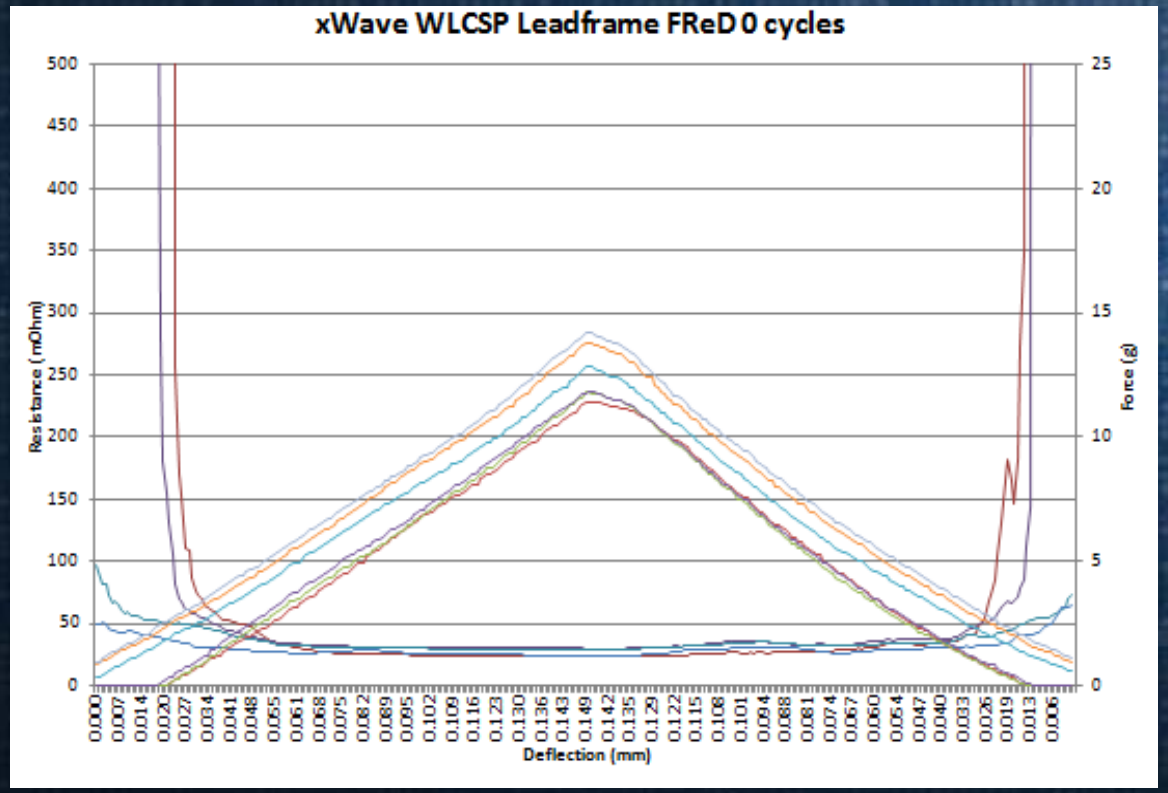


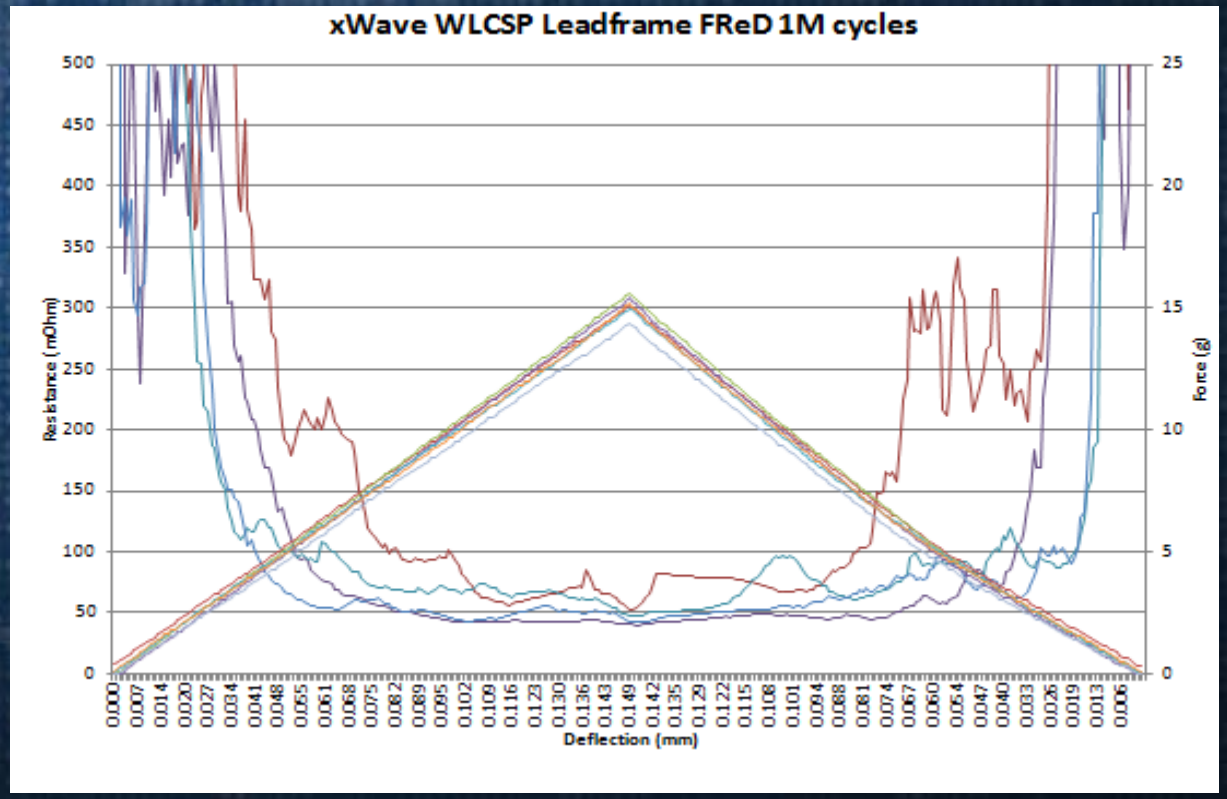




WLCSP xWave Life Cycle

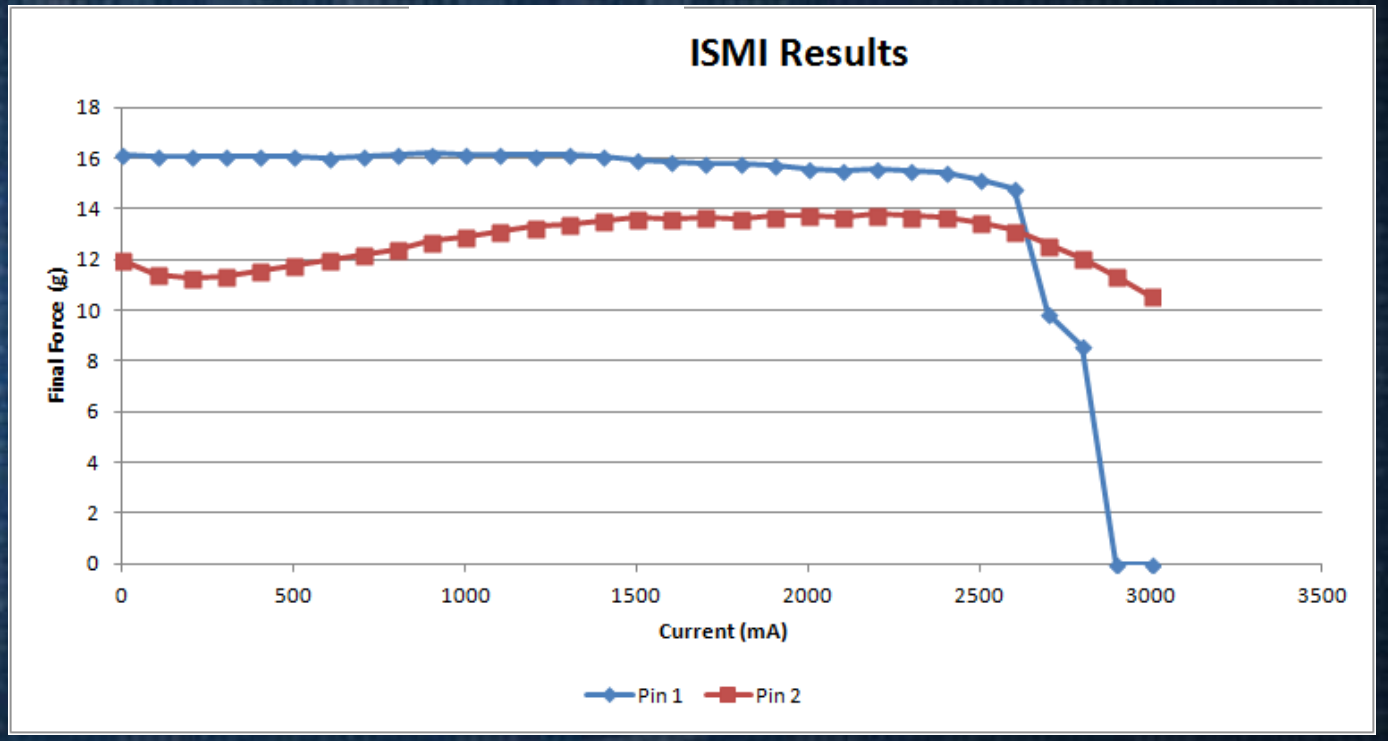
- Stable low contact resistance through 1M cycles
- No force degredation over 1M cycles





WLCSP xWave DC Performance

- **Current Carrying Capacity**
  - 2.6A based on ISMI method
  - Limited testing
  - Pressure applied to signal lead only
  - Expect higher current carrying capacity when deflecting grounds and signals



Package Test and Wafer Test in 1

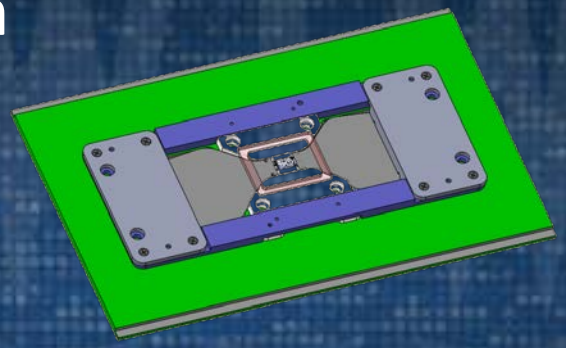
- **Same hardware can be used for both packaged test and wafer test**
  - Manual Alignment Frame (MAF) attaches to Probe head to convert to final test
  - Manual Actuator (MA) attaches to MAF
  - Simple change over from Wafer to Packaged parts for QA or RMA's

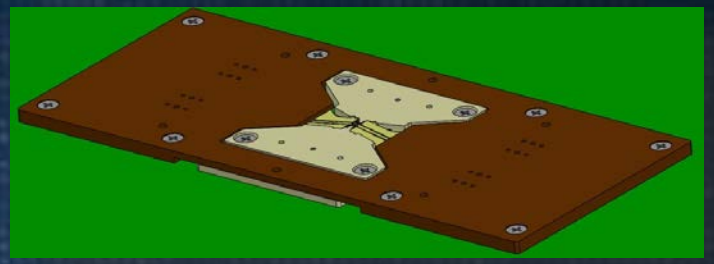
Summary/Conclusion

- 5G, ADAS, Wireless, Satellite cmWave and mmWave markets growing rapidly and moving from package to WLCSP at speed
- WLCSP xWave is based on the same technology that's proven in the field to 1.5M cycles and going
- Overcame infinite plane and force profile to take the xWave technology from final test applications to wafer test.
- Optimized signal path for the best signal integrity
- Test data shows similar excellent performance expected from Wafer Level version of xWave

Follow on work

- **2 ongoing Beta sites**
  - Dual site 16 lead 250um pitch Ku/Ka band (12-40GHz)
  - Single site 150 lead 180um pitch 5G (28GHz)





Item	January					February				March				April				May				June			
	W01	W02	W03	W04	W05	W06	W07	W08	W09	W10	W11	W12	W13	W14	W15	W16	W17	W18	W19	W20	W21	W22	W23	W24	W25
Probe Card Design / Build / Test Tasks																									
Initial Probehead Design																									
Prototype Probehead Build / Manufacturing																									
Prototype RF Testing																									
Prototype Mechanical Testing																									
Receive PO for Probe Card (Probehead FOC)																									
PCB Design / Build (PCB Vendor)																									
Optimize Beta Probehead Design																									
Approve Beta Probehead Design																									
Beta Probehead Build/ Manufacturing																									
Beta Probehead RF + Mechanical Verification																									
Beta Probe Card Assembly																									
Beta Probe Card Delivery																									



SW Test Workshop

Semiconductor Wafer Test Workshop

TPEG™ MEMS RF+ Technology for Vertical Probe Heads



Tommaso Masi *Technoprobe*

Alberto Berizzi *Technoprobe*

June 3-6, 2018

Outline

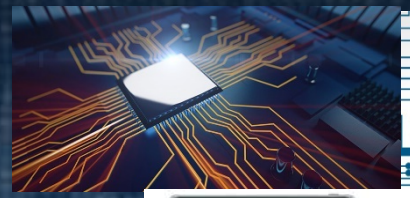
- Introduction
- Technoprobe TPEG™ RF+ architecture
- Production test vehicle
- Modeling data
- Internal experimental validation data
- Conclusions
- Future work

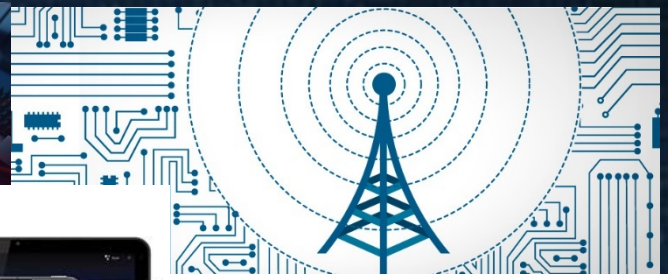
Introduction

- **Standard vertical probe heads do not have satisfactory RF properties.**
  - On the other hand, they offer a series of advantages over other typical RF technologies based on flexible membranes.

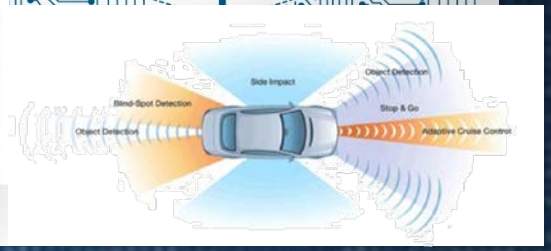
- **Technoprobe developed a new PH architecture that provides excellent RF properties based on TPEG™ MEMS vertical PH technology.**
  - This technology improves the return loss (RL), the insertion loss (IL), as well as the other RF related specs…..up to 10 GHz
  - The enhanced RF performances are obtained thanks to additional GND paths inside the PH connected both to the GND of the device and to the space transformer, to control signal impedance

PC Market Segments : High Speed and RF









Probes: High Speed Challenges

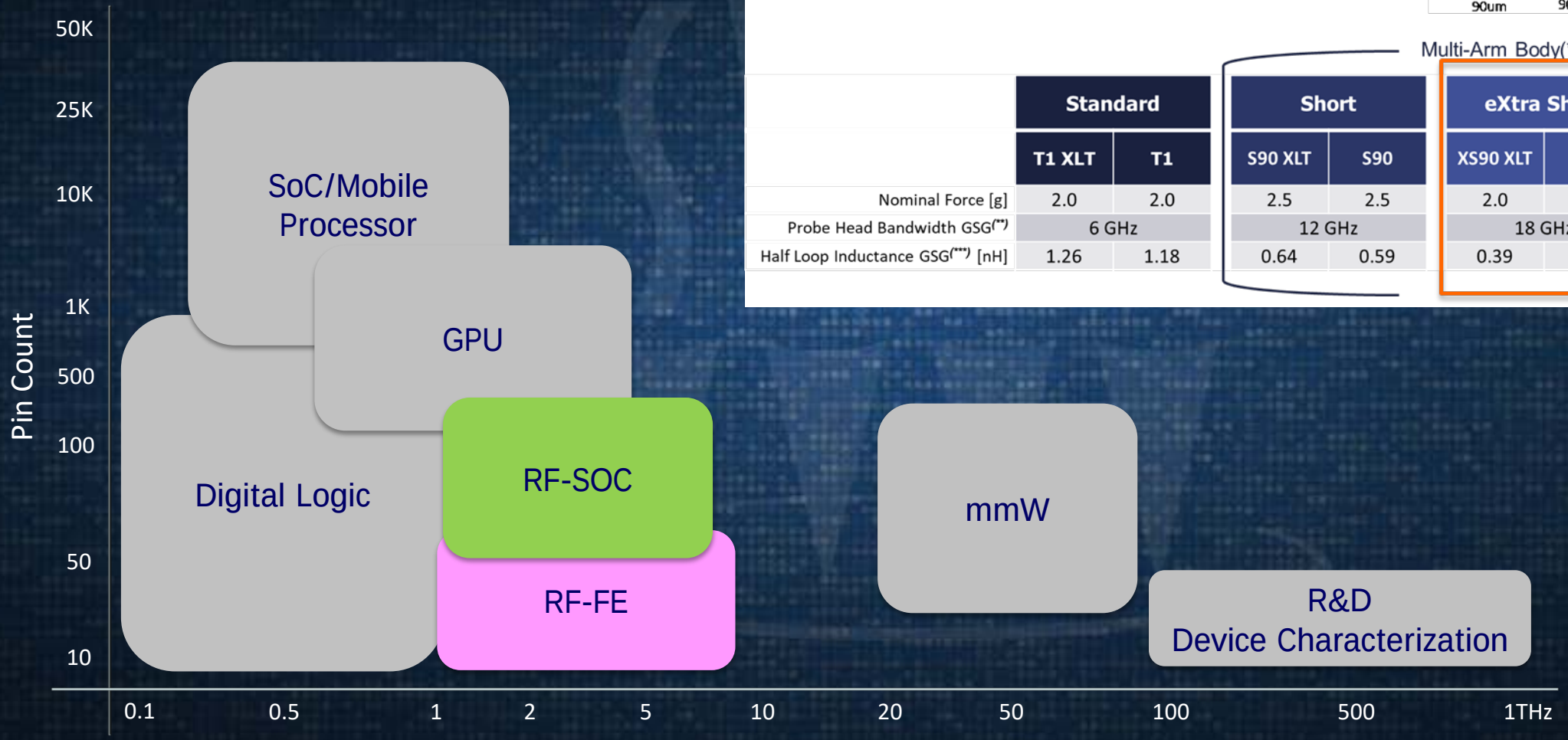
- **Challenges:**
  - Probe cards struggle between having a long needle to optimize the mechanical performance and a short needle to optimize the frequency performances
  - Shorter needles will generate higher forces than ideal
- **Technoprobe Solution: Vertical MEMS Probe Head**
  - Multi-arm needle body allows shorter needles and maintains standard forces

	Standard		Multi-Arm Body(*) Short		eXtra Short		Ultra Short
	T1 XLT	T1	S90 XLT	S90	XS90 XLT	XS90	F90(4*)
CCC [mA]	820	820	1100	1100	1000	1000	1000
Resistance [mΩ]	142	133	59	54	51	46	31
Half Loop Inductance GSG(***) [nH]	1.26	1.18	0.64	0.59	0.39	0.35	0.23

(*) *Technoprobe has licensing rights to use Multi-Arms Patent*

(4*) *in development*

RF-SOC and RF Front End: Available TP Technology





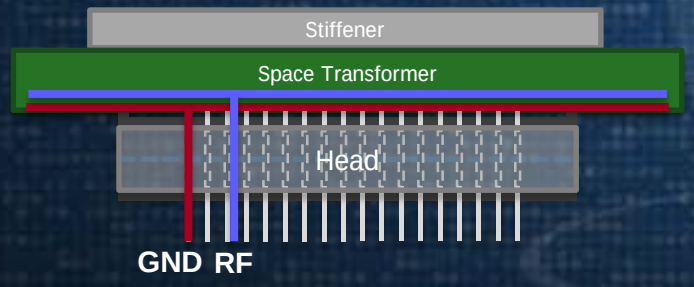
Multi-Arm Body(*)

	Standard		Short		eXtra Short		Ultra Short
	T1 XLT	T1	S90 XLT	S90	XS90 XLT	XS90	F90(4*)
Nominal Force [g]	2.0	2.0	2.5	2.5	2.0	2.0	2.0
Probe Head Bandwidth GSG(**)	6 GHz		12 GHz		18 GHz		24 GHz
Half Loop Inductance GSG(***) [nH]	1.26	1.18	0.64	0.59	0.39	0.35	0.23

TPEG™ RF architecture – Patent Pending

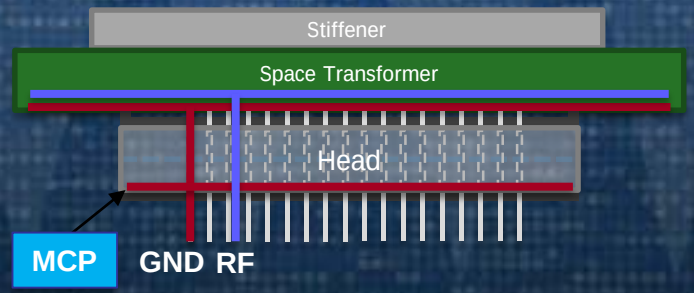
- **Challenge:**
  - RF device layouts are not optimized for RF probing and often short needles are not enough to match RF performance required by customer's application
- **Technoprobe Solution (RF and RF+):**

Standard Architecture



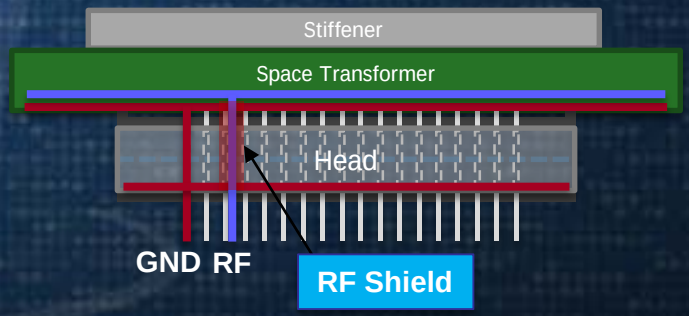
- GND and RF Signals are not matched for all the length of the needles creating not optimized IL, RL and LI (Loop Inductance)

RF Architecture
(Patent pending)



- GND plane is added closer to the DUT thru TP proprietary MCP technology (Multi-Conductive-Plates) optimizing GND noise and LI

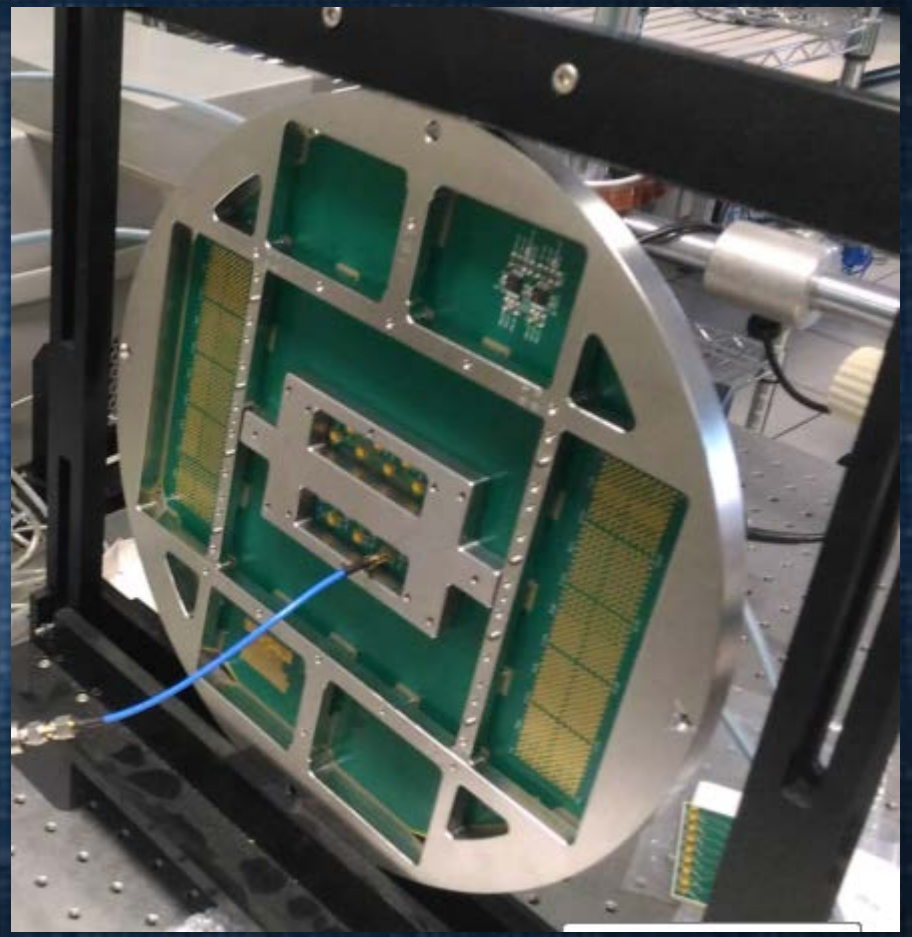
RF+ Architecture
(Patent pending)



- Shield is created around RF signals inside the head using TP proprietary SRF technology (Shield-RF) optimizing IL, RL, LI and GND noise

Production test vehicle

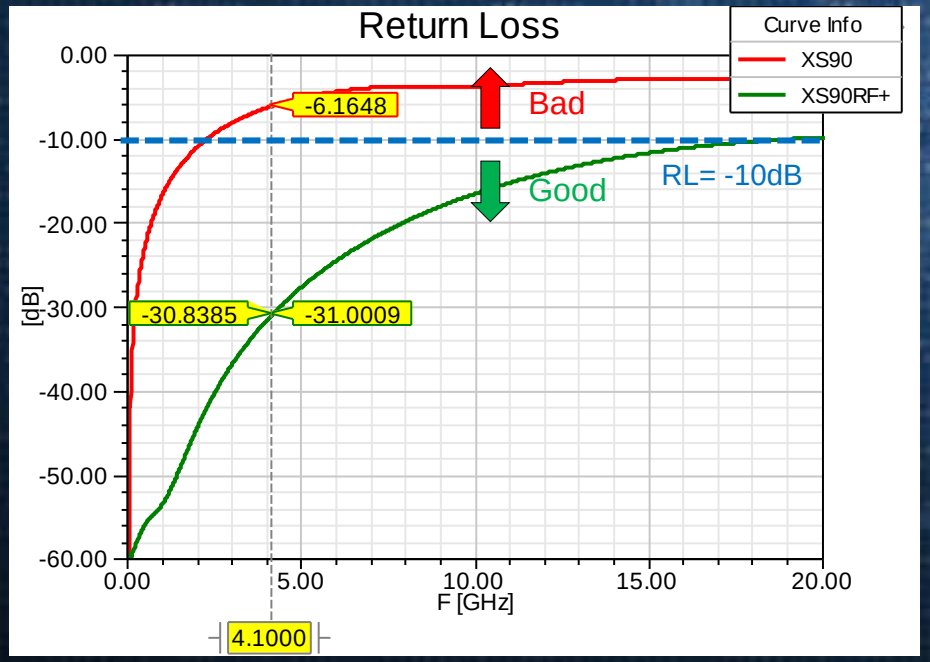
- **Device**
  - SAW filter
  - Pitch is 370 µm and uses minimal grounding
  - 4 pins / DUT: IN, OUT and 2x GND
- **Probe card**
  - Probing x8 diagonal pattern
- **Tester platform**
  - UltraFLEX 300mm with RF interface (LEGO block)
- **RF requirement**
  - Required filter response mask given by customer

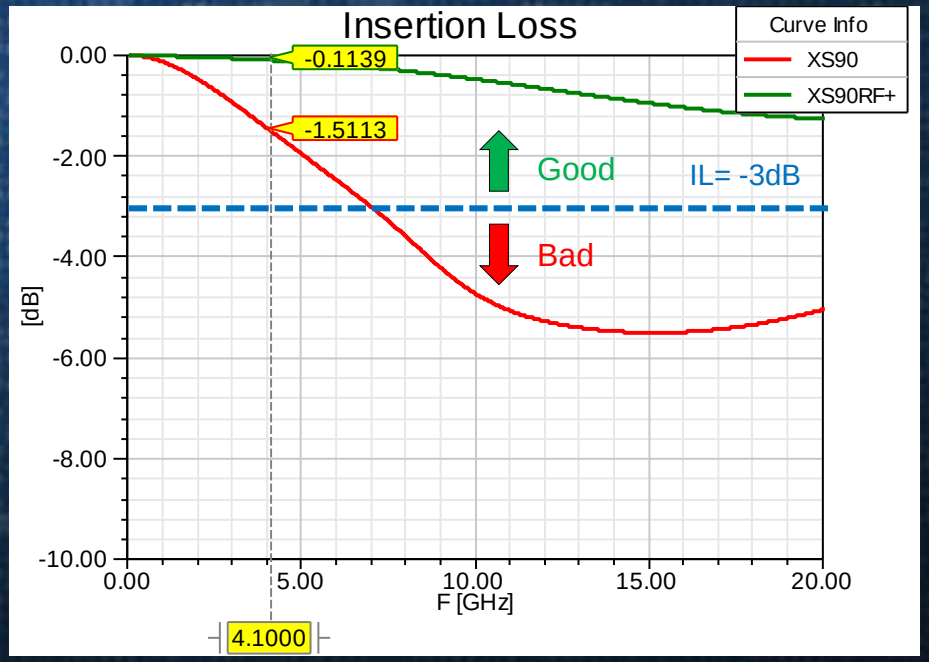


Modeling Data

PH only

- **RF+ architecture based on TPEG™ MEMS XS90 probing technology allows to improve frequency performances**
- **FEM 3D simulation of standalone probe head was performed:**
  - Both return loss and insertion loss show significant improvement
  - Filter response is in spec with respect to customer proprietary filter s-parameter model





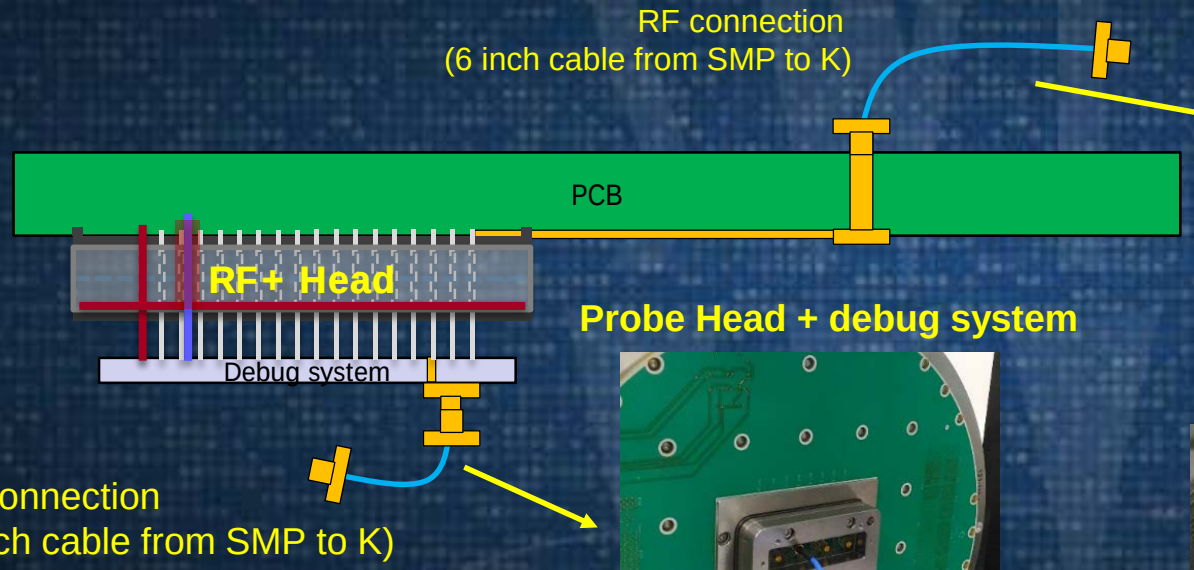
Experimental data

- **Three different experimental setups have been used**
- **RF characterization**
  - RL and IL measured with test fixture and VNA up to 20 GHz
- **DC tests with dedicated wired space transformer**
  - DC continuity test with prober
  - Leakage test on probe card analyser
- **RF tests on prober**
  - Probe card was tested on customer wafer filter (Filter shape under IP no sharable results)

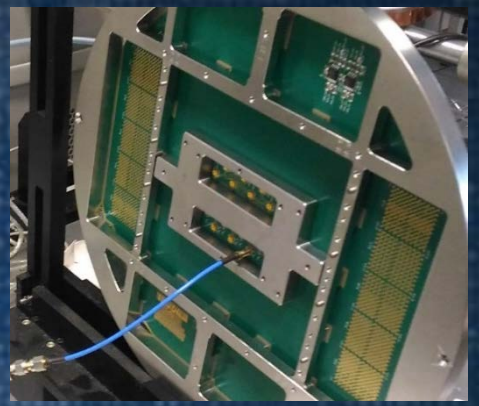
RF Characterization

Experimental setup

- **Measure system fixture for RF+ architecture**



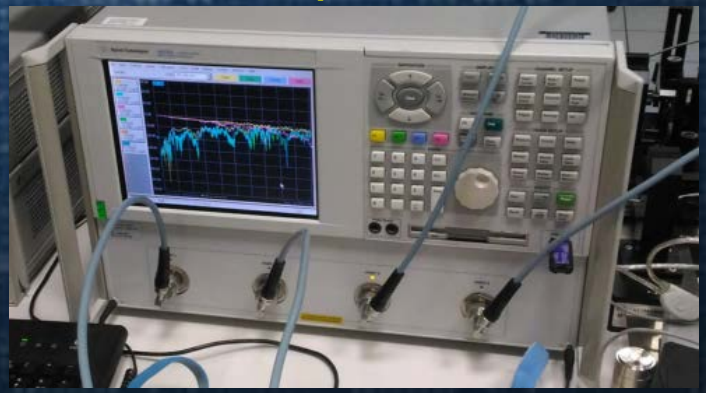
Probe card tester side view



Probe Head + debug system

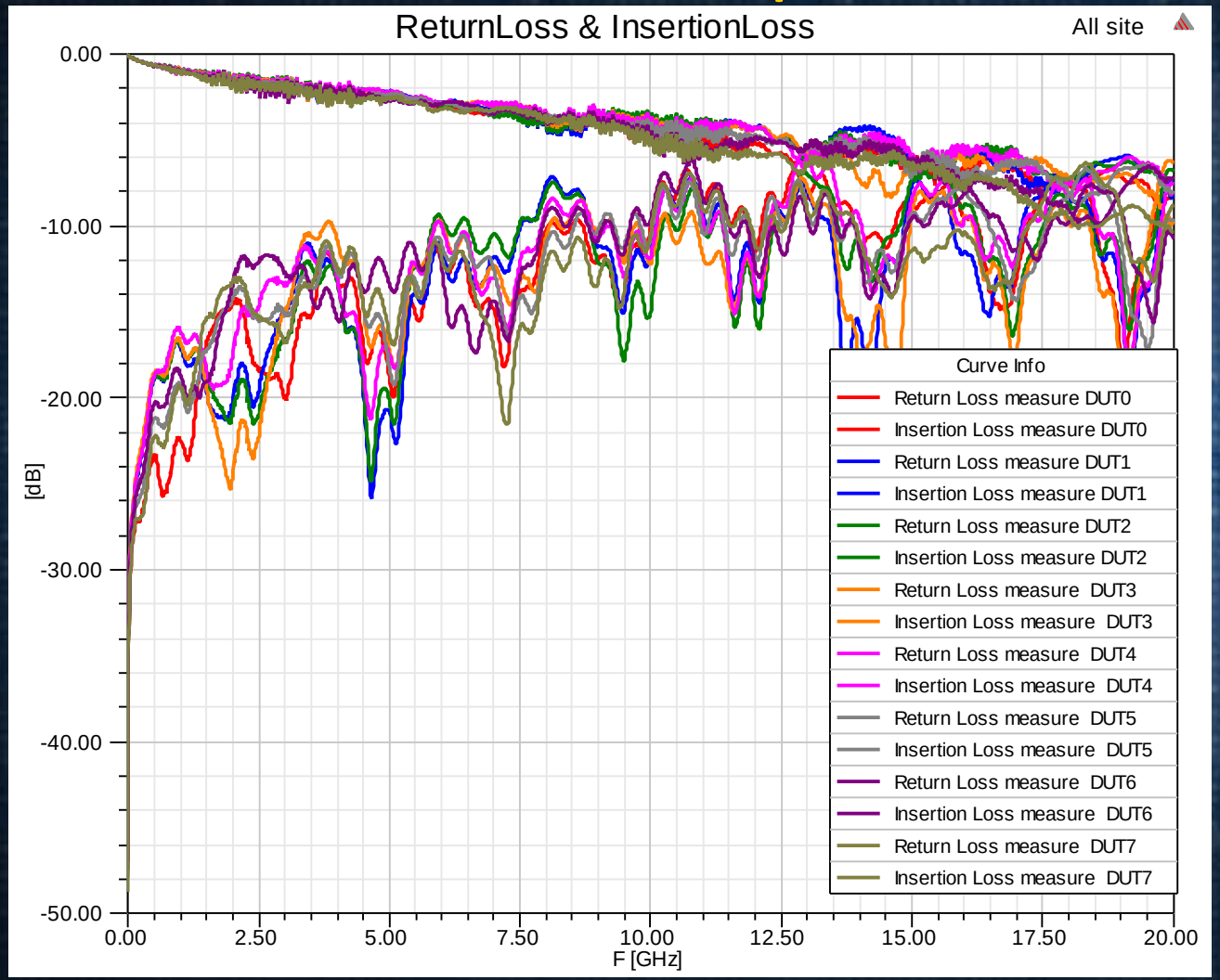


VNA up to 20 GHz



RF Characterization

Experimental results: RL and IL

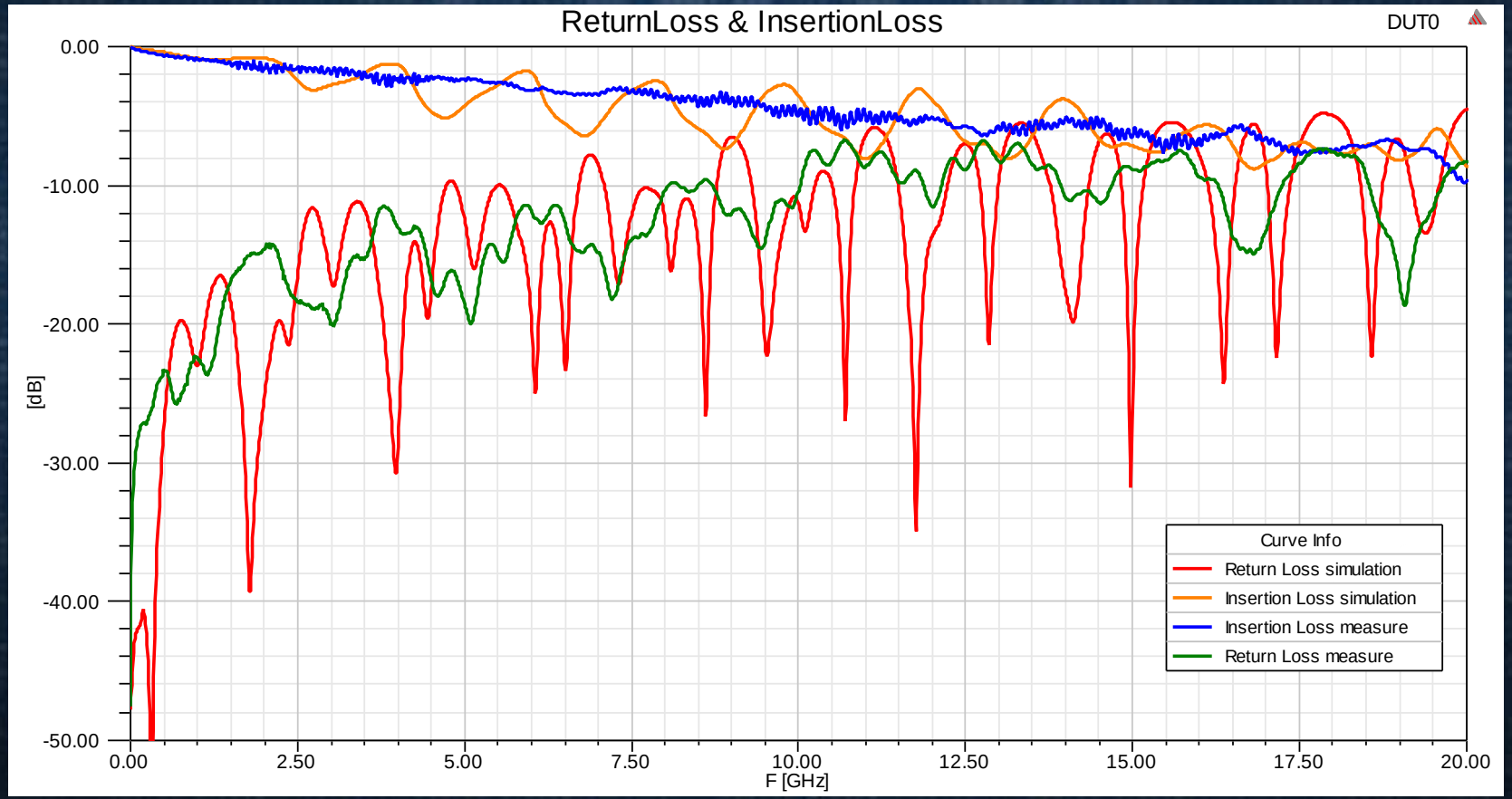


- All 8 sites show similar value of return loss and insertion loss
- Differences are given by PCB design
- Maximum working frequency is 8 GHz because of PCB design: filter device have to work DC to about 5 GHz
- From simulation with higher performance PCB, RF+ architecture is able to work up to 10 GHz (or more)

RF Characterization

Experimental vs. Simulation results

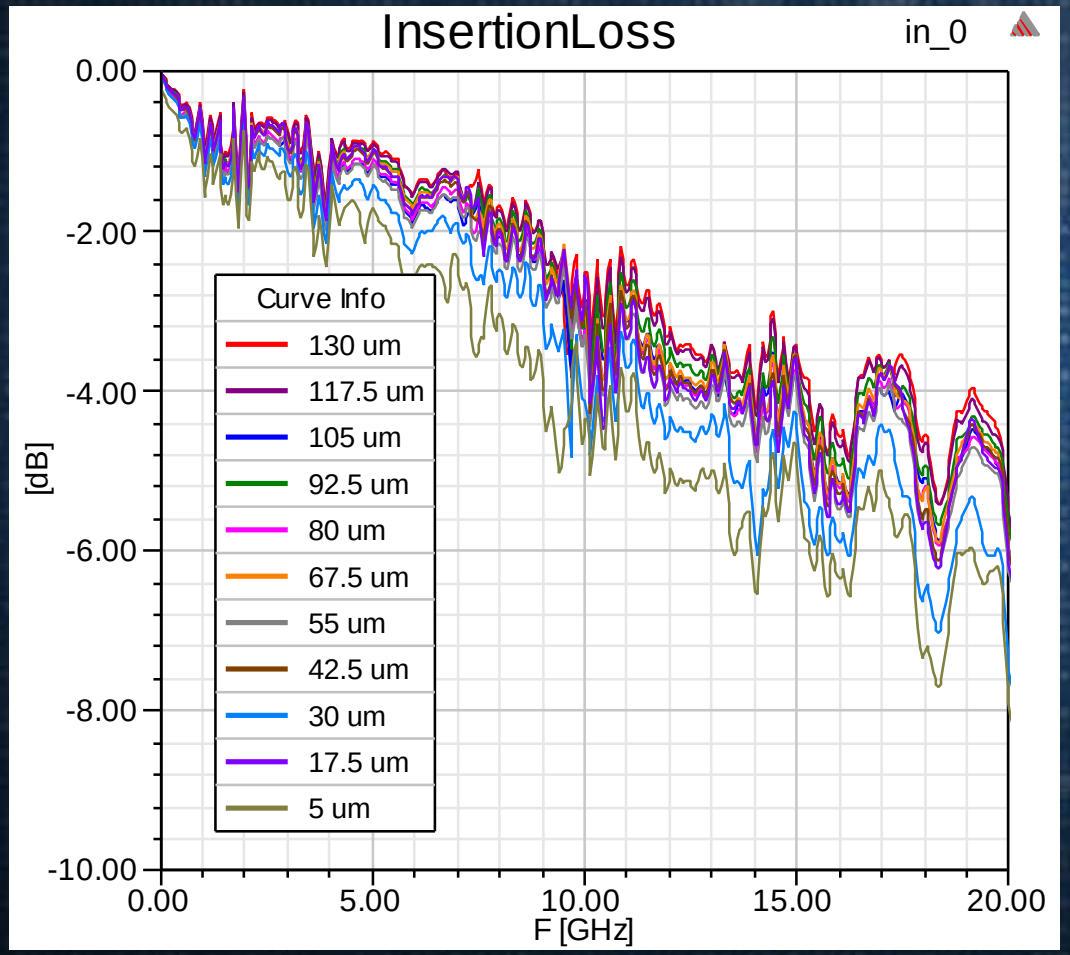
- **Comparison between simulated and measured results allowed to validate the consistency of 3D FEM simulation models**

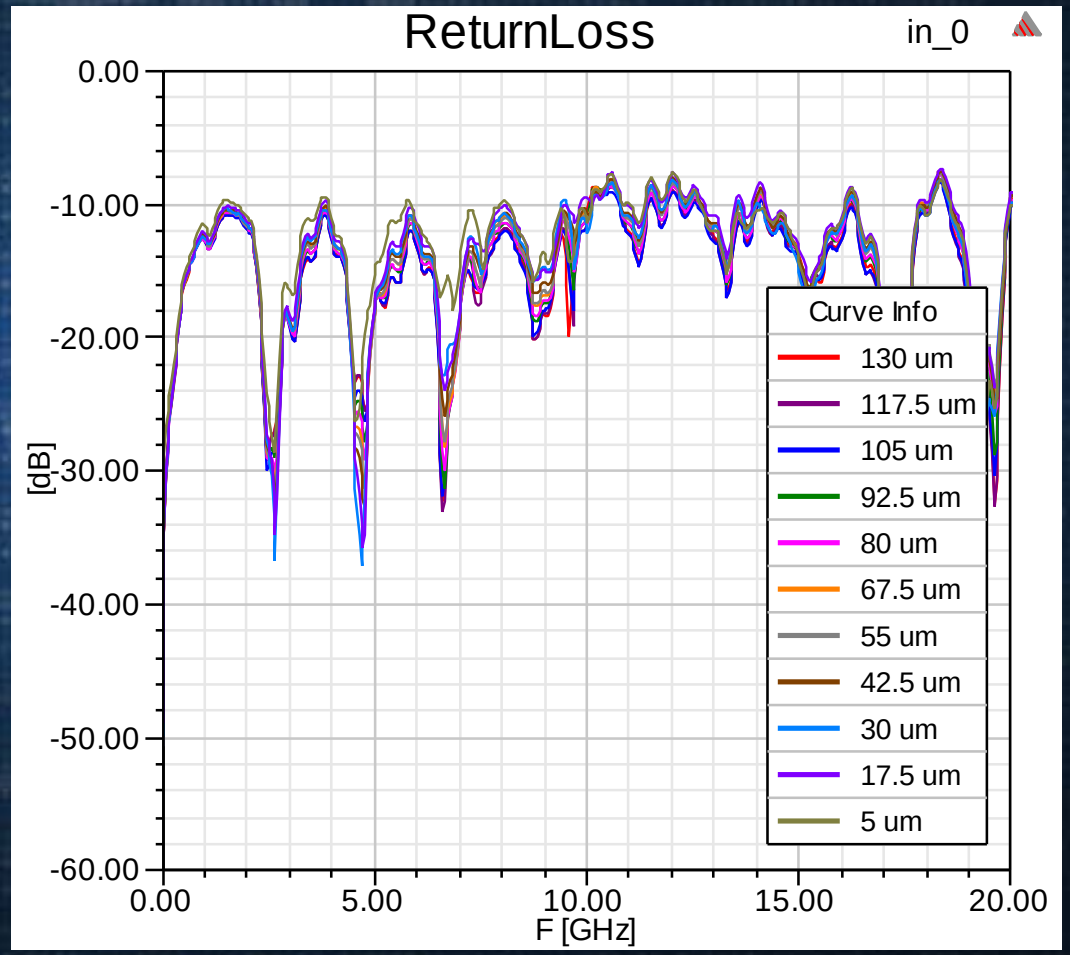


RF characterization

IL and RL varying working overdrive

- **Characterization with different overdrive: technology shows low sensitivity to working OD**





Space Transformer DC Tests

Experimental setup



- Dedicated wired space transformer designed and manufactured
- Probe card loaded on Accretech UF3000EX prober
- Blank wafers used to measure Path Resistance by means of Keithley Kelvin equipment

Space Transformer DC Tests

DC continuity test between GND and shield

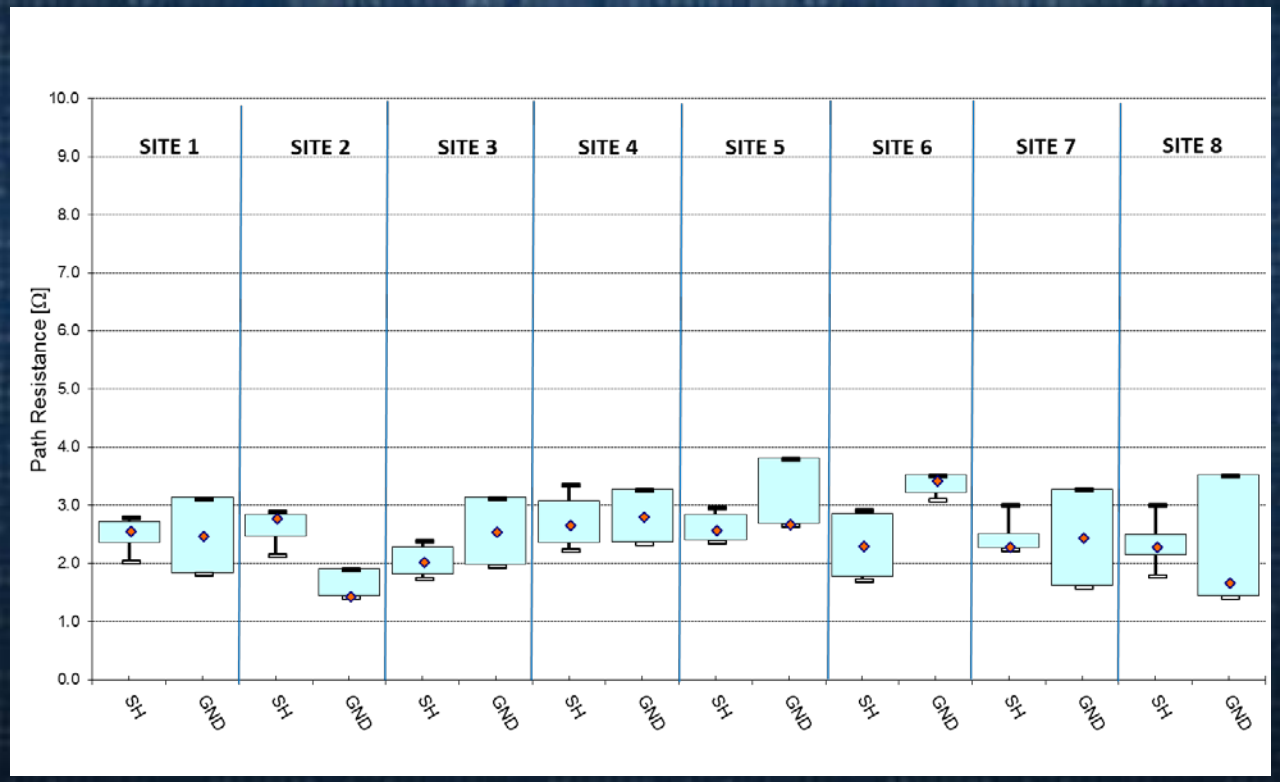
- Path Resistance tests were performed to measure the electrical continuity between GND probes and metallic shield inside the PH while probing on a nonconductive silicon wafer

- Next slides are show Path Resistance test results in function of PH site and of working OD

Space Transformer DC Tests

Path Resistance results in function of PH site

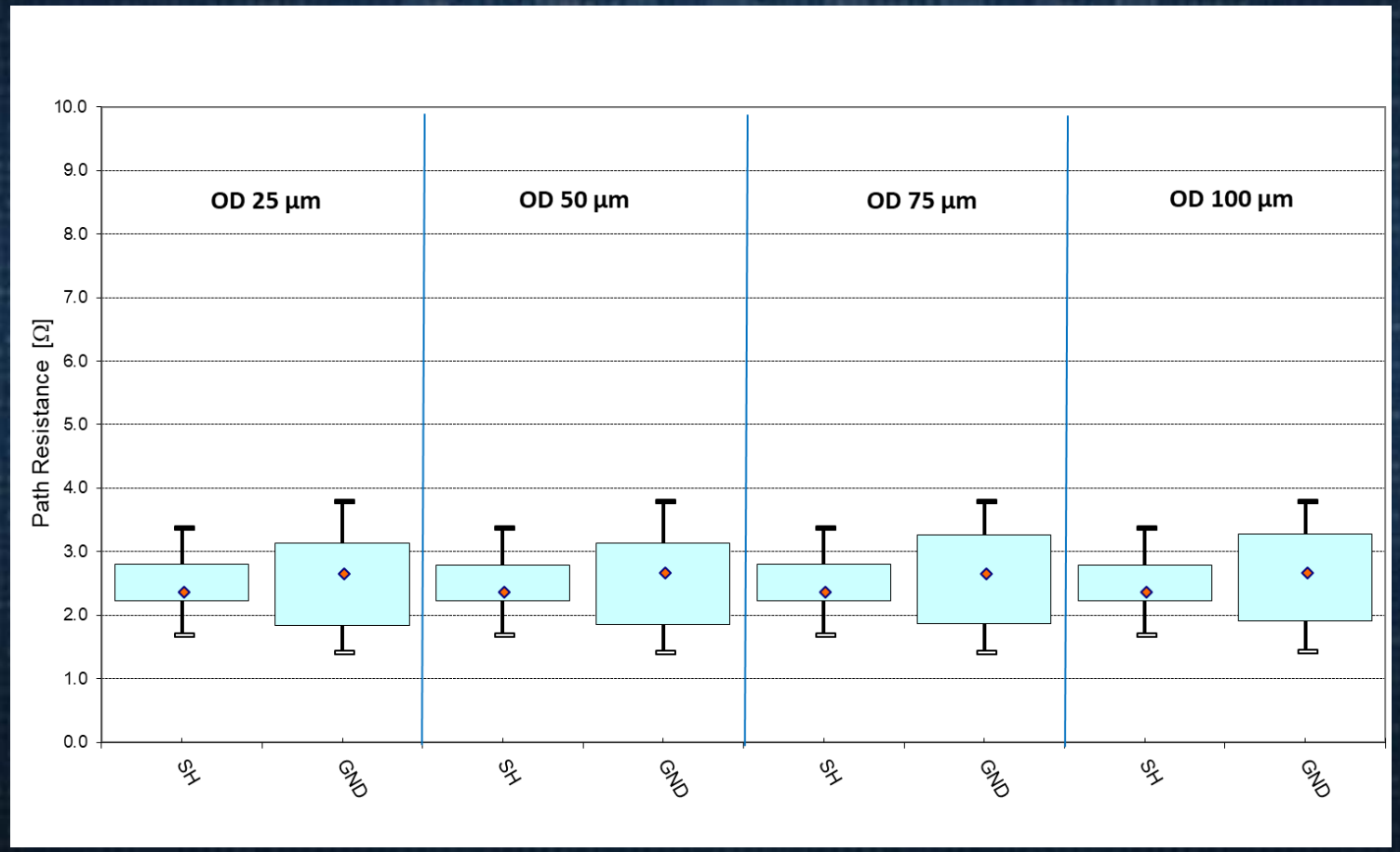
- **Path Resistance tests in function of PH site at a fixed working OD (75 µm)**
  - Results are stable and comparable



Space Transformer DC Tests

Path Resistance results varying working OD

- **Good Path Resistance stability observed in the whole working OD range:**



Space Transformer DC Tests

Leakage test on probe card analyzer

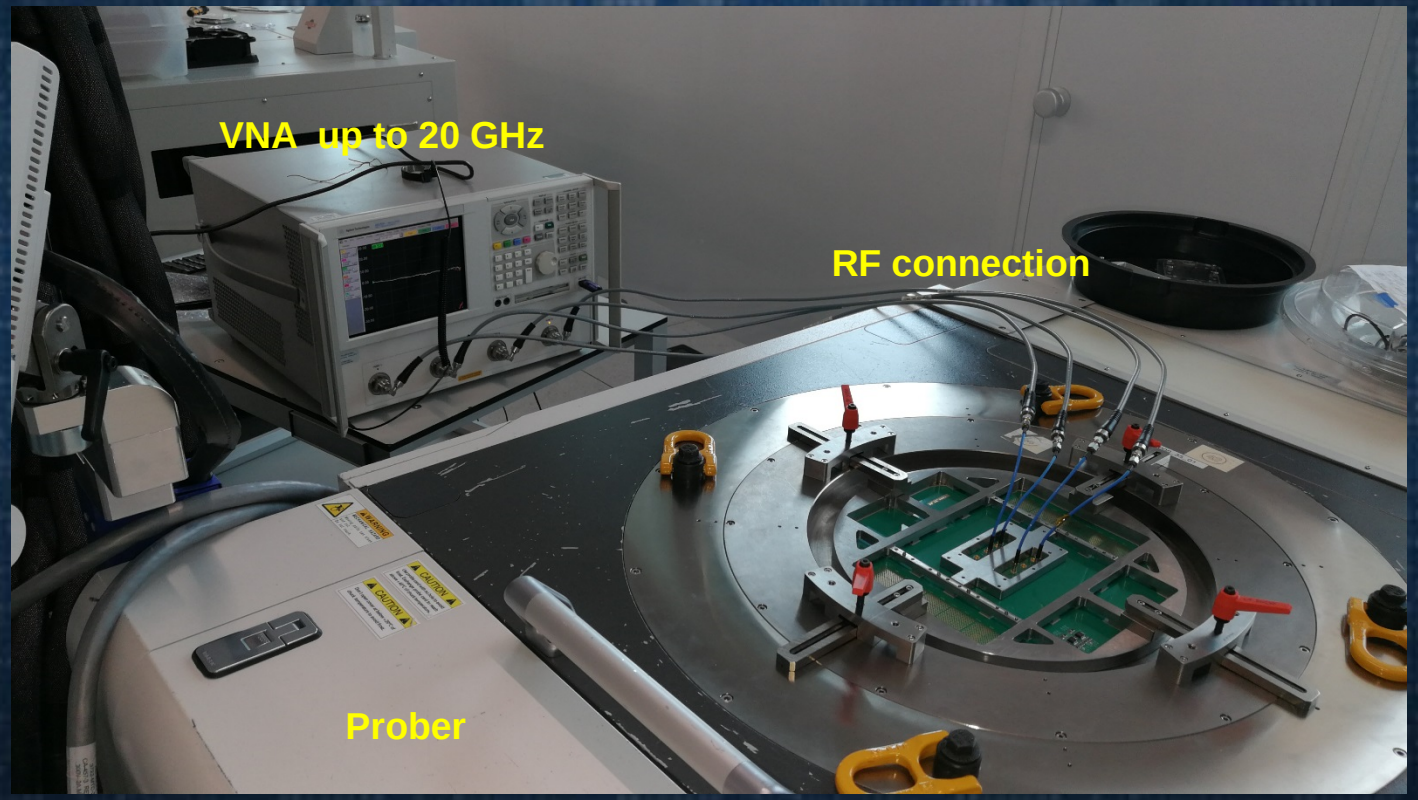
- Leakage tests were performed on Rudolph PRVX4 probe card analyzer
- No shorts have been detected in the whole working OD range
- Leakage measurements were below 0.12 nA @ 5 V (vs. 10 nA ref spec)



RF Tests on Prober

Experimental setup

- RF+ architecture has been validated on the prober using customer wafer and VNA up to 20 GHz to measure filter + probe card response



RF Tests on Prober

Experimental results on Customer wafer

- **On all 8 sites, we were able to measure filter shape compliant with required mask at different working OD**

Site Number	Test @50 OD	Test @75 OD	Test @100 OD
Site 1	PASS	PASS	PASS
Site 2	PASS	PASS	PASS
Site 3	PASS	PASS	PASS
Site 4	PASS	PASS	PASS
Site 5	PASS	PASS	PASS
Site 6	PASS	PASS	PASS
Site 7	PASS	PASS	PASS
Site 8	PASS	PASS	PASS

Conclusions

- **RF+ architecture is able to combine good frequency performance with the advantages of TPEG™ MEMS vertical technology**
  - High parallelism
  - Pin to pin onsite reparability
  - Low pad damage
- **RF results aligned with model**
- **Ready for on onsite test**

Future work

- **Evaluate feasibility of:**
  - More complex device
  - Higher parallelism
- **Probe head technology has the same powerful of standard vertical technology into manage device complexity… Need to understand space transformer capability into deal with high number of RF pins**

Thanks for your Support !

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SW Test Workshop

Semiconductor Wafer Test Workshop

Enabling High Parallelism in Production RF Test

Patrick Rhodes

Ryan Garrison

Ram Lakshmanan

FormFactor

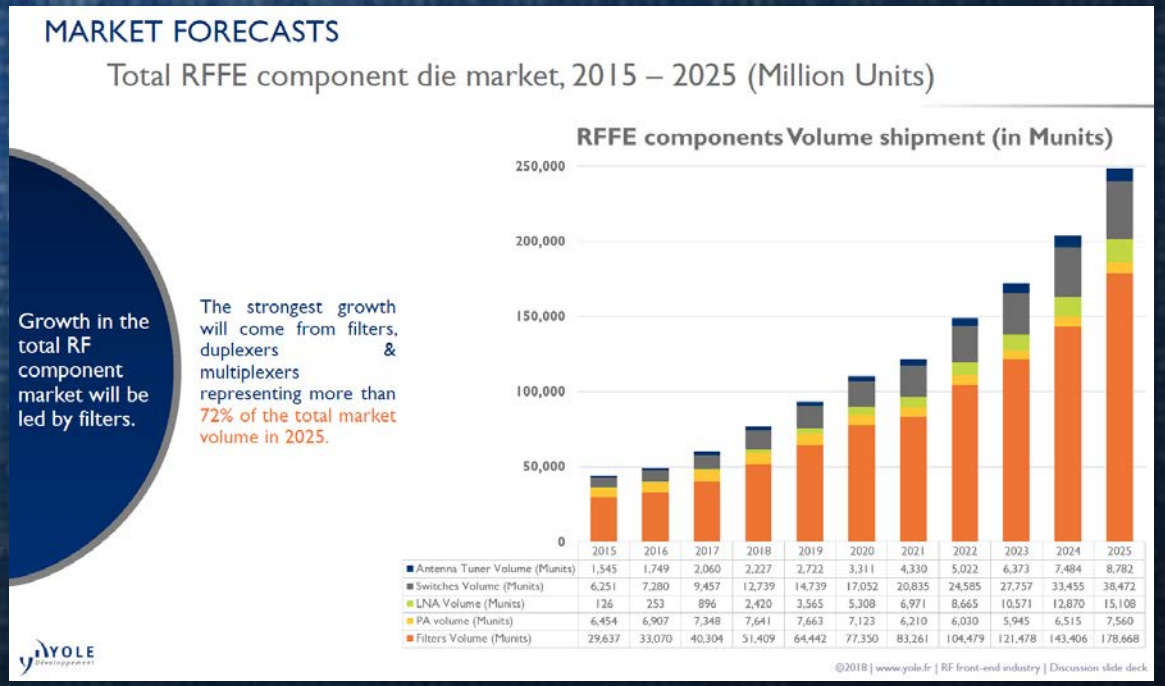
June 3-6, 2018

Connectivity is Driving Change

The connected world is driving the growth of RFICs in the market. These RFICs include – Filters, PAs, Switches for the front end and WiFi, BlueTooth, combo devices at the SoC level

Typically probing needs are:

- ❑ Operating frequency: <10GHz
- ❑ Loss Characteristics: -3dB IL/-10dB RL
- ❑ Ground Inductance: <0.8nH
- ❑ Higher Parallelism: larger volumes to test and increasing ATE capabilities



Credit: Yole, 2017

Example of Test Challenges

- **Combo devices:**
  - High RF channel count
  - Large general I/O count
  - High power requirements
  - Long test times
  - Delicate solder structures
- **High Speed Digital**
  - Large high speed channel count
  - Large dies
  - Stringent pad damage requirements

…all in a volume mfg. environment



X8 Array with >3000 Contacts and 6 GHz signals

Limited options for probe technology, all with trade-offs

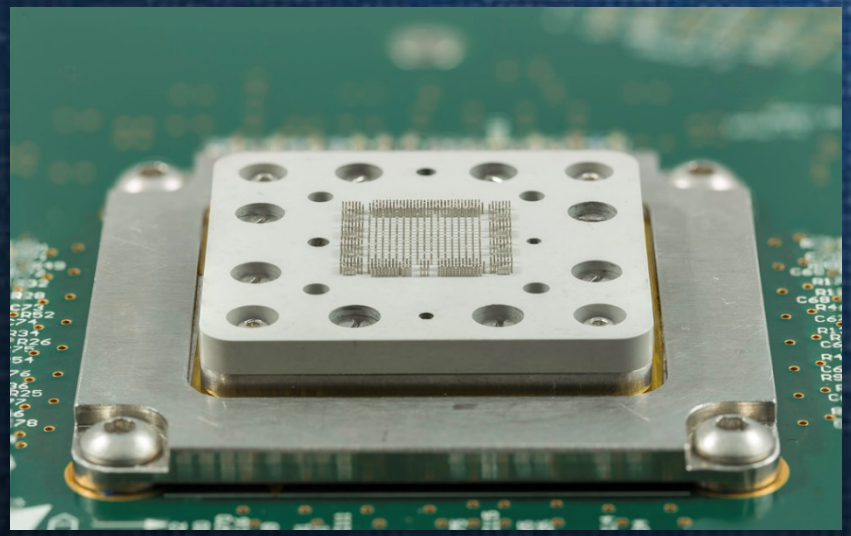
Limitations with Existing Solutions

- Traditionally, device manufacturers have deployed probe cards that support high frequency signals (>3 GHz) OR mechanically robust multi-site probe cards, but not both
- Many of the ingredients needed to get to a mechanically robust, frequency capable, multi-site probe card have been around for years, but gaps remained

Pogo Pin Limitations

The GOOD:

- Readily available
- Low cost
- High CCC



The LACKING:

- Pitch and frequency limited
- High inductance
- Maintenance-intensive
- High force

Getting to Higher Parallelism in RF Test

- **We'll explore a new combination of the existing ingredients, as well as a technological sweetener that completes the picture, for a robust, multi-site probe card for production RF test**



+



+

A New Ingredient!

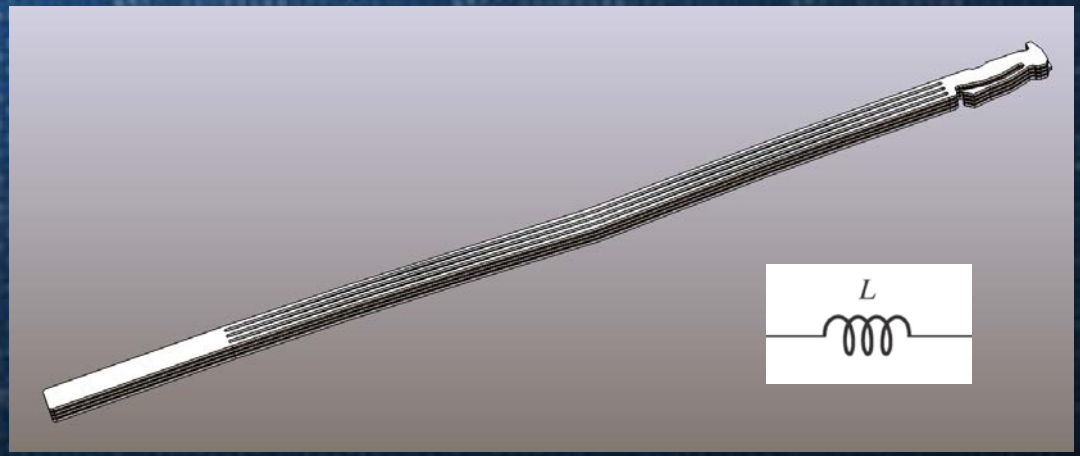
Ingredient 1 – Vertical MEMS

The GOOD:

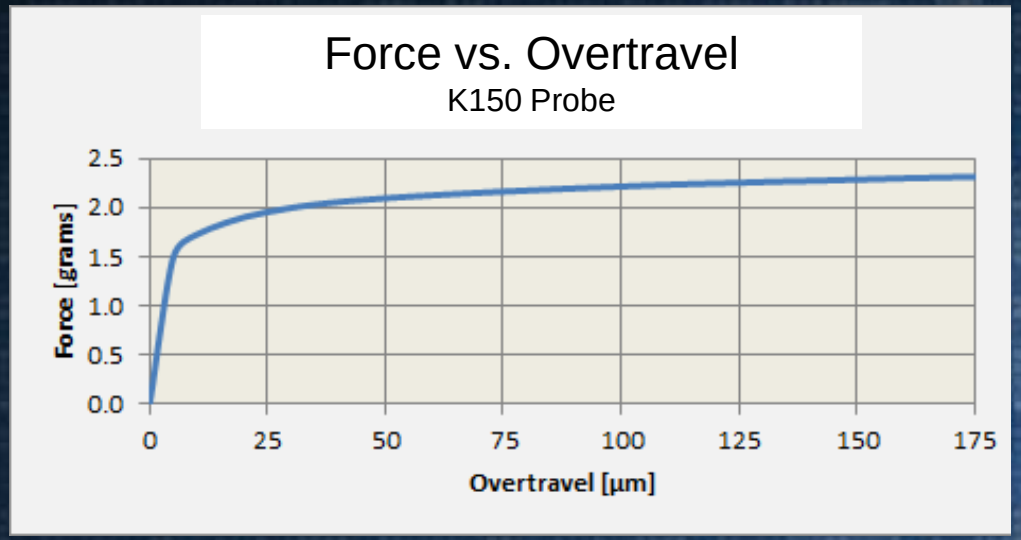
- ***Lots of people make these now, but only some are reasonably short***
- **Low Force (~2 grams at maxOT)**
- **Long Lifetime**
  - Mechanically these will exceed 1M touchdowns, considering both fatigue and wear
- **High CCC (~1A, depending on type)**
- **Easily Replaceable**
- **Scalable to large arrays and many sites**

The LACKING:

- **Vertical MEMS probes are essentially series inductors in traditional implementations**



Ingredient 1 Details



Buckling action of these probes makes good contact quickly, and leaves plenty of usable overtravel

Probe Type	K400 (7-leaf)	K150 (4-leaf)	K80* (3-leaf)
Probe Technology	Vertical MEMS	Vertical MEMS	Vertical MEMS
Available Probe Tip Shape	Flat	Flat, Pointed	Flat, Pointed
Minimum Pitch [µm]	130 Inline Single Row (→105)	112 Inline Single Row (→87)	112 Inline Single Row (→87)
	200 Square Grid	150 Square Grid	130 Square Grid
	300 anywhere	175 anywhere	150 anywhere
Flat Tip Size (um)	80 x 200	51 x 76	51 x 55
Pointed Tip Size (um)	-	16 x 16	16 x 16
Probe Force at Production OT(g)	5~6	2.1~2.3	1.9~2.1
Max OT [um]	350	175	125
CCC [A]	1.5	1.1	0.8
Probe Length [mm]	2.95/3.75	2.79	2.79
Operating Temperature	-40~160C	-40~160C	-40~140C
Loop Inductance	0.6-1.2 nH GSG	0.4 nH GSG	0.4 nH GSG
@ Assembly Minimum Pitch	1.0-1.8 nH GS	0.75 nH GS	0.75 nH GS
Repairability	Single Probe Replaceable		

Ingredient 2 – Membrane Space Transformer

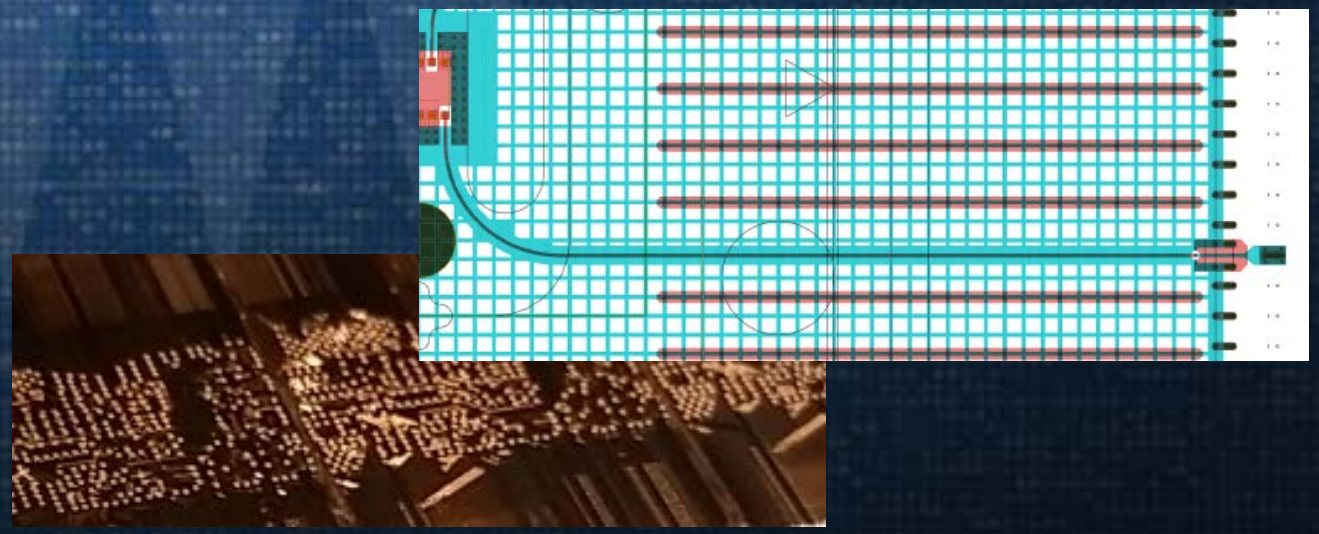
(now with only 1 job – space transformation)

The GOOD:

- ***These have been around for a long, long time***
- **Straightforward transmission line routing from one end to the other**
- **Short lead times**
- **More cost effective than typical MLO space transformers**

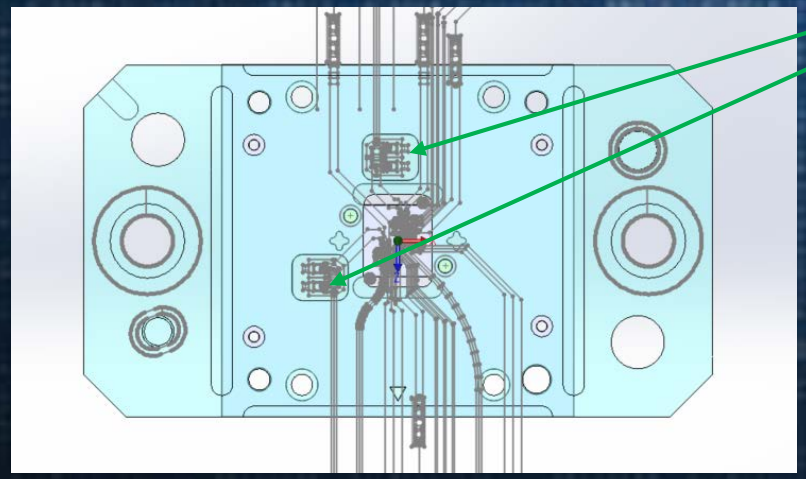
The LACKING:

- **Traditional use of these as a space transformer AND a contactor has limitations**
  - Large arrays can be mechanically unwieldy
  - Repairs often not possible



Benefits of Ingredient 2

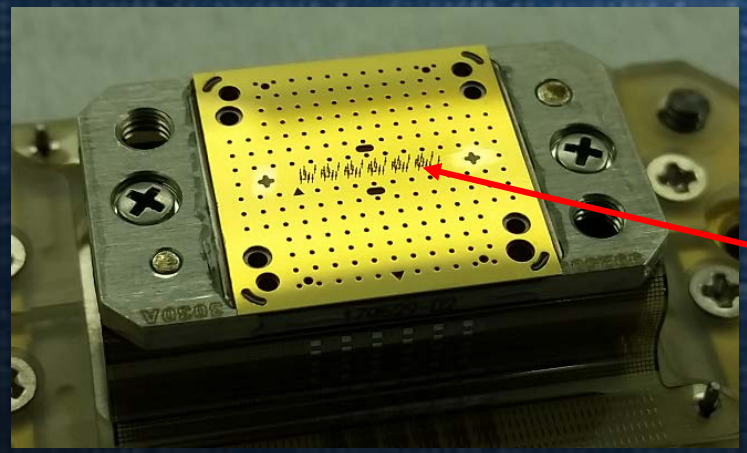
- Use of the membrane as a space transformer only is far simpler than using it as a space transformer AND contactor
- It frees the membrane up for some *fringe benefits*



1. Additional space in general – landing pads for vertical probe distal ends take up less space
2. Loopbacks – see also: extra space
3. Component placement – right on the membrane face, underneath the spring head and very close to the die

Ingredient 3 – The New One!

So now we have vertical MEMS probes and a membrane space transformer. This is great for DC applications, *but that's not the endgame*. The combination is part way there, but now we're dangling an inductor off the end of a nice transmission line.



Bringing Balance to the Force:

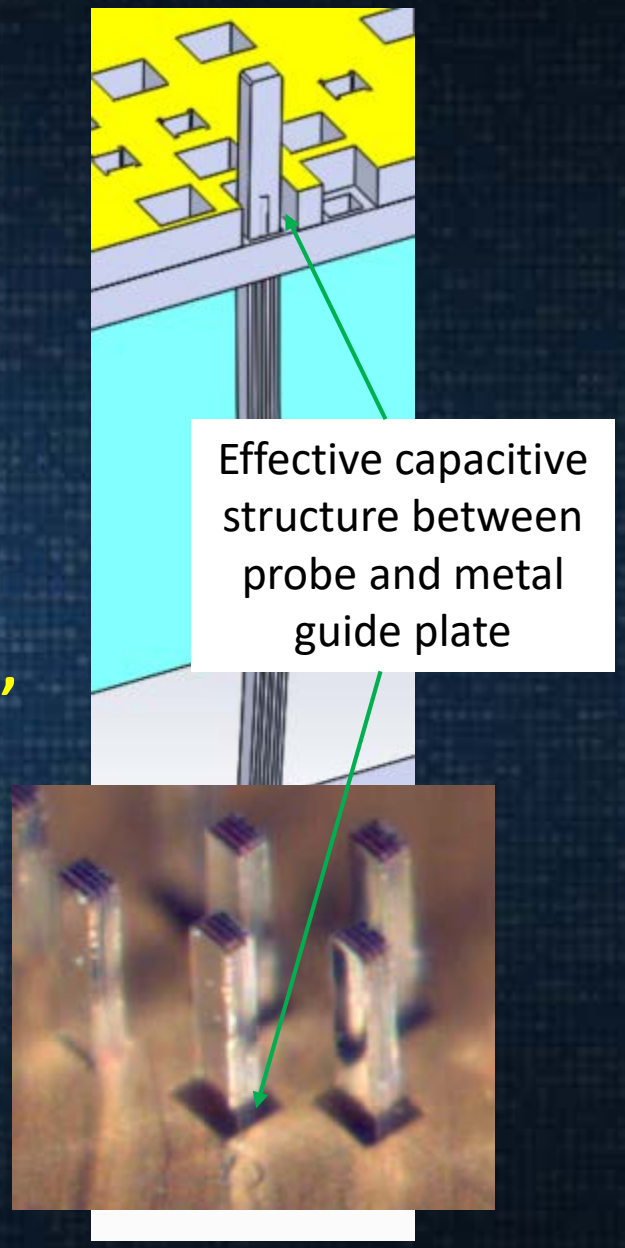
- **Add a metal layer to the guide plates**
- **Connect these metal layers to GND**
- **Connect all the GND probes to this metal layer**
- **Isolate all other probes from this metal layer**

All GND probes are always in contact with the metal guide plate, all non-GND probes are isolated from the metal guide plate

Benefits of Ingredient 3

So now we have <u>metal+ceramic guide plates</u>:

- **Enjoy the capacitance that the metal layer adds…and the balancing effect to the typically inductive vertical MEMS probe**
- **Further enjoy the ground plane between the die and space transformer**
- **Continue to enjoy the robust mechanical characteristics of ceramic guide plates (long lifetime, accurately feature placement, etc)**

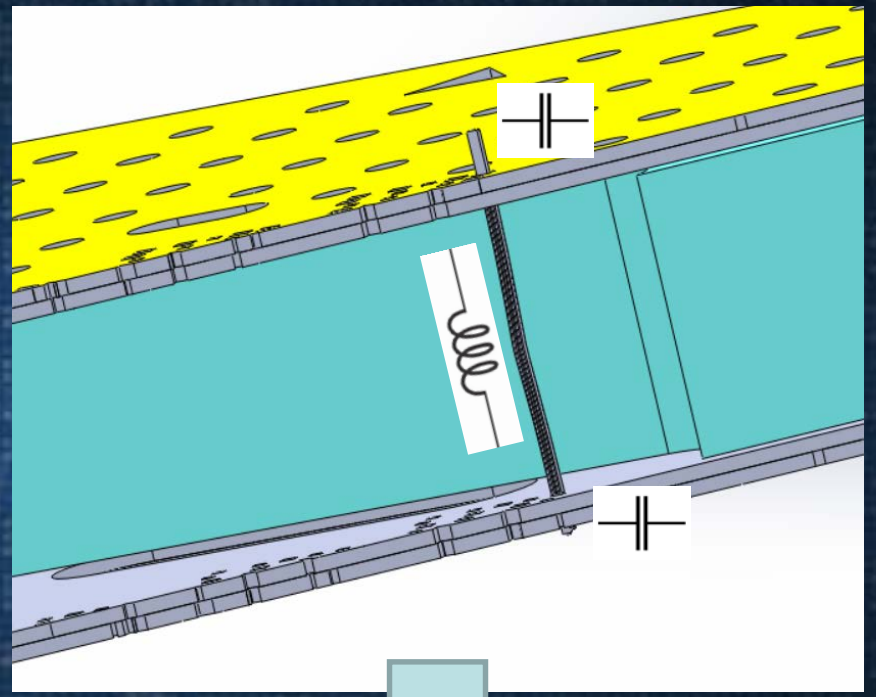


→Loss characteristics are improved over typical vertical MEMS probe cards

→The die and space transformer are nicely shielded from one another

Putting it Together (Pyramid + Katana = Pyrana)

- **Frequency performance – to about 10 GHz considering insertion and return loss**
  - Dependent on die layout and other factors
- **Isolation – die and space transformer aren't talking to one another**
- **[Standard benefits of vertical MEMS]**
- **[All the pluses of a thin-film space transformer]**



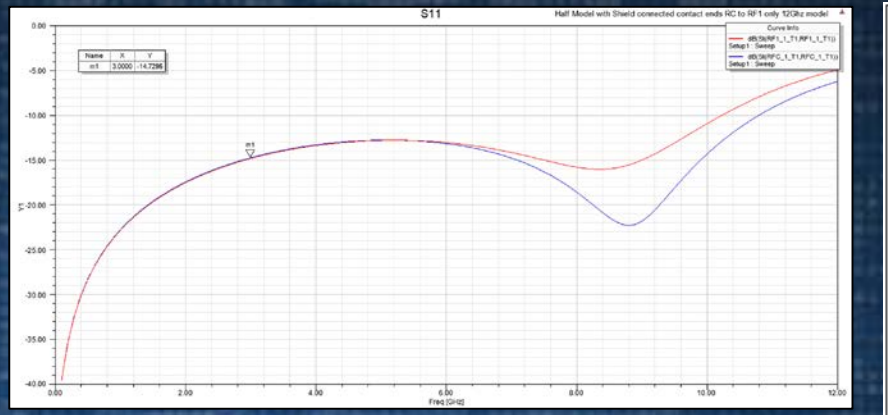
It's imperfect, but it moves the probe head back towards a 50 ohm environment; the space transformer is already there

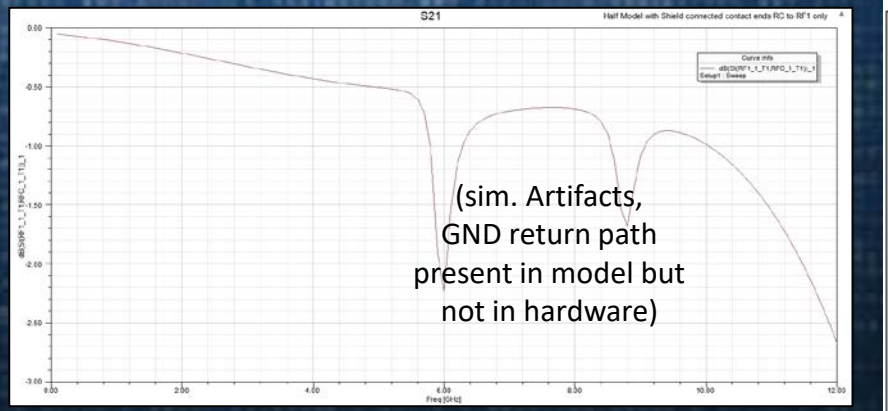
How We Got Here: Simulations

(spring head only)

- The spring head remains the least ideal portion of the signal path
- Simulations for RL/IL suggest loss contributions, and measurements largely agree

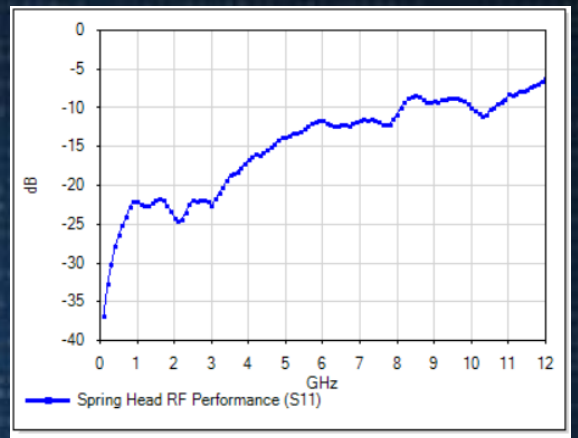
Simulated

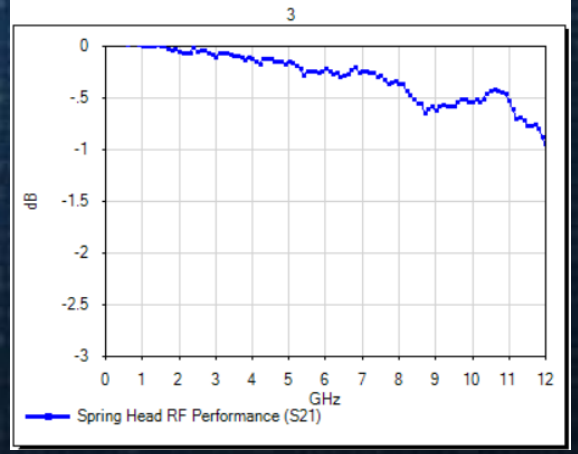




(sim. Artifacts, GND return path present in model but not in hardware)

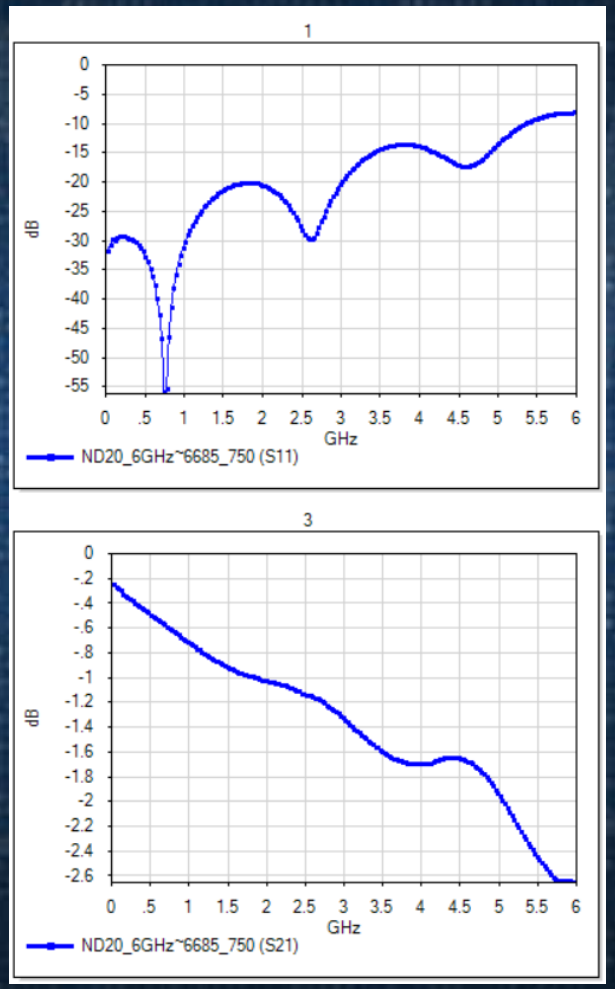
Measured/De-embedded

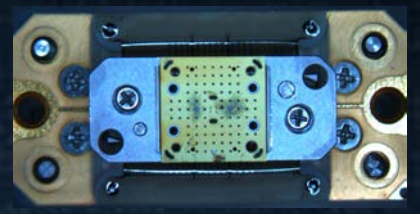




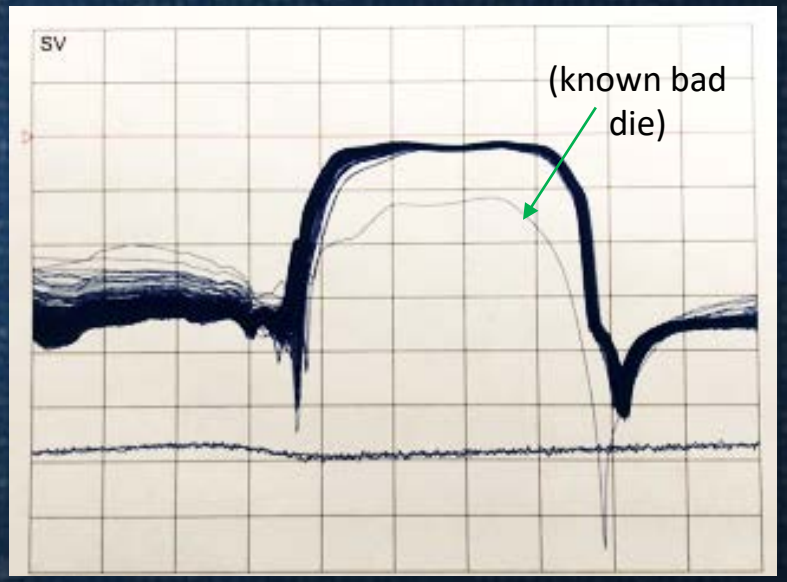
Case 1: Testing a Filter

- ***Need***: **mechanically robust probe technology with low loss (able to see defined passband), DC to 6 GHz**
- **Entire signal path shown in S-parameters at center (connector to probe tip)**
- **Defined passband as seen through the probe card at right**



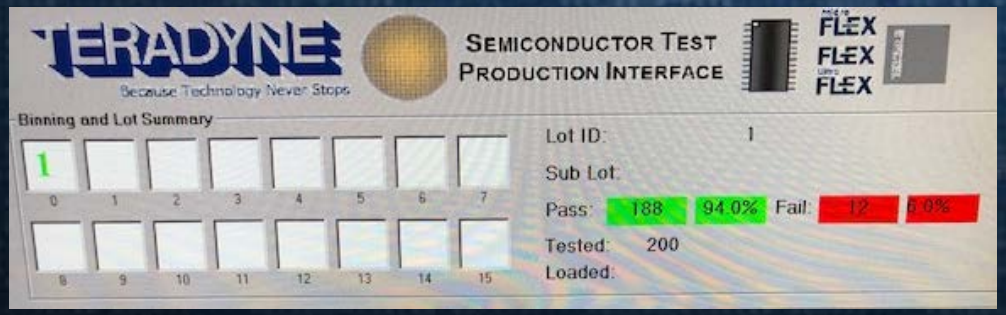


PV6: Smallest Pyrana Probe Head



Case 2: Testing a Large Die, Lots of RF lines

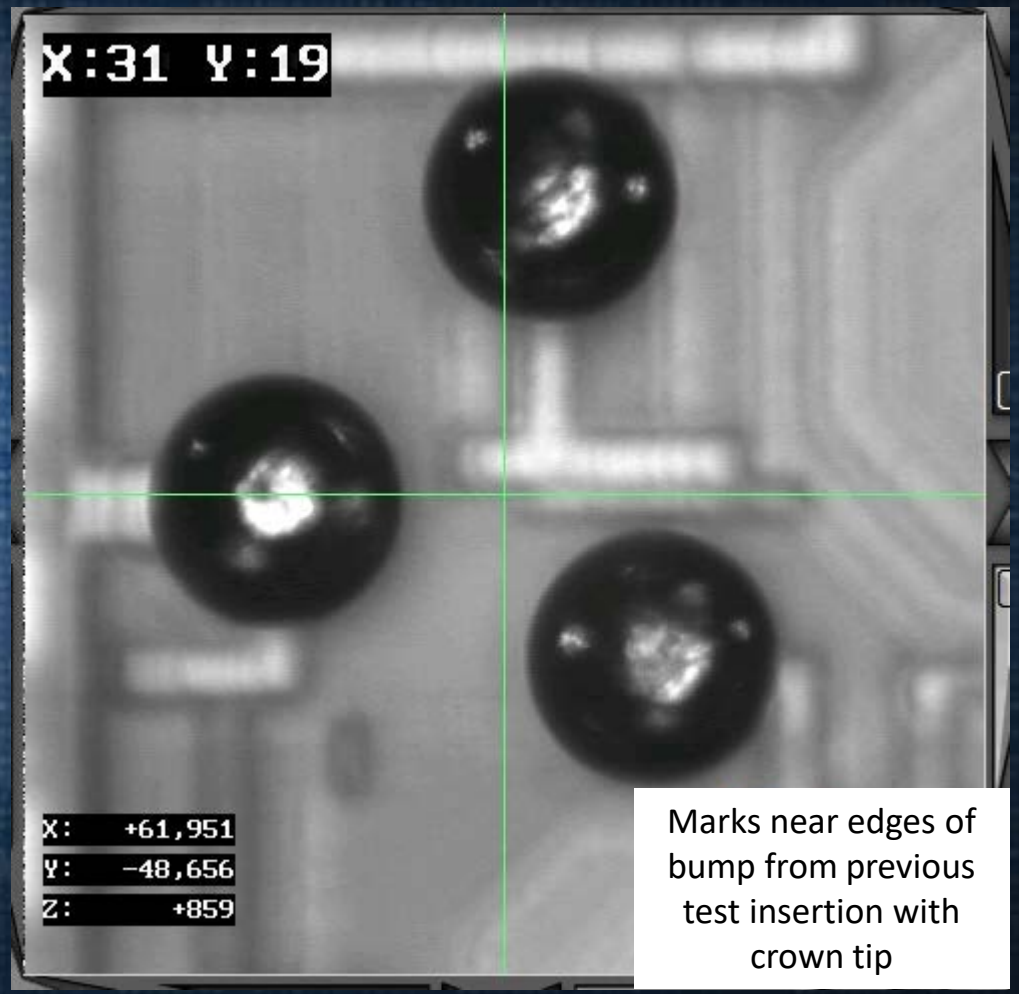
- **A device with 32 RF lines for multiple radios shows yield loss due to insertion/return loss and crosstalk with more traditional probe technology**
- **Using a vertical head with a metal guide plate maintains yield >90% over the course of a full wafer**
  - Uncalibrated, but with repeatable results
  - RF power levels as seen by tester better than expected
- **Isolation and attenuation issues attributable to the contacts are largely addressed**
- **Heads used in a non-cleanroom engineering environment suffered damage due to overcurrent events, handling, etc, *but repairs were generally straightforward***



Test Data, about as sanitized as it gets!

Case 2: Probe Marks

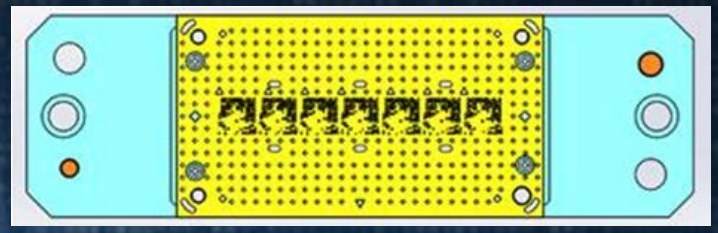
- Low force and modest but non-zero scrub minimizes bump damage while maintaining good contacts
- Bumps at right are 90 um tall, 120 um diameter
- Top ~1/3 of hemisphere is *coined* but otherwise undisturbed

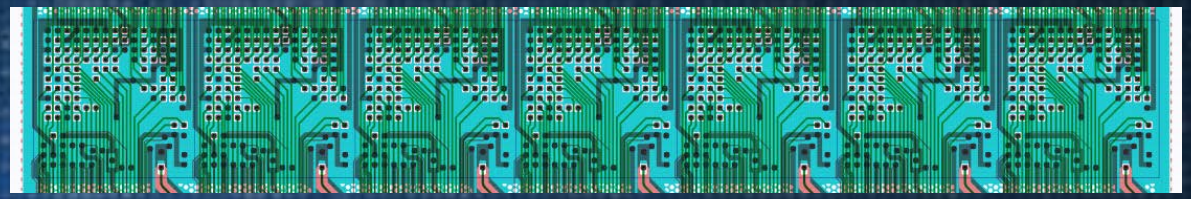


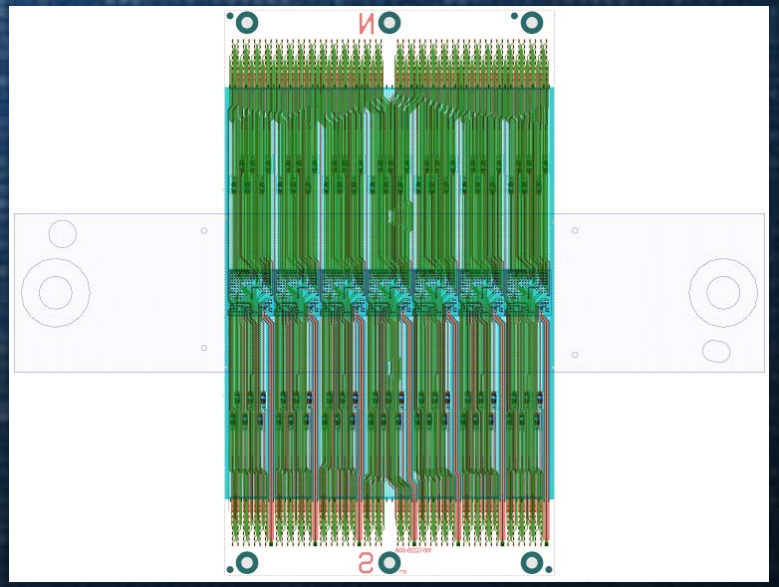
Marks near edges of bump from previous test insertion with crown tip

Case 3: Scaling Up

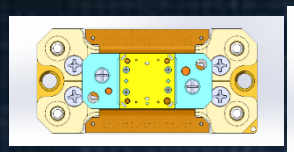
- 7-site testing of a Bluetooth device on a Teradyne UltraFlex tester
- Array size approximately 24 mm in the long dimension
- *Need*: probe technology that takes advantage of 7-site tester capability, without mechanical shortcomings
- *This design is complete, parts are in manufacturing, and will be evaluated over the second half of 2018*
- *Additional multi-site designs now in process*

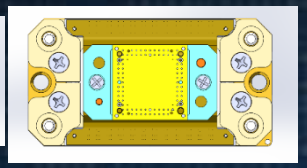




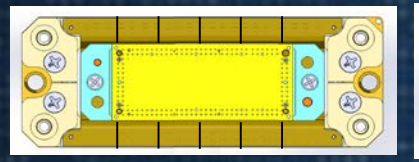


Pyrana – Additional Details





PV6	PV10
6mm x 6mm	10mm x 10mm





PV35	PV75
35mm x 10mm	75mm x 12mm

- **4 standard sizes for probe heads, with active areas shown**
- **Coverage for a wide range of devices, site counts, pin counts**
  - Filters to RF-SoCs
  - Inductance-sensitive devices, including MEMS sensors and power amplifiers
  - Tens of sites
  - Tens to thousands of probes
  - *Pin count is typically not the limiting factor*
- **Standard probe head footprints make generic, low-cost PCBs a real possibility**

Additional Product Data: www.formfactor.com/product/probe-cards/rf-mmw-radar/pyrana/

Pyrana Future

- **New vertical probe card architecture is opening new doors right now, but there's more to come:**
  - Drive to higher frequencies to support expanded applications
  - Improved pitch capability
  - Lead time reduction
- **Actively pursuing improvements to the Pyrana architecture to address all of these**

Wrap Up

- **Pyrana is an effective combination of a couple of existing, proven technologies plus a new ingredient**
- **It offers the possibility of much higher parallelism for all kinds of devices with signals up to 10 GHz**
  - Today's 10 GHz limit represents a trade – a lower frequency limit for a number of mechanical advantages
  - This limit is a soft one, as we're already driving toward improved bandwidth capability

Thank You!

- **Patrick Rhodes – Product Engineer, Patrick.Rhodes@formfactor.com**
- **Ram Lakshmanan – Marketing Manager, Ram.Lakshmanan@formfactor.com**
- **Please question away!**

SWTW18-14

Optimizing cleaning processes based on force to puncture ITS materials

Alex Poles
International Test Solutions

Introduction

- Perform Force vs. over travel (OT) tests to determine the yield strength of elastic probe cleaning materials.
- Compare and validate experimental results to a theoretical model.
- Consider polymer elasticity properties for determination of optimal cleaning processes.
- Evaluate effect of probe area to puncture force through material surface.

Test Parameters

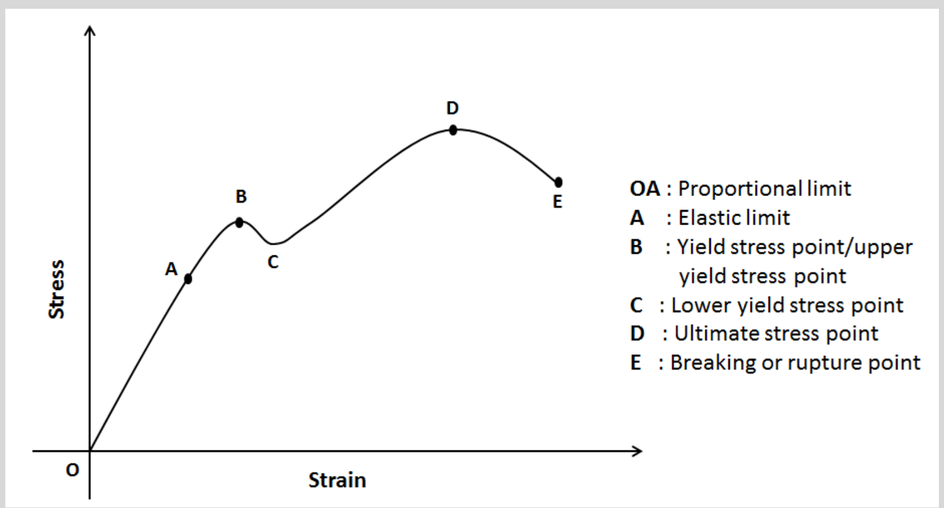
Probe Size	(Vertical – 100um, 76.2um, 50.8um)				
Materials Used	PV-OE0E	PV-AD0E	PF-AHHE	PP150-03	PP300-03
Cleaning Material	—	—	—	xx	xxx
Shaping Material	x	xx	xxx	—	—
Max OT			230um		
Temperature			25C		

x = abrasiveness

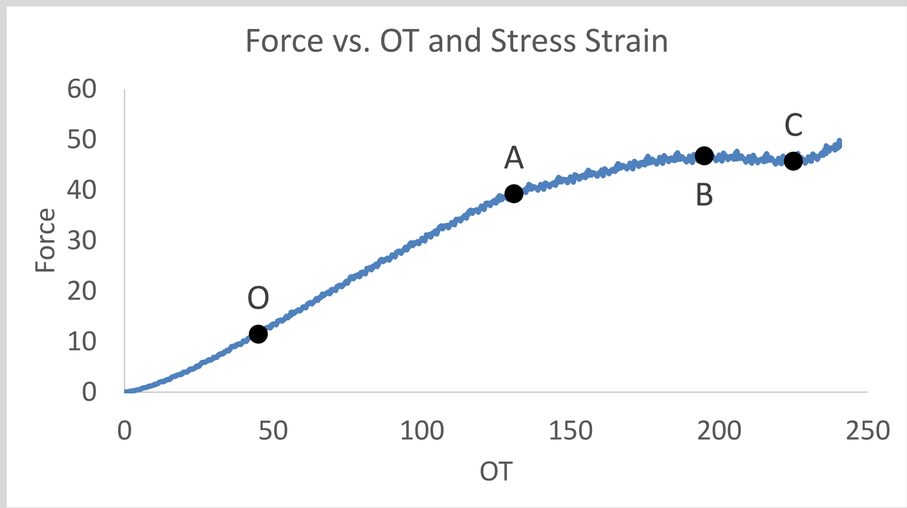
Mathematical Model

- Force was measured as a function of over travel on various elastomeric materials.
- The waveforms produced (right) are comparable with a stress-strain curve for ductile materials (left).
- As the probe approaches the force at the elastic limit (A), it will begin to penetrate through the surface of the polymer.

Theoretical



Experimental



$$Y.S. = \frac{F_y}{A_p}$$

$Y.S.: Yield\ Strength\ (constant)$

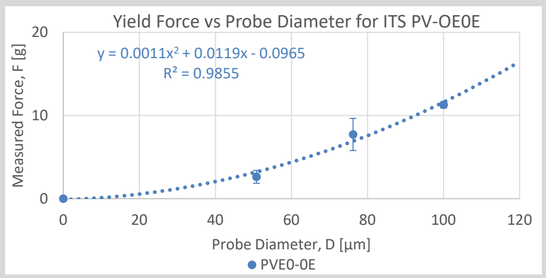
$F_y: Force\ Requried\ for\ Yielding$

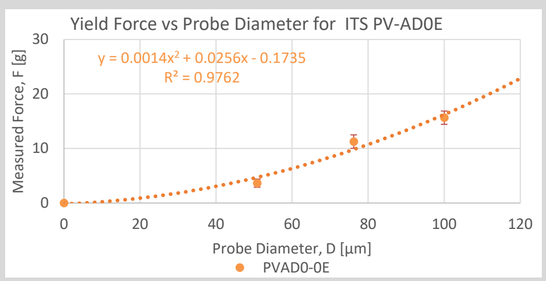
$A_p: Probe\ Area$

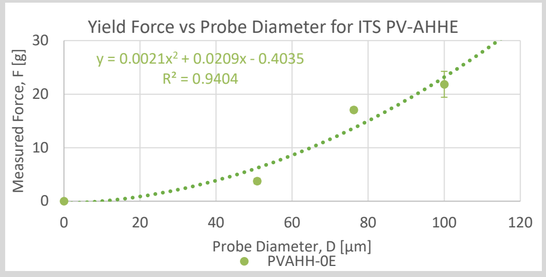
- The compliant nature of ITS materials causes differences in the curves.
- Force vs. OT curves resemble the shape of the stress-strain curve.
- The region between O → A can be approximated as the elastic region.
- Forces between A → B may begin to permanently deform the polymer.

Results

Tip Shaping Materials



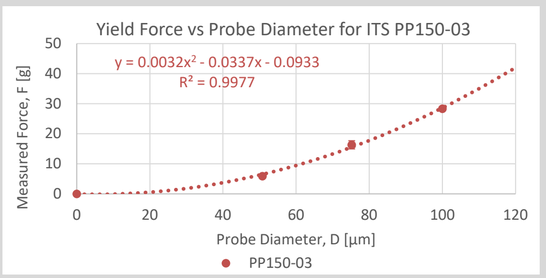


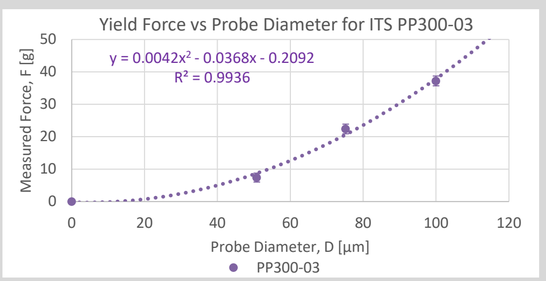


Curve Fits:
Quadratic (2nd order polynomial)

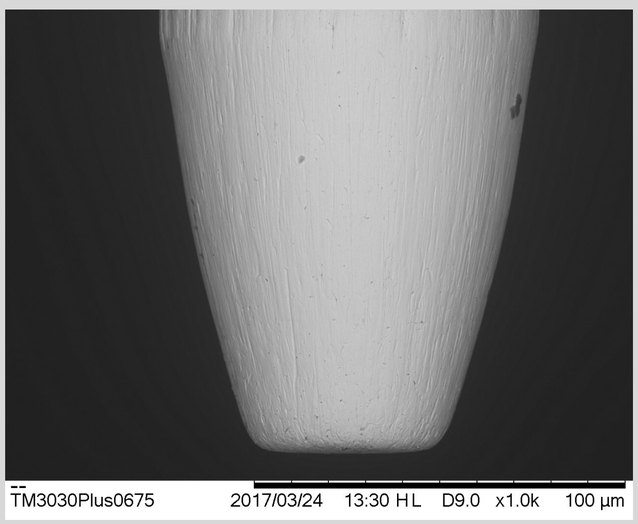
- ITS can generate a model that will predict when a probe punctures the polymer.
- Threshold force curve is shown. Forces above the curve will penetrate polymer.
- Tip cleaning materials aim to remain below the line, while shaping is intended to remain above.

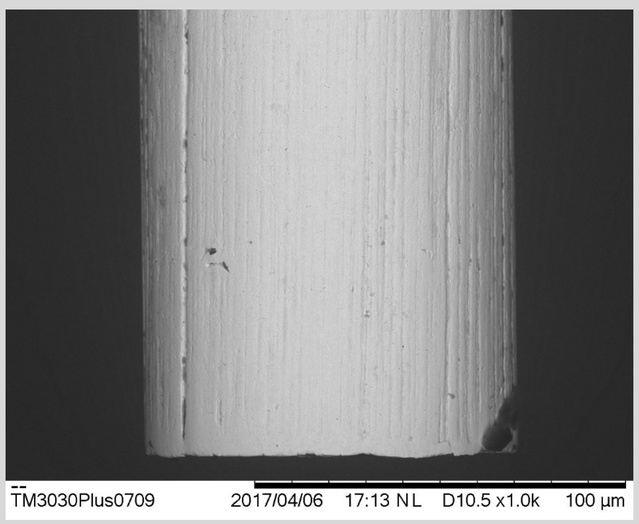
Tip Cleaning Materials

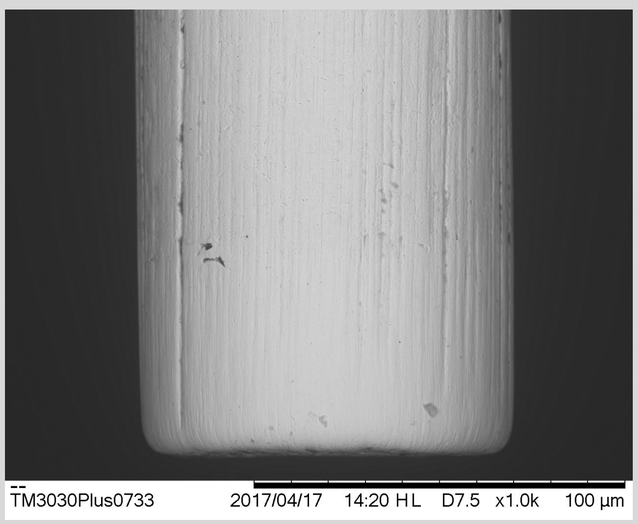




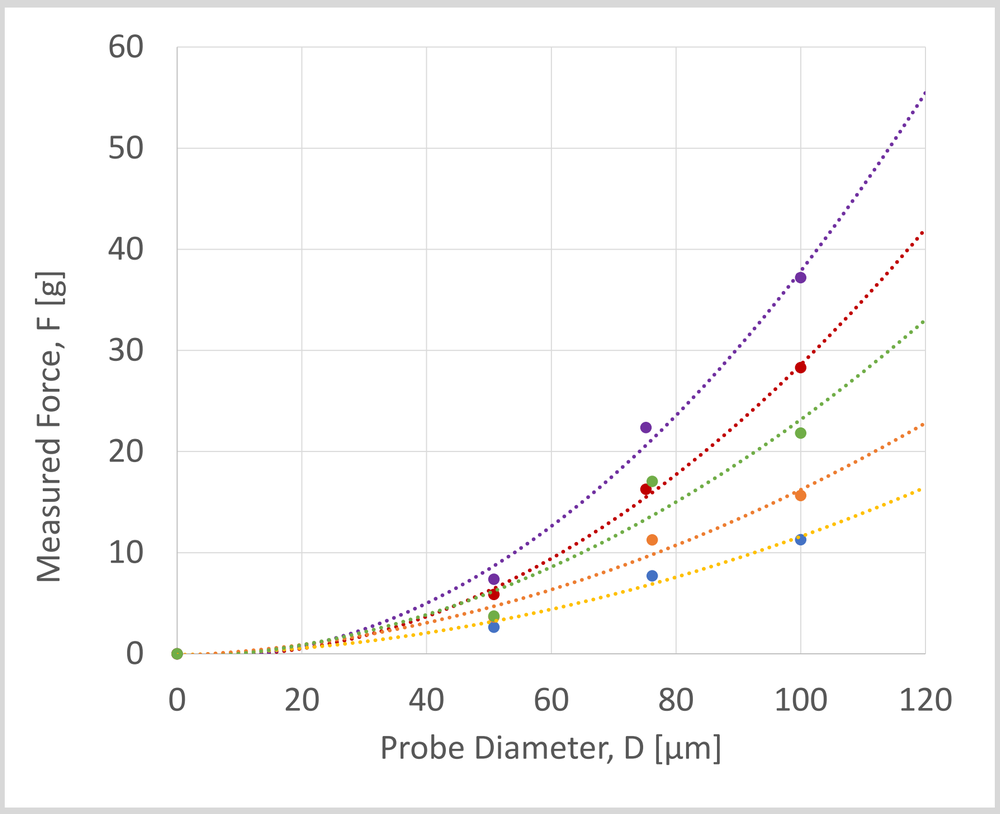
Photos below are taken on 100um diameter vertical probes after 25,000 TDs.







Analysis – Elasticity Considerations

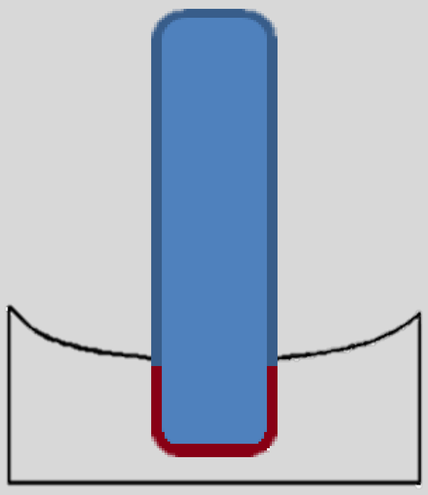


- Probe Polish materials are very elastic and require increased force and over travel to penetrate the surface.
- PP300-03 has more abrasive (increased hardness) causing higher puncture force.
- Probe Vertical materials puncture more easily due to lower elasticity.
- Puncture force increases as material hardness increases.
  - PV-AHHE is the most abrasive of the PV materials.
- As probe diameter decreases, required puncture force decreases.
- This is a function of probe area as shown in mathematical model.

Analysis – Cleaning vs. Shaping

Shaping

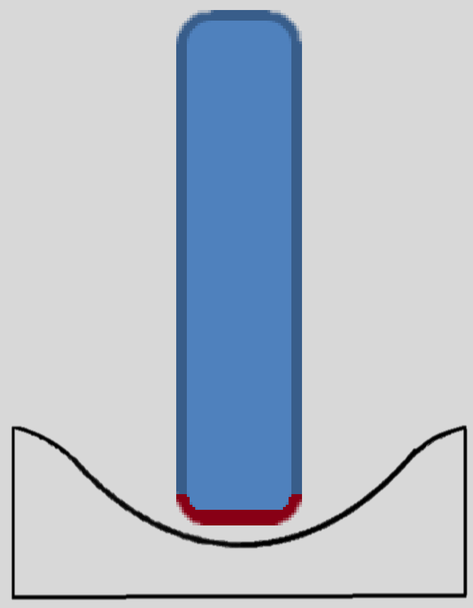
- Shaping occurs when:
  - Probe breaks through surface of polymer.
  - Plastic deformation occurs in the material.
  - Permanent, noticeable indentation in the material.
- Results in sharpening of probe tips.
- Creates a taper along probe length.



Affected area of punctured probe being shaped.

Cleaning

- Cleaning occurs when:
  - Over travel remains within material's elastic limit.
  - Material will rebound to its original shape.
- Results in mild rounding or smoothing of probe tip.



Affected area of probe undergoing cleaning.

Conclusion

- Shaping occurs once the probe punctures the material and causes increased wear and a dramatic taper of the tips.
- Cleaning occurs below threshold force in which puncture occurs.
- A wide range of materials and probe geometries may be used to evaluate the puncture force for tip shaping/cleaning.
- The required puncture force can be predicted for a variety of elastomeric materials.

Contact

- For further inquiries regarding this project:

  Mail: alexp@inttest.net

  Cell: +1 702-489-1094

- For more information, please contact: International Test Solutions - 1595 Meadow Wood Lane - Reno, NV 89502 (USA)

  www.inttest.net

  Mail: techsupport@inttest.net

  Phone: +1 775-284-9220

POSTER #10

Wafer Sort At Extreme Temperatures

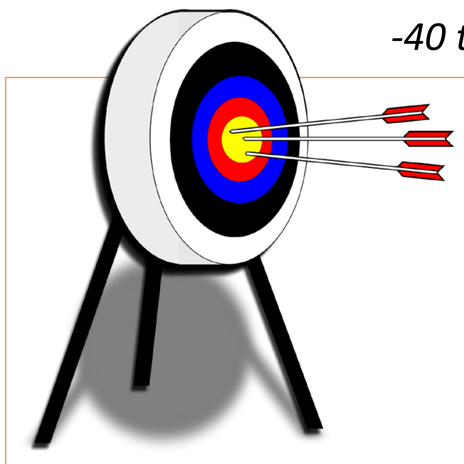
Roger Sinsheimer, Chris Buckholtz
Teradyne, Inc.



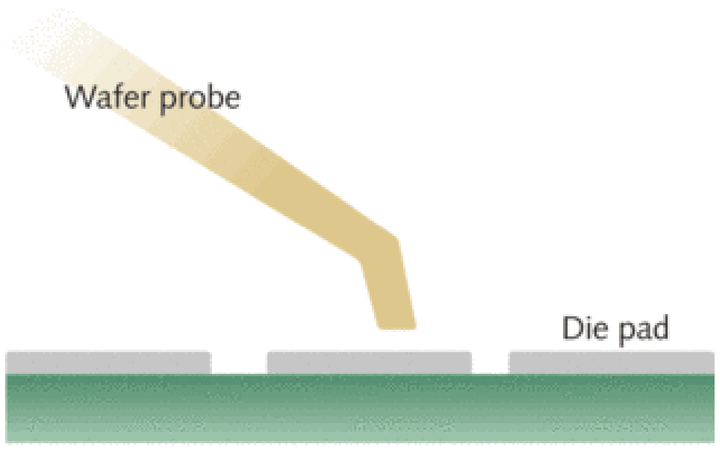
COLD!
-40 to -55° C

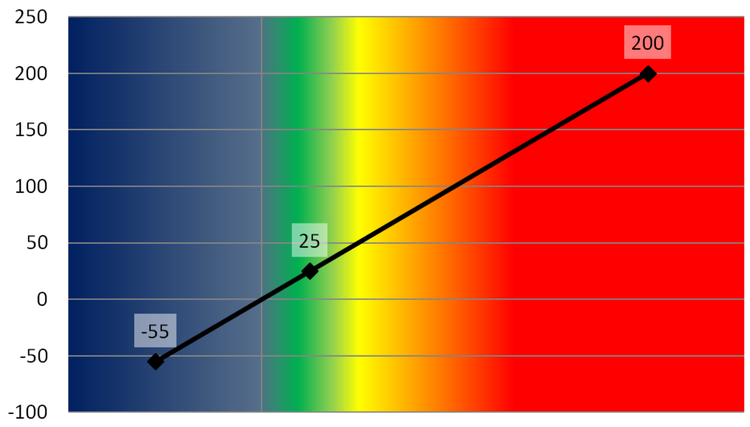
HOT!
+125 to 200° C

Welcome to the Badlands!



Hitting the target!





- If the goal is to probe at three temperatures it is highly recommended that two – or three – temperature-specific probe heads be designed to ensure that the probe tips will land on the probe pads in the desired locations at the target temperatures.

The smaller the probe pads, the greater the concern

- The probe head and the probe card X-Y plane expansion / contraction do not perfectly match the CTE (Coefficient of Thermal Expansion) of wafers
- As probe temperatures change there will be variation of location of the probe tips within the touchdown pattern, hence the practice of utilizing temperature-range-specific probe heads

For Hot Sort the Wafer Chuck is the Heat Source

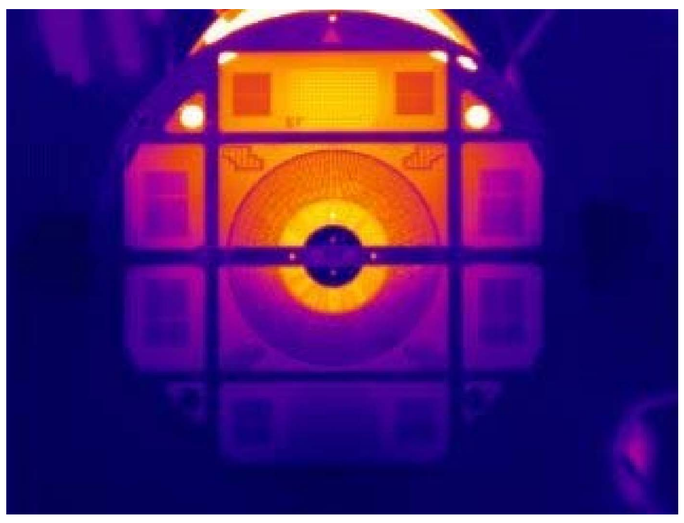


Image from:



- Motion of the wafer chuck affects the probe card assembly temperature profile, therefore the probe needles' z-position
- Getting a wafer, checking probe tip height with the prober's upward-looking camera, probe tip cleaning / polishing – all of these move the wafer chuck away from the probe head for several minutes.
- Process steps that move the chuck away from the probe card will result in significant asymmetric cooling (or heating) of the probe card assembly, which in turn means that the probe needles can move significantly in Z during these process steps

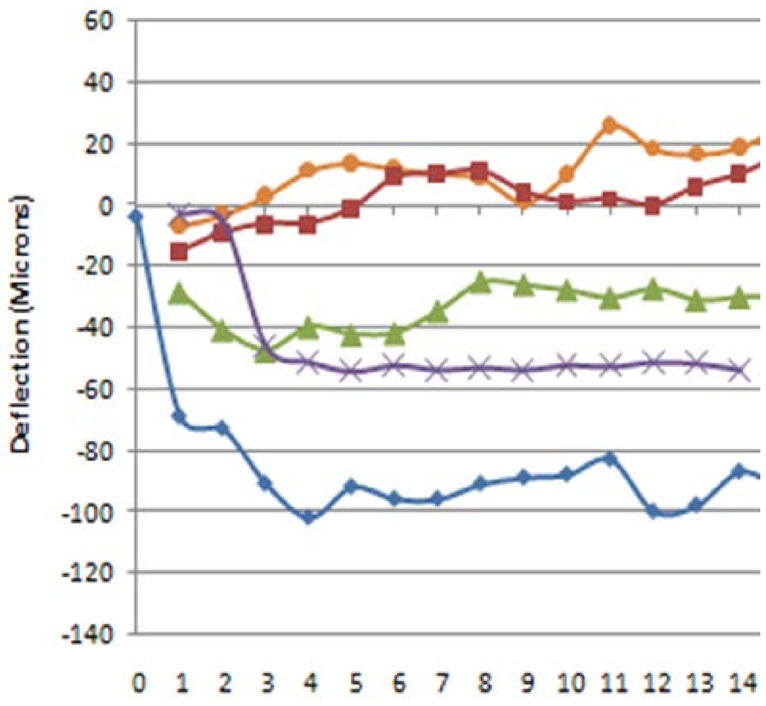
Thermal Mass (Flywheel Effect) to the Rescue:

- Designing in a large mass of thermally-bonded metal above the probe head stabilizes probe card and probe head temperature during those periods when the chuck isn't under the probe head



CTE of Probe Card Assembly Materials

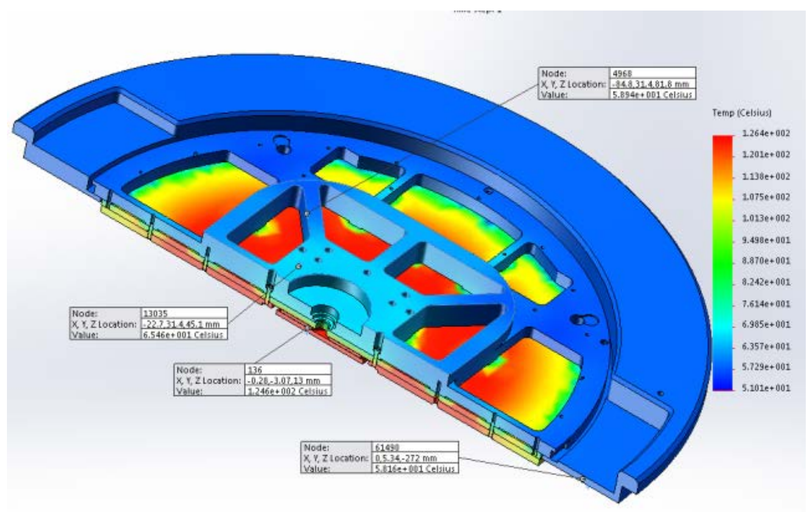
- PCB materials tend to have high CTE (Coefficient of Thermal Expansion) values in the Z-axis (thickness):
  - This means that the probe head can move significantly in Z as the probe card heats or cools – just due to the PCB thickness changing
- The probe card stiffener will also be growing and shrinking due to its own, different CTE in the X-Y plane, resulting in bowing of the probe card either upwards or downwards:
  - This motion is driven by the construction of the probe card, the design and material of the probe card stiffener, whether there's a heat shield on the probe card assembly and the design of the wafer sort interface



- POGO Probe Card used to collect data
- PCB is expanding or contracting causing probe card Z-Movement
- X Scale on the graphic is TIME in MINUTES
- BLUE in the Z height of the average of 4 needles on one probe head
- ORANGE/RED/PURPLE/GREEN lines are locations on the PCB near the probe head at 12/3/6/9 o'clock positions.
- Graphic illustrates that some things are going up, some down, some not moving, etc.

Typical Hot Sort Probe Card Temperatures

- Conductivity is a significant source of heat transfer in wafer sort. This heat transfer is a function of probe head size (% of wafer being touched down upon) and the ΔT between the probe head and the chuck set point
  - This means that test time can change not just the probe card temperature but also the magnitude of Z-deflection seen during temperature sort
- Radiation is also a significant driver
  - For hot sort, a metallic wafer-side heat shield – with an air gap between the shield and the PCB – is a great idea to keep the PCB / probe card stiffener cooler
- A rule of thumb is that tester side of the probe card PCB will reach a temperature of ambient plus 1/3rd the ΔT relative to ambient, for example this RoT predicts that a 150°C sort temp will drive the <u>tester</u> side of the probe card PCB to roughly 65°C



The Wafer Touchdown Pattern Matters

- **DO THIS**: One way to stabilize / manage the temperature of the probe card / head is to use a spiral touchdown pattern, one which moves progressively towards or away from the center of the wafer.
- **DO NOT DO THIS**: A touchdown pattern where the touchdown-to-touchdown pattern arbitrarily / randomly jumps from the center of the wafer to the edge — and back
- **OR THIS**: Start at one edge of the wafer and march across the wafer testing die as if typing out a page of text



VS.

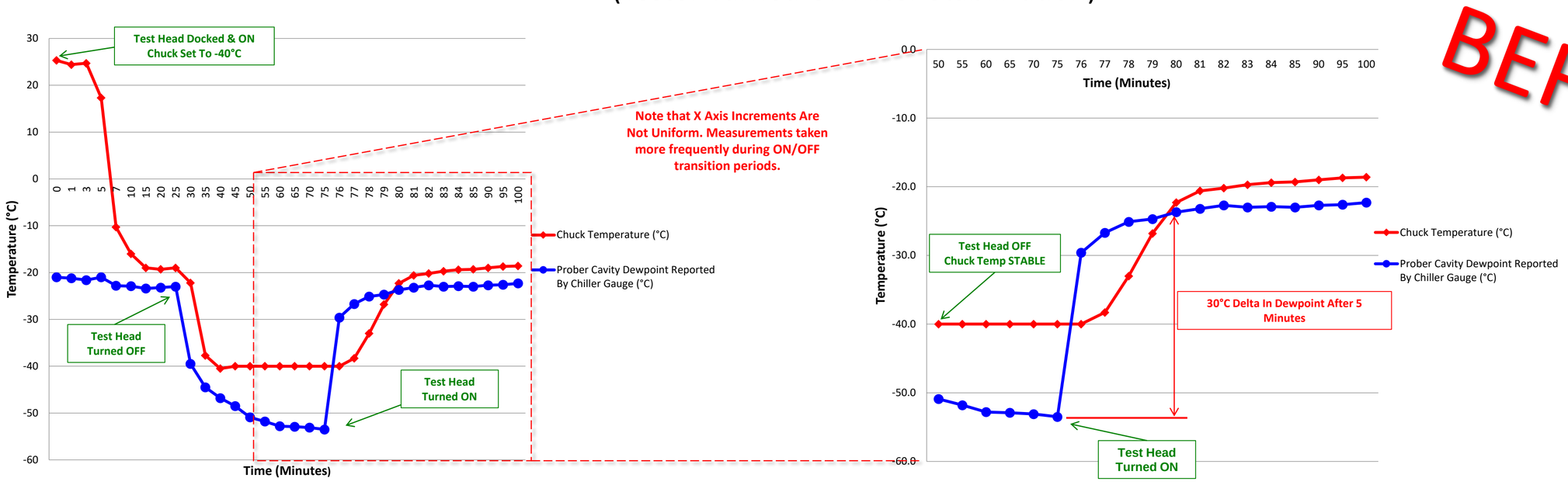


-40° Case Study

- Accretech UF3000EX
  - Prober software requires dew point 5°C less than the chuck temperature to allow the chiller to try to hit a set point.
    - Optimal Δ is ≤-10°C
  - To achieve -40° chuck temp the prober cavity dew point needs to be ≤-45°C (*optimally ≤-50°C*)
- Input Air Dew Point
  - Recommended
    - House Input: -90°C
    - Post prober air dryer: ≤-70°C
  - Required
    - At prober input: ≤-70°C
    - Room: ≤ 6°C
- 24 Slot UltraFLEX Tester with UltraProbe
  - Issues with reaching -40° chuck temperature (*≤-50°C prober cavity dew point*)
  - Existing cold seal handle solution allowed test head fans to draw air from prober cavity
    - Difficult to maintain dew point of ≤-50°C

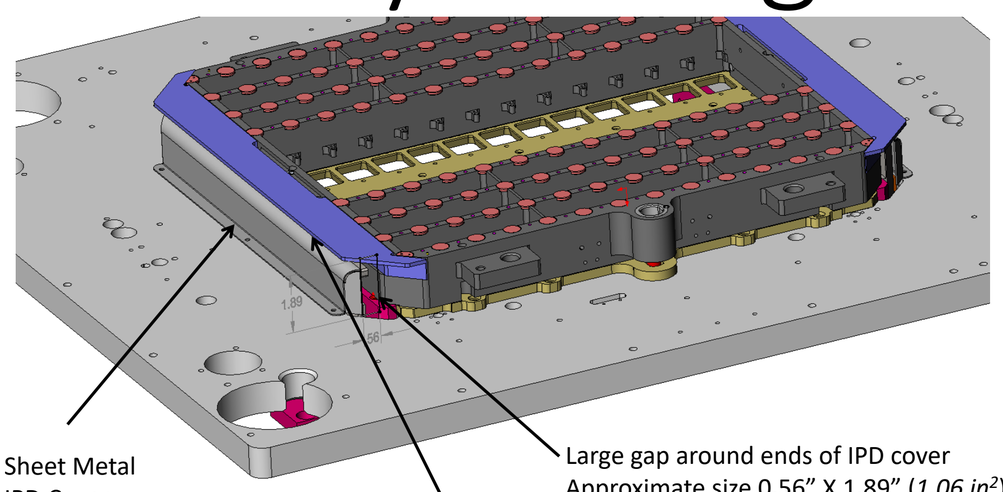
-40° Case Study, continued

Chuck Temperature vs. Dewpoint
(Tester Turned On After Stabilization)



BEFORE

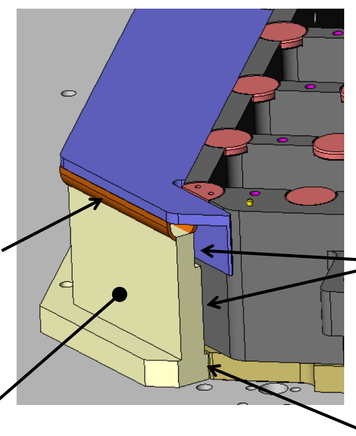
Primary Leakage Path from Prober Cavity:



Sheet Metal
IPD Cover

Large gap around ends of IPD cover
Approximate size 0.56” X 1.89” (*1.06 in²*)

Gap Around PIB side of IPD
Approximate Size .085”x11.5”+ .56 x 1.5” (*1.82 in²*)

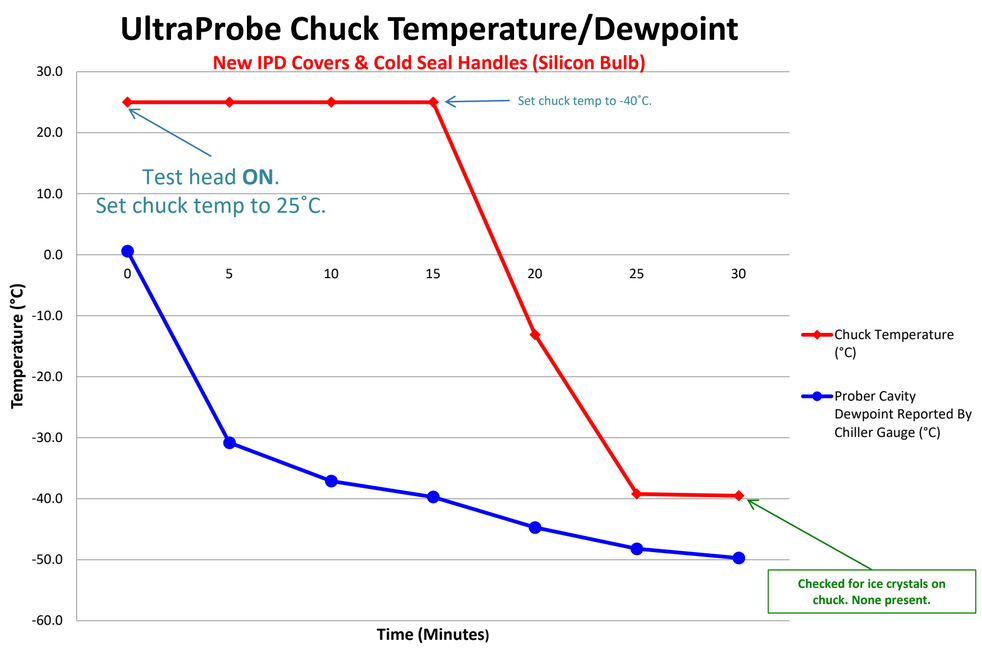


Redesigned Cold
Seal Handle with
Silicone Seal

Redesigned
Machined IPD
Cover

0.10” gap from cover to stiffener
to avoid scraping during docking

Machined Cover Is Mounted
Flush to Existing Plastic ICT on Tester



AFTER

Four Characterization Runs – Same Results Each Run

The Hot and Cold Sort Bottom Line

- The thermally-driven dance of all of the system components in Z has multiple significant potential consequences:
  - Overdrive will change as material expansion and contraction take place:
    - Overdrive changes will move the centroid of the scrub marks in unintended / unanticipated ways
    - If overdrive exceeds the manufacturer’s specifications the probe head will be damaged
    - If overdrive is insufficient otherwise good parts will be binned as bad or underperforming due to out-of-spec’ CRes, reducing test yield

Ensuring Success at the Extremes

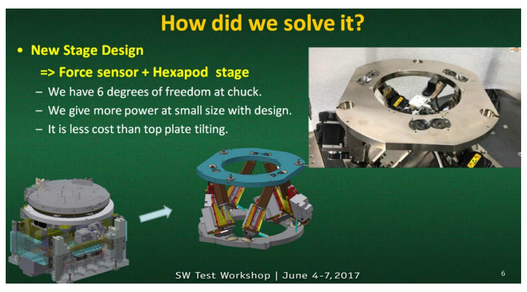
- Extreme temperature guidelines are dependent upon application:
  - The prober should soak for at least two hours after reaching target chuck temperature
  - Probe card soak – at *least* 15 minutes with the probe tips ~ 250µm above the wafer – e.g. not touched down
  - ***After*** probe card soak use the upward-looking camera to set the zero-point for probing
  - Re-check periodically to ensure in-spec’ probe needle overdrive
- Additional Probing guidelines:
  - Complete sealing of prober cavity for cold sort
    - Seal any seams or metal-on-metal interfaces
  - For cold sort meet or exceed Teradyne-recommended facilities CDA purge specs
  - Use new Cold Seal Option with UltraFLEX when probing at ≤-20°C
  - Clean *Dry* Air or N_2 purge is essential for cold, recommended for extreme hot sort (*>125°C*)

SWTW18-8

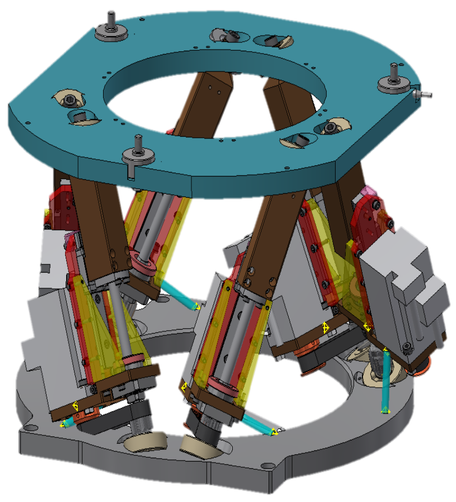
A second study on chuck automatic tilting and chuck force sensing for minimizing probe pin damage and optimization of overdrive

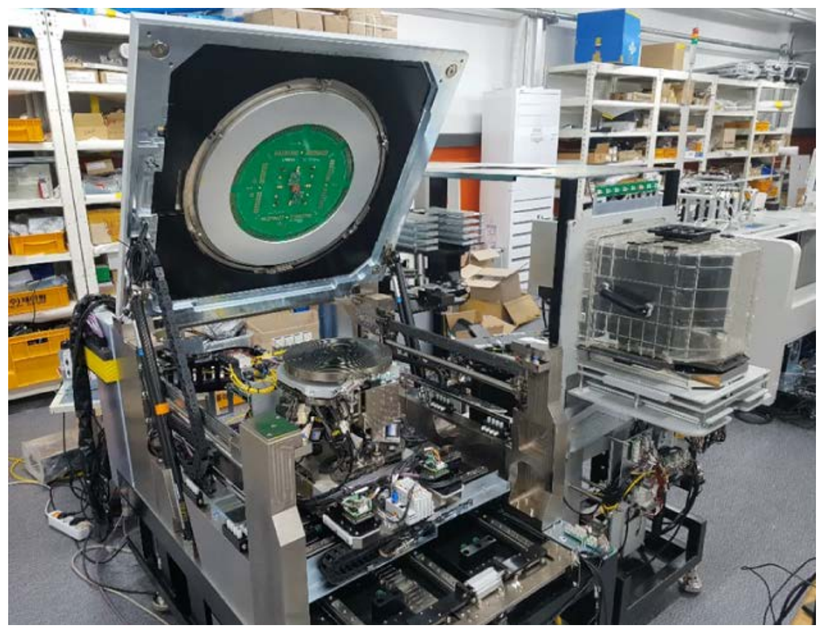
Mr. Byung-Hyun Shin
Semics - Korea

- **Introduction**
  - We had to improve on Hexapod Z since last year.



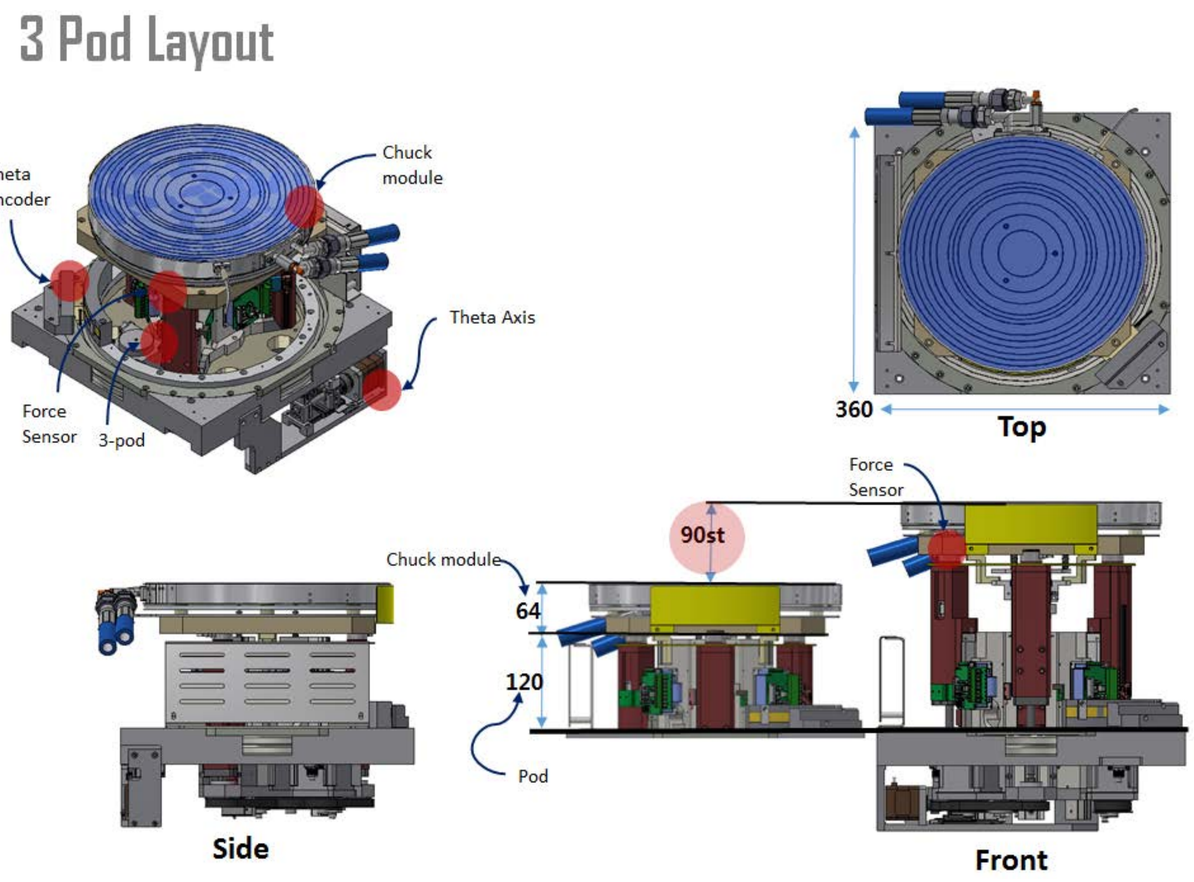






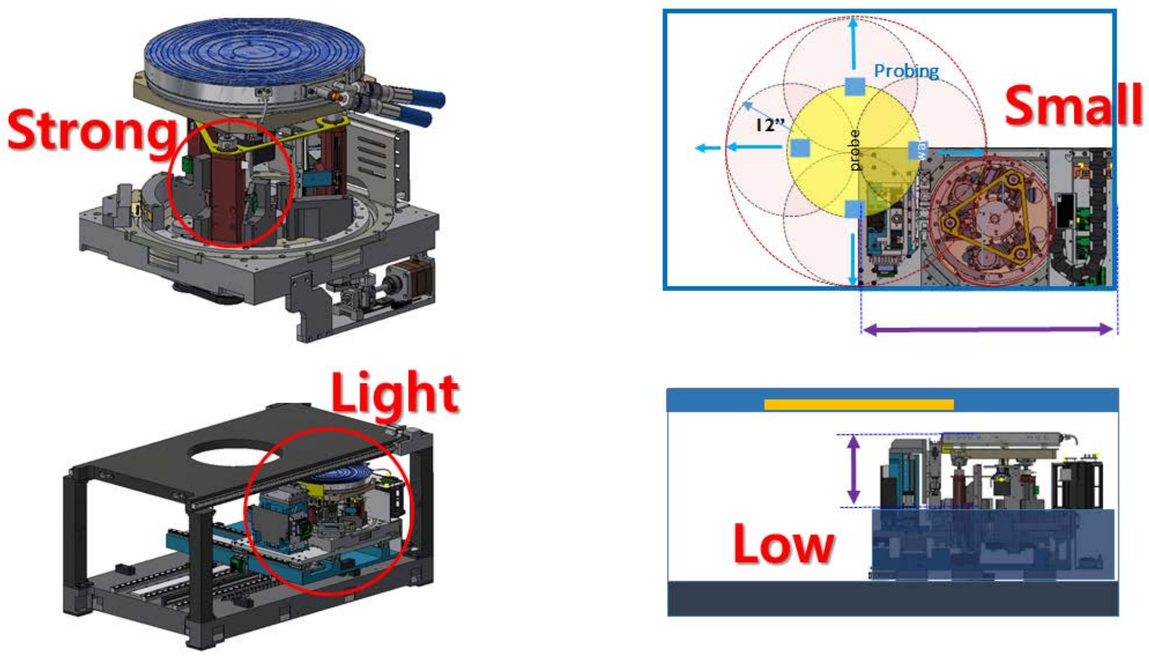
XY moving of Hexapod was not required for Z operations.
The module height was too high to allow for a compact configuration.

- **3POD concept**
- Low module height (120mm) to long stroke distance (90st) can be operated.
- Provides the ability to make parallel contact with the card posture in the individual actions of the pod.
- We can accurately recognize and remember the distribution of force acting on the chuck.



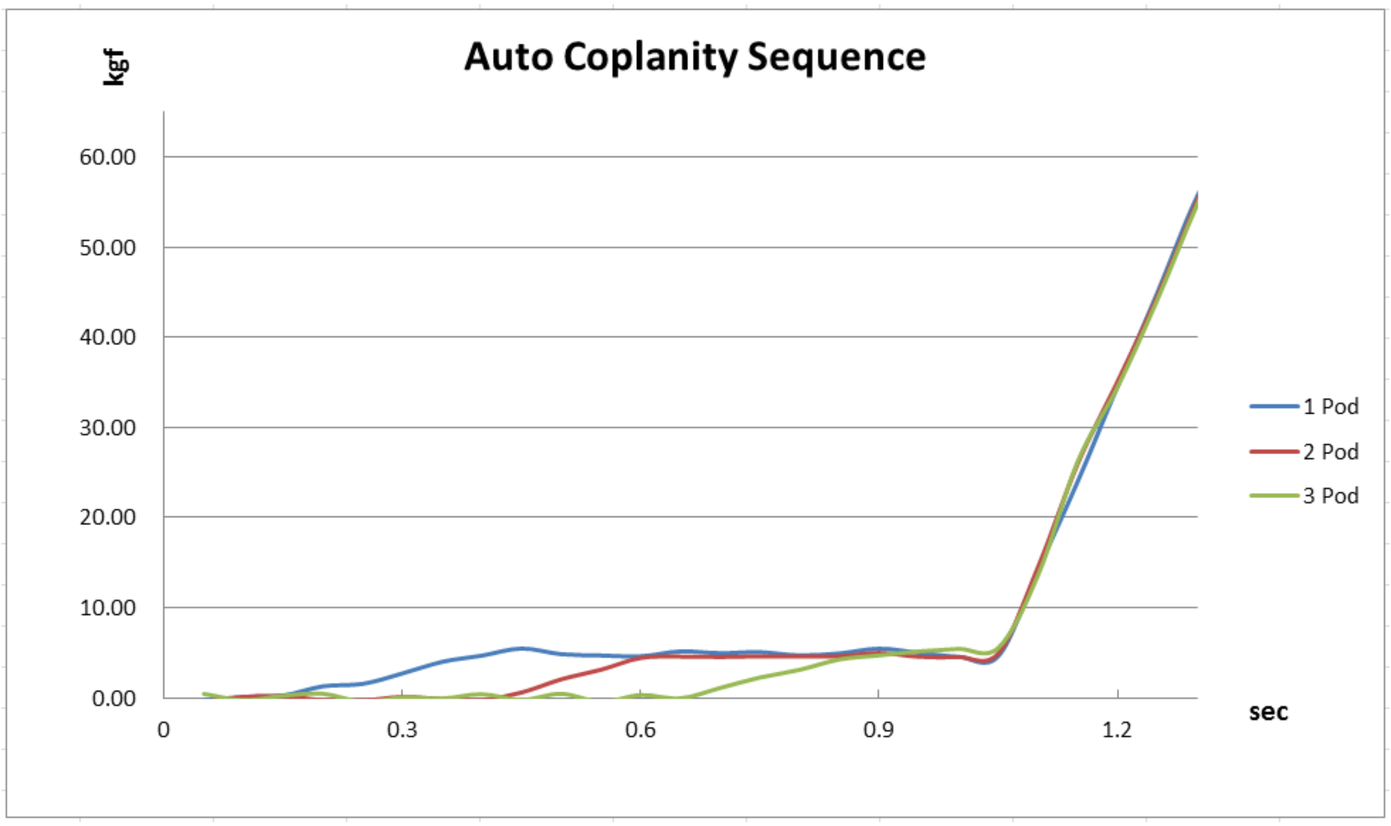
3 Pod Spec

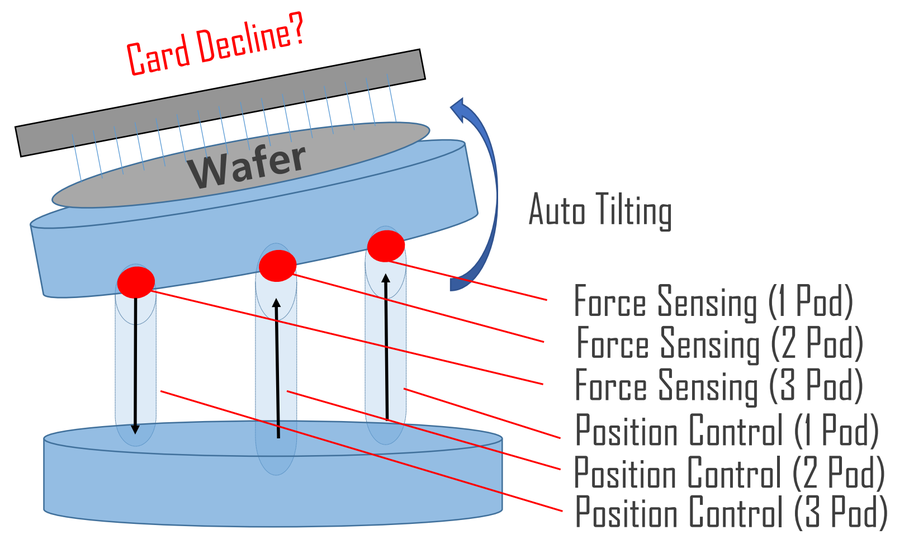
1, Active Stiffness				
1.1 center Zone	Withstand load max	540	kgf	
(Under 200 dia)	Stiffness (active off)	2	kgf/um	
	Stiffness (active On)	100	kgf/um	
	Response Time	100	msec	Compensation completion time after load action
	Overshoot	15	%	deflection compared to deflection of off case
	Control accuracy	±2	um	Z direction
	Control accuracy	±2	um	x,y direction
	Co-Planarity	±2	um	tilting direction
1.2 Eccentric Zone	Withstand load max	180	kgf	
(at 260 dia)	Stiffness (active off)	0.7	kgf/um	
	Stiffness (active On)	30	kgf/um	
	Response Time	100	msec	Compensation completion time after load action
	Overshoot	15	%	deflection compared to deflection of off case
	Control accuracy	±3	um	Z direction
	Control accuracy	±3	um	x,y direction
	Co-Planarity	±3	um	tilting direction
2. Auto Tilting				
2.1 theta_x	Tilting Range	±0.3	deg	
	Max Tilting Velocity	1	deg/sec	
	Tilting Resolution	0.1	arcsec	4x10^-5 deg
2.2 theta_y	Tilting Range	±0.3	deg	
	Max Tilting Velocity	1	deg/sec	
	Tilting Resolution	0.1	arcsec	4x10^-5 deg



More rigid
It has a smaller size
Made lighter
At a lower height
We were able to put the core functionality of the 3pod in the narrow space of the Prober.

- **3 POD Test**
  - The Measurement of Auto tilting Test.





0 ~ 0.45 sec Block : First Contact at 1 Pod Position,
1 & 2 & 3 Pod Continue to Up
~ 0.7 sec Block : Second Contact at 2 Pod Position,
1 Pod Stop to Up, 2 & 3 Pod Continue to Up
~ 1.0 sec Block : All contact and Up to same Load
1 & 2 Pod Stop to Up, 3 Pod Continue to Up
~ Time of change Card : Motion with same decline

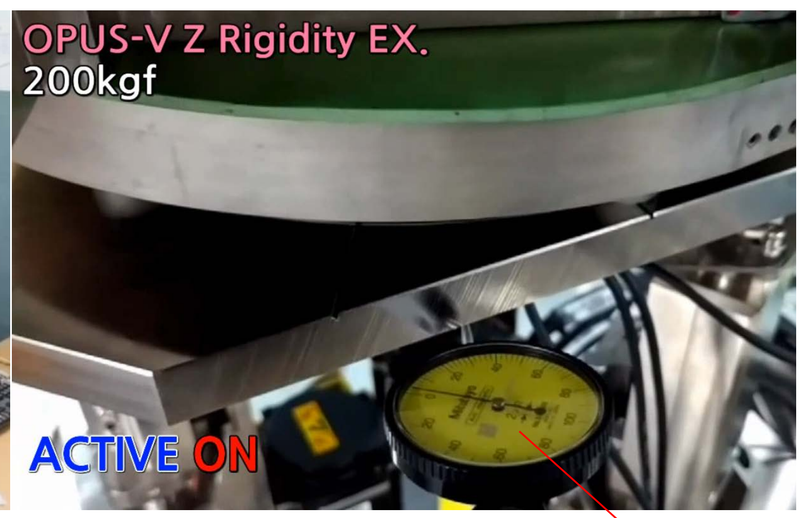
12 inch Tablet PC

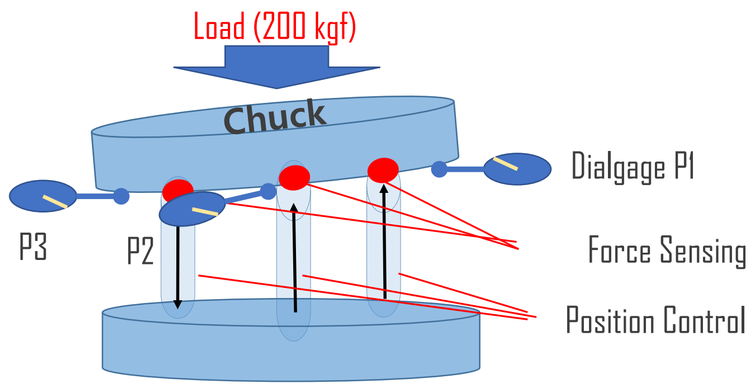
Contents :

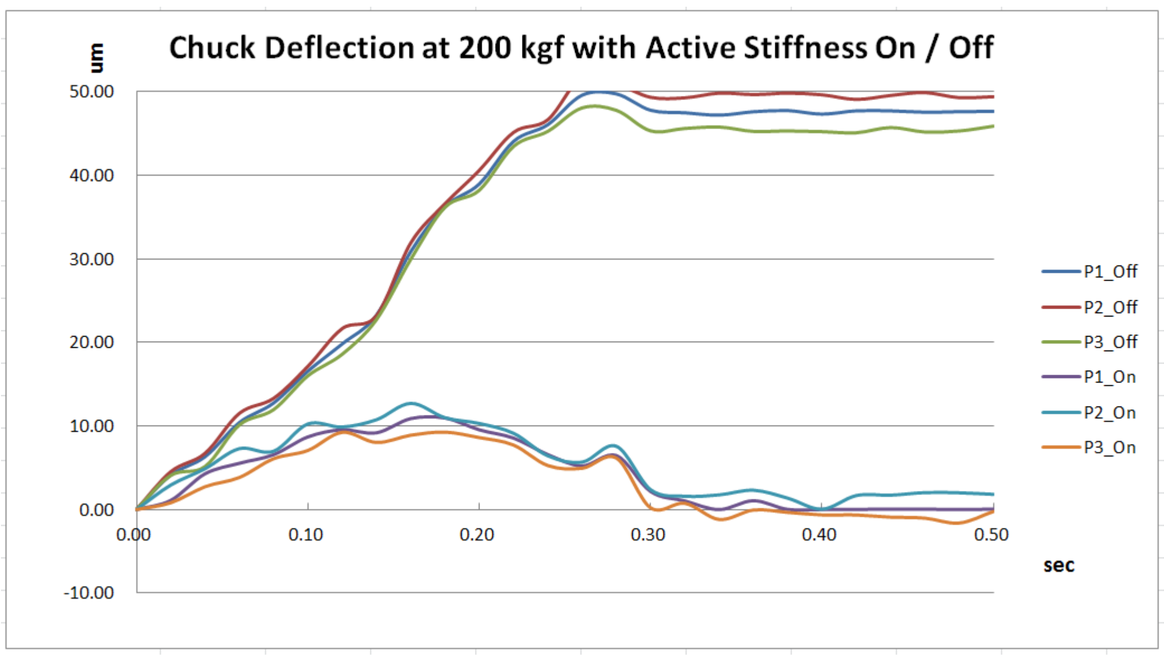
1. Hexapod dancing
2. Shortcut of 3pod CAD Model
3. Testing of Auto Tilting
4. Testing of Active Stiffness
5. Shortcut of OPUS V Prober
6. Shortcut of Group Prober

- Measurement of Active Stiffness Test.







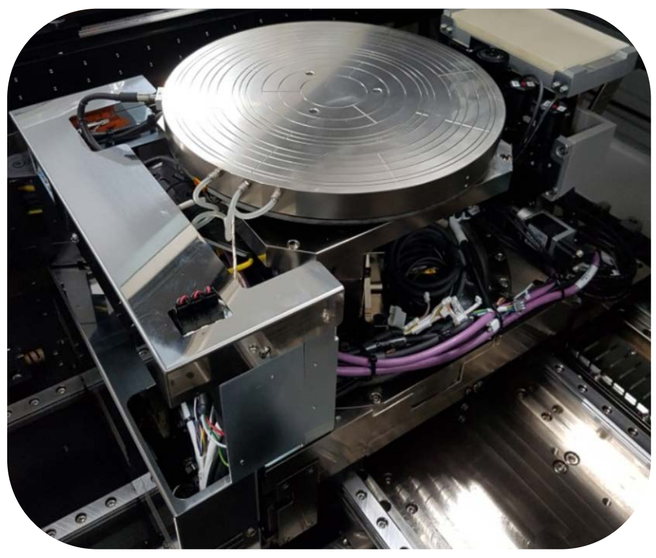


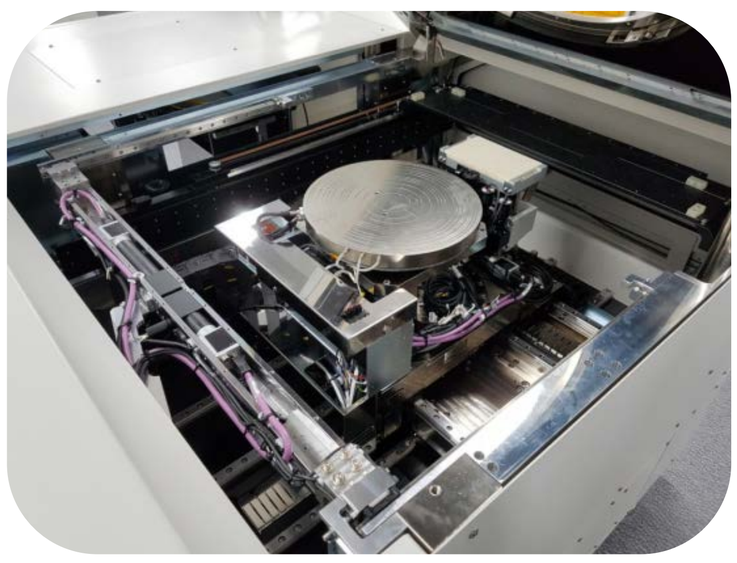
P1_Off ~ P3_Off : Off mode of Active Stiffness
Put down 200kg in the around center by a forklift.
As put it down slowly, the displacement also increases slowly.
P1_On ~ P3_On : On mode of Active Stiffness
Put down 200kg in the around center by a forklift.
As put it down slowly, The displacement increases more slowly,
then decreases and approaches zero.

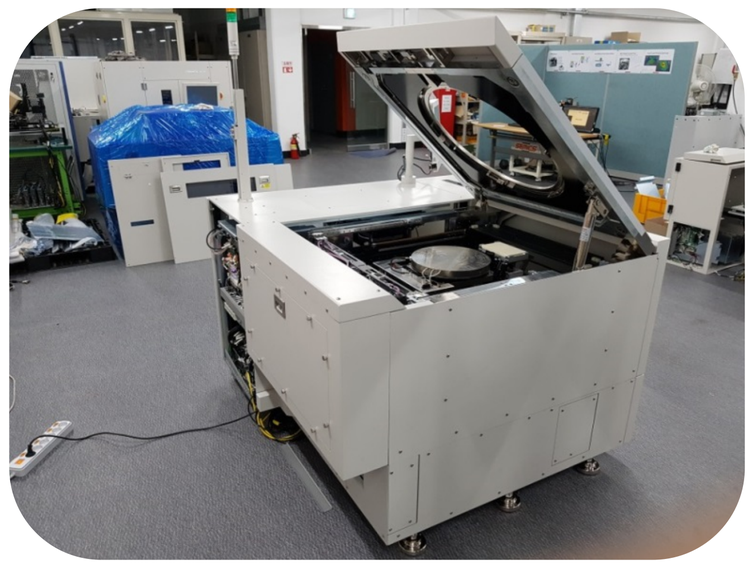
- The benefits of applying 3POD.

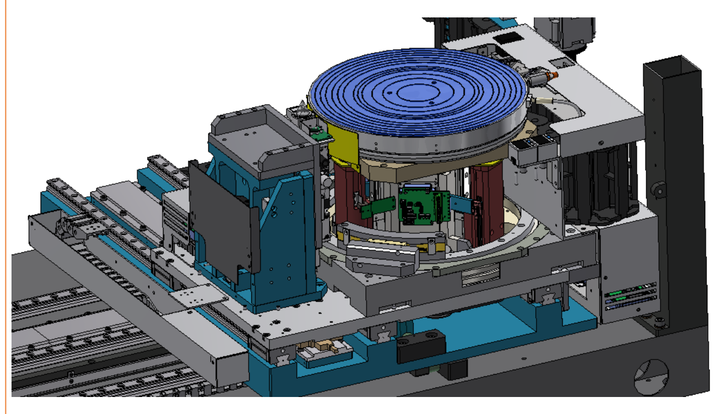
  The only Z Stage with “Chuck Auto Tilt Function“ for easy co-planarity.
  The only Z Stage with “Active Stiffness” for highest rigidity.
  The only Z Stage can withstand over 800 kgf payload. (with change of option)
  Z Stage with the most "optimal space utilization and unit modularization".
  Z Stage with the most "light weight realization".

- **Actual Application of 3POD : Opus V and Group Prober**

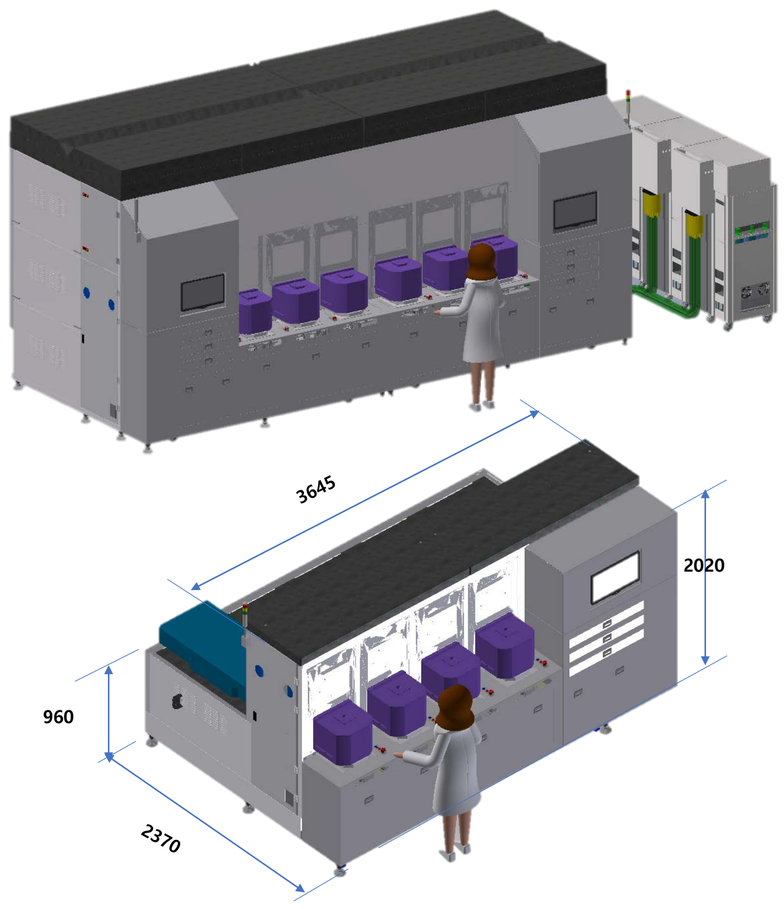


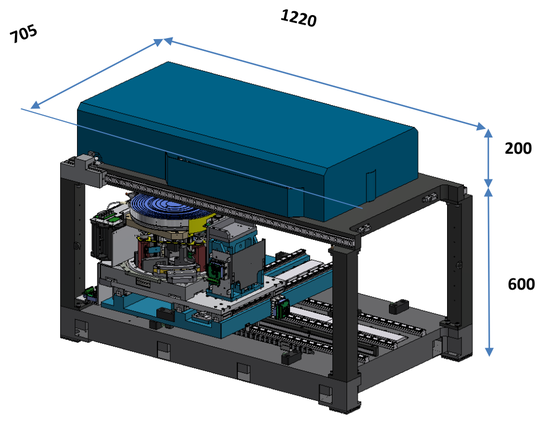


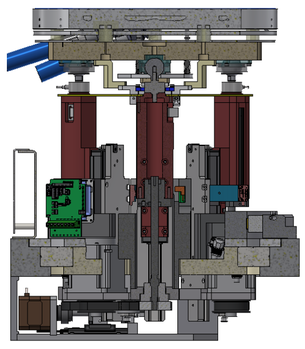












Questions ?

If you have any questions, please contact

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Useful Links for Technical Posters

Why semiconductor testing people are great. (Youtube)

- https://www.youtube.com/watch?v=RBWn-6FdQ3Y&feature=youtu.be

SWTW18-60

Modern Probe Card Analysis…
Addressing Emerging Needs Cost-Effectively

Kjell Lundberg, Greg Olmstead, Deb Ahlgren, Audria Hurst, John Strom, Andrew Frazier
Rudolph Technologies

Introduction

Advances in semiconductor and test technologies have conspired to pose new challenges to probe card and probe card analyzer suppliers and their customers.

This session addresses those challenges and potential solutions.

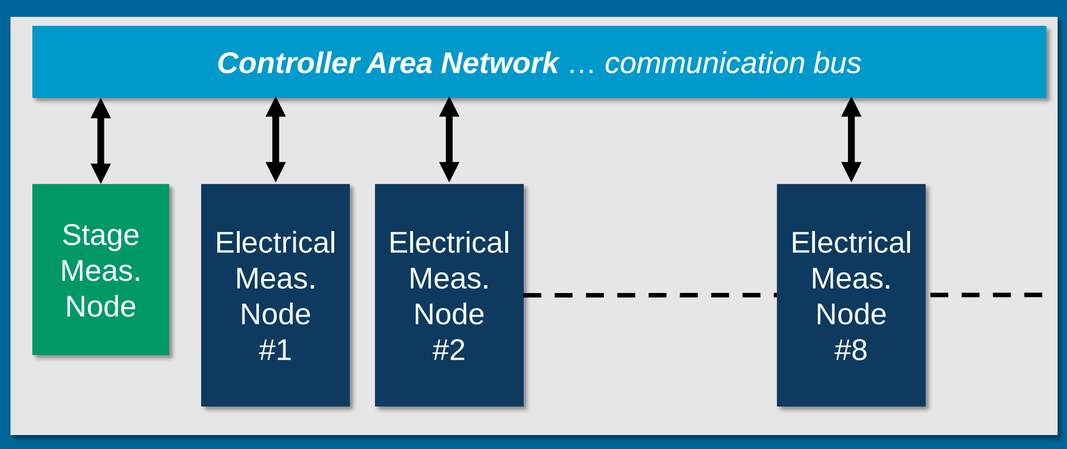
- **Scalable architecture delivers**
  - Higher channel counts
  - Flexible circuit and power control for enhanced test coverage
  - Enhanced throughput –modularity and parallelism
  - Electrical states for advanced debugging and repair
- **“Infinite plane” for Probe Card Interface expansion**

Scalable Architecture for Expansive Channel Counts

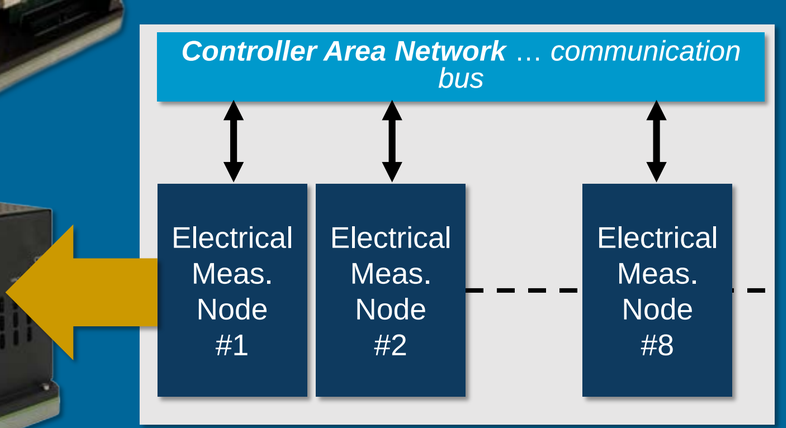
Challenge: Modern probe cards require higher channel counts and re-configurability.

Solution: Implement scalable design

- 14,400 channels ... scalable to market requirements.
- Electrical Measurement Nodes (EMNs) attach/detach from CAN bus as needed
- Electrical measurements taken directly by devices within EMN







Scalable Architecture for Expansive Channel Counts

Node Controller Board

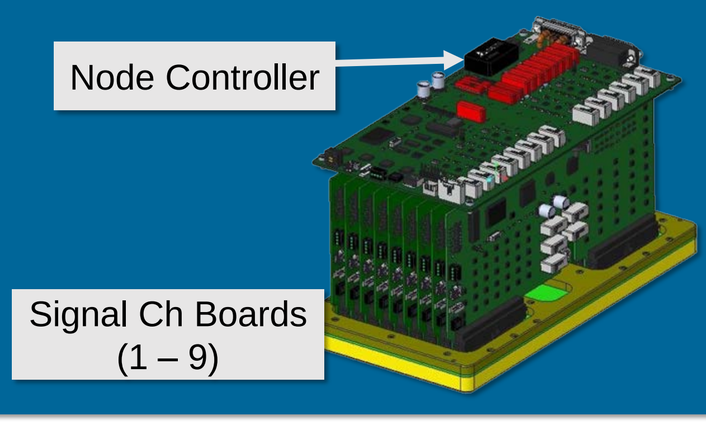
- Contains meters and programmable supplies
- Improved measurement fidelity
- Connections for external supply inputs (driven by state control)

Signal Channel Boards (1-9)

- Standard signal measurement channels or low current utility channels

Utility Channel Board

- Low and expanded high current capable utility channels

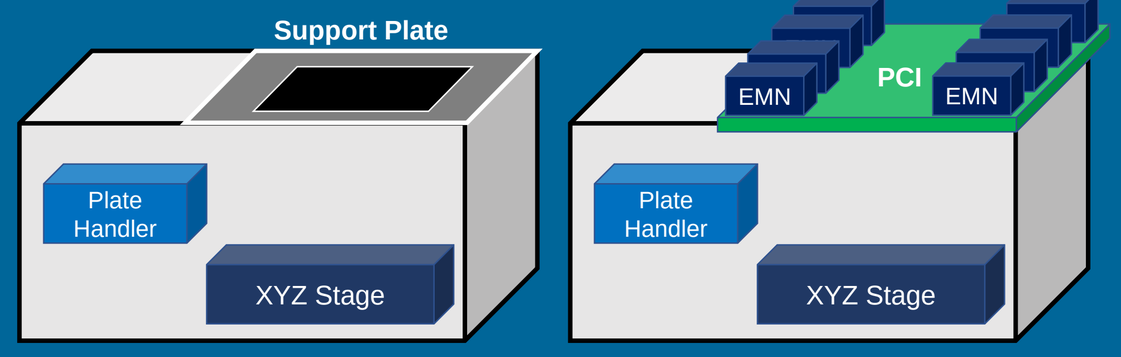


“Infinite Plane” Architecture

Challenge: Protect Probe Card Interface investment.

Solution: Implement an Infinite Plane architecture.

- Legacy compatibility as well as large expansion in X, Y, and Z



Flexible Power and Circuit Control – Enhanced Test Coverage

Challenge: Probe card designs require multiple power supplies

Solution: Multiple programmable supplies.

- Connection to industry standard voltage levels via programmable supplies
- Current limit can also be set for the programmable supplies

External Port Connection

- Connect to an external port allowing for an external device connection (power supply, meter, etc.)
- Driven from within the probe card’s state definition

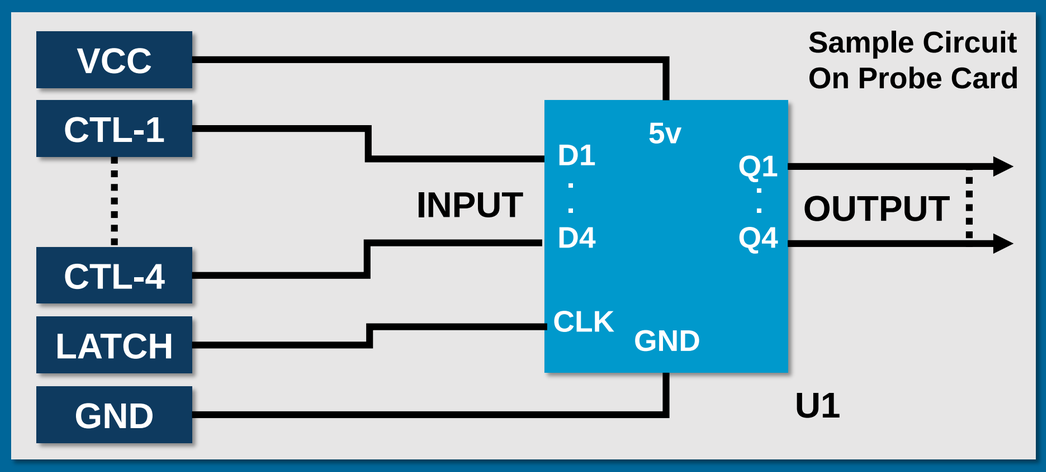
Enhanced Circuit Control Within Probe Card Definition

Challenge: Advanced probe card electrical designs require enhanced circuit control to expand test coverage.

Solution: Analyzer supports state definition and activation during probe card test.

Example: Sample circuit on probe card requires sequencing four bit input (D1-D4) from 0 to F (HEX) to drive output and corresponding circuitry.

- Generate entries in probe card state definition to establish power connections and perform logic actions
- Once a state is defined, it can be assigned to specific probes and/or components
- State will be activated when testing these specific probes and/or components. State can also be activated manually while in debug mode.



Steps to generate state definition for sample circuit on probe card.

Define Power State:
VCC, GND

↓

Define Control Line Inputs:
CTL - 1, 2, 3, 4

↓

Define Clock Input:
LATCH

↓

Define Logic State to Sequence Input from:
0 to F

↓

Assign State:
Probe, Component, Global

Debugging and Repairing Electrical State Issues – Stepping Through Defined States

Challenge: Must validate and troubleshoot advanced circuits on probe card.

Solution: Enhanced circuit control provides sequenced definitions allowing for active 'step-mode' debugging.

Example: Corresponding devices/circuitry connected to output of U1 are not functioning properly thus need to actively troubleshoot input/output conditions.

- Operator can step through state definition's power and logic entries as desired and verify circuit input/output conditions

Debugging and Repairing Electrical State Issues – Stepping Through Defined States

- Input and output test points can be monitored while stepping through defined state actions.
- Power supply current draw will also be monitored during state activation triggering fault conditions when exceeding established current limits

Step through defined Power State that connects:
VCC, GND

↓

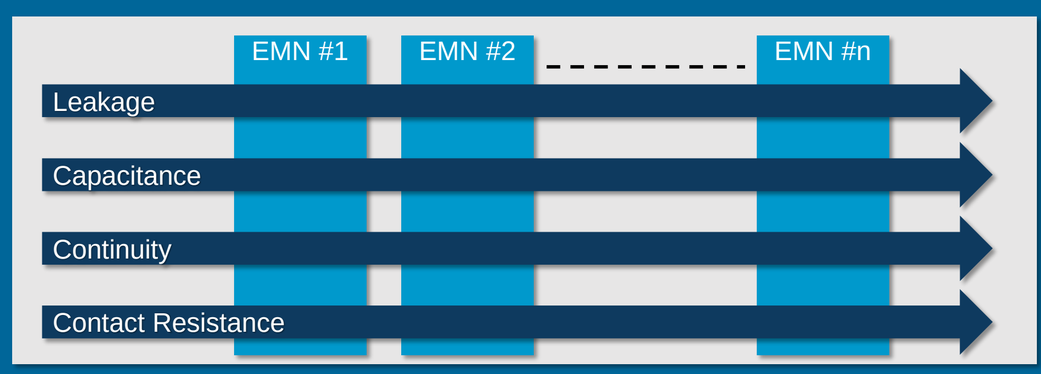
Step through defined Logic State that sequences input from: **0 to F**

Parallelism and Test Modularity Deliver Throughput Improvements

Challenge: Advanced probe cards require an extensive suite of electrical tests to achieve acceptable test coverage.

Solution: Scalable analyzer architecture supports many electrical test measurements in parallel.

With each Electrical Measurement Node (EMN) having independent meters, electrical measurements are performed in parallel across nodes when possible.

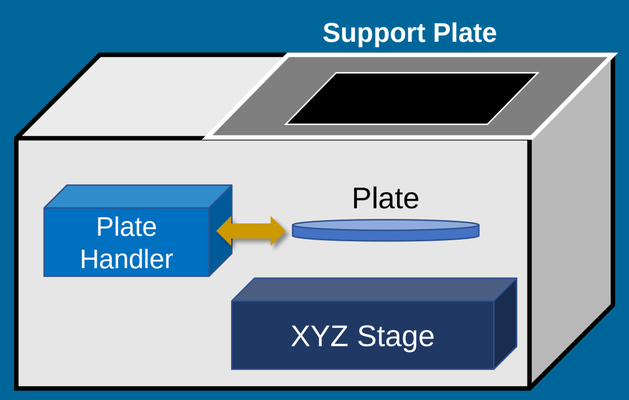


Parallelism and Test Modularity Deliver Throughput Improvements

Challenge: Tests of advanced probe cards require manual user interaction with system during active test.

Solution: Optimize automation of analyzer; implement automated plate handling.

- Accessory plates will be loaded/unloaded automatically during test (cleaning, contact resistance, leakage at overtravel, etc.)
- Accessory plate size allows for single touchdown of entire array during test
- Accessory plate loading/unloading does not compromise probe card or PCI placement thus optimizing productivity/stability/repeatability

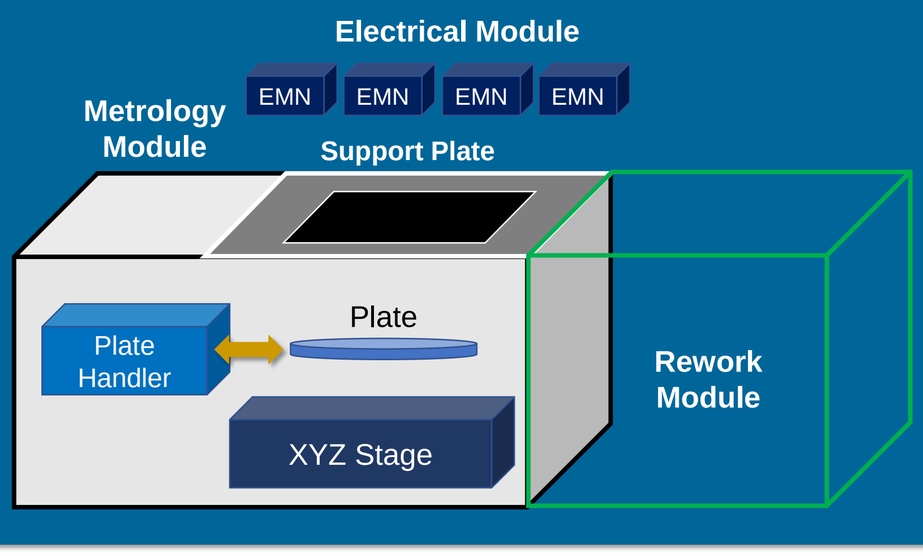


Parallelism and Test Modularity Deliver Throughput Improvements

Challenge: Advanced probe cards require incremental (and more advanced) testing to validate performance. This must be delivered cost effectively.

Solution: Analyzer architecture must be modular to support flexible requirements; the architecture must be cost-effective.

- Metrology with automated plate handling
  - Stage components for testing planarity, alignment, contact resistance, cleaning
- Electrical
  - Electrical measurement system for testing leakage, capacitance, confirming bussed channels, detecting shorted channels, capacitor/resistor measurements, enhanced circuit control
- Rework
  - Provide capability for probe-side access

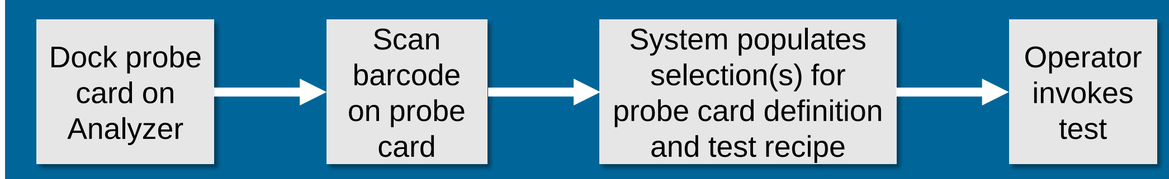


Process Control – Probe Card ID

Challenge: Probe and probe card manufacturing floors increasingly support multiple probe card technologies. Recipe management becomes complex driving the need for process control.

Solution: Drive card/recipe selections using barcode identifier on probe card.

- The number of selections presented will be controlled based on configured mode (multiple or golden single)
- This flow is similar to the SECS/GEM mode of controlled card/recipe selection

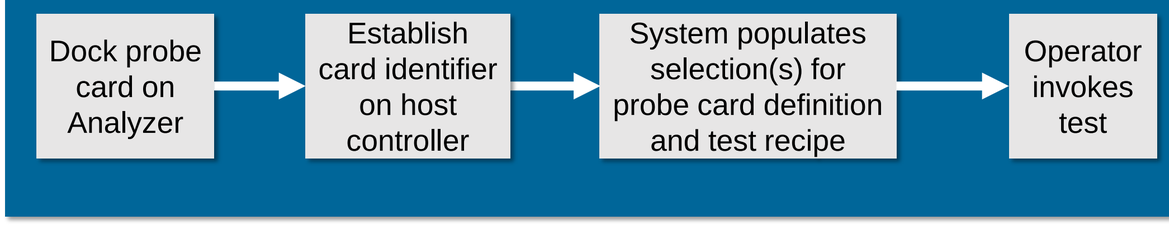


Process Control – SECS/GEM

Challenge: Incremental probe card manufacturing and probe floor complexity drive the need for process control and reporting of tool status.

Solution: Provide SECS/GEM capability.

- Controlled card/recipe selection via host controller (similar to barcode driven test)
- System status mode and requests: remote/local, idle/processing/running, up/down time
- Alarm event reporting, handling, and logging

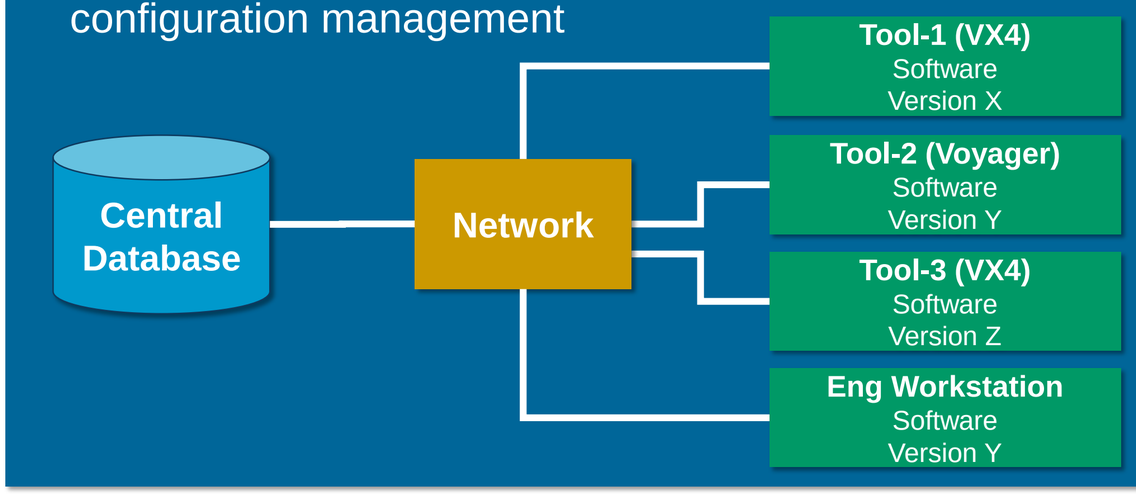


Centralizing Database – Flexibility

Challenge: Probe and probe card manufacturing floors increasingly support multiple generations of probe card technology and analyzer capability. Recipe and software revision management becomes complex.

Solution: Implement flexible database design so that analyzers are not required to run same software version.

- Tools running different software versions are able to share same database
- Card and recipe definition versions managed by tool and database
- Centralized database also allows for remote tool configuration management

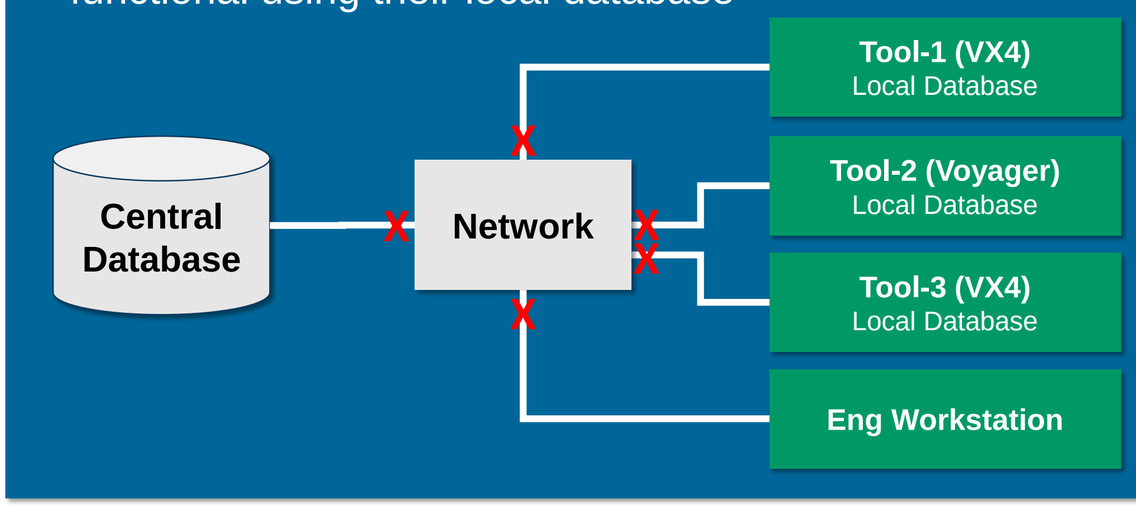


Centralizing Database – Fault Tolerance

Challenge: Fluctuations in power source or network availability disrupt manufacturing process.

Solution: Implement fault tolerant distributed database design.

- Local database used as primary source
- Local and centralized database are synchronized
- If centralized database or network go down, tools are still functional using their local database



Summary

This paper addressed some of the new challenges and potential solutions to probe card and probe card analyzer suppliers and their customers.

- Scalable architecture for expansive channel counts
- Infinite Plane architecture supports Probe Card Interface flexibility
- Flexible power and circuit control for enhanced test coverage
- Parallelism and Test Modularity deliver throughput improvements

Contact Information

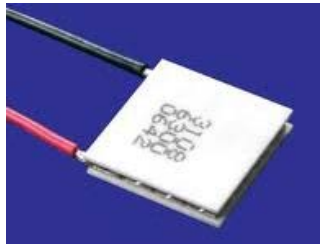
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A short history of wafertest and todays 2 most common cooling technologies for thermal chuck systems

Outline of various Thermal control methods

- In the early 1970s temperature testing started to be performed on wafer level. The wafer sizes were roughly 2” in diameter and if temperature control was performed, it happened by way of a peltier element inside the chuck, a thermo-electric device on which one side heats up and the other cools down depending on which direction the current flows. The applications were simple wafer sort during which the functionality of the chip is confirmed prior to dicing in its individual components and packaging. This gives the manufacturer the opportunity to discard the bad devices early on in the production process thereby saving the packaging and final test costs for those devices, as well as to match the quality of good devices to markets.
- The simple heating concept behind most hot testing of semiconductor wafers today is the same as we see in everyday cooking applications. A resistance heater is built into a plate (i.e., chuck) that is slightly larger in diameter than the wafer that will rest on it during test.
- A good “hot chuck” is recognized not only by how hot it can get, but how fast it gets there, how uniform the temperature is across its diameter, how rigid and flat it is, and how electrically quiet it can remain during test. As the need for cold test began to increase with the increase of semiconductor devices in automobiles, as well as in space and military applications, a common and very successful solution came to market that combined the resistance heater of the simple hot chuck together with the flow of a coolant through the chuck.



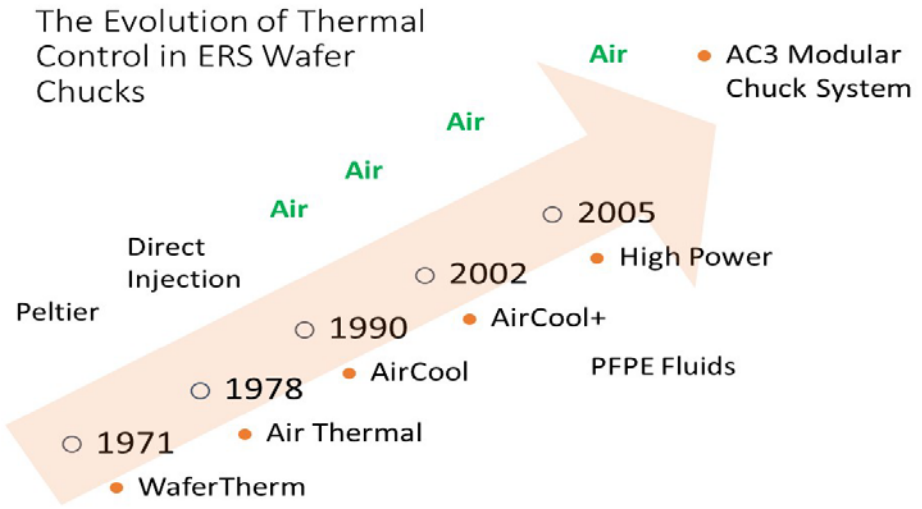
Left: peltier element

Right: resistance heater

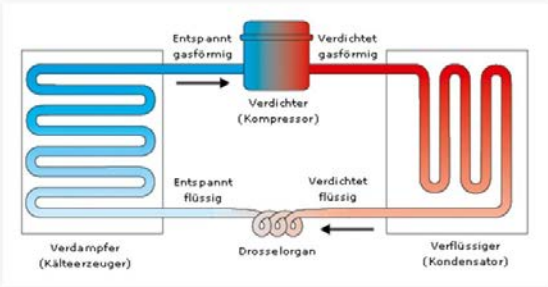


Thermal Control Methods balance Heating and cooling

1) Thermoelectric effect, peltier elements, heating and cooling, liquids required
2) Direct injection of expanding gas (i.e. freon), resistance heating
3) Recirculation of water/ glycol, resistance heating
4) Recirculation of PFPE liquids, resistance heating
5) Separation of compressed air (air booster), resistance heating
6) Super chilled air with advanced heat exchanger system, resistance heating

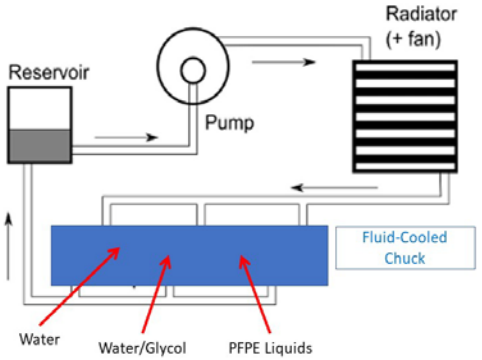


Cooling By Direct Injection of Expanding Gas



Direct injection of expanding gas. Pro: high cooling capacity Con: reliability concerns

Cooling By Recirculation of Fluids at Room Pressure



Liquid cooling Pro: high cooling capacity Con: high maintenance

Cooling By Separation of Compressed Air



Separation of Compressed Air Pro: inexpensive, no maintenance Con: limited cooling capacity

Cooling is critical - To control the temperature of the chuck - and thus the temperature of the wafer under test - tool designers employ a number of technologies The 2 most common chiller cooling technologies today are: synthetic cooling liquids and air.

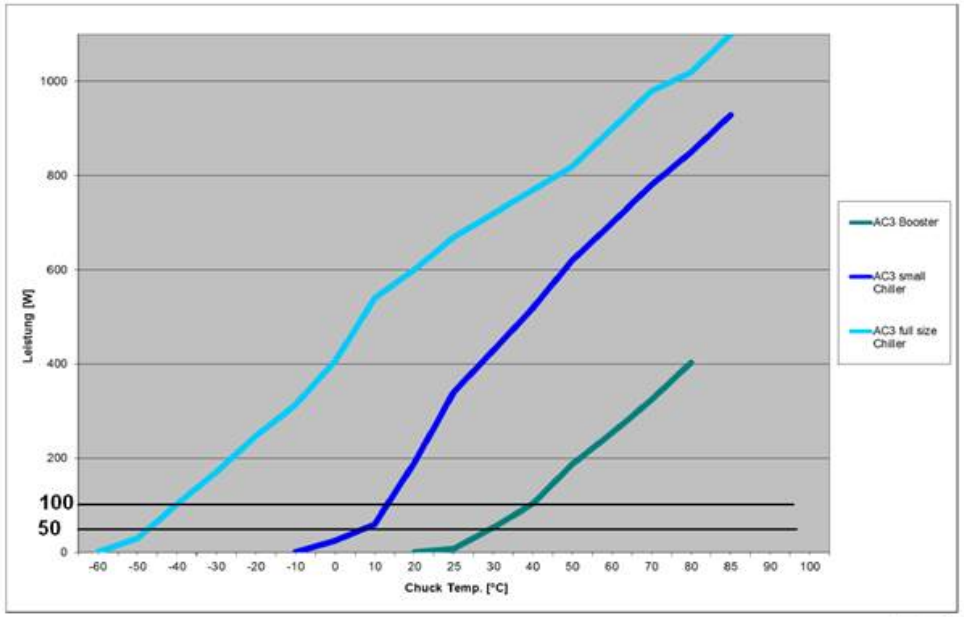
Liquid - The use of synthetic cooling liquids such as perfluorpolyether (PFPE), sold under various brand names is widespread and accounts for the majority of older cold chillers in operation. These inert liquids are chemically stable as long as the operating limits are not exceeded, and they can be used in a broad temperature range typically from about -70°C to +120°C. Because they are very poor conductors of electric current, they do not pose a danger of short-circuits in the case of leakage. Compared to water, the thermal properties of these coolants are less suitable for heat removal. Depending on the type, these coolants are sometimes closer to air than to water. In contrast to water, even to purified water, synthetic cooling liquids, however, are rather costly. Since these liquids evaporate over time even in closed circuits, the systems need regular refills. In addition, they require a complex infrastructure to handle their logistic and environmental implications. Though they are not highly toxic, these liquids are subject to hazardous waste legislation that adds to their already high operating costs. In case their operating temperature range is exceeded, there is a theoretical risk that they could disaggregate into their chemical constituents. These can include highly toxic and otherwise hazardous gases such as fluorine or chlorine. This limitation restricts the use of PFPE-based liquids to relative low temperatures; at the same time, their utilization is associated with high costs and technical complexity.

Air – A newer invention uses air as the cooling medium since virtually every semiconductor manufacturing line has a ready supply of pressurized clean dry air (CDA) easily accessed at the wall utilities behind the equipment in the factory. In contrast to water, other liquids, and synthetic cooling agents, when air is used as the coolant, it does not impose any limitations with respect to the temperature ranges required for semiconductor test. In addition to any use as a coolant, large amounts of CDA (or other very dry gas) will be necessary as an environmental purge to prevent frost in the wafer test area inside of the equipment. Failure to reliably prevent frost in the test area can result in the destruction of the very expensive electrical probes used during cold wafer test. That requirement for environmental dry air (or gas) purge exists independent of whatever coolant is used to achieve the temperature in the wafer chuck.
The drawback of air as a coolant is its relatively low thermal capacity. However, given the availability and flexible handling of air, this drawback does not have a high material impact. The heat exchangers used in ERS's AC3 thermal system effectively cancels out the drawback of the lower thermal capacity, while benefitting from the smaller footprint, lower utilities costs and application flexibility associated with using air as the coolant. The patented heat exchanging system on the AC3 extracts maximum cooling from the chilled air and then utilizes that same air to purge the test area. This effectively reduces the consumption of air and mains power.

With test floor space at a premium, the more compact air chillers have been gaining in popularity over the last 10 years. Lower maintenance requirements and operating costs translate directly into productivity gains and uptime. As the need for cold test continues to increase in sync with automotive semiconductor applications, environmental responsibility and lowering power consumption continue to drive the demand for maximizing efficiency. Reducing chemical consumption remains on top of the list for environmental health organizations and therefore clean and green chiller technology continues its march forward.

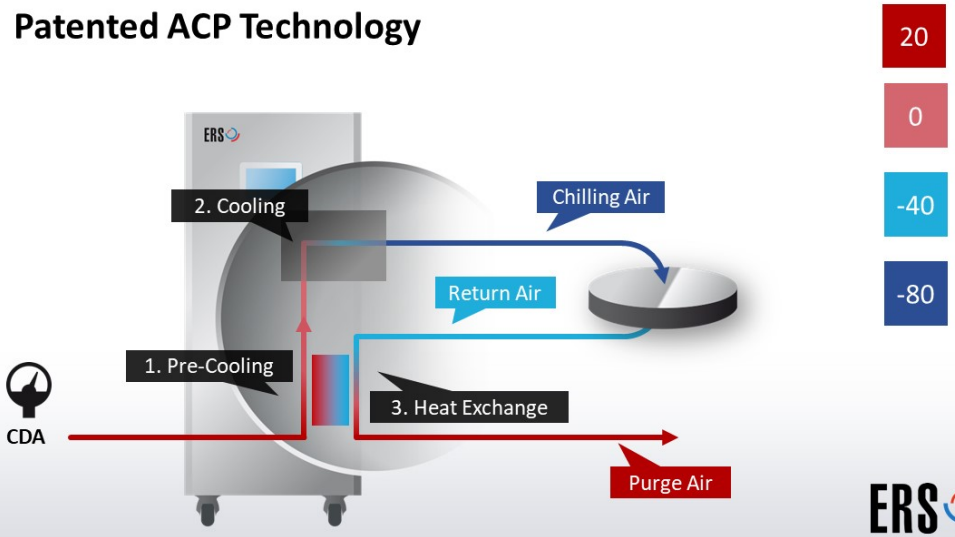
While not all applications can be served by air, there is a substantial segment where air is suited as the ideal cooling medium. The notable exception may be high parallel memory test at deep cold temperatures where the cooling capacity of liquid system needs to be in the 400-600W range.

Performance Chart of Different Chuck Systems



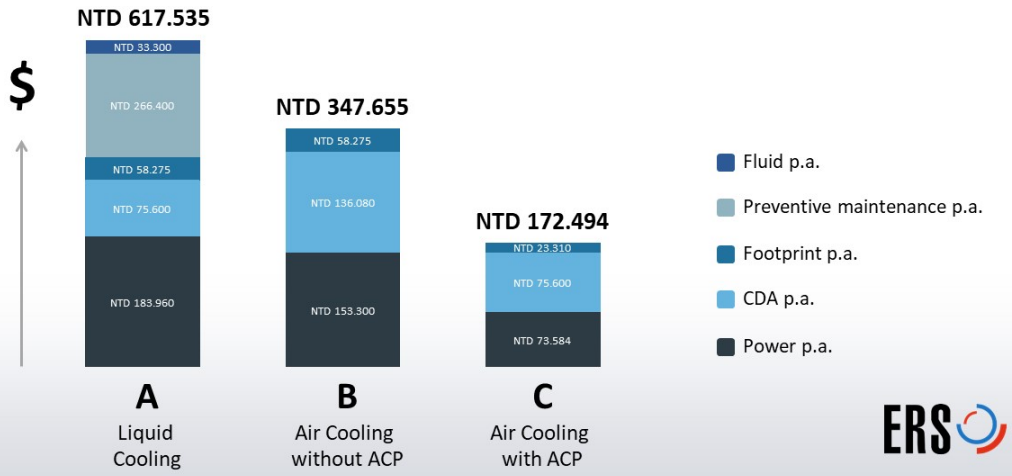
ERS

Patented ACP Technology



ERS

Operating Costs for Cold Test, All Costs Considered



ERS