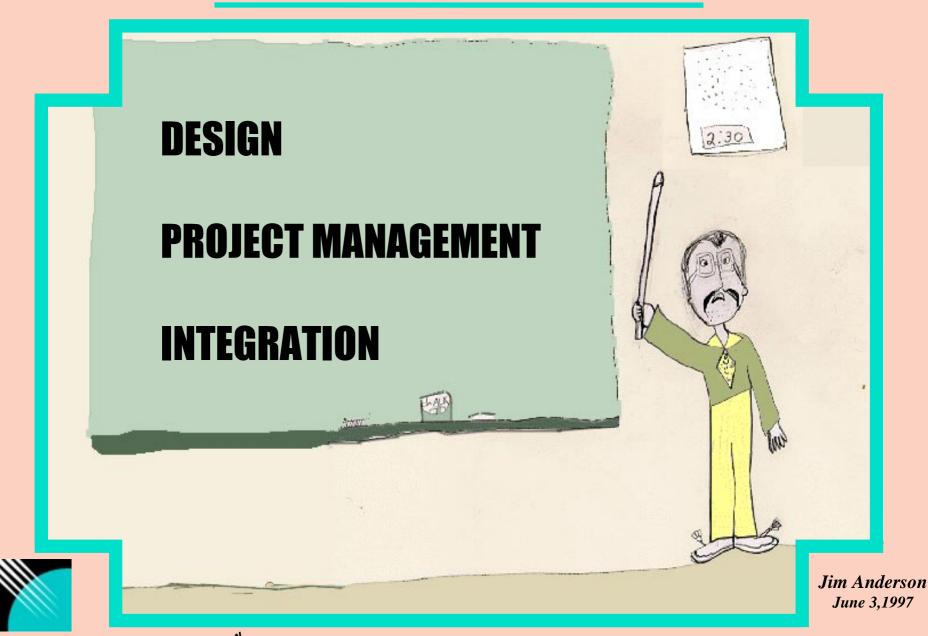
Design Concepts For A Total Integrated Solution

PRESENTED BY JIM ANDERSON

SOUTHWEST TEST WORKSHOP

SAN DIEGO, CALIFORNIA JUNE 1997





DESIGN SYSTEM DESIGN

>> CUSTOMER INITIATIVE - CONCEPT **SPECIFICATION**

>> SYSTEM PERFORMANCE

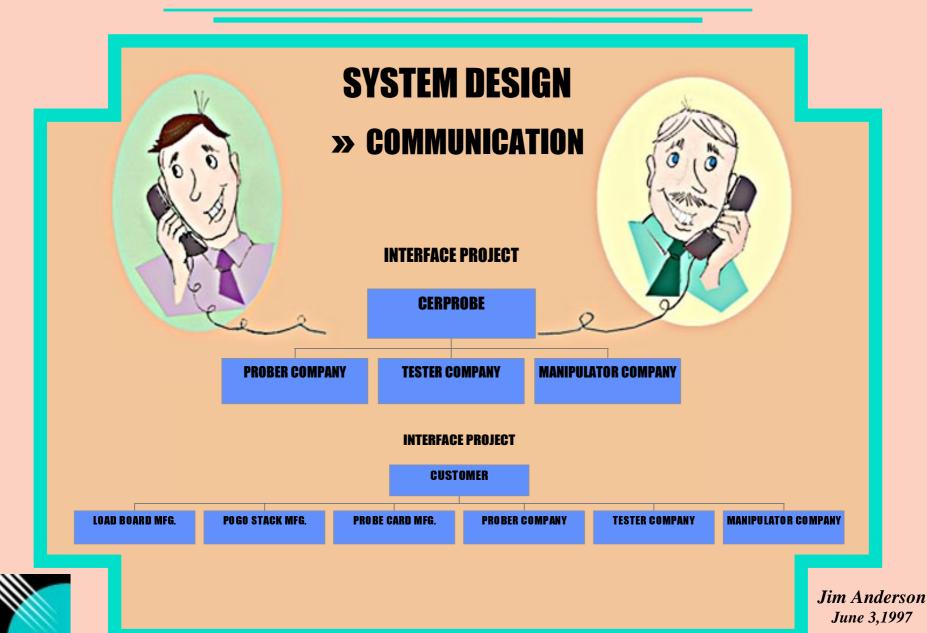
SINGLE SPECIFICATION

Pulse Rise Time Round Trip Delay System Impedance System Capacitance Bandwidth









- >> SYSTEM PERFORMANCE SPEC DRIVES DESIGN
 - **□ CONTROL IMPEDANCE**
 - **Maintain constant width lines**
 - Maintain constant distance from signal path to reference path or plane
 - Minimize vias and other discontinuities in the line
 - □ Relieve ground planes around those necessary vias
 - Provide a ground current return path of same length as signal path

>> SYSTEM PERFORMANCE SPEC DRIVES DESIGN

- **MINIMIZE CROSSTALK**
 - □ Reference signal lines to low inductance ground plane
 - Maximize the distance between lines-maintain minimum of 2.5X dielectric
 - □ Separate critical paths on to separate layers
 - □ Place well grounded guards on either side of more critical lines as shields
 - □ Separate analog and digital grounds
 - ☐ Where necessary, route signals over fully shielded lines such as semi-rigid coax



- >> SYSTEM PERFORMANCE SPEC DRIVES DESIGN
 - MINIMIZE GROUND BOUNCE
 - □ Provide low inductance power and ground planes
 - Provide sites for bypass capacitors close to the DUT
 - ☐ Tie ground lines on top and bottom surfaces to the ground plane at frequent intervals
 - □ Isolate AC signals from critical areas of the board using inductors, in those cases where both areas need to be at the same DC level.

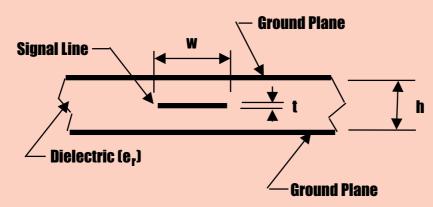
- **» START AT THE BOTTOM WORK UP**
 - □ PROBE CARD
 - **POGO STACK**
 - □ PERFORMANCE BOARD



- **» START AT THE BOTTOM WORK UP**
 - ☐ PROBE CARD
 - ☐ The DUT drives the design
 - **☐ Size of DUT**
 - Parallel testing
 - □ Direction of array
 - □ Tester site layout
 - □ Area for device mounting

SIGNAL TRANSMISSION >> START AT THE BOTTOM - WORK UP

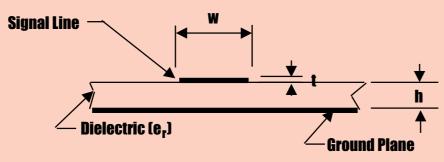
- **PROBE CARD**
 - **Stripline**
 - Efficient for frequencies up to 4-5 GHz
 - □ Can increase layer count



$$z_0 = \sqrt{\frac{60}{e_r}}$$
 In $\left(\frac{4h}{0.67\pi \,\text{w}\,(0.8 + t/\text{w})}\right)$

SIGNAL TRANSMISSION >>> START AT THE BOTTOM - WORK UP

- **PROBE CARD**
 - Microstrip
 - Efficient for frequencies up to 2-3 GHz
 - ☐ Easy to add matching resistors or other components to the signal path



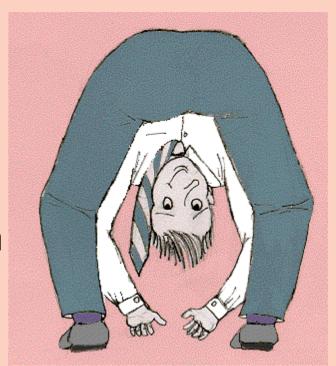
$$z_0 = \sqrt{\frac{87}{e_r + 1.41}} \quad \text{In} \quad \left(\frac{5.98h}{0.8w + t}\right)$$

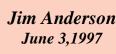


- **» START AT THE BOTTOM WORK UP**
 - □ PROBE CARD
 - **□Combination**
 - Watch out for the difference in propagation delay
 - Adjust physical line lengths to equalize electrical line lengths and minimize signal skew

- **» START AT THE BOTTOM WORK UP**
 - □ POGO STACK
 - Choosing the pogo pattern
 - ☐ Two wire array
 - □ Co-planar array
 - □ 5 wire array
 - □ Coaxial
 - ☐ Isolate signals
 - ☐ Isolate signal grounds from power grounds

- » BOTTOMS UP
 - **PERFORMANCE BOARD**
 - □ Translation
 - **Tester Pin Out Pattern**
 - **□Probe Card/Pogo Pattern**
 - Equal Line Length
 - Device Population
 - Connector City







MECHANICAL DESIGN

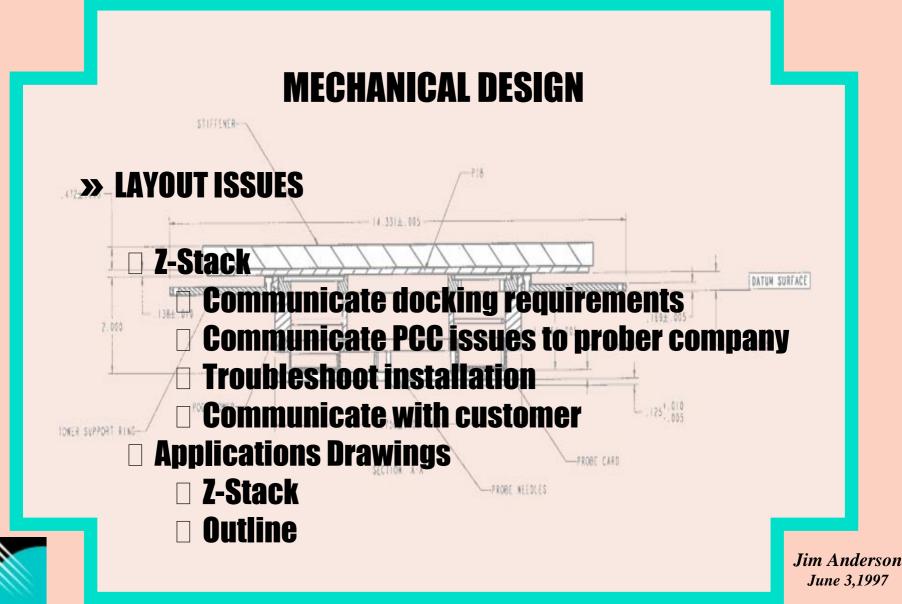
>> PCC vs. NON-PCC METHODOLOGY

- » PCC
 - □ Probe card/ carrier
 - □ Pogo stack/ adapter (or insert) ring
 - □ Load board/ stiffener
 - Docking

MECHANICAL DESIGN

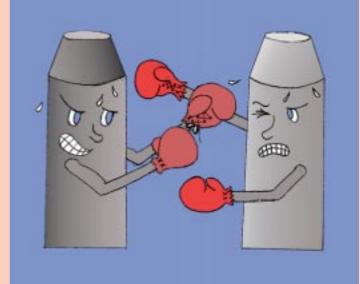
>> PCC vs. NON-PCC METHODOLOGY

- >> Non-PCC
 - □ Probe card/ stiffener
 - □ Pogo stack
 - Insert/ clamp ring assembly
 - Load board/ stiffener
 - Docking



MECHANICAL DESIGN

- » LAYOUT ISSUES
 - ☐ The pin fights
 - Why we need alignment pins
 - □ PCC
 - □ Probe card carrier to insert ring
 - Pogo stack to- same pin in insert ring
 - Load board/ stiffener to same pin in insert ring
 - **Non-PCC**
 - □ Probe Card/ stiffener to pogo stack
 - Load board to same pin in pogo stack







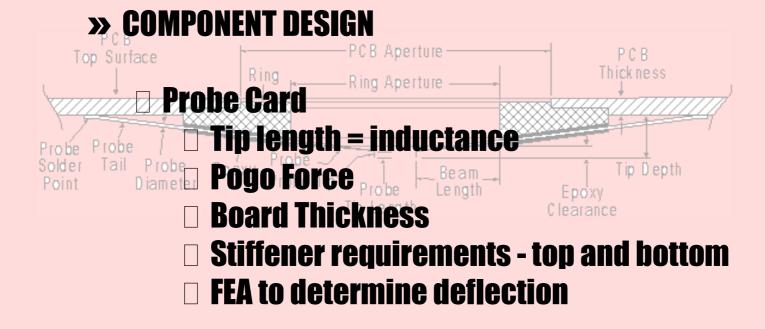
MECHANICAL DESIGN

» LAYOUT ISSUES

- Design from the bottom up
 - □ Prober top plate (ring carrier)
 - Probers optimal probing height
 - Probe tip depth (minimize)
 - Probe card thickness
 - Minimum load board height (from top plate)
 - □ Choose pogo pin



MECHANICAL DESIGN



Jim Anderson June 3,1997

MECHANICAL DESIGN

>> COMPONENT DESIGN

- Pogo Stack
 - Housing should be metal
 - Other materials driven by design of signal transmission
 - Provide pogo overdrive features
 - □ Pogo's easily removable
 - ☐ Flange mount for probers with PCC's
 - □ Cam followers for clamp mount for probers without PCC's



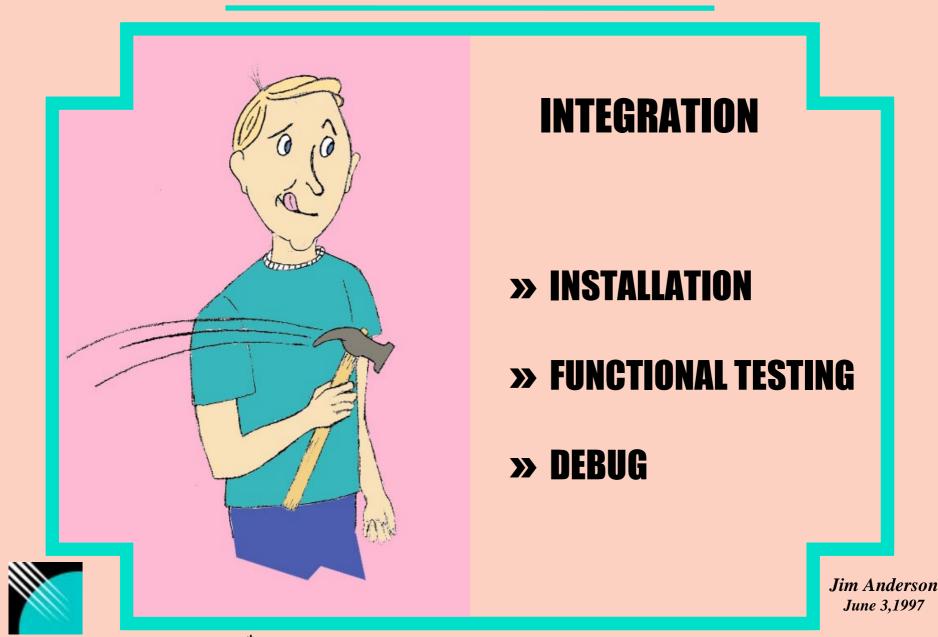
MECHANICAL DESIGN

» COMPONENT DESIGN

- □ Load Board
 - Provide stiffener
 - Mount stiffener directly to test head
 - ☐ Float load board
 - Do not bolt load board to pogo stack
 - Make sure 'z' height sufficient for devices

PROJECT MANAGEMENT

- **» ASSUME LEADERSHIP ROLE**
- >> PROJECT MANAGER/TEAM
- >> CONCURRENT DEVELOPMENT
- **» GANTT CHARTS**
- >> DESIGN REVIEWS W/CUSTOMER

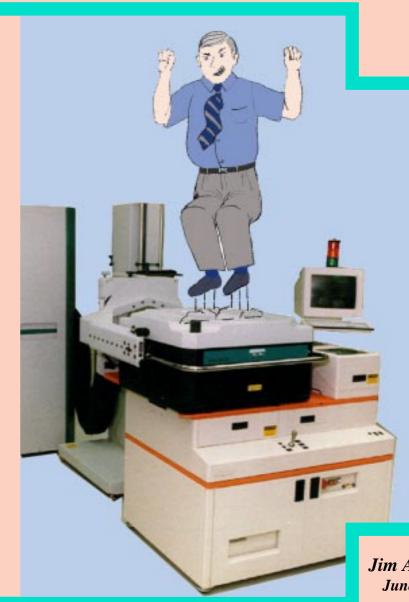


INSTALLATION

» INSTALL	
Docking	1
□ Insert / Clamp Ring	2
□ Probe Card	3
□ Pogo Stack	5
□ Load Board	8
» FIT CHECK	
□ Probe card loading	4
 Probe card to Pogo Stack 	6
 Pogo Stack to Load Board 	9
» CALIBRATE	
 Probe Card to Pogo Stack 	7
□ Pogo Stack F.A. to Docking R.A.	10
□ Docking R.A. to Test Head	11

FUNCTIONAL TESTING

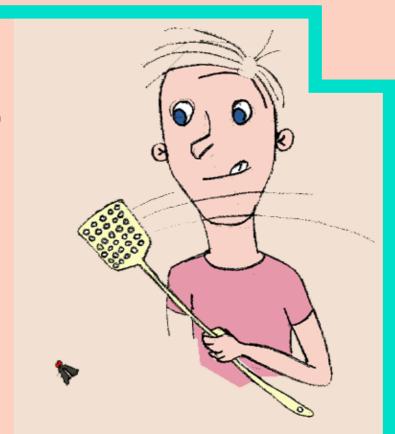
- **» SHORT OUT SIGNALS ON PROBE CARD**
- **» WRITE OPENS/SHORTS TEST** - ASSIGN CHANNELS
- >> PERFORM TEST
- >> EVERYTHING IS PERFECT **RIGHT?**



DEBUG

LEVEL 1 DEBUG: VERIFY CHANNELS AND CHECK FOR THE OBVIOUS

- >> ON PROBE CARD: OHM OUT **POGO PIN PAD/VIA TO PROBE LAND**
- >> TEFLON TAPE ON POGO PAD/VIAS



- >> OHM OUT LOAD BOARD PAD FOR TEST HEAD OUTPUT TO **PROBE LAND**
- >> TEFLON TAPE ON LOAD BOARD (BOTH SIDES?)

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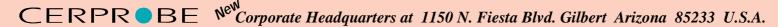




DEBUG

LEVEL 2 DEBUG: 'Z' HEIGHT ISSUES

- **» VERIFY FLAT MOUNTING SURFACE FOR POGO STACK**
- >> VERIFY HEIGHT OF POGO (TOP AND BOTTOM) FROM MOUNTING SURFACE
- >> VERIFY PROBE CARD MOUNTING SURFACE
- >> VERIFY 'Z' HEIGHT REPEATABILITY OF PROBE CARD LOAD
- **» OHM OUT POGO PIN**
- >> VERIFY 'Z' HEIGHT ON DOCKING VS. PRINTS



DEBUG

LEVEL 3 DEBUG: ITS AN 'X' 'Y' THING

- >> REMOVE PROBE CARD AND POGO STACK: ✓ ✓ FIT
- >> ALIGNMENT PINS- P.C. CARRIER -TO-CHANGER CLAMP & PROBE CARD-TO-POGO STACK?
- >> ALIGNMENT PINS: P.C. CARRIER -TO-CHANGER CLAMP & **POGO STACK-TO-INSERT RING** /RING CARRIER?



SUMMARY

- **» TAKE CONTROL**
- **» DRIVE THE SYSTEM CONCEPT AND SPECIFICATION**
- **» ESTABLISH AND MAINTAIN STRUCTURED COMMUNICATION**
- **» ONLY DO BUSINESS WITH AN INTEGRATOR**