

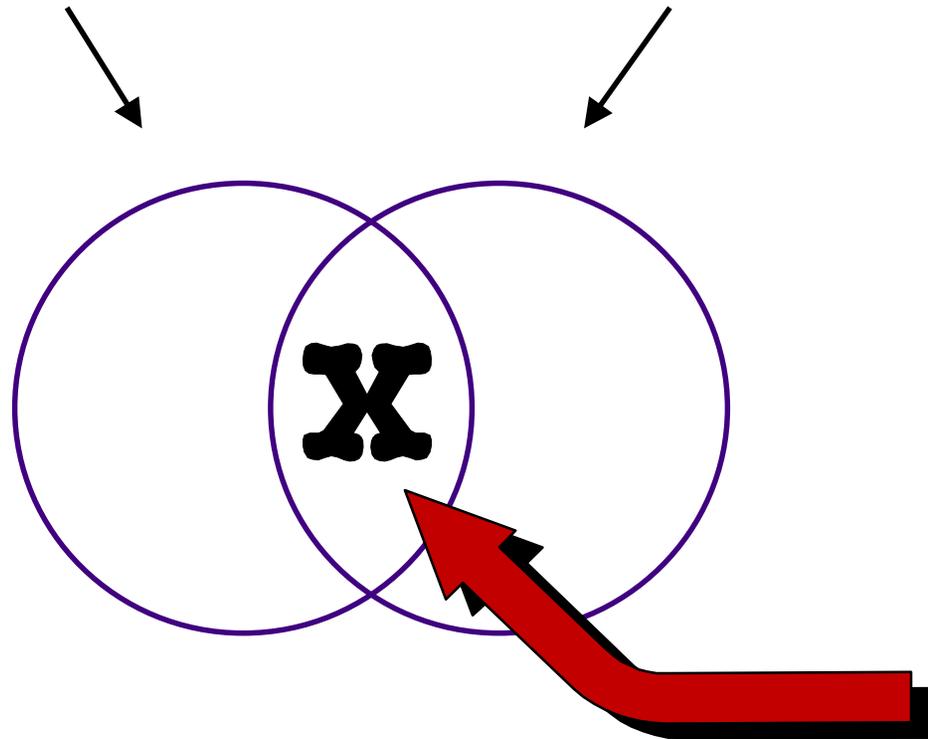
Microwave Probing

HP 84000 RFIC On-Wafer Test
Merging Two Worlds of Test



Low Volume
On-Wafer Testing

High Volume
Package Testing



**High Volume
On-wafer
Testing**

Agenda / Outline

➤ Background

- Market needs
- HP in RF and on-wafer test

➤ RF & uW Probing Issues

➤ Calibration Issues

➤ HP 84000 Wafer Probe Project Overview

➤ Results

➤ Summary

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Background:

Market / Technology drivers for on-wafer test systems for the late 1990's

► Wireless Communications RFIC's

- Cellular Telephones
- Cordless Telephones
- Direct Broadcast Satellite TV

► Implications

- High Volumes
- Low Frequency (<3GHz)
- Silicon (not just GaAs anymore)
- Higher levels of IC integration
- Commercial not Military applications

Background:

Commercial drivers for on-wafer test systems for the late 1990's

► Cost of Test

- System price
- System throughput

► Time to Market

- Ease of use
- Fast programming & correlation to bench

► Production Worthiness

- Repeatability
- Reliability , supportability
- Data Integrity
- Integration into existing data handling systems
- Integration into existing testing processes

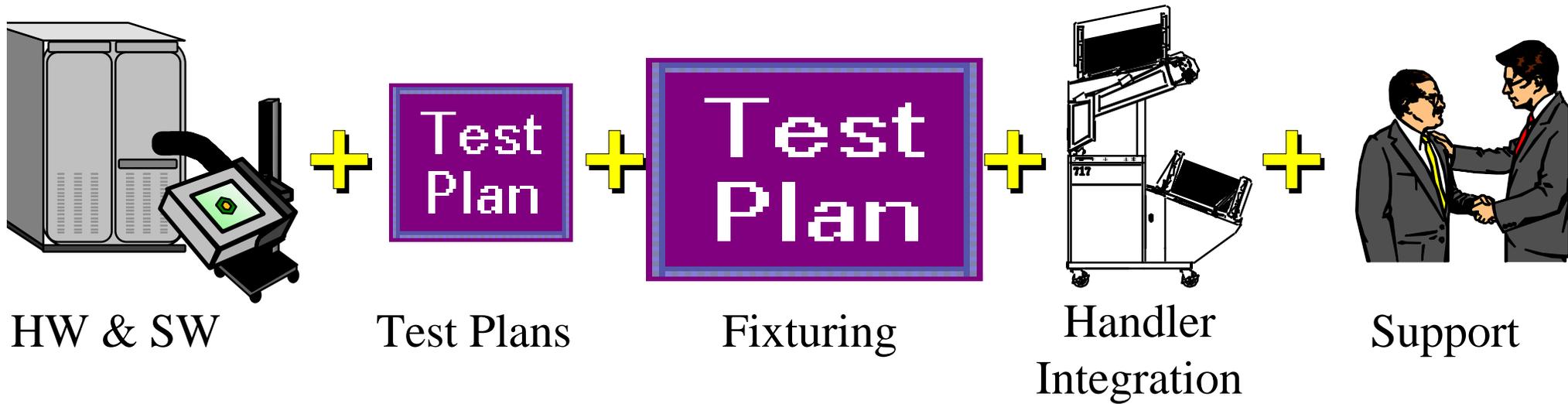
Background:

HP in RF & Microwave on-wafer testing

- ▶ >20 years of experience
- ▶ RF and microwave systems 0 to 26, 50, 65 and 110 GHz
 - Hundreds of systems installed worldwide
- ▶ HP has had many years to learn the "art" of on-wafer testing at high frequencies
 - Signal integrity
 - Calibration errors, standards, and de-embedding
 - Touchdown repeatability and accuracy
 - Test system accuracy / stability / dynamic range

Background:

HP 84000 in production RFIC testing



The Total Solution for your RFIC testing
since 1994

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RF & Microwave Probing Issues

Test: On wafer or package? Simple economics!

It is easy to evaluate the particular situation and determine if the cost of testing and removing bad die before packaging is less costly than the cost of packaging bad die.

RF & Microwave Probing Issues

IC Design for RF Testability

Item:	Reason:
Must have DC ground return pad on each side of the chip to be probed	Prevents bias oscillations
Must tie all grounds together on chip to eliminate common lead inductance	Prevents common lead inductance-induced RF degradation
Must use "standard" RF signal footprint for pads (e.g. G-S-G or G-S)	Allows common use of probes in all RF applications
Must have RF ground adjacent to RF signal pads	Good RF launch onto the chip
RF Pad spaced logically around the chip perimeter	Allows signal isolation and mechanical spacing for relatively large probes

RF and uWave Probing Issues

Probe requirements

Item:

- ▼ Controlled Impedance of Entire Path
- ▼ Probe to Probe Coupling / Shielding
- ▼ Proximity of Ground Pads on chip launch (directly from probe G-S or G-S-G layout)
- ▼ Low RF/uW probe loss to source/receive desired signals
- ▼ Proximity of Decoupling Caps & Low Series Inductance
- ▼ Size of Probes and Connectors
- ▼ Ease of Setup and Adjustment
- ▼ Ruggedness and Life
- ▼ Cost of Probe Card

Reason:

- ▼ Improves accuracy and repeatability, reduces reflections & interfering signals
- ▼ Needed to properly launch signal and maximize controlled impedance path
- ▼ Many devices require higher power >0dB at probe tip at uW frequency
- ▼ RF & Microwave devices have high Ft and will oscillate readily
- ▼ Allows more RF signals to DUT
- ▼ Cost of Test

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RF and uWave Probing Calibration

▼ Calibration and de-embedding process

- Calibrate to connectorized calibration plane with traceable standards + verification device
- Calibrate at probe tips using on wafer standards
- Calculate an error model for the delta which includes adapter, cables and probes
- Use de-embedding model for all measurements including power and noise

RF and uWave Probing Calibration

▼ Why use a two level approach to calibration at the probe tips?

- Calibration of power and noise is easily calibrated at the connectorized plane and is readily de-embedded to the probe tip
- Can use LRM calibration which doesn't require a difficult to create "open" standard at probe tip
- Changing a probe card only requires a simple on wafer LRM cal to collect error model before resuming testing
- Performance of the test system to a connectorized calibration plane is the basis of measurement integrity and performance verification of the test system

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HP 84000 Wafer Probe System (Nextbench at HP MWTD)

▼ Test system mechanical interface to prober

- Hard docking to an adapter assembly
- Allows access to probes and cards
- Easy to dock/undock for system cal and verification
- Short RF cables
- Requires special prism optics from side to allow easy docking and undocking

HP 84000 Wafer Probe Project (Nextbench at HP MWTD)

▼Photos and Drawings

- Picture of testhead docked to wafer prober
- Picture of prober docking adapter
- Picture of probe card with GGB probes (Picoprobe)
- Picture of membrane probe
- Picture of probe tips
- RF measurement de-embedding test result comparison

HP 84000 Wafer Probe Project (Nextbench at HP MWTD)

▼ Next steps on HP84000 next bench project

- Integrate industry standard wafer mapping software
- Integrate industry standard wafer prober control
- Integrate industry standard data analysis
- Integration of the above with HP84000 operator and developer UI, calibration and PVST (Performance Verification and Self Test)
- System performance specifications finalized

End result is complete production worthy, high volume, on wafer test system

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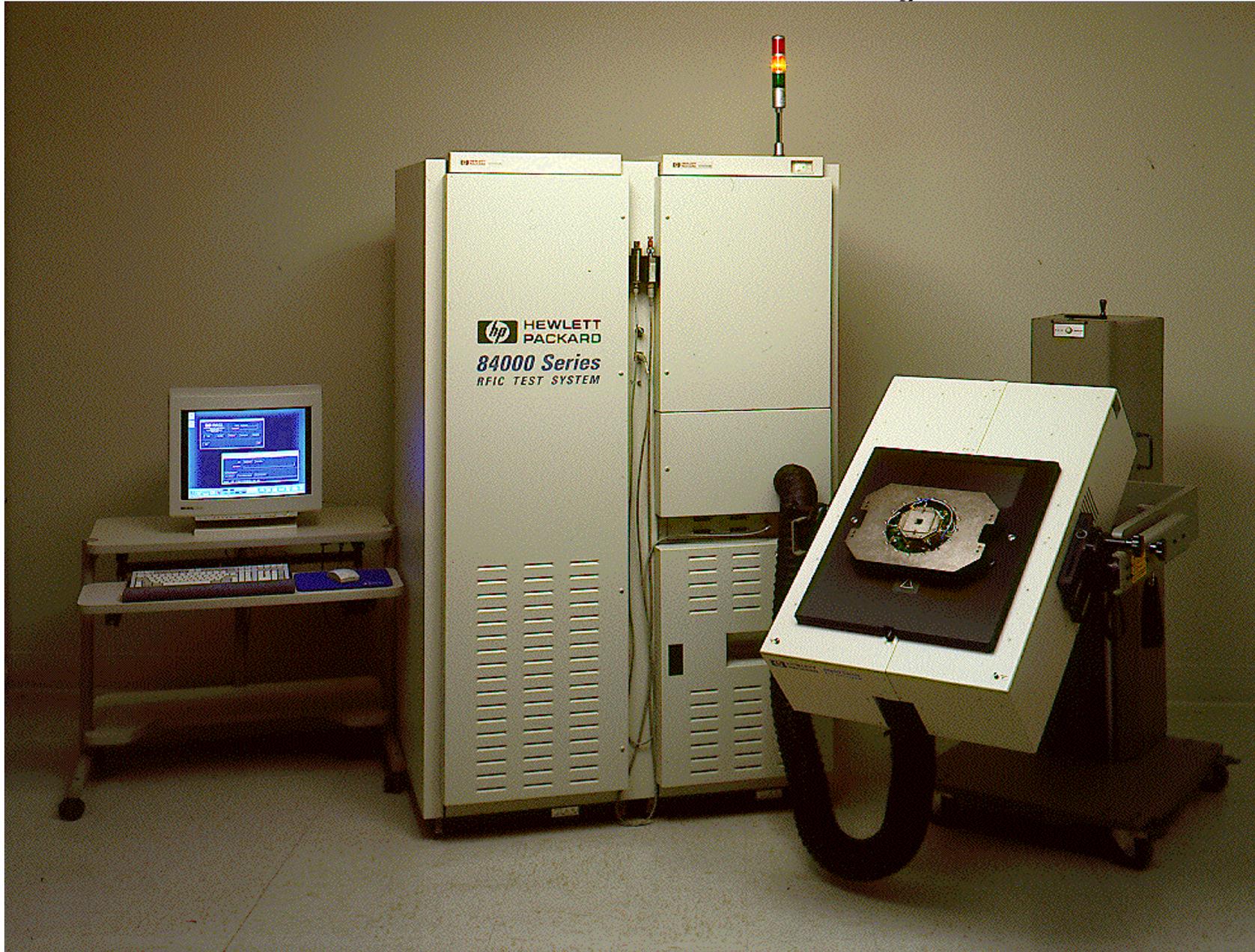
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HP 84000 Series RFIC Test System



Summary

- ▼RF and Microwave testing on wafer is needed
- ▼HP has long history of RF/uW on wafer
- ▼RF and Microwave on wafer test issues must be considered
- ▼RF HP84000 Wafer Probe Project Overview