An Integrated System for Controlling the Unit Probe Process in a Parallel Test Environment

- Objective
- Approach & Goals
- Environment
- Process Flow
- Functional Descriptions
- Summary

Objective:

- Realize maximum attainable probe yields while minimizing rework and equipment downtime.
  - Prevent the occurrence of process variations.
  - Provide means to detect and correct out-of-control processes as quickly as possible.

Approach used to Implement Probe Process Control

- Integration
- Automation
- Use characteristics of the probe process to gaugearacteristics.

Goals of Process Control

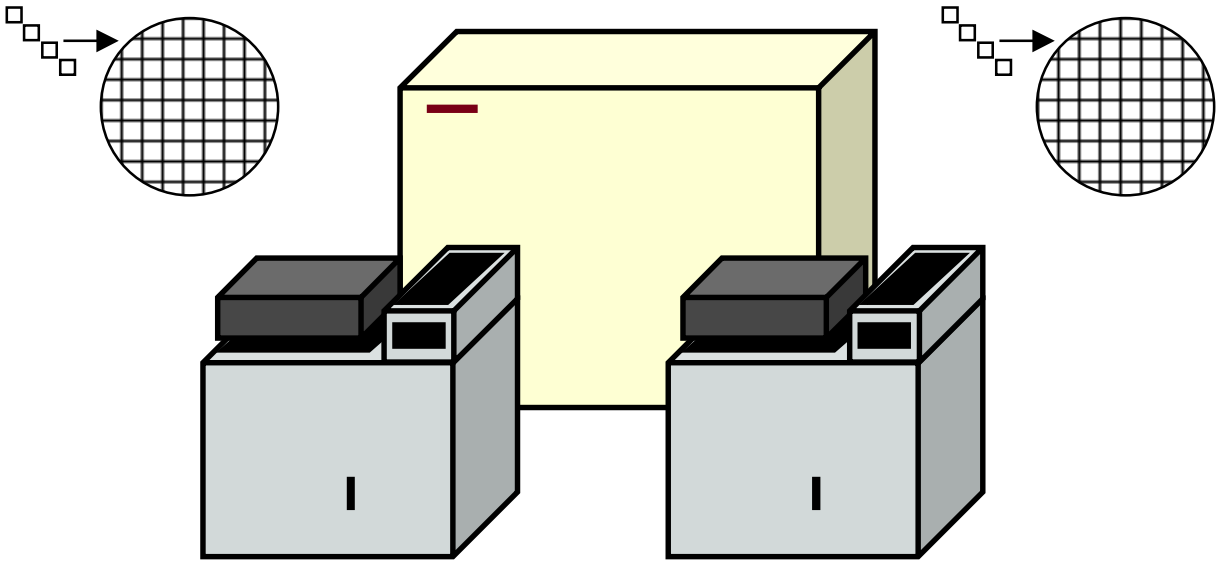
- Ensure integrity of hardware setup.
- Take advantage of parallel probing to measure the probe process.
- Detect process problems as they occur.
- Provide tools to debug problems.
- Ensure data integrity before lot is completed.
- Reduce dependence on correlation wafers.

Probe Environment

- Equipment set:
  - Advantest T3324 and T3326A testers (256 pins per head, 2 heads per tester).
  - TSK APM-90A probers (full CASU capability).
  - Cantilever epoxy-ring probe cards.
- Organizational purpose:
  - Volume manufacturing.
- Type of devices tested:
  - CMOS Microcontrollers with RAM, ROM, EEPROM, A/D with 28-100 pins.

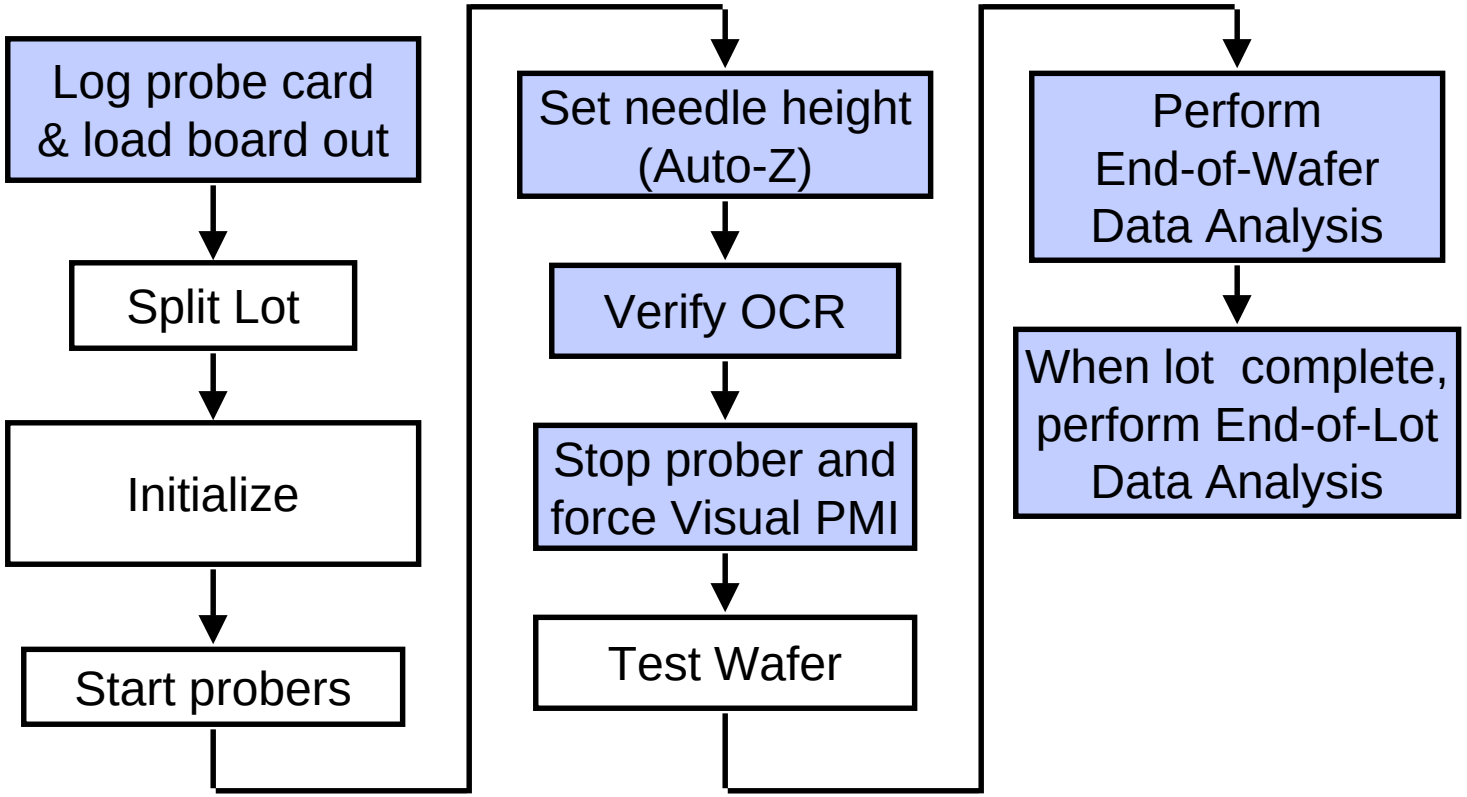
Typical Tester/Prober Configuration

A wafer lot is split into two groups, half the wafers are probed on head 1, the other half on head 2. Wafers are probed in simultaneous mode.



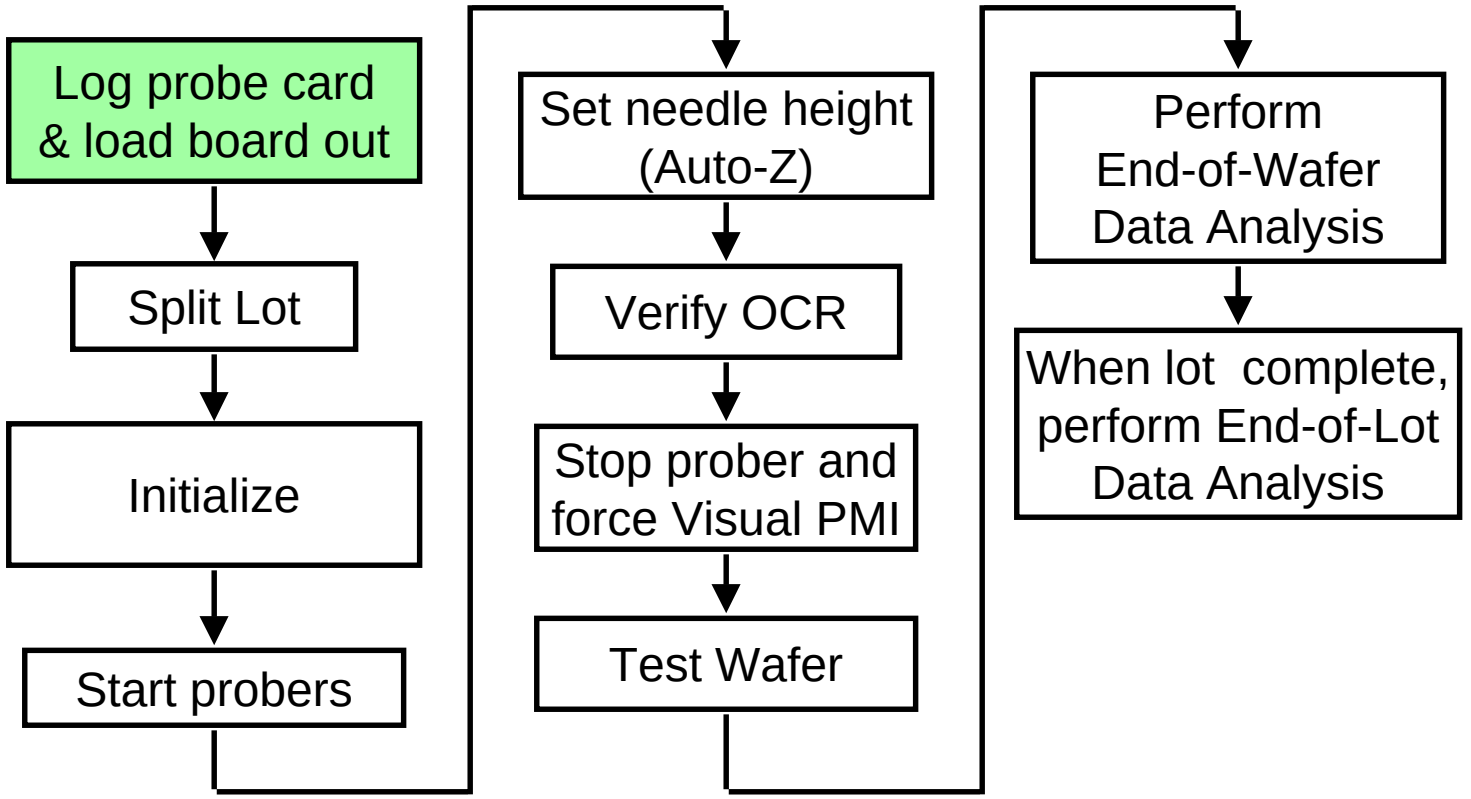
Head 1 Head 2

Probe Process Flow



Shaded boxes represent control points which will be discussed in further detail

Probe Process Flow



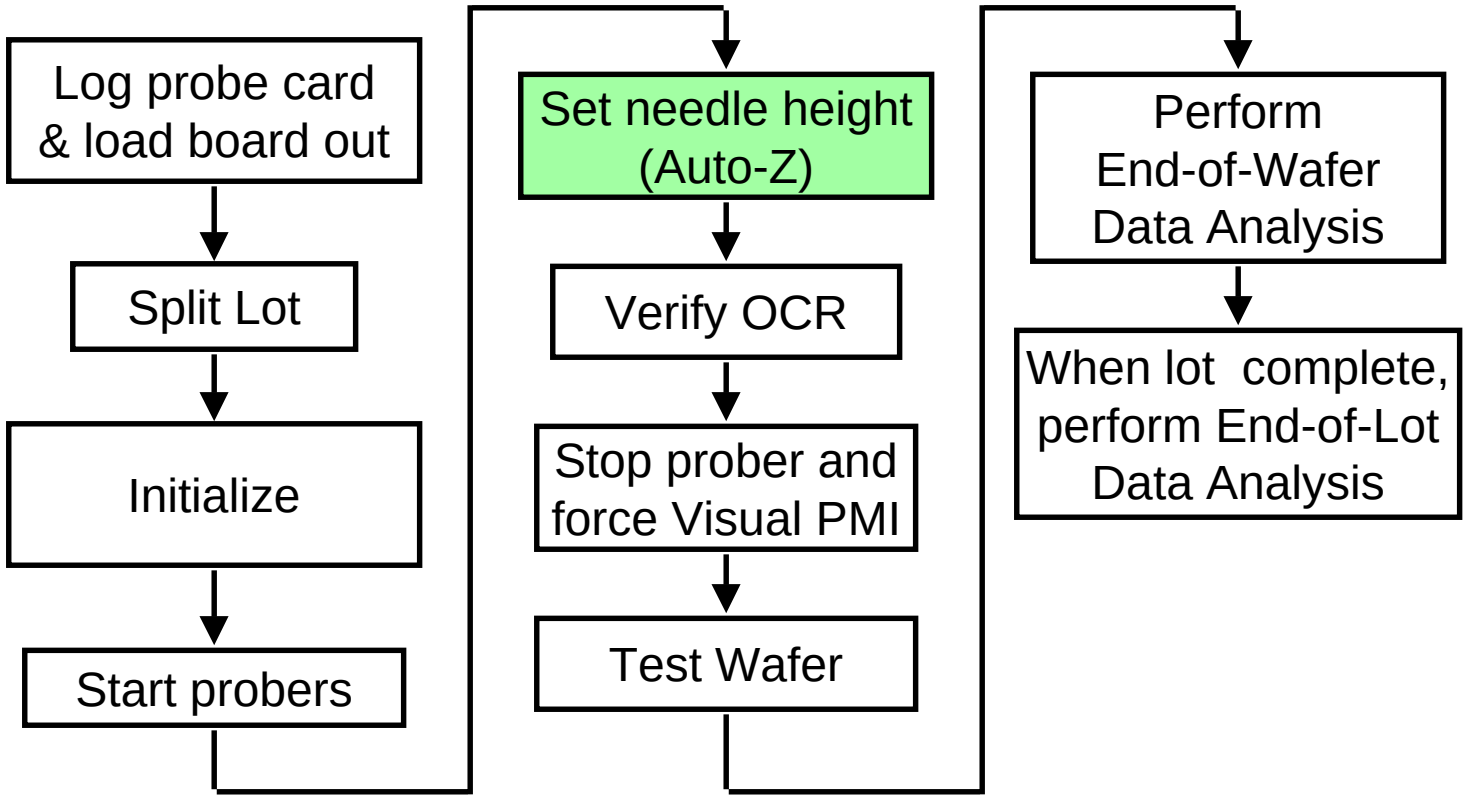
Probe Card and Load Board Control

- Correct load board and probe card must be ready for use before probing can start.

  Probecard Tracking System program:

  - Ensures correct hardware is used for device to be tested.
  - Enforces probe card repair cycle which ensures only good probe cards (those in a “ready” state) are available for use.
  - Uses bar codes to log hardware in and out.
  - Collects usage data including probe card touchdown count.

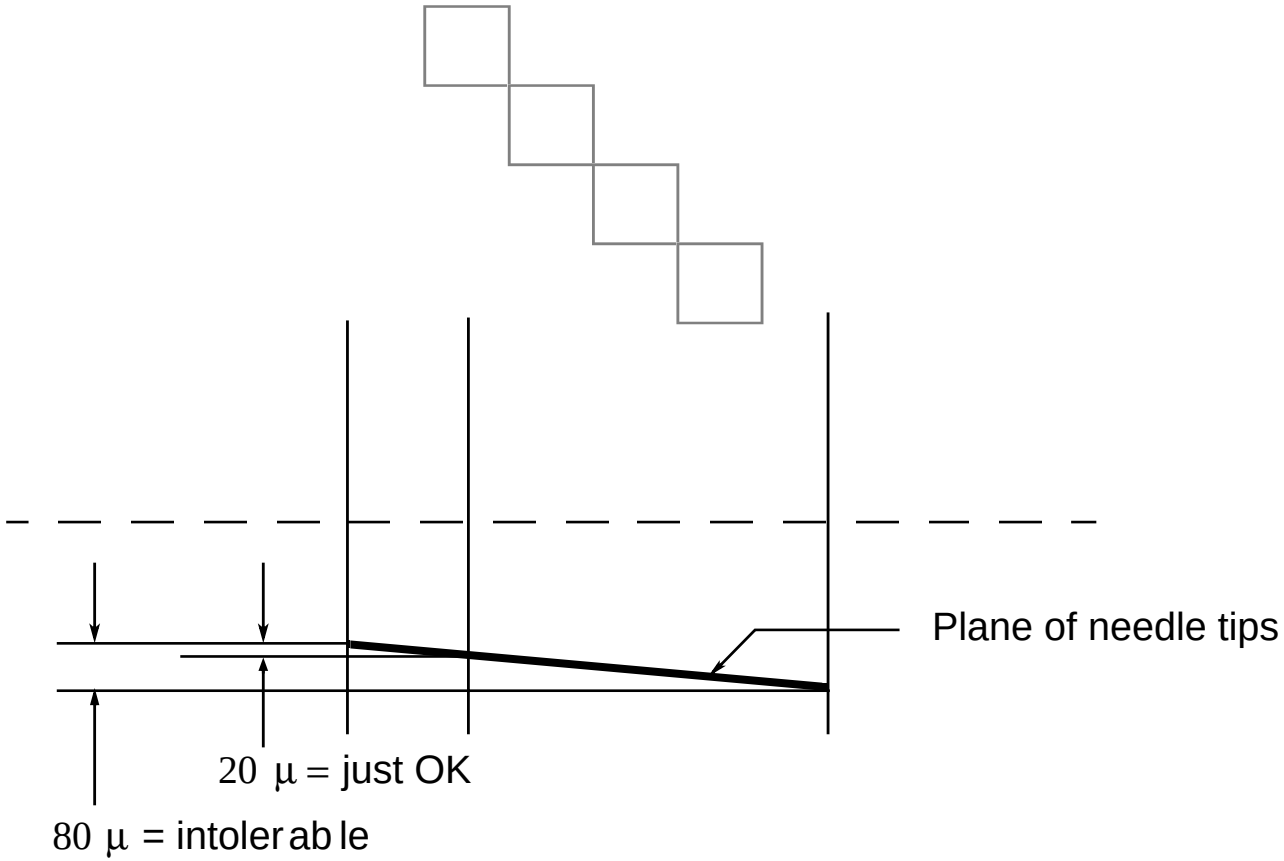
Probe Process Flow



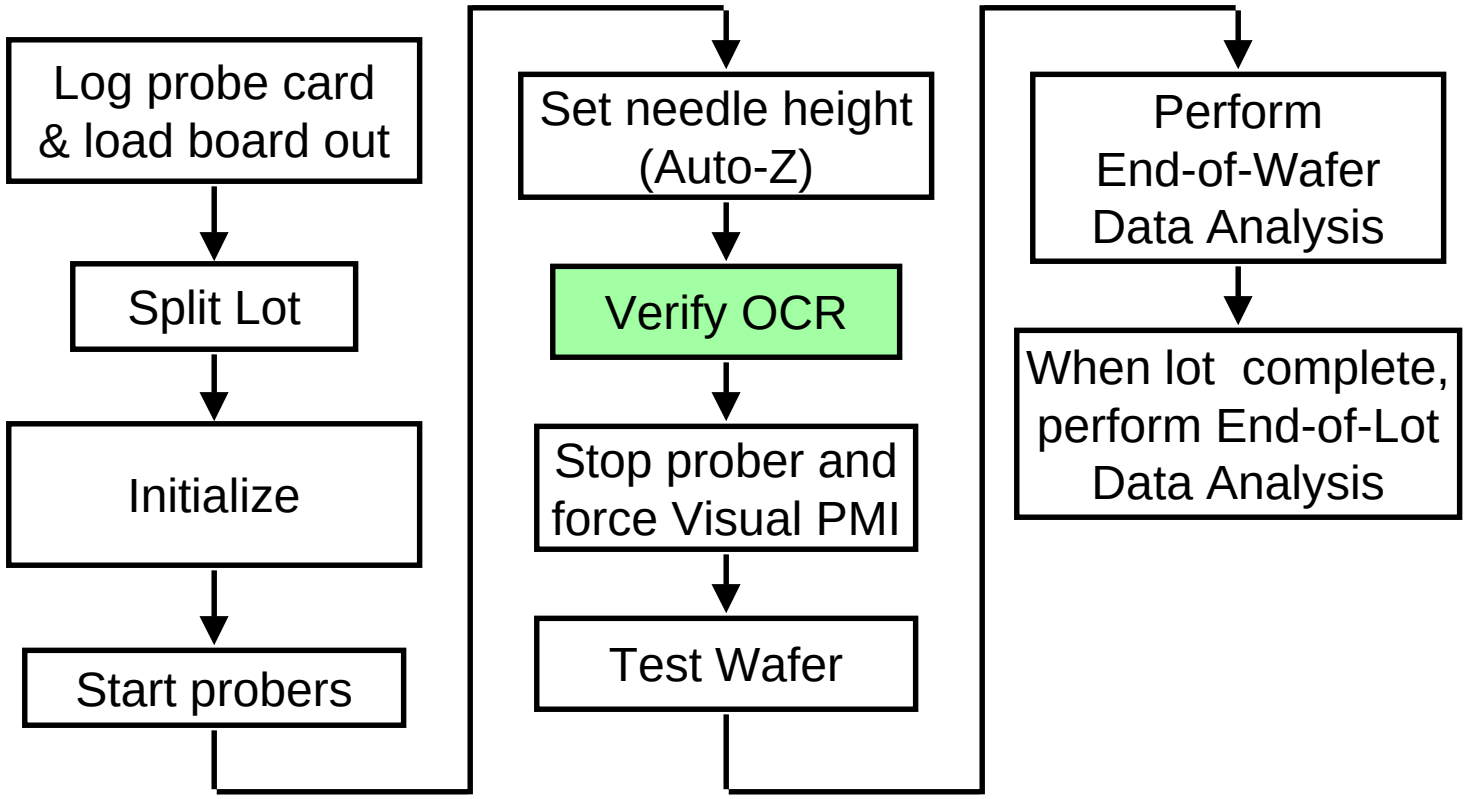
Automated needle height setting (Auto-Z)

- Probe Card needle height is set by an automated process that verifies probe card contact and planarity.
  - All signal pins for all DUTs must make contact for routine to pass.
  - All signal pins verified to be within 30 micron planarity window.
  - Routine is independent of test program.
  - Debug tools built into routine.

Diagram showing magni¼ed planar ity sensitivity for diagonal 4-dut probe arr ay



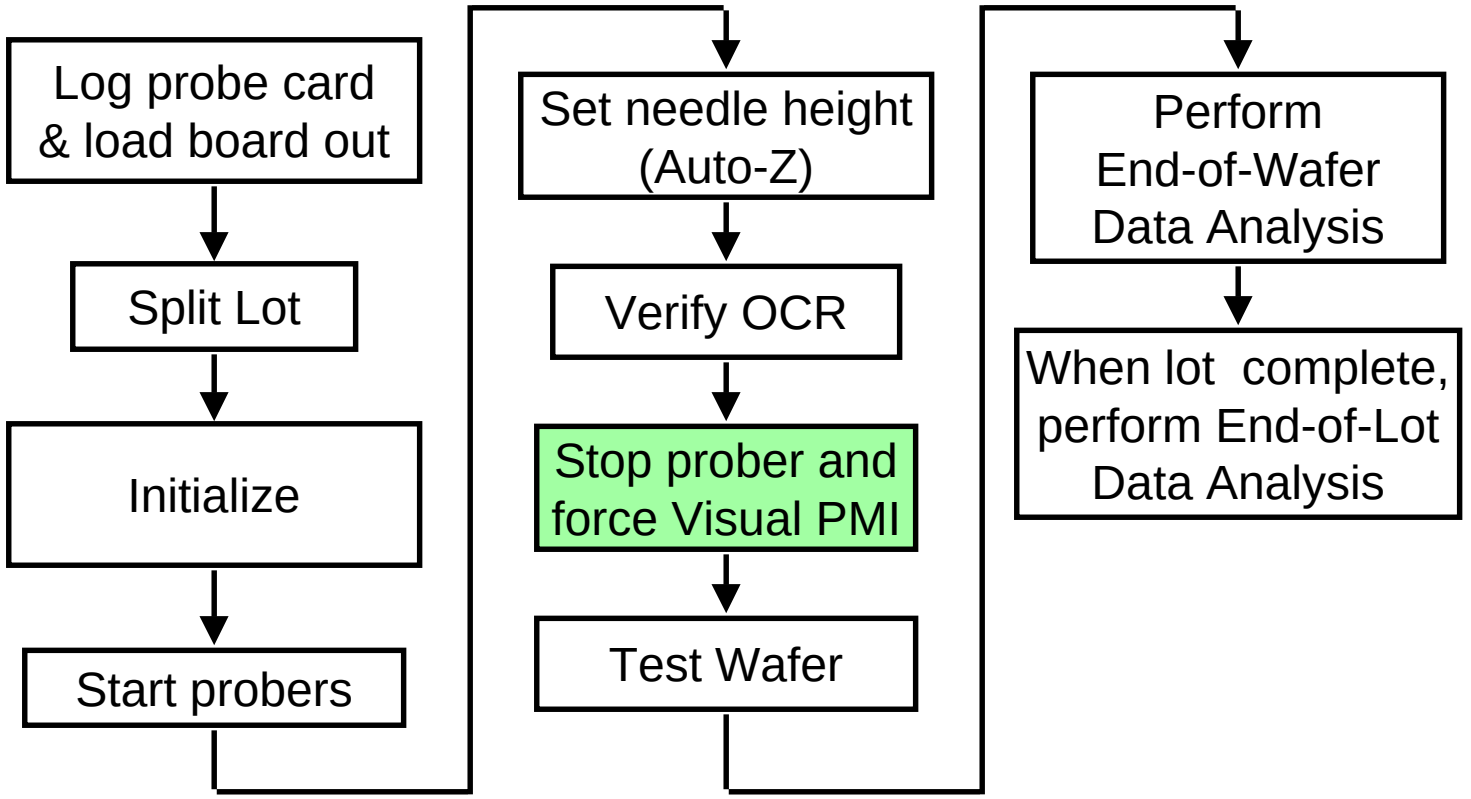
Probe Process Flow



OCR verification

- Ensures correct lot and wafer numbers are reflected in wafer data.
- Ensures correct result map is used at off-line ink.

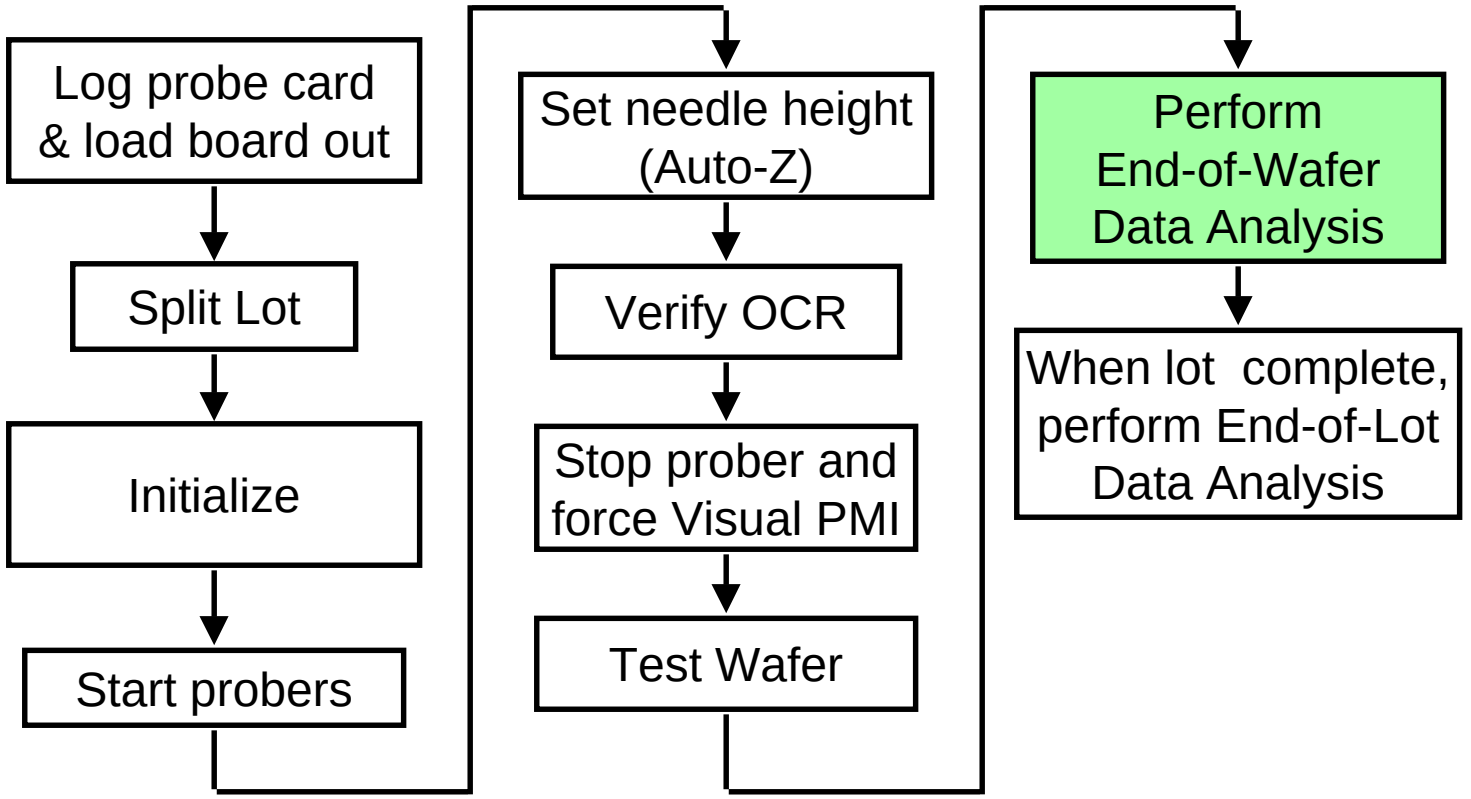
Probe Process Flow



Probe Mark Inspection

- Prober automatically halted on first wafer of each lot on each head for Probe Mark Inspection.
  - Automated Probe Mark Inspection feature doesn't function reliably.
  - Prober camera used to perform operator visual Probe Mark Inspection.
  - Ensures good probe marks and prevents cracked glass.

Probe Process Flow

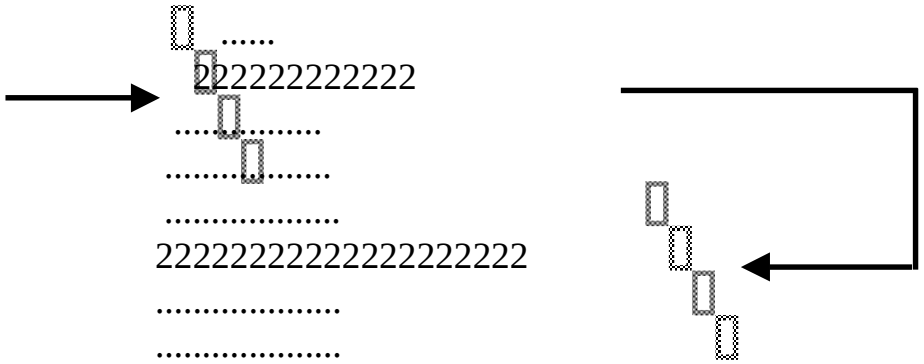


End-of-Wafer Data Analysis

- Wafer map automatically checked for error conditions:
  - Site-dependent fails.
  - Wafer yield below minimum yield specification.
  - Excessive opens failures have occurred.
- If an error condition is detected:
  - Prober stops and alarms, error message is displayed on the tester monitor.
  - Operator refers to STOP (System Troubleshooting Operation Plan) specification to address problem before more wafers are affected.

End-of-Wafer Data Analysis

Map of wafer probed using a 4-site diagonal probe array with an obvious “site-dependent fail” pattern.



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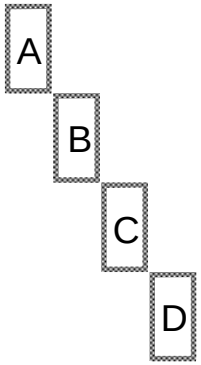


Probe site B is failing at a higher rate than the others.

(. represents good die)

End-of-Wafer Data Analysis

- Site-dependent fail algorithm
  - Sensitivity is set by number of die per wafer (DPW):

    $$S = (J \times DPW) / (K + DPW)$$

    J and K are constants which optimize algorithm behavior.
  - Sensitivity S represents allowable die delta between sites.
  - Percentage yield calculated for each site.
  - If a given site had yielded as well as the best-yielding site, would the number of die gained be > S?
  - If so, site-dependent fails have occurred.

End-of-Wafer Data Analysis

Wafer map which has less obvious pattern of site-dependent fails.

.44.K.
.....2...
6.32..7.FG.8...2
.....336.8.....3
...F..2...44....F..
....F.....G6.....6.
5..BBB.....B.....66
.83F.7.8...F...63..8
34.....8..6..2....88
.A.....6.F....F.
..4...F...F.2.C...88
7...7F..3F7.3.73.373
6..6..F...JB...F.A
FF.F.....FK.....
.....F.F..
33337F

End-of-Wafer Data Analysis

Assume sensitivity S is 15 die and note that Site B yielded the highest: 79.4%

If Site A yielded 79.4%, how many more die would have passed?
(.794 - .651) x 63 = 9 < 15, => no site-dependent fails on site A

For Site C, 10 more die would have passed => no site-dependent on Site C

For Site D, 18 more die would have passed => site-dependent fails exist on Site D

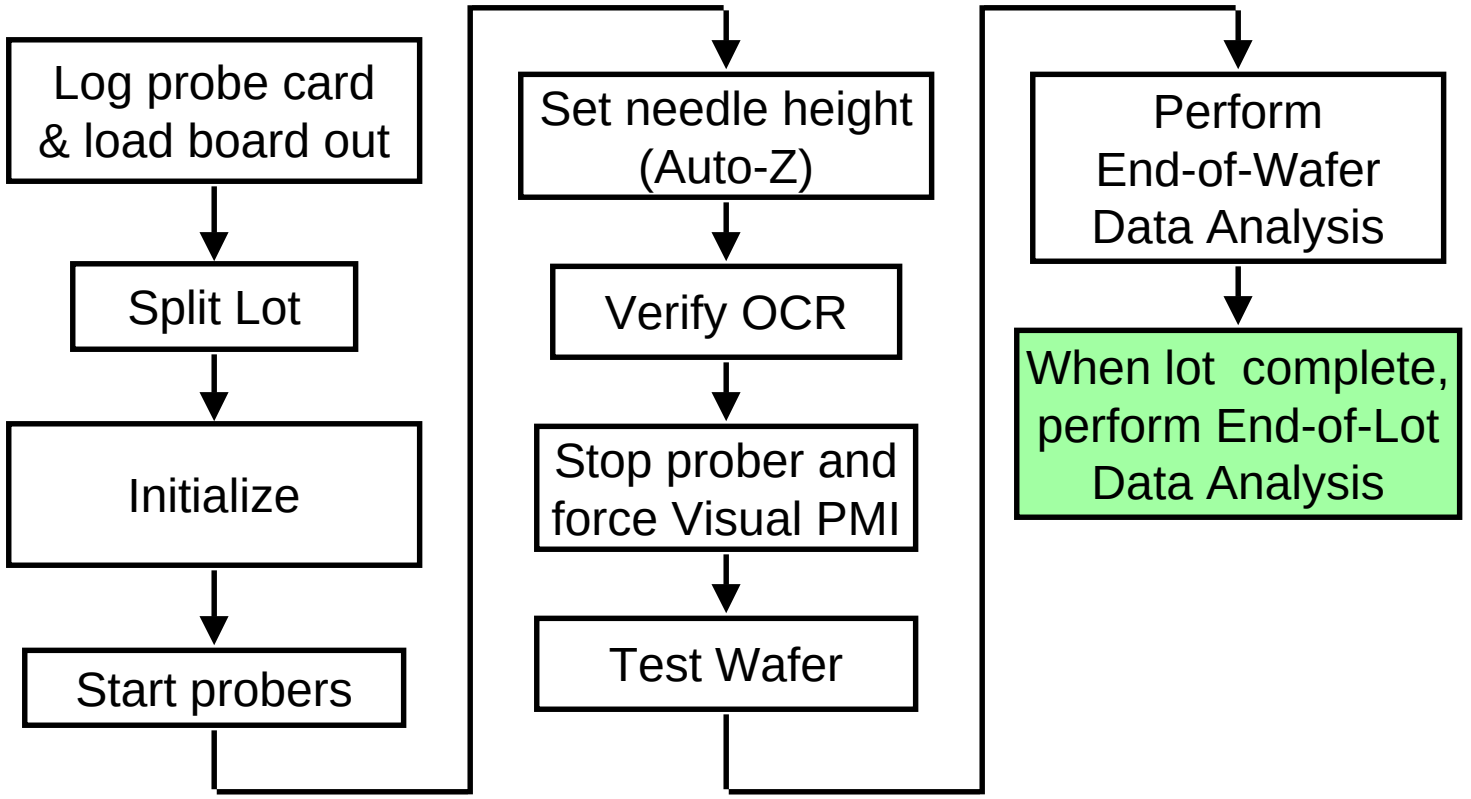
End-of-Wafer Data Analysis

- If wafer falls below minimum yield, it is scrapped
  - minimum yield failures are examined to ensure that results are valid.
- If an excessive number of opens occurs, wafer is examined to verify failures are real.
- If any of the three end-of-wafer error conditions occur:
  - prober is halted
  - operator refers to STOP specification to address problem

End-of-Wafer Data Analysis

- Other functions performed at end-of-wafer
  - Wafer map is written to server
  - Summary data file updated
  - Probe card touchdown count incremented
  - Probe process data written to server
    - Includes probe process information:
      Lot number, device number, tester program, prober device file, probe card, load board, tester test head, by-site yield, start and stop times, etc
    - Used to provide probe process measurements such as equipment utilization and reprobe rate.

Probe Process Flow



End-of-Lot Data Analysis

- List of wafers which had error conditions (site-dependent fails, minimum yield, opens) is displayed.
  - Operator reviews data to determine if reprobes are necessary.
  - All reprobes are completed before lot is closed out.

End-of-Lot Data Analysis

- Lot results reporting routine:
  - Head-to-head T-test
    - Compares each fail bin's distribution using a T-test to determine if the two "sublots" (wafers probed on head 1 versus wafers probed on head 2) are statistically from the same population.
    - If there is a difference detected, a table is displayed showing the distribution for that bin by wafer by head.
    - Operator refers to STOP for instructions to resolve problem.
    - Problems resolved before lot report is distributed.

End-of-Lot Data Analysis

Lot number: V1234567
Failed head-to-head t-test for SHRTS: t = 11.793. (24 wafers)

Head 1		Head 2	
Wafer #	# die	Wafer #	# die
1	69	13	4
2	41	14	6
3	70	15	9
4	62	16	3
5	50	17	1
6	37	18	0
7	38	19	8
8	46	20	5
9	48	21	7
10	41	22	2
11	33	23	1
12	36	24	8
Average:	47.58		4.50
Std dev:	12.30		2.99

End-of-Lot Data Analysis

- Lot results reporting routine:
  - A composite wafer map is generated.
  - Summary report is e-mailed to cognizant device engineer.

Advantages Gained

What operational improvements have been realized?

Advantages Gained

- Probe Card/Load Board Tracking System:
  - Ensures that correct hardware is used.
  - Ensures probe card will be fit for use in production.
  - Compiles use and repair history for probe cards and load boards.

Advantages Gained

- Auto-Z
  - Identifies contact problems before they affect production probing.
  - Ensures needle contact height is set correctly.

- “Forced” Probe Mark Inspection
  - Ensures needle placement and scrub are optimum.
  - Cracked glass incidents substantially reduced.

Advantages Gained

- Site-Dependent Fail Monitor
  - Detects setup and equipment problems as they occur.
  - Doesn't rely on device or fabrication process-specific characteristics (yield history) to detect problems.
  - Reprobe rate reduced from ~15% before implementation to 2-3%

Advantages Gained

- Head-to-head T-test
  - Checks that two groups of wafers from the same wafer lot yield similarly.
  - Has been successful in identifying test system problems.

Advantages Gained

Number of these incidents drastically reduced:

"Honey, its work calling again.
There's another low yielding lot, and they think it's a test problem!!"

Summary

Implementing this integrated probe process control system has resulted in several benefits:

- Setup time is reduced
- Yields are increased
- Rework is reduced
- Correlation wafers not needed for setup
- Accurate yield data is generated