

Experience with Multi-Die-Probecards in Production Use

(1) Introduction

(4) PC-Performance control

(2) Incoming inspection of probecard

(5) First results of evaluation new PC-technology

(3) Probecardmanagement

(6) Question for the future

SIEMENS

Microelectronics Center GmbH & Co. OHG

HL DD PF

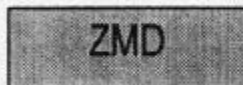
Semiconductor Fabs



Employees 2000
Investment 1,8 bill US\$



Employees 1400 (future)
Investment 1,9 bill US\$



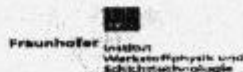
Employees 400 (1989 - 3200)
Investment 70 mill US\$

High Standard of education



TECHNISCHE
UNIVERSITÄT
DRESDEN

26000 Students



Fraunhofer ILT
Institut für Laserphysik und
Schichttechnologie

High Tech companies

Multimedia Software
GmbH Dresden



Wacker Siltronic

Applied Materials



Dresden - a rising location of microelectronics

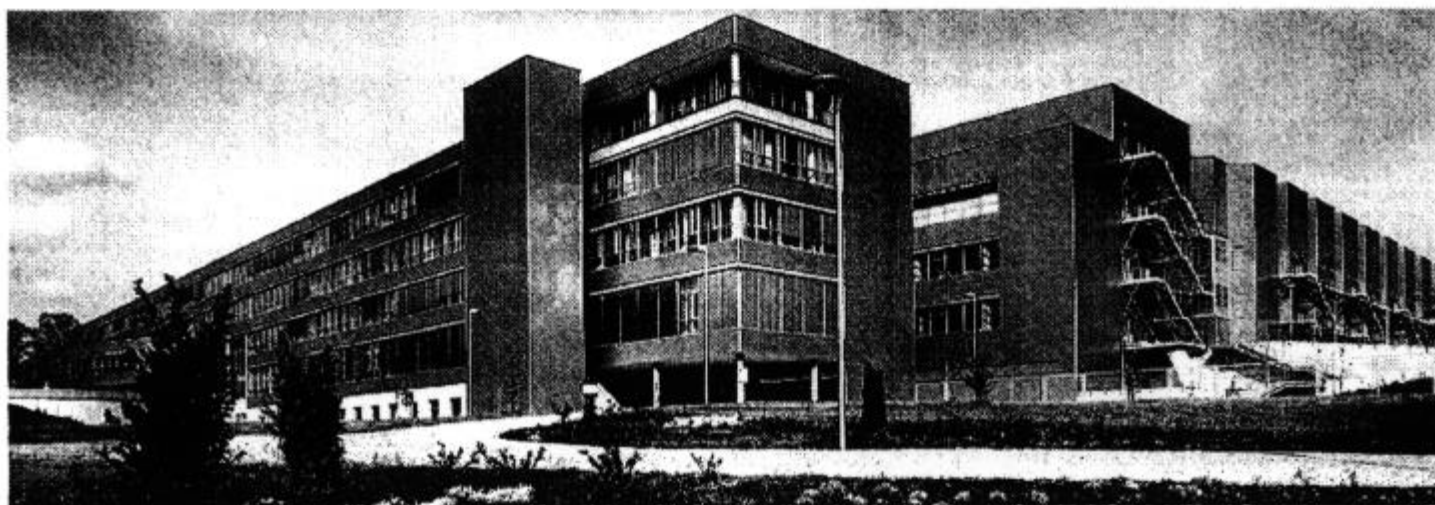
SEE ME AT
top

History

Project decision	23.12.93
Laying the foundation stone	06.06.94
Ready for Equipment	02.05.95
Startup	10.11.95
Start of qualification	01.03.96
16M DRAM shipment qualification	01.09.96
3 million chip delivered	30.10.96

Datas and Facts

Quarter micron technology	
Cleanroom area	2x5400 m ²
Cleanroom class	1
WSPW	≥ 7500
Throughput time	
Golden Wafer	
300mm line	



Cleanroom class:

1000

Testfloor size:

2268 m², length 103 m, width 25 m

Equipment:

Memory-Tester

Japanese Vendors

Logic-Tester

US Vendors

Parametric-Tester

US Vendor

Prober

Japanese Vendor

Laser-Cutter

US Vendor

Products:

16M DRAM, 16M SDRAM, 64M DRAM, Logic

Probecard supplier:

Japanese Vendors

PC number under production:

90

Measurement temperature:

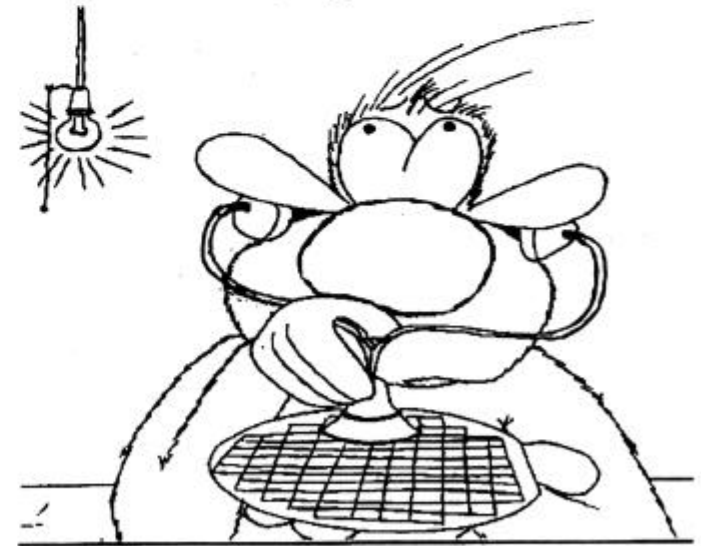
87°C

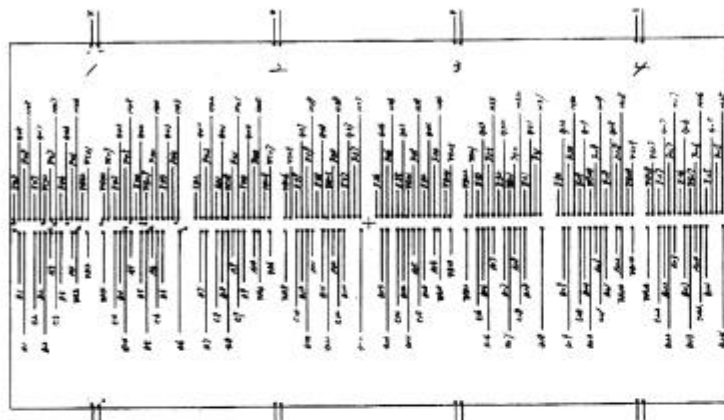
Wafermapping

Paperless production

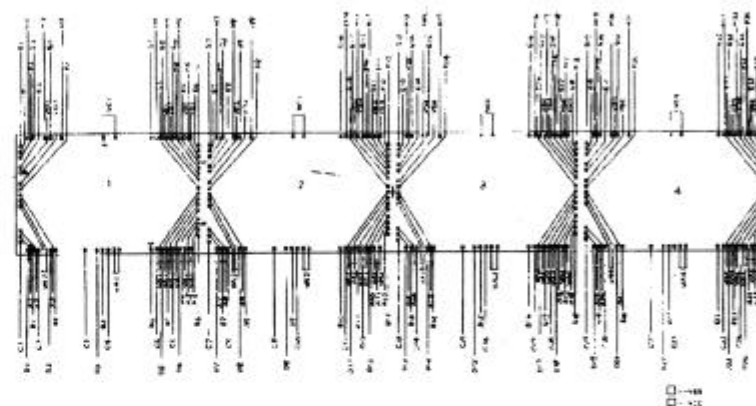
Employees:

60

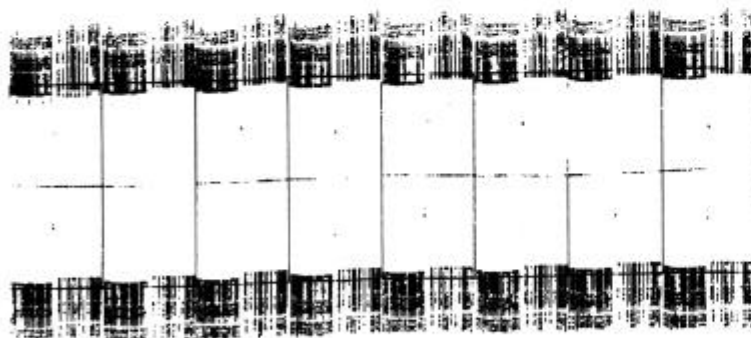




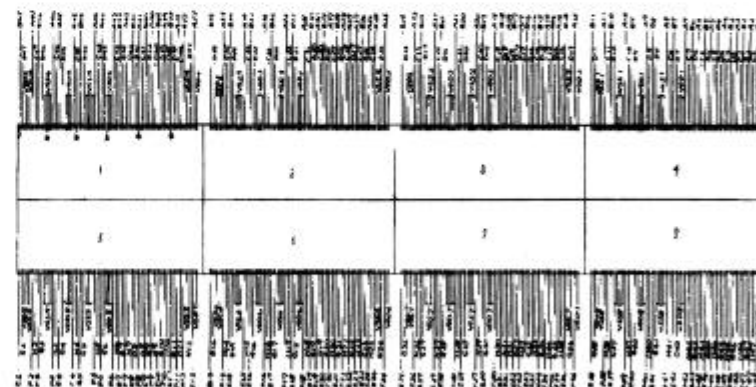
16M DRAM 1x8 DUT



4MCD DRAM 1x8 DUT



16M DRAM 2x8 DUT



16M SDRAM 2x4 DUT

Physical parameters

sagness = f (force, temperature) 15...20µm
 manufacturer tolerances
 needle planarity 20µm
 needle position 15µm
 needle-z-movement=f (temperature) 5...15µm

parallelism headplate/chuck 10µm
 manufacturer tolerances
 chuck-position-accuracy 5µm
 chuck-surface-movement=f (temperature) 20µm
 chuck-z-movement=f (force) 15µm
 chuck-y-movement=f (force) 10µm

thickness 5...30µm
 sagness 20µm
 twisting 10µm



High
 measurement
 quality is
 a result of
 perfect
 teamwork all
 components



Hardware

stiffner
 performance board
 ceramic carrier
 epoxy
 needle

headplate
 chuck

wafer

Probecard

Prober

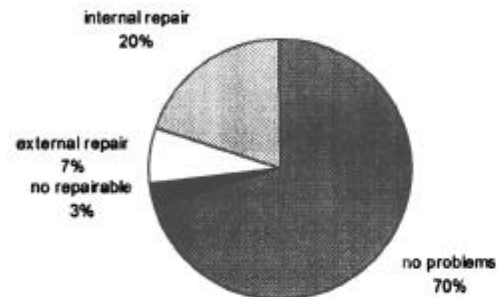
Wafer

SIEMENS HL DD PF		Date:																																																																																								
Probecard-Inputcheck																																																																																										
probecard-ID	probecard-no																																																																																									
manufacturer																																																																																										
device	DUT																																																																																									
Optical Check probe tips ☐ solder pads ☐ added facilities ☐ Precision Point Check <table border="1" style="width: 100%; border-collapse: collapse; font-size: 0.8em;"> <thead> <tr> <th></th> <th>max</th> <th>min</th> <th>mean</th> <th></th> </tr> </thead> <tbody> <tr><td>x-position-err</td><td> </td><td> </td><td> </td><td>µm</td></tr> <tr><td>y-position-err</td><td> </td><td> </td><td> </td><td>µm</td></tr> <tr><td>planarity</td><td> </td><td> </td><td> </td><td>µm</td></tr> <tr><td>alignment</td><td> </td><td> </td><td> </td><td>µm</td></tr> <tr><td>leakage</td><td> </td><td> </td><td> </td><td>nA</td></tr> <tr><td>scrub length</td><td> </td><td> </td><td> </td><td>µm</td></tr> <tr><td>scrub diameter</td><td> </td><td> </td><td> </td><td>µm</td></tr> <tr><td>scrub angle</td><td> </td><td> </td><td> </td><td>°</td></tr> <tr><td>contact resistance</td><td> </td><td> </td><td> </td><td>Ω</td></tr> <tr><td>probe force</td><td> </td><td> </td><td> </td><td></td></tr> <tr><td>capacitors</td><td> </td><td> </td><td> </td><td></td></tr> </tbody> </table> Tester Check contact loop ☐ difference first/last contact < 25µm ☐ probe mark inspection ☐ hardcode ☐ reference measurement <table border="1" style="width: 100%; border-collapse: collapse; font-size: 0.8em;"> <thead> <tr> <th></th> <th>tester</th> <th>board</th> <th>probecard</th> <th>lot #wafer</th> <th>yield-compare</th> <th>% YB</th> </tr> </thead> <tbody> <tr><td></td><td> </td><td> </td><td> </td><td> </td><td> </td><td></td></tr> <tr><td></td><td> </td><td> </td><td> </td><td> </td><td> </td><td></td></tr> <tr><td></td><td> </td><td> </td><td> </td><td> </td><td> </td><td></td></tr> </tbody> </table>				max	min	mean		x-position-err				µm	y-position-err				µm	planarity				µm	alignment				µm	leakage				nA	scrub length				µm	scrub diameter				µm	scrub angle				°	contact resistance				Ω	probe force					capacitors						tester	board	probecard	lot #wafer	yield-compare	% YB																					
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<table style="width: 100%; border: none;"> <tr> <td style="width: 15%;">rework</td> <td style="width: 15%;">YES ☐</td> <td style="width: 15%;">NO ☐</td> </tr> <tr> <td>return</td> <td>YES ☐</td> <td>NO ☐</td> </tr> <tr> <td>release</td> <td>YES ☐</td> <td>NO ☐</td> </tr> </table>			rework	YES ☐	NO ☐	return	YES ☐	NO ☐	release	YES ☐	NO ☐																																																																															
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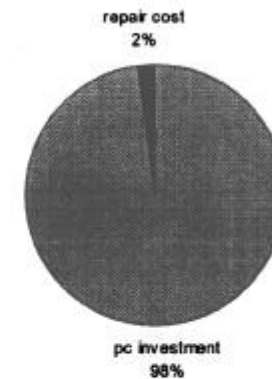
SIMEC probecard quality

Lifetime	500.000TD/year
Card sagness	max. 15µm
Differential delay	< 0,1ns
Tip shape	flat with rounded edges
Tip diameter	< 40µm
Planarization	<± 25µm
X/Y-Position	< 20µm
Scrub length	15-20µm
Contact resistance	< 10Ω
Isolation resistance	> 200MΩ
Needle-Z-movement	< 15µm (25°C/97°C)

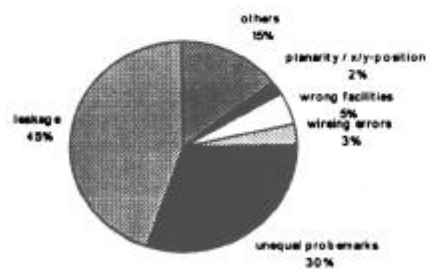
Repair during lifetime



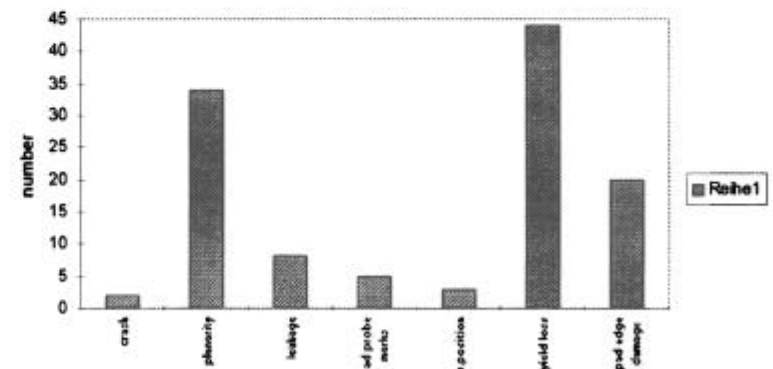
Repair cost

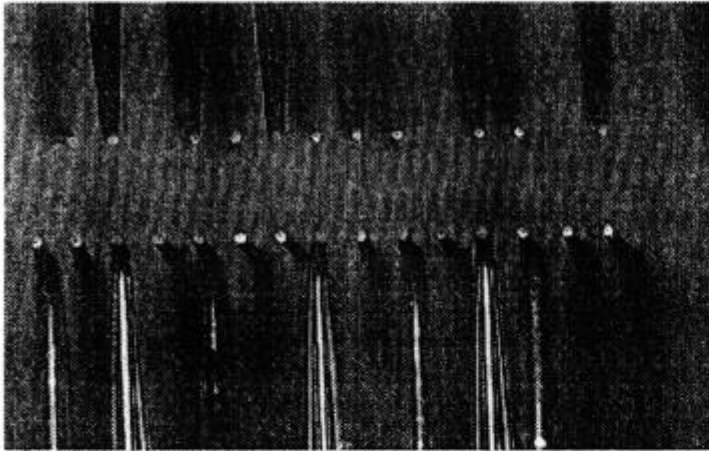


Incoming control errors

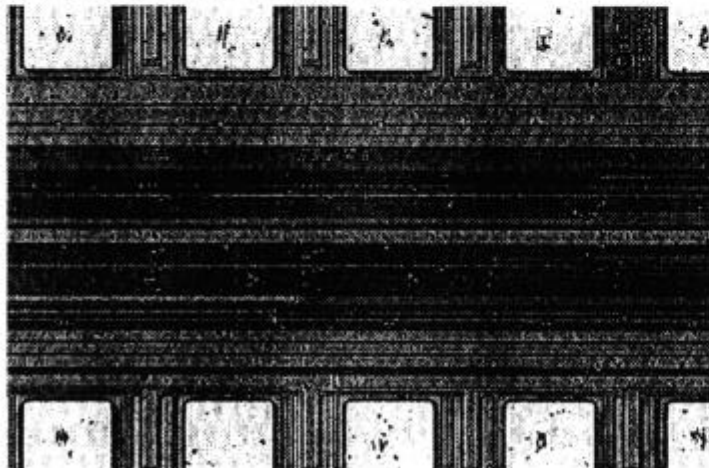


PC- Problems during lifetime (100 cards/ 1 year)

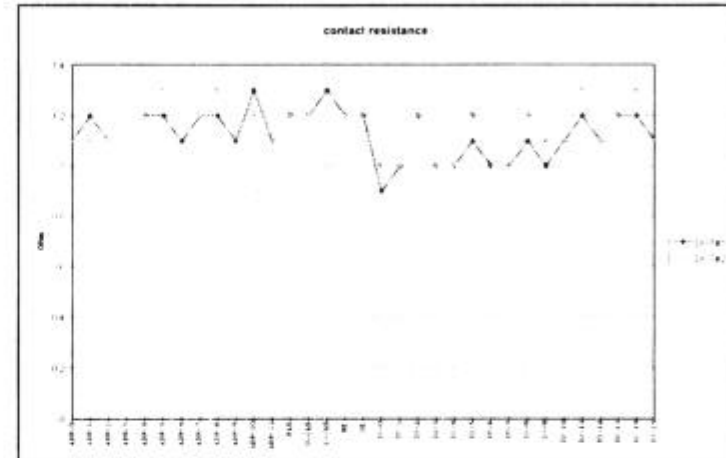




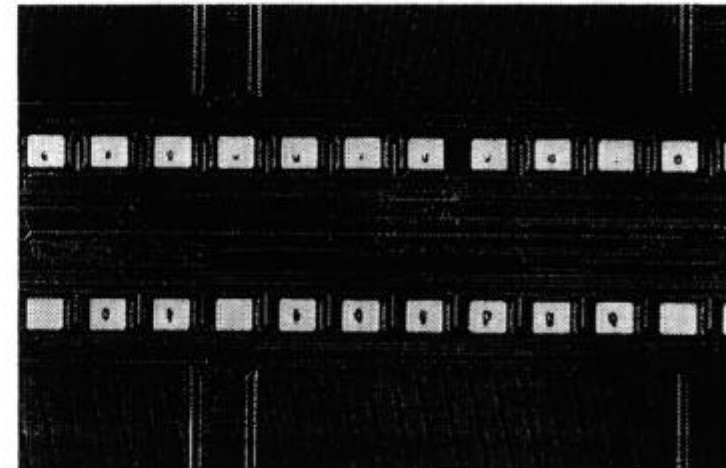
needle tips comes not vertical



unequal probe marks



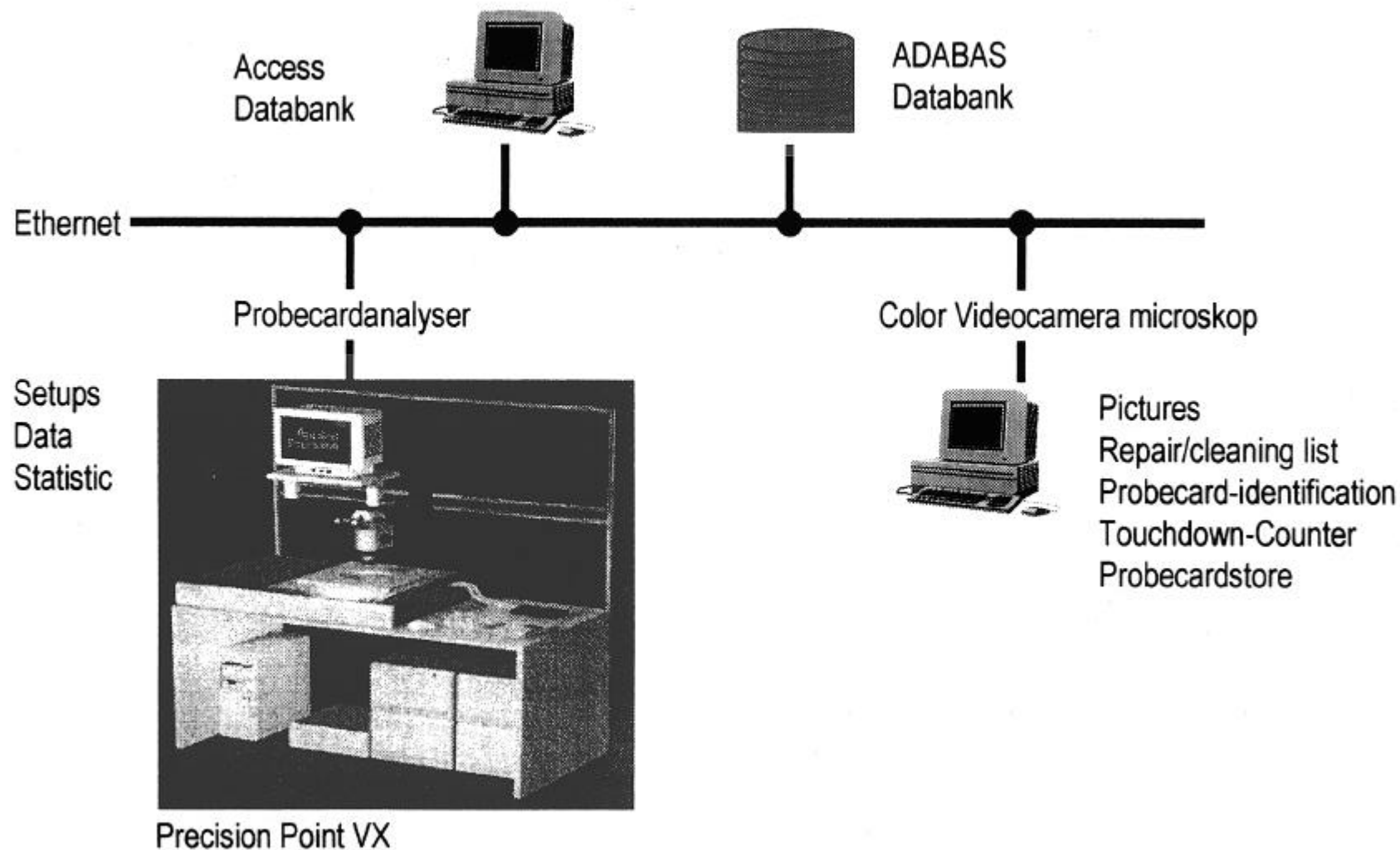
contact resistance

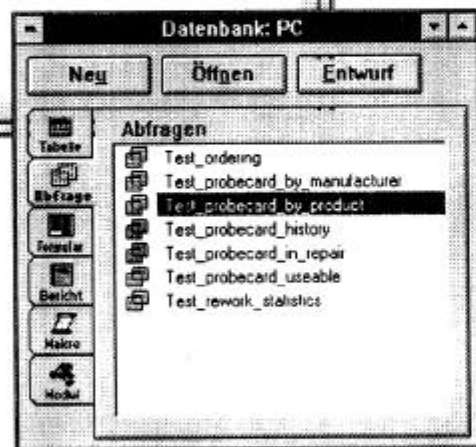
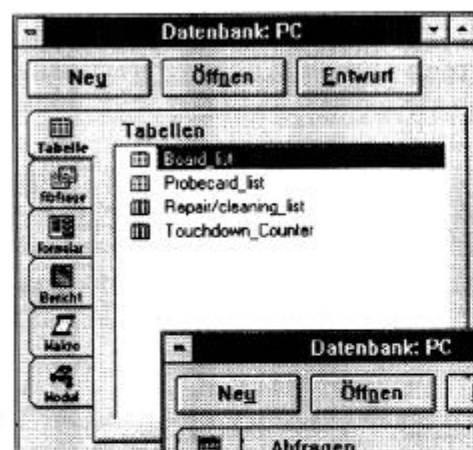


unequal probe marks

some problems - not vertical needle tips, multi needle layers

te.





Board_list
typ
tester
order_number
order_date
pieces
in_date
remarks

Probecard_list
pc-no
pc-id
order_number
order_date
in_date
out_date
tester
device
dut
typ
manufacturer
remarks

Repair/cleaning_list
pc-no
in_date
out_date
reason
prober
action

Touchdown_Count
pc-no
jan 97
feb 97
mar 97
may 97
jun 97
jul 97
aug 97
sep 97
oct 97
nov 97
dec 97

Tabellen: Reasons
alignment
crash
incoming control
first/last contact > 40µm
ICC5
leakage
needle step in passivation
probe marks uneven
probe marks to big
damage on pad edge
planarity
product change
tester diagnostic
VF-OPN
VF-SHT
X/Y-position
yield loss postfuse
yield loss prefuse
yield loss reference

Tabellen: Actions
full - check
full - check, ref.-measurement
partial - check
cleaning brush
cleaning brush, acetone
cleaning brush, acetone, grinding foil
cleaning brush, iso
cleaning brush, grinding foil
cleaning brush, grinding foil, iso
cleaning precision point
cleaning grinding foil
cleaning ultrasonic bath
return
rework aps
rework hit
rework MJC
rework TCL

Auswahlabfrage: Test_probecard_history				
pc-no	in_date	out_date	reason	action
24	05.06.1996	12.06.1997	incoming control	full - check, ref.-measurement
24	24.08.1996	28.08.1996	VF-OPN DUT2	cleaning precision point
24	18.09.1996	20.09.1996	VF-OPN DUT2/3	cleaning brush, acetone
24	30.11.1996	30.11.1996	no contact DUT5 VDD in contact loop	cleaning precision point
24	16.01.1997	17.01.1997	tester diagnostic	cleaning precision point
24	25.01.1997	25.01.1997	product change	cleaning precision point
24	30.01.1997	30.01.1997	tester diagnostic	cleaning precision point
24	07.02.1997	07.02.1997	product change	cleaning precision point
24	10.02.1997	10.02.1997	tester diagnostic	cleaning precision point
24	22.02.1997	22.02.1997	tester diagnostic	cleaning precision point
24	09.03.1997	09.03.1997	tester diagnostic	cleaning precision point
24	23.03.1997	23.03.1997	tester diagnostic	cleaning precision point
24	30.03.1997	30.03.1997	VP-OPN	cleaning precision point
24	13.04.1997	13.04.1997	tester diagnostic	cleaning precision point
24	19.04.1997	19.04.1997	yield loss	cleaning precision point
24	24.04.1997	24.04.1997	tester diagnostic	cleaning precision point

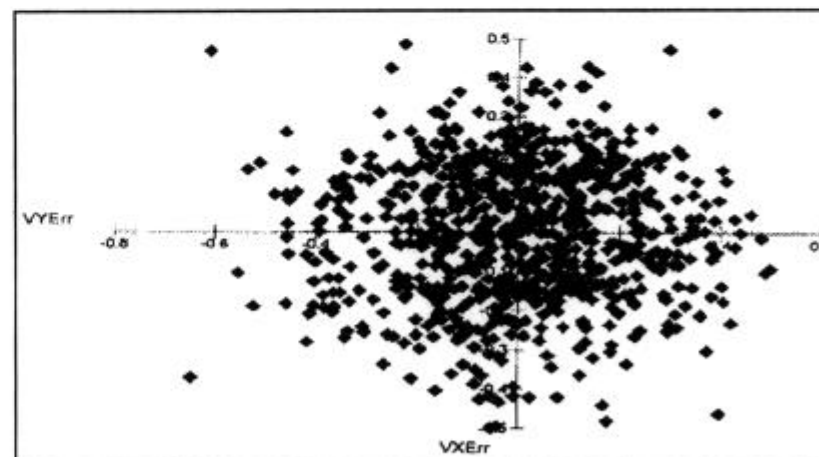
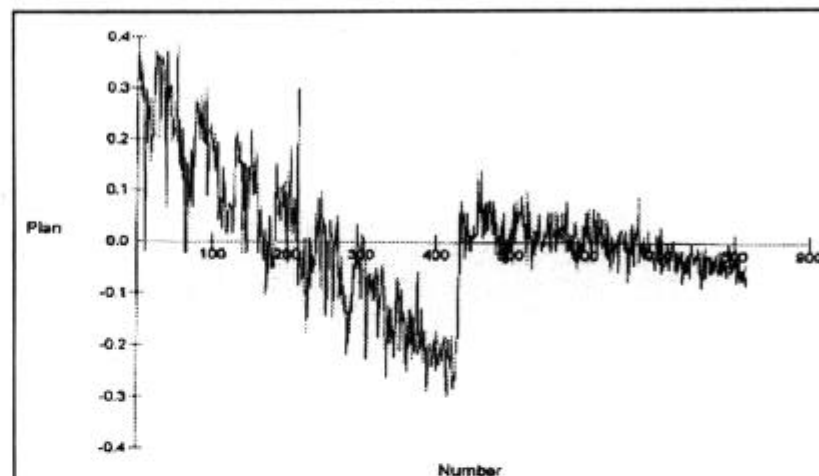
CpTest Format: 4.0
 SN: ES3002.62 Test: 1
 Date: 11/04/98 Time: 11:08:01
 File Name: ES3002.62CPT1_0001
 Card electrical:
 85nA - Allowable leakage 10volts - Forcing Voltage
 3.000 ohms - Allowable contact resistance 10mA - Forcing current
 Card physical:
 Units: MICRONS
 100 Elec OT 100 Vision OT 120 Max OT
 13 Planarity (max. Z dev +/-)
 20 Elec Align (max. X,Y dev +/-)
 20 Vision Align (max. X,Y dev +/-)
 0 Probe spring rate (grams/um)
 2.5 Probe force (max. dev +/-)
 8300 Specified probe depth 8280 Actual probe depth
 Test fixture:
 No.: Adv5365 Height: 15240
 Save 10 tests before deleting

ENDED HEADER PAD=66 3,88 3;

Product: ES3002
 Vendor: MUC
 Comments: EINGANGSPRUEFUNG
 Tech: PIETZSCHMANN

Passed	374	431	432	432	432	431	-	-	-	-
Failed	58	1	0	0	0	1	-	-	-	-
Not Found	0	0	0	0	0	0	-	-	-	-

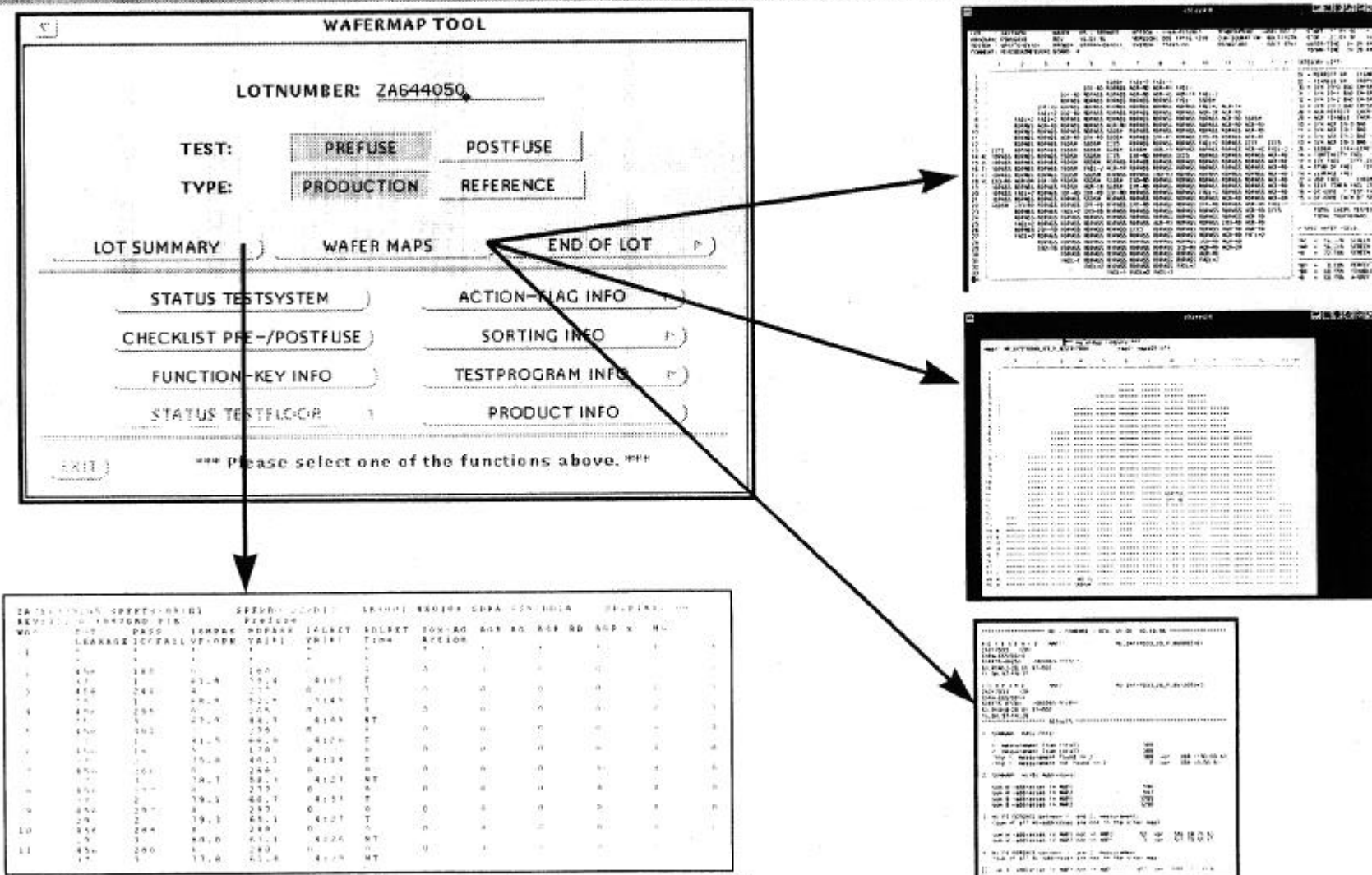
Ch	EC	Tr	Pad	Leak	CRes	VXErr	VYErr	VALign	Plan	Force	Scrub	ScrAng	Dia
250	85C2	JUTS	E23	>9999"	.720	0.5	0.5	0.7	-1.7		21.8	-0.3	32.9
342	96C		F23	>9999"	.710	2.5	-0.0	9.3	-1.7		36.8	0.0	35.1
45	GND		VB3	1810"	.200	7.1	-1.1	7.2	11.57		12.9	-6.1	35.4
45	GND		VB11	1810"	.198	7.6	-1.3	8.0	3.3		15.5	-10.4	29.8
45	GND		VB15	1810"	.220	-0.4	-0.5	0.7	1.7		25.2	-8.9	31.5
45	GND		VB23	1810"	.206	8.5	-6.1	8.9	-1.0		14.8	-0.2	34.3
45	GND		VD29	1810"	.210	9.4	0.0	9.4	6.0		28.1	5.9	28.2
45	GND		VD25	1810"	.188	5.3	1.4	5.5	3.3		29.5	2.2	30.9
45	GND		VD21	1810"	.180	2.8	-8.4	8.9	-2.2		34.0	2.8	32.9
45	GND		VD17	1810"	.198	3.8	-3.4	5.0	-0.5		33.9	1.2	32.0
45	GND		VD13	1810"	.200	-1.2	-4.4	9.5	-3.1		32.2	1.1	30.2
45	GND		VD30	1810"	.198	5.5	-1.3	5.8	4.4		31.0	3.4	35.2
45	GND		VA4	1810"	.208	6.4	0.9	6.4	0.6		28.0	-6.1	34.1
45	GND		VC30	1810"	.198	2.3	-0.5	2.4	0.0		9.4	9.5	33.9
45	GND		VB7	1810"	.205	6.7	-4.0	7.8	3.3		13.5	-4.2	27.6
45	GND		VC22	1810"	.195	4.7	3.7	6.1	0.8		12.4	8.8	37.8
45	GND		VC18	1810"	.195	4.0	5.3	6.8	0.8		15.2	7.3	34.9
45	GND		VB19	1810"	.203	-2.7	0.0	2.7	-2.9		17.8	-0.5	32.2
45	GND		VC8	1810"	.178	0.0	3.4	3.4	-0.2		13.8	-2.9	34.1
45	GND		VB27	1810"	.185	-10.2	-8.9	13.5	0.4		16.8	1.2	33.2
45	GND		VB31	1810"	.225	-11.5	-4.0	12.2	1.2		17.4	-2.3	27.6
45	GND		VC14	1810"	.190	2.6	-2.5	3.7	-3.4		20.7	-6.6	34.2
45	GND		VA24	1810"	.195	-1.0	4.2	4.3	-4.2		36.0	0.9	33.9
45	GND		VC10	1810"	.183	1.6	-3.5	3.9	2.4		31.8	-0.7	36.9
45	GND		VD6	1810"	.190	-7.0	4.8	8.5	-2.3		21.1	-1.7	33.3
45	GND		VD28	1810"	.210	7.5	1.3	7.6	2.1		30.1	2.2	34.6



prober	count wafer	mean yb	st dev yb	min yb	max yb
SPFPRO-02	193	78.66	5.25	67.0	89.1
SPFPRO-03	203	78.92	4.35	67.0	86.0
SPFPRO-04	293	77.41	4.41	67.0	88.8
SPFPRO-05	271	78.32	5.50	67.0	90.9
SPFPRO-07	341	78.41	5.21	67.0	88.5
SPFPRO-08	294	78.06	5.05	67.0	88.8
SPFPRO-12	197	79.28	5.24	67.3	91.3

probecard	count wafer	mean yb	st dev yb	min yb	max yb
NK0013	197	78.41	4.73	67.0	89,1
NK0014	278	78.52	5.16	67.6	88,6
NK0016	178	80.05	5.06	67.6	88,3
NK0017	281	78.00	5.31	67.0	89,5
NK0018	177	79.68	5.50	67.0	91,2
NK0019	172	80.00	4.58	67.0	89,0
NK0024	168	79.40	4.83	68.0	88,7

middle of august to middle of september 96

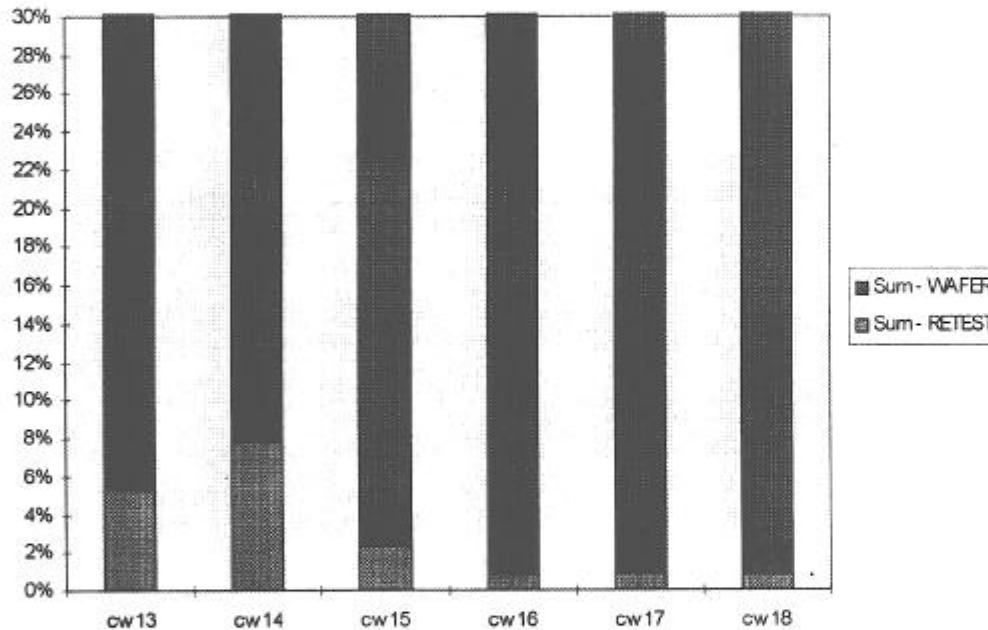


Prefuse Checks

Problems	Limit
Zero/Low-Yield	< 7%
Contact	> 1% not on wafer edge
TSLY	< 97%
DUT	> 20% DUT-Yield-difference
Lot-Yield	$Y_A < 50\%$ $Y_B < 45\%$
Wafer-Yield	> 10% Wafer-Yield-difference

Postfuse Checks

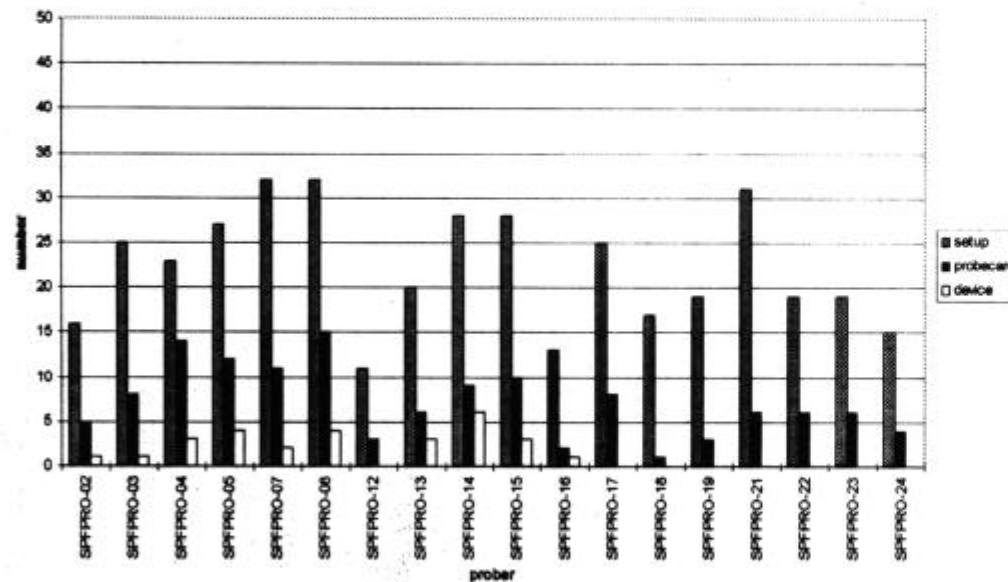
Problems	Limit
Contact	> 0,3% of total chip prefuse
ICC5	> 0,6% of total chip prefuse
5V-FCN	> 0,6% of total chip prefuse
Yield	< 98%
DUT	> 10% DUT-Yield-difference



Possibilities of improvement

- Setup quality
- Control probecard quality
- Effectiv cleaning
- Online performance control
- Reference measurements
- SPC

number of setups, probecard changes and device changes



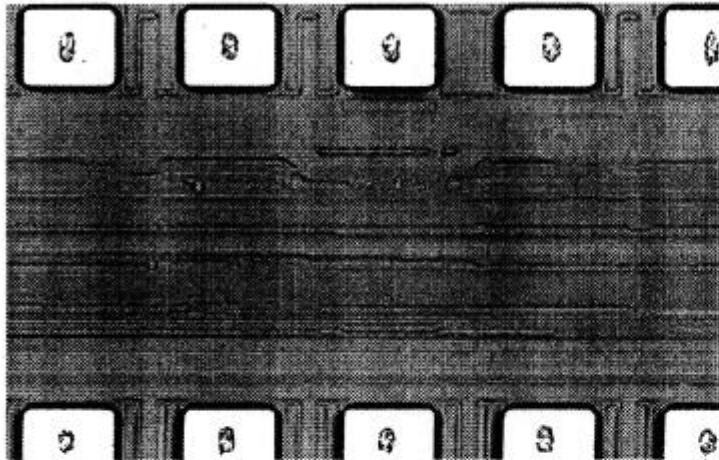
Possibilities of improvement

- Setup quality
- Control probecard quality
- Find out prober tolerances
- Dispatch function
- Soaktime

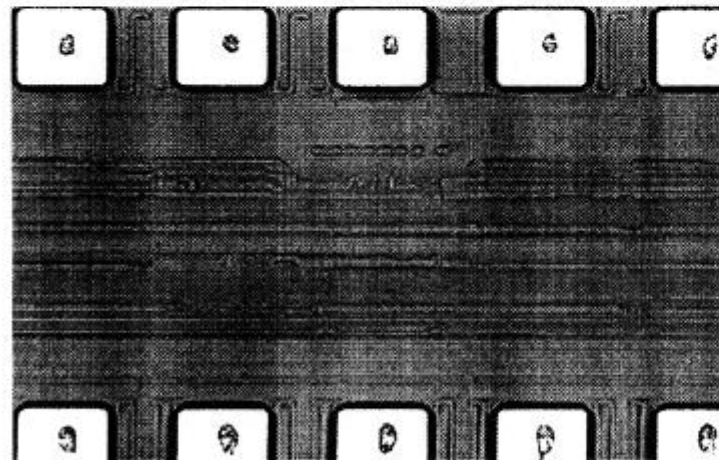
Product	Data	cw 01/97 - 16/97
4MCD	Wafer	0,19%
	System	0,17%
	Lot	7,14%
ES3DD2	Wafer	0,07%
	System	0,09%
	Lot	5,30%
ES5DD2	Wafer	0,05%
	System	0,09%
	Lot	13,46%

Possibilities of improvment

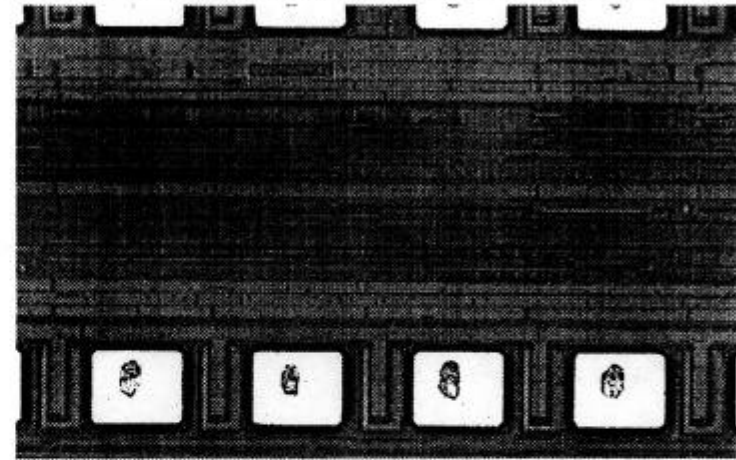
- Setup quality
- Control probecard quality
- Probemark inspection
- Pad layout



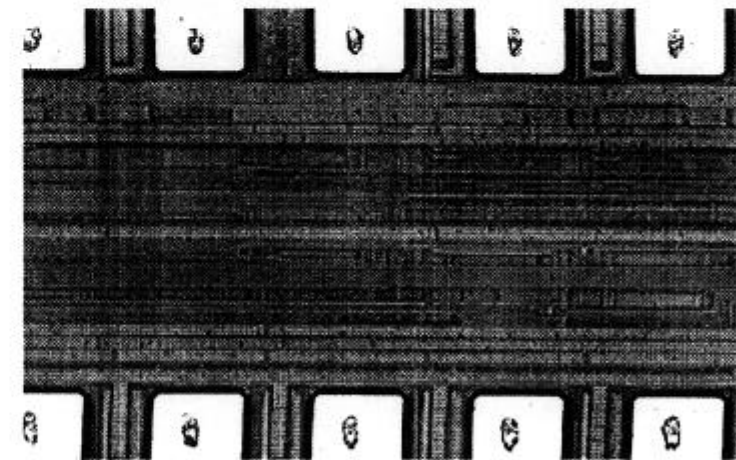
unequal probe marks antinotch



unequal probe marks notch

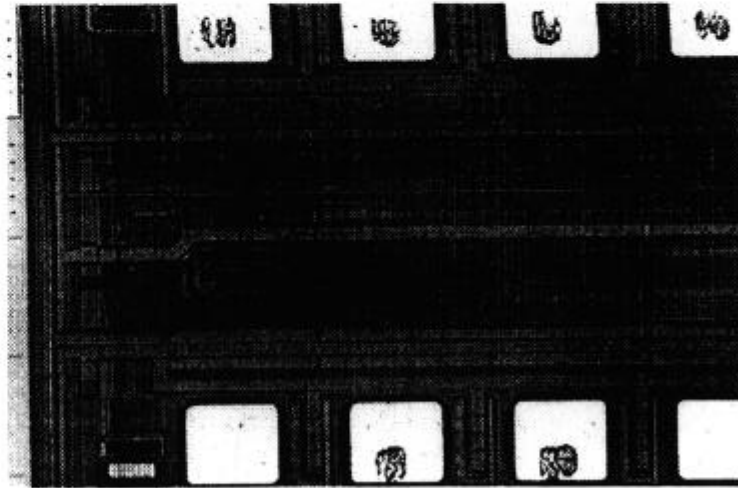
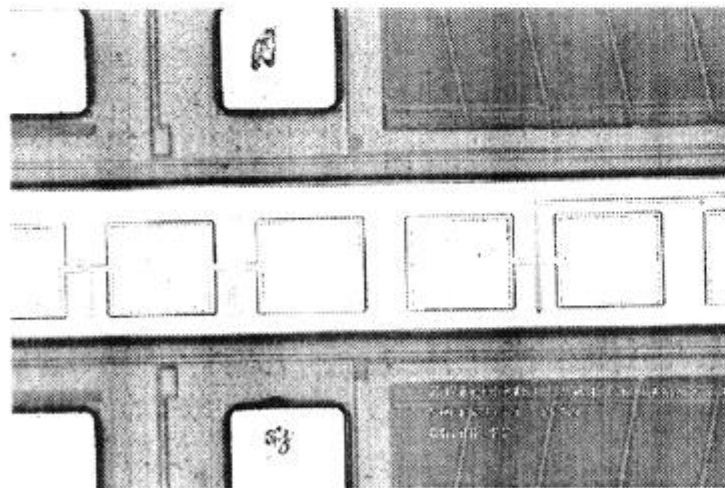
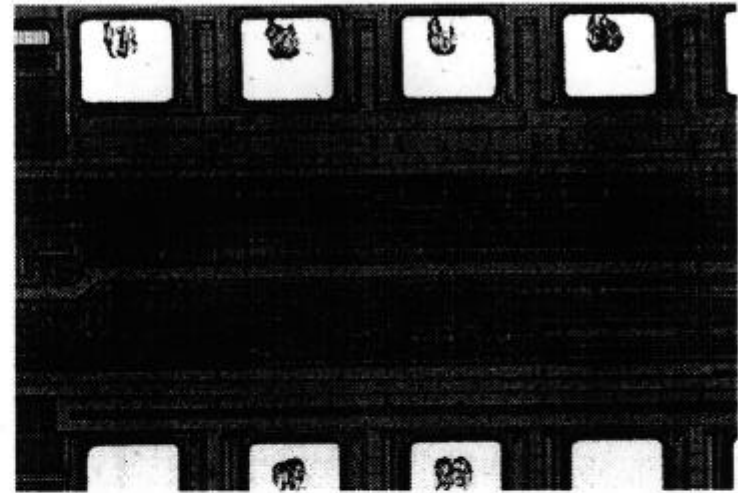
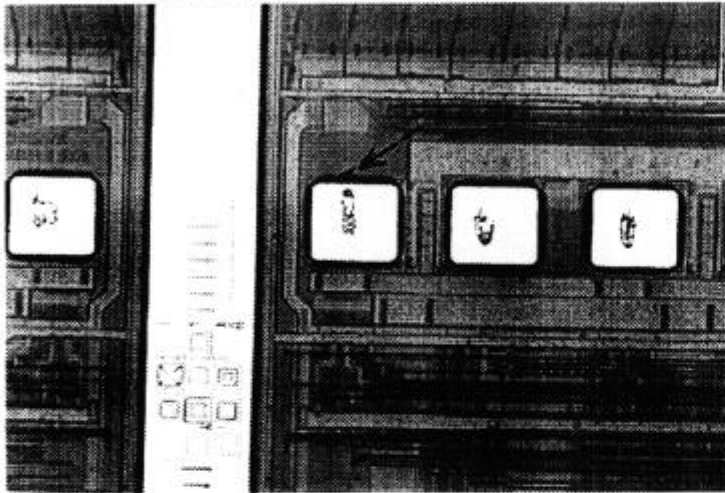


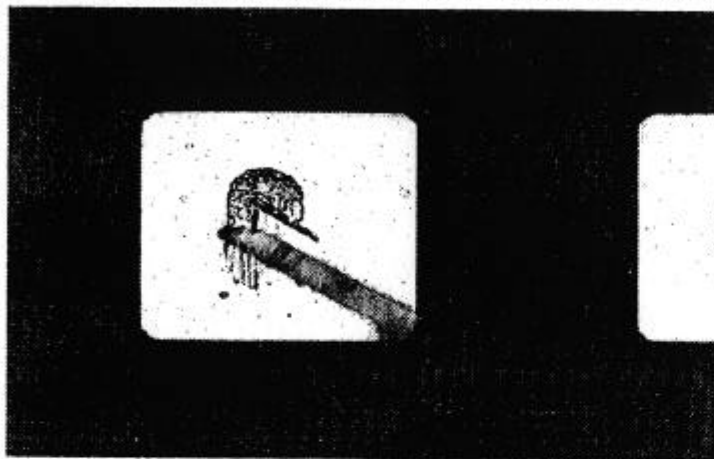
with prober-correction-software antinotch



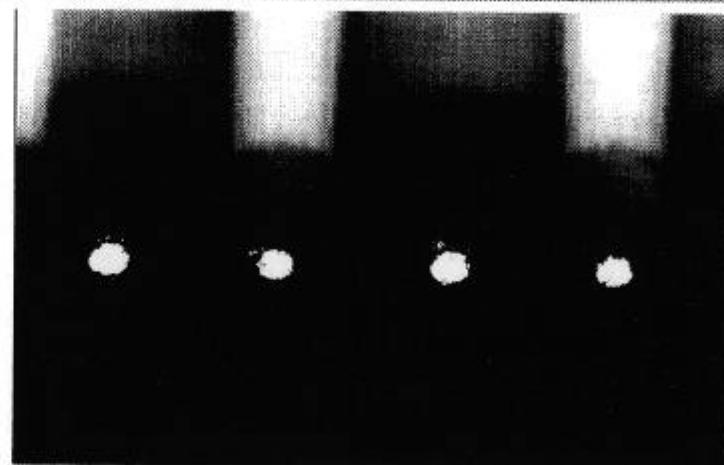
with prober-correction-software notch

some problems - unequal probe marks on wafer edge

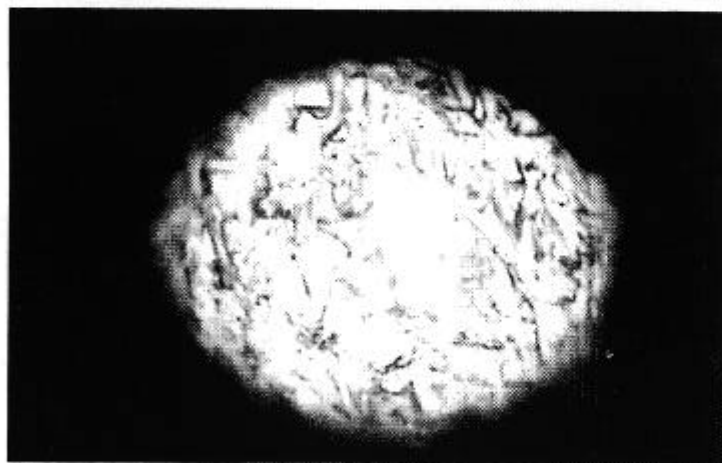




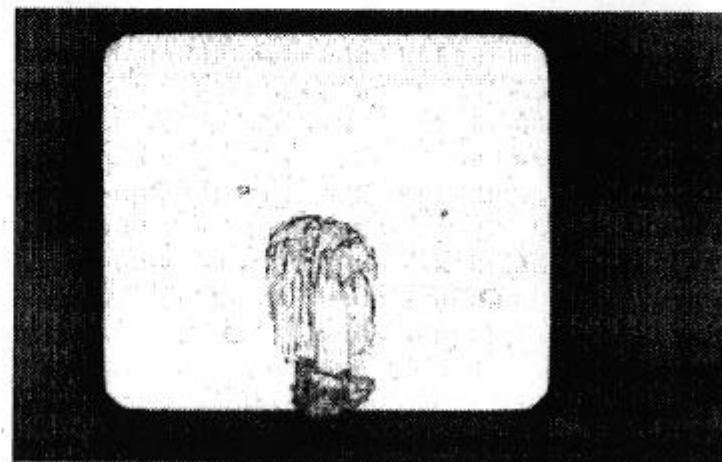
VF-OPN in Postfuse



dirty needles



dirty needle



loosed dirt

Customer wishes

Equal quality during lifetime (year/500.000 TD's)

No cleaning out of prober

1000 TD without cleaning

Same testquality for all pad layouts

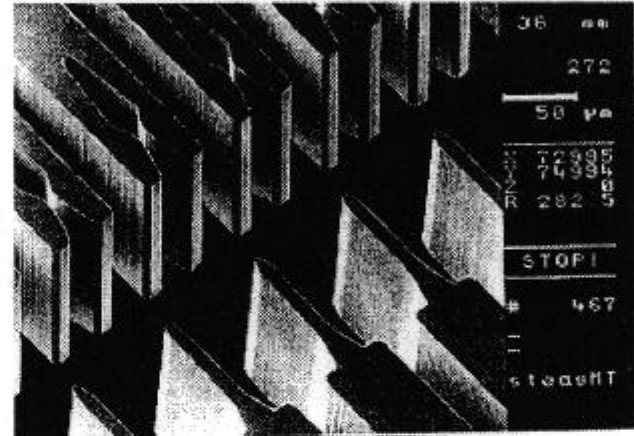
Increase of cost from 8 DUT to 16 DUT max. factor 2

Delivery time < 4 weeks

Customer support

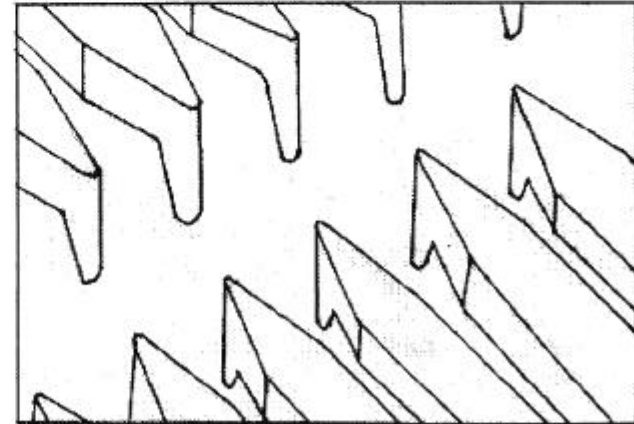
Service

The key is microsystem technique?



connector
source "Chip" 3/92

If that is possible -



this is also possible ...