Halving Cost of Test Using Parallel Multi-Die Approach for Mixed Function Testing

Hervé DESHAYES

STMicroelectronics
COTRED Project

- Funded by European Union under ESPRIT program
- Semiconductor Equipment Assessment
- STMicroelectronics, TEMIC-MHS, Schlumberger ATE
- Assessment of tester designed to reduce Cost of Test
COTRED Project Objectives

• To halve the Cost of Test of complex microcontrollers, comprising purely digital and/or embedded analog functions
• To ensure that ITS 9000CV fulfills the technical requirements of the users
• To evaluate the single to parallel program transfer efficiency and ease of use
Microcontroller Test Requirements

- Product complexity
  - Match mode
  - Analog
    - A/D and D/A
    - Wireless applications
    - TV applications
  - Embedded memories (ROM, EPROM, E²PROM, Flash)
  - Timing and level calibration

- Test at speed
  - 4MHz to 80MHz
  - Test time between 1 and 10 seconds

- Pad pitch and die area
Why Parallel Test?

- Test more units with the same investment
- Optimize all hardware resources
  - QFP80 by 2
  - SDIP56 by 3
  - SO28 by 6
  - DIP16 by 8

- Better Return on Assets
  - Low ASP of Microcontrollers (declining by 10% per year)
  - VLSI testers cost from $0.5M to $2M
  - High pin count needed for some low volume parts
Cost of Test Analysis

- Test-related spending
  - Operating cost
  - Ramp up cost
  - Maintenance cost
  - Capital equipment cost

- Using ACOLYTE©
  - EXCEL® based cost analysis model
  - 126 parameters

\[
COT = \frac{\sum_{\text{test\_related\_spending}}}{\sum_{\text{good\_parts}}}
\]
Key for Cost of Test Reduction

Sensitivity: COT vs ATE cost, # of sites

- Equipment Cost (k$)
- Cost of Test / Good Die (¢)

Number of sites:
- 1
- 2
- 3
- 4

Graph showing the relationship between equipment cost and the cost of test per good die for different numbers of sites.
Issues for Parallel Test

• Wafer sort
  – Probing issues: pitch, layout, use of vertical probing
  – Handling and index time compared to test time

• Final test
  – Parallel handler (high parallelism & high efficiency)
  – Sorter and index time compared to test time

• Partner approach is mandatory
• Tester optimized for parallel test
  – Minimal overhead
  – Parallel resources
Importance of Overhead

Sensitivity: COT vs. Overhead, # of sites

COT (¢/Good Die) vs. Multi-Site Overhead (%)

Number of sites:
- 1
- 2
- 3
- 4
ST Micro’s Parallel Test History


Wafer Sort
Production
(Rousset)

Final Test
Production
(Muar, Malta)

Previous generations  ITS 9000CV
Achievement at STMicroelectronics

• Test Time
  \[ \text{Test time}_n \approx \text{Test time}_1 \]
  – overhead is minimal

• COT per die (Throughput)
  – All products are tested by 2, 3, 4 or 6.
  – Transfer of single program into parallel automatic
  – Vertical probing using COBRA technology.
Wafer Test Time vs. # of sites

![Bar chart showing the relationship between wafer test time per wafer (in minutes) and the number of sites.

- Test Time per wafer (min.): 0, 10, 20, 30, 40, 50, 60, 70, 80
- # of sites: 1, 2, 3, 4, 5, 6, 7, 8

The chart indicates that as the number of sites increases, the test time per wafer decreases.
Cost of Test Reduction at STMicroelectronics

- Overall global gain ratio compared to single site
  - Wafer sort > 3
  - Final Test > 2

- COTRED objective exceeded: COT reduced by 70%

![Graph showing cost of test reduction](#)
ITS 9000CV features

- Parallel by 16
  - 8 per test head
  - 2 test heads simultaneously
- Parallel test program
  - Automatic transfer from single test program
- All tests (DC, ftest, APG scan, match, DAC/ADC) can be executed in parallel.
- Full compatibility with ITS9000 Family.
- Meets COTRED objectives
Key for Cost of Test Reduction

Sensitivity: COT vs ATE cost, # of sites

Cost of Test / Good Die (¢) vs Equipment Cost (k$)

- Number of sites: 1, 2, 3, 4
- CV, Prober, etc.
Conclusion

• The only effective way to reduce the cost of Test is to maximize parallel capability.
  – not only software but also hardware
  – all test features must be in parallel

Future of Parallel Test

• The number of test sites will increase (tester, prober, handler, probe card)
• More parallel resources