Overview of WLBI system approaches

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Trends in the Electronics Industry

- **IC Technology**
  - Higher pin count
  - Higher power
  - Higher speed

- **Major Drivers**
  - Cost/Performance
  - Quality
  - Time-to-Market
  - Product Miniaturization, i.e. lighter, thinner, shorter, and smaller

![IC Density Trends Graph]

Source: Intel/CE

Memory increase = 1.5/year

CPU increase = 1.35/year
IC quality & reliability

- **Test**
  - Finds manufacturing defects that cause failure
  - Not feasible to search for all potential defects
  - One second on VLSI tester - 2¢ to 15¢
    » Exhaustive testing all combinations not economically feasible

- **Burn-in**
  - Stress causes weak devices to fail
  - Temperature stress
  - Voltage stress

- **Test during burn-in**
  - Long cycle functional testing is time-consuming
    » Trend to offload to lower cost TDBI systems
Burn-in Cost Trend is Not Sustainable

- **Burn-in is a requirement for latest generations of VLSI devices**
  - New failure modes emerging due to shrinking geometries
  - Researchers have failed to find an effective alternative

- **Show stopper for many applications dependent on advanced packaging (i.e., KGD)**

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**Cost per Burn-in Socket Position**

(Includes burn-in-boards, drivers, ovens, backplanes)

- **Product**: 8086, 286, 386, 486, 386SL, P5

- **Source**: Intel

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**Pie Charts**

- **> 1µm Feature Size**
  - Particles
  - Oxide Film Defects
  - Mask Defects
  - Ion Contamination
  - Corrosion
  - Crystaline Defects
  - Misaligned Vias
  - Al Voids
  - Short Circuits

- **< 1µm Feature Size**
  - Particles
  - Oxide Film Defects
  - Mask Defects
  - Ion Contamination
  - Corrosion
  - Crystaline Defects
  - Misaligned Vias
  - Al Voids
  - Short Circuits
Wafer Level Probing Lowers Burn-in Cost

- MCC cost models predict 50% cost savings for wafer level burn-in wrt current practice
  - Other savings also significant
    » Reduced IC fab/assembly/test cycle time, lower WIP
    » Improved reliability feedback and control
    » Enables new paradigm for assembly & test

- Full wafer probing for IC burn-in/test is achievable now

- Key components of Wafer Level Burn-in/Test (WLBT) system now coming into focus
IC “Back-end” Processes

Full testing and reliability conditioning takes place at the wafer level - new equipment, processes, strategy. Supports bare die as well as existing packaged IC markets.
WLBT Cost Comparison

- Fixed quantity of product each year
- 1 Meg FSRAM product
- Have sufficient capacity to keep product moving

Assumptions
- 1.5 year product life
- 15 hour burn-in (+ 4 additional hours ramp up/down, etc)
- $10K/WLBT probe + $10K/probe fixture
### WLBI Cost Saving

#### Typical Final Test Yields

<table>
<thead>
<tr>
<th>IC Product</th>
<th>Final Test Yield</th>
</tr>
</thead>
<tbody>
<tr>
<td>8-Bit MPU</td>
<td>95%</td>
</tr>
<tr>
<td>20,000 Gate Array</td>
<td>90%</td>
</tr>
<tr>
<td>4M DRAM</td>
<td>95%</td>
</tr>
<tr>
<td>16M DRAM</td>
<td>90%</td>
</tr>
<tr>
<td>64M DRAM</td>
<td>75%</td>
</tr>
<tr>
<td>4K GaAs SRAM</td>
<td>80%</td>
</tr>
<tr>
<td>32-Bit MPU (386)</td>
<td>90%</td>
</tr>
<tr>
<td>32-Bit MPU (P54C)</td>
<td>75%</td>
</tr>
</tbody>
</table>

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- Graph shows cost of scrapping packages
- Assumes 80% final test yield, 2% burn-in fallout

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$0.10$ $1.00$ $10.00$

Burn-in cost/die

$0.00$ $1.00$ $2.00$ $3.00$ $4.00$ $5.00$ $6.00$ $7.00$ $8.00$ $9.00$ $10.00$

Package cost

- Yielded (total) cost/die
- Yielded (burn-in only) cost/die
- WLBI cost/die
WLBT Value Added

- Laser repair of burn-in fails is feasible after wafer level burn-in, but not available after pkg burn-in

- Assumptions
  - 50% repairability of burn-in fails
  - Distribute ASP of repaired die over population produced that year

![Graph showing 16M DRAM Volume and ASP from 1992 to 1997](image)

- Burn-in Fallout (Assume half of fails are repaired)
  - 2.0%
  - 1.5%
  - 1.0%
  - 0.5%
  - 0.1%

![Bar graph showing 16Meg DRAM Volume](image)

- Assumes 5% of market

- ASP:
  - $0,000,000
  - $50,000,000
  - $100,000,000
  - $150,000,000
  - $200,000,000
  - $250,000,000
  - $300,000,000
  - $350,000,000
  - $400,000,000
  - $450,000,000
  - $500,000,000
  - $550,000,000
  - $600,000,000
  - $650,000,000
  - $700,000,000
  - $750,000,000
  - $800,000,000
  - $850,000,000
  - $900,000,000
  - $950,000,000
  - $1,000,000,000
  - $1,050,000,000
  - $1,100,000,000
  - $1,150,000,000
  - $1,200,000,000
  - $1,250,000,000
  - $1,300,000,000
  - $1,350,000,000
  - $1,400,000,000
  - $1,450,000,000
  - $1,500,000,000
  - $1,550,000,000
  - $1,600,000,000
  - $1,650,000,000


- (est)
Additional WLBT Benefits

- **Fully Automatable**
  - Reduce load/unload time
  - WLBT fits into highly automated IC assembly processes
    » Potential for inventory reduction
    » Cycle time improvements

- **Keep from packaging (or shipping) weak devices**
  - Yield loss at WLBT recoverable by laser repair
  - Early identification of “rogue” lots
  - Enabler for “single insertion” test/screening
    » All die fully conditioned at wafer level
    » Solution for KGD (Flip-chip)

- **Rapid reliability feedback on wafer/lot basis**
  - Improves time-to-volume

- **Eliminate traditional wafer probe step**
  - Massively parallel test during burn-in reduces time spent on expensive VLSI tester
Wafer Burn-in Worldwide

■ WBI Technology for Ram’s*
  — Memory Cell DC Stress to screen Bit Failures
  — Entire RAM Dynamic Stress for remaining failures

■ WBI suppliers
  — Espec
  — Asia Electronics

■ Several captive programs
  — Some IC manufacturers developing hardware
    » Cost effective KGD
    » Reduce cycle time
    » Improved reliability feedback
    » Potential for laser repair of DRAM burn-in fails

* Furayama, et al. Wafer Burn-in (WBI) Technology for RAM’s — IEDM-93
Hypothetical 200mm Wafer Parameters

- Die: 652
- Signal Pads: 18,908
- Power Pads: 2608
- Total Pads: 21,516
- Total Power: 650 W
# Feasibility Criteria

## Target Product

<table>
<thead>
<tr>
<th>Attribute</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>Diameter</td>
<td>200mm</td>
</tr>
<tr>
<td>Pad Metallurgy</td>
<td>Aluminum/ Sn-Pb</td>
</tr>
<tr>
<td>Minimum Passivation</td>
<td></td>
</tr>
<tr>
<td>Well (Pad) Size</td>
<td>75µ X 75µ</td>
</tr>
<tr>
<td>Maximum Passivation Well Depth</td>
<td>8.0 µm</td>
</tr>
<tr>
<td>Minimum Pad Pitch</td>
<td>150µ peripheral, 200µ array</td>
</tr>
<tr>
<td>Maximum Pad Density</td>
<td>150 pads/ cm²</td>
</tr>
<tr>
<td>Maximum z Variation, Pad-to-Pad</td>
<td>1.0µm</td>
</tr>
<tr>
<td>Maximum Power Density</td>
<td>5 W/ cm²</td>
</tr>
<tr>
<td>Temperature Range</td>
<td>25°C - 150°C</td>
</tr>
<tr>
<td>Maximum Burn-In Time</td>
<td>1.68 hrs</td>
</tr>
<tr>
<td>Clock Frequency</td>
<td>DC - 20 Mhz</td>
</tr>
</tbody>
</table>
# Feasibility Criteria

## Target Probe Coupon

<table>
<thead>
<tr>
<th>Attribute</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>Probe Coupon Diameter</td>
<td>250mm</td>
</tr>
<tr>
<td>Dimensional Tolerance</td>
<td>+/- 12µm absolute</td>
</tr>
<tr>
<td>Maximum Probe Point Size</td>
<td>25µm X 25µm</td>
</tr>
<tr>
<td>Maximum Probe Point Current</td>
<td>100mA</td>
</tr>
<tr>
<td>Maximum Probe Point Resistance</td>
<td>1.0ž</td>
</tr>
<tr>
<td>Minimum Reuses, Same Pad</td>
<td>3</td>
</tr>
<tr>
<td>Minimum Lifetime, Reuses</td>
<td>200</td>
</tr>
<tr>
<td>Minimum Lifetime, Hours at Temp.</td>
<td>5000</td>
</tr>
<tr>
<td>Maximum Isolation Resistor Density</td>
<td>150 resistors/cm²</td>
</tr>
<tr>
<td>Isolation Resistor Values</td>
<td>5kž - 20kž</td>
</tr>
<tr>
<td>Max. Isolation Resistor Voltage Drop</td>
<td>7.5V</td>
</tr>
<tr>
<td>Max. Unisolated Signal Line Res.</td>
<td>100ž</td>
</tr>
<tr>
<td>Max. Voltage Variation, VCC to Gnd</td>
<td>5%</td>
</tr>
<tr>
<td>Power Isolation</td>
<td>Must be provided.</td>
</tr>
<tr>
<td>Decoupling Capacitors</td>
<td>Max. 3 die/cm²</td>
</tr>
<tr>
<td></td>
<td>Must be provided as needed.</td>
</tr>
</tbody>
</table>
WLBT Challenges

■ Probe card
  — High density interconnect
  — CTE matching of probe to silicon
  — Co-planar probe tips
  — Uniform, “low” resistance contacts to aluminum pads/solder bumps

■ Probe card environment
  — Precise alignment of probe to wafer
  — Uniform force delivery of probes to wafer
  — Mechanically decouple probe card from system
    » CTE matched components independent of non-CTE matched components
  — Thermal management of junction temperatures
    » All die subjected to uniform stress
      • V, T, ramp
Three-Layer Probe Isolates Challenges

- Can optimize each piece
  - Multiple layers for high density routing
  - Compliant material to “soak up” non-planarities
  - Robust probe points for probing Al pads

CTE-Constrained Multilayer Interconnect

Membrane with probes and vias only (no routing) bonded under tension to a CTE-constrained support ring

Z-axis compliant conductor
Existence Theorem

- Matsushita Electric Industrial Co. Ltd has developed a 3 layer probe card
  - Membrane-type probe points
  - Compliant z-axis conductor
  - Glass substrate multilayer

- Probe card components Cte-matched to Silicon
- Uses atmospheric pressure for contact force
WLBT System

- Wafer cassette incorporating probe card
- Cassette Loader/Unloader based on auto-prober
- Standard wafer-handling equipment
- System development focuses on interface specifications

![WLBT Alignment System](Image)

![Wafer Level Burn-in System](Image)
Potential WLBI System market

<table>
<thead>
<tr>
<th>8&quot; wafers/day</th>
<th>1996</th>
<th>1997</th>
<th>1998</th>
<th>1999</th>
<th>2000</th>
</tr>
</thead>
<tbody>
<tr>
<td>16M DRAM</td>
<td>15353</td>
<td>17890</td>
<td>22696</td>
<td>15293</td>
<td>9753</td>
</tr>
<tr>
<td>64M DRAM</td>
<td>674</td>
<td>5721</td>
<td>15825</td>
<td>44033</td>
<td>72849</td>
</tr>
<tr>
<td>256M DRAM</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1715</td>
<td>1353</td>
</tr>
<tr>
<td>1M SRAM</td>
<td>6279</td>
<td>10022</td>
<td>13063</td>
<td>16082</td>
<td>18400</td>
</tr>
<tr>
<td>(32 bit+) µP</td>
<td>4789</td>
<td>6082</td>
<td>7173</td>
<td>7940</td>
<td>9058</td>
</tr>
<tr>
<td>Candidate Product (wafer)</td>
<td>27096</td>
<td>39715</td>
<td>58756</td>
<td>85063</td>
<td>111414</td>
</tr>
<tr>
<td>New capacity this year</td>
<td>12619</td>
<td>19041</td>
<td>26307</td>
<td>26351</td>
<td></td>
</tr>
<tr>
<td>% WLBI</td>
<td>0%</td>
<td>0%</td>
<td>0.001%</td>
<td>0.050%</td>
<td>2.000%</td>
</tr>
<tr>
<td>$450K/x10 station</td>
<td>$0</td>
<td>$0</td>
<td>$26,440</td>
<td>$1,887,478</td>
<td>$98,358,411</td>
</tr>
</tbody>
</table>

![Graph showing 8" wafers/day and $450K/x10 station over years]

![Graph showing 16M DRAM, 64M DRAM, 256M DRAM, 1M SRAM, and (32 bit+) µP over years]
WLBT System Wish List

■ Probe Card
  — <$10K
  — 500 - 5000 uses
  — 100% yield
  — Quick Turn
  — “good” electrical environment

■ Cassettes
  — Controlled environment
  — One design fits particular wafer size (150mm, 200mm, 300mm, . . .)

■ Utilize existing equipment for off-line alignment station and test electronics
  — Greatly improved equipment utilization
Quick Turn Multilayer Interconnect Using LDW

- Quick turn of new probe design
- Route around defects
- Lower cost - standardized substrate

- Four layer design
- Bottom two layers (not shown above) contain a mesh of four programmable reference planes

- 40 µm pitch
- 20 µm line width

Top two layers are reserved for x-y signal lines

4.0 inch
WLTB Probe Laboratory

- **Test Electronics**
  - Up to 2000 pins
  - Total Current source up to 330A @ 8.0V

- **Mechanical Fixture**
  - Wafer Size - Up to 8”
  - Force - 4 - 6000 lbs, 2 lb resolution
  - Alignment - +/-0.5 mils
  - Planarization - Self-Planarizing
  - Chuck - Vacuum chuck with active cooling

- **Mechanical Fixture**

- **Fixture Close Up**

- **Profilometer**