Full Wafer Burn-In and Test

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**Wafer Level Burn-in & Test; How Things will Change**

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Introduction; Full Wafer Burn-in and Test

Two Key Enabling Technologies for WLBT, that have been lacking in the past, are suitable interconnect boards and a robust wafer to board contactor.

The following presentation will discuss GORE’s solutions
Wafer Contactor
Desired Properties

- Low electrical resistance / contact
- Low force / contact
- Minimal impact to the wafer pad
- Reliably contact many final metals
  - Al, Au, Cu, Solder(s)
- Easy to use with low maintenance
- Affordable!
Interconnect Board Desired Properties

- High temperature stable (150 - 175°C)
- Very high planarity over 200mm wafer area
- CTE matched to Silicon (~3 ppm/°C)
- Protected from shorts on the wafer (Power and Signal)
- Low thermal mass for fast cycling
- High Density contact pads
- Low, predictable electrical resistance
- Able to operate from DC to 100+ MHz
- Reasonable cost / board in volume
Gore Inferno™ Wafer Level Interconnect Board

Inferno™ 2061
For use in Tokyo Electron Limited’s WLBI system
5 Layer Inferno™ Board
Cross Sectional View

- Wafer Contact Side
- Low CTE Core

Blind Via

Buried Via

Not To Scale
Construction Method

- Standard PCB equipment is used to make either 5 or 7 metal layer circuits.
- Starting from a copper plane layer, multiple laminations are used to form each layer.
- Lased micro-vias are formed to connect Layer 2-6 and Layers 1-2 and 6-7.
Inferno™ IC Board Dielectric

- A specially formulated, high temperature dielectric reduces the out-of-plane (Z-axis) CTE for increased reliability
- This thermoset dielectric will allow reliable burn-in cycling to 150°C
- When combined with the constraining core, in-plane CTE is designed to match silicon
Contacting the wafer

Approximately to scale
Current Manufacturable Rules

- CTE matched to Silicon
- 75 μm Lines / Spaces
- 5 or 7 layer construction
- Via Sizes:
  - 75 μm blind via
  - 50 μm buried via
- 100 - 150 μm Flip chip contact pads
- Common Ground
- Individual Routed powers
  - (<0.5 ohm, matched)
- Feature placement 25 μm true position over 200 mm
- Planarity 25 μm across 200 mm
- 100-400Ω Resistors in evaluation
Wafer Contactor Requirements

- Good electrical performance over range of motion
  - Continuous Metal in Z axis with Compliance to create fully mated surfaces
- Low Pressure contact with minimal surface damage
  - Low modulus with Smooth contactor surface
- Ability to contact multiple chip footprints
  - Fine pitch contacts, 50 µm columns on 100 µm centers
- Reliable Contact
  - Withstand temperatures >175°C
  - New contactor with each cycle
Wafer Contactors

- GoreMate™ II Wafer Contactors
- Diameter 50 µm
- Pitch 100 µm
- Roughness less than 3 µm
- ~20 to 25 µm compliance at 20 ºC
Carrier Structure:
Expanded Polytetrafluoroethylene (ePTFE)

- ePTFE Nodes
- Fibrils

2 µm
X-Section
50/50/100 µm Parts

50 µm thickness
50 µm diameter on
100 µm pitch
X-Section from Top Down

100 µm pitch

50 µm Ø
50 µm columns on 100 µm pitch

Contactor Column
diameter ~ 50 µm

IC board Contact Pad
diameter ~ 150 µm
Pressure Effects on Contactor

Resistance and Compliance of GoreMate™ Wafer Contactors

![Graph showing the relationship between pressure (psi) and resistance (megohms) and compliance (%)]

- X-axis: Pressure (psi)
- Y-axis: Resistance (megohms)
- Purple line: Compliance (%)

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Contact Capability with TEL System

Opens per Million Attempts (OPMA)

Frequency

Opens per Million Attempts (OPMA)
Wafer Maps

Room Temperature

150°C

Inferno™ Board Flatness signature

Wafer Defects Only

Contact Bin 0
Contact Bin 1
Contact Bin 2
Contact Bin 3
Contact Bin 4
Contact Bin 5
Contact Bin 6
Wafer Defect
Wafer Maps at Temperature

Initial Room Temperature Contact

150°C Contact on Same Assembly

Contact Bin 0
Contact Bin 1
Contact Bin 2
Contact Bin 3
Contact Bin 4
Contact Bin 5
Contact Bin 6
Wafer Defect

99.50%
99.83%
99.58%
100.00%
100.00%
99.74%
GoreMate™ Wafer Contact Technology Roadmap

- Contact to other Wafer metallurgies - Al, Cu, PbSn
  - May require new final metal or metal finish
  - Summer 1999 - Proof of Concept and Technology
  - If proved, Developmental Material for use - Fall 1999
  - Commercial Product - January 2000 Target

- Increase Compliance by at least 100%
  - Proof of concept in mid to late 1999
  - If concept proved, Commercial January 2000
Summary

- A system for contacting wafers for Burn-In and testing at the wafer level has been developed.
- Interconnection to the system has been reliably accomplished during burn-in using a compressible, z-axis conductive interface to a wafer interconnect board.
Acknowledgements

✺ Motorola - Austin
  ✺ Testing of system, statistical experimentation on the reliability of contactors and interconnect boards.
  ✺ Data which was presented on the contact capability here

✺ Tokyo Electron Limited - Yamanashi
  ✺ Development of the system and feedback on contactors and interconnect boards