A High Performance C4 Probe: TFI™

By

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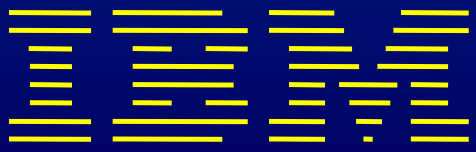
IBM Microelectronics



A High Performance C4 Probe: TFI™

AGENDA

- Introducing IBM's Advanced C4 Probe Technology
- Development Background
- Technology Description
- Application & Use
- Interface Requirements
- Performance
- Summary

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Introduction

- IBM's Advanced C4 Probe Technology TFI (Thin Flexible Interposer)
  - Collaborative Effort Between IBM Sites
  - SWTW: First Public Report
    - Provide Awareness to Probe Community
  - Patented Technology

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Development Background

- Traditional C4 Area Array Probes: Inadequate for Escalating Technical Demands
  - High End Semiconductors
    - Tighter Pitch
    - Large # of I/O's
    - Higher Power & di/dt
    - Higher Frequency

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Technology Description

- TFI Probe System
  - Interface Pellicle Probe (IPP)
  - Multi-Layer Ceramic Space Transformer (MLC SXF)
    - With Pedestal
  - Fixturing
  - Printed Circuit Board (PCB)

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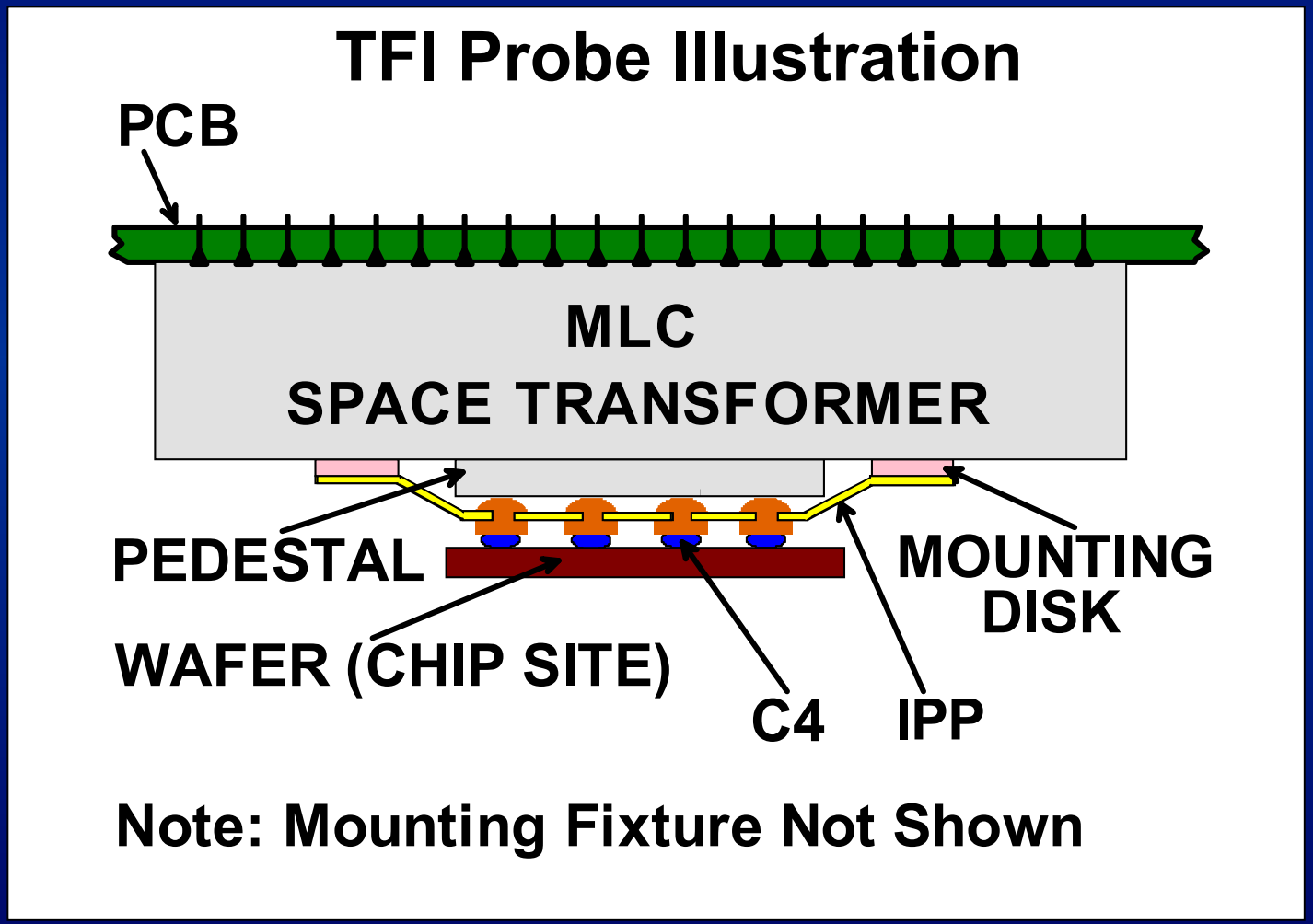
Technology Description



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Technology Description

- IPP - Interface Pellicle Probe
  - Probing/Contact Element
    - Vertical & Rigid Probe
  - Array of Copper Studs On a Plated Polyimide Film
    - Protective Metallurgy
  - Copper Studs Match Device Footprint
  - Photolithographically Defined
    - Auto-Sculpted
  - Diverse Densities and Configurations

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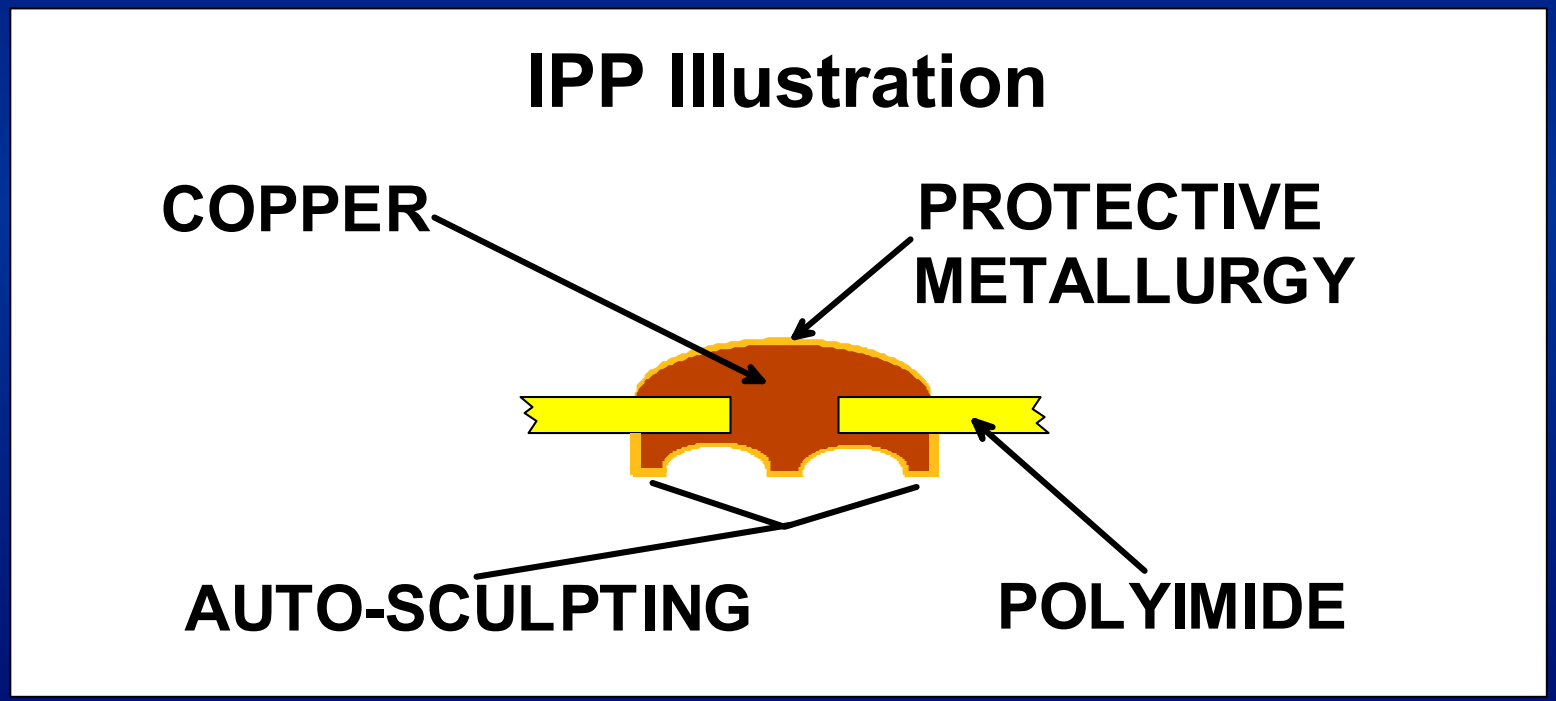
Technology Description



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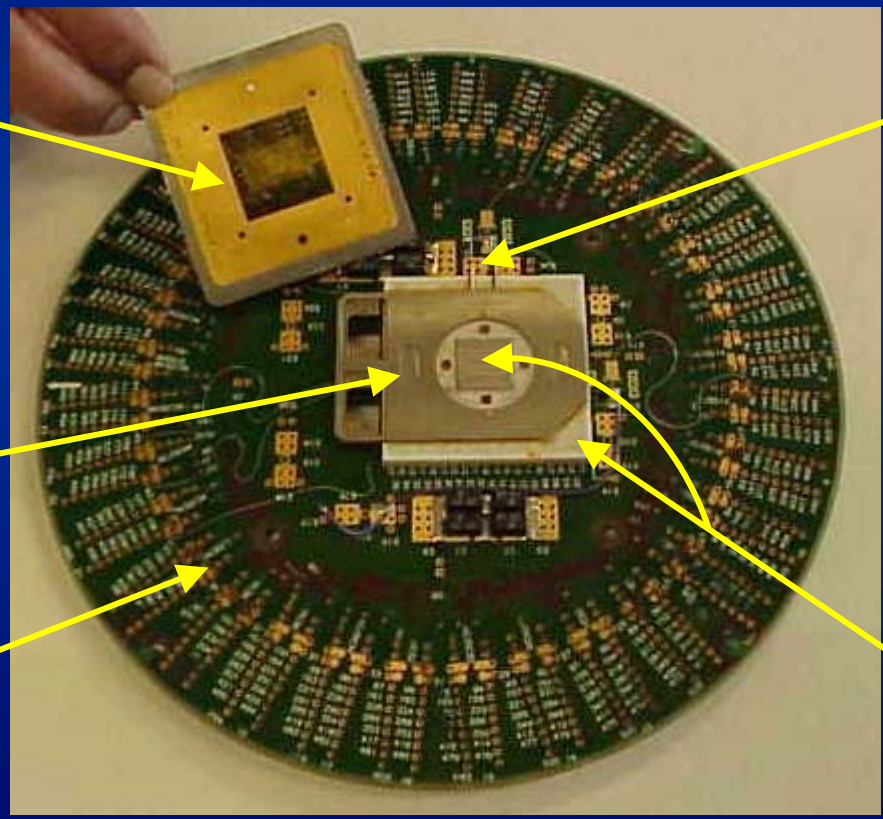
Technology Description

TFI Probe



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Technology Description

- How Does it Work?
  - Precision Assembly & Alignment to PCB
  - Vacuum Mounted IPP
    - Installation & Alignment Ease
  - Sculpting
    - Low Contact Force/Resistance
    - Minimize PbSn 'Pick-up'
    - C4 Reflow Integrity
  - C4 'Compliance'

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Application and Use

- C4 Bumps
- Single DUT
- High Power / High Frequency / di/dt
- Very High Pin Count Area Array
  - Layout Independent
  - >/= 4 on 8 Pitch

High End Logic / ASICS

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Application and Use

- **Experience in IBM**
  - **Initial Probe Fixture Set-up Precision**
    - **Prober**
    - **Test Head**
  - **Multiple Tester & Prober Platforms**
    - **HP, Advantest, Teradyne, etc….**
    - **TEL, E-Glas, etc…...**
  - **Manufacturing Use**
    - **Thousands of Wafers; Many Diverse P/N's**
    - **8mm to 25mm Chips**

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Requirements

- Wafer / TFI Co-Planarity: +/- 0.2 mils
- C4 to Probe Misalignment: +/- 2.0 mils
- Chuck Tilt: +/- 0.2 mils
- Vacuum: 20 inches

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Performance

- Probe Force: 2 - 5 Grams/Pad
- Overdrive: 2 - 5 mils
- Inductance: 20 pH
- Bandwidth: 3db @ 20+ GHz)
- Temperature: - 55c to 85c
- Dimensionally Scalable
  - Pitch, I/O Count & Layout

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Performance

- C4 Bump (PbSn)
  - Evaporated
  - Plated
- Cleaning
  - On-line: Brush
  - Off-line: Chemical and/or Brush
- No Tweaking
  - Limits Metrology Tool Need

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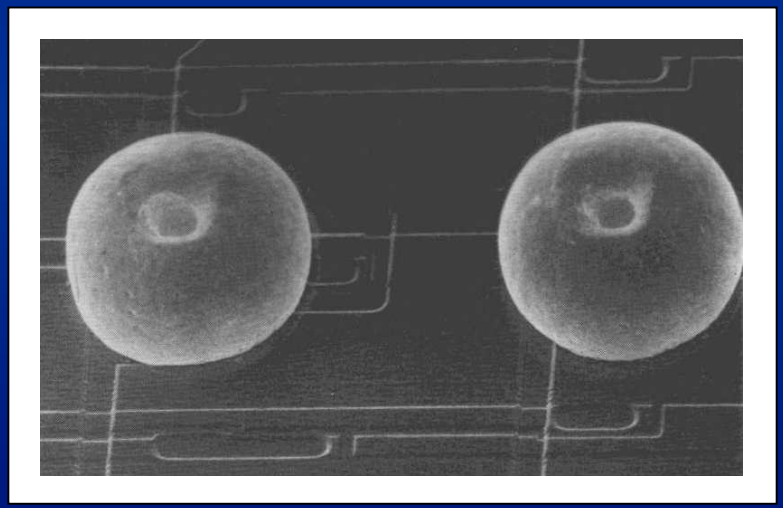
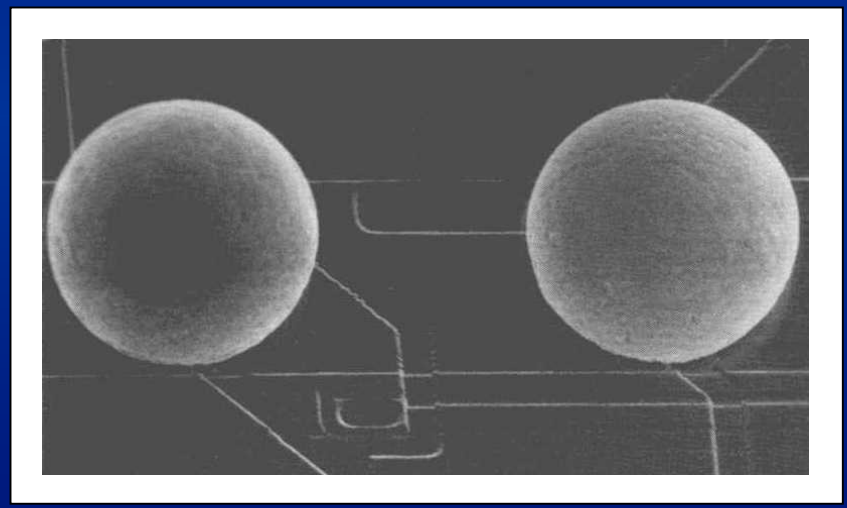
Performance

- **Reflow: C4 Integrity**



Post Probing



Post Reflow

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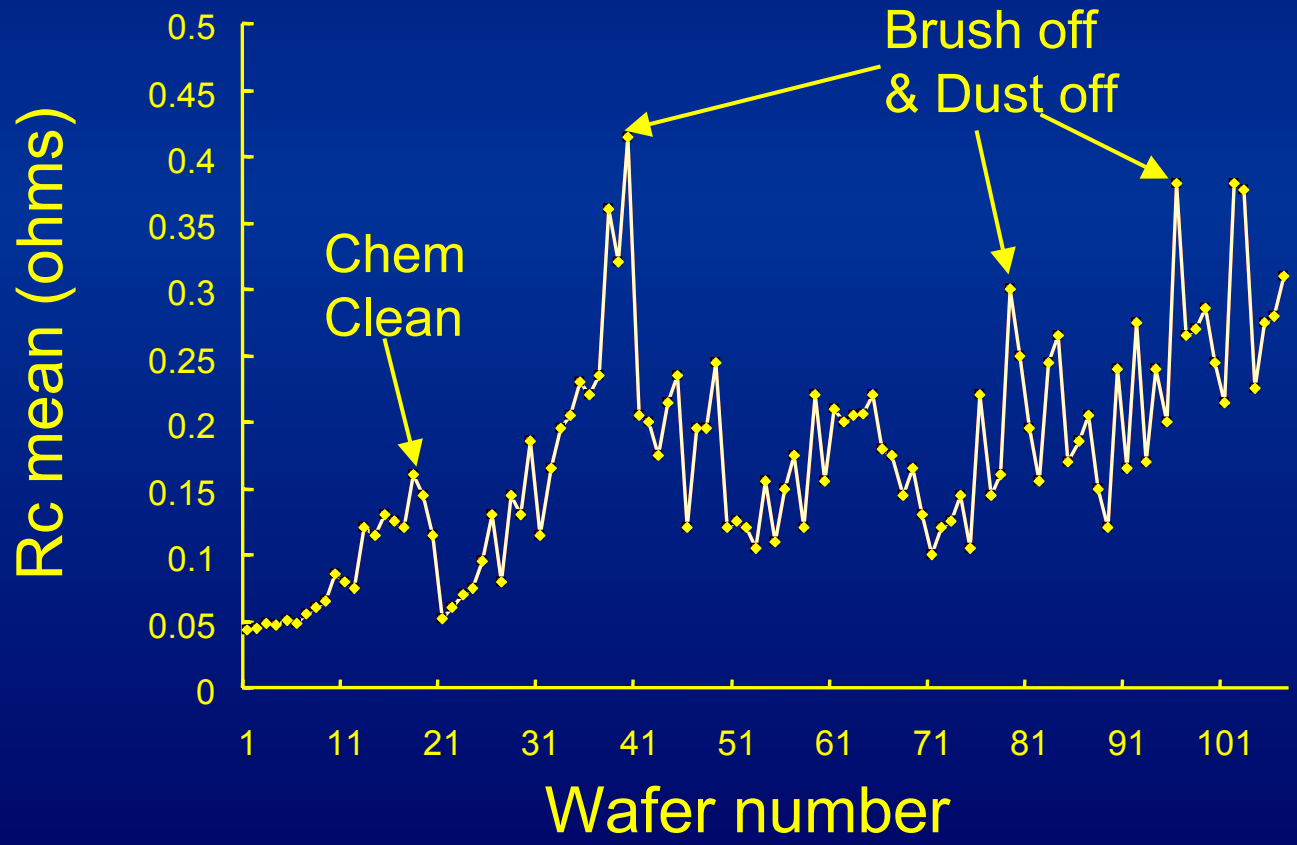
Performance

- **Contact Resistance**



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Summary

- TFI: A New IBM C4 Probe Technology
  - Addresses High Performance Demands
  - Implemented in Wafer Test Manufacturing
  - Scalable For The Future

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