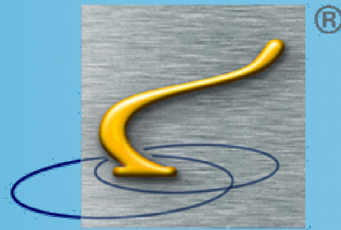

High Parallelism Memory Test Advances based on MicroSpring™ Contact Technology

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Robert Martin – Technical Sales Eng.

Southwest Test Workshop

June 2001

FormFactor

Contents

- Introduction to FormFactor
- FormFactor Mission
- 100 mm Four Touchdown Probe Solution
  - Cost of Ownership
  - Specifications
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    - Electrical
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FormFactor

Introduction to FormFactor

FormFactor

- Established 1993
- Livermore, CA
- 325 Employees

WaferProbe™ Probe Card Products

- PH50, PH75 and new PH100
- T1/T2.1 MicroSpring™ contact technology
- High parallelism memory and C4 probing

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FormFactor Mission

Reduce the cost of test through:

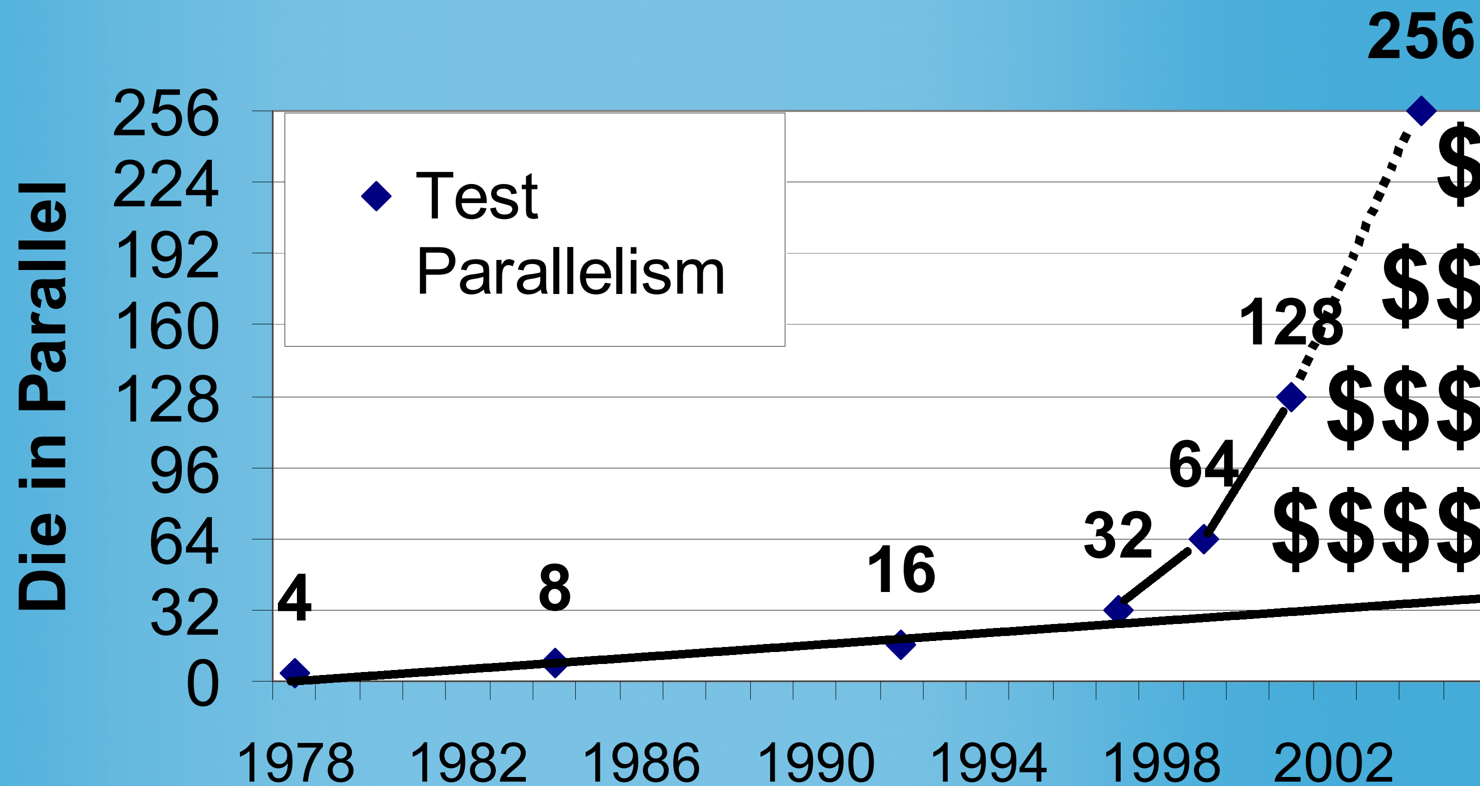
- Increased parallelism
- Improved productivity
- Reduced maintenance and cleaning

Meet new technology needs:

- Reduced pad size and pitch
- Improved electrical and mechanical performance
- Support new tester platforms

Extend technology developed for DRAM to provide solutions for FLASH and logic probing

Trends in High Parallelism Probing



Test Cost of Ownership Analysis

8" Virtual FAB - 25,000 wafer starts per month

Product - 128M SDRAM

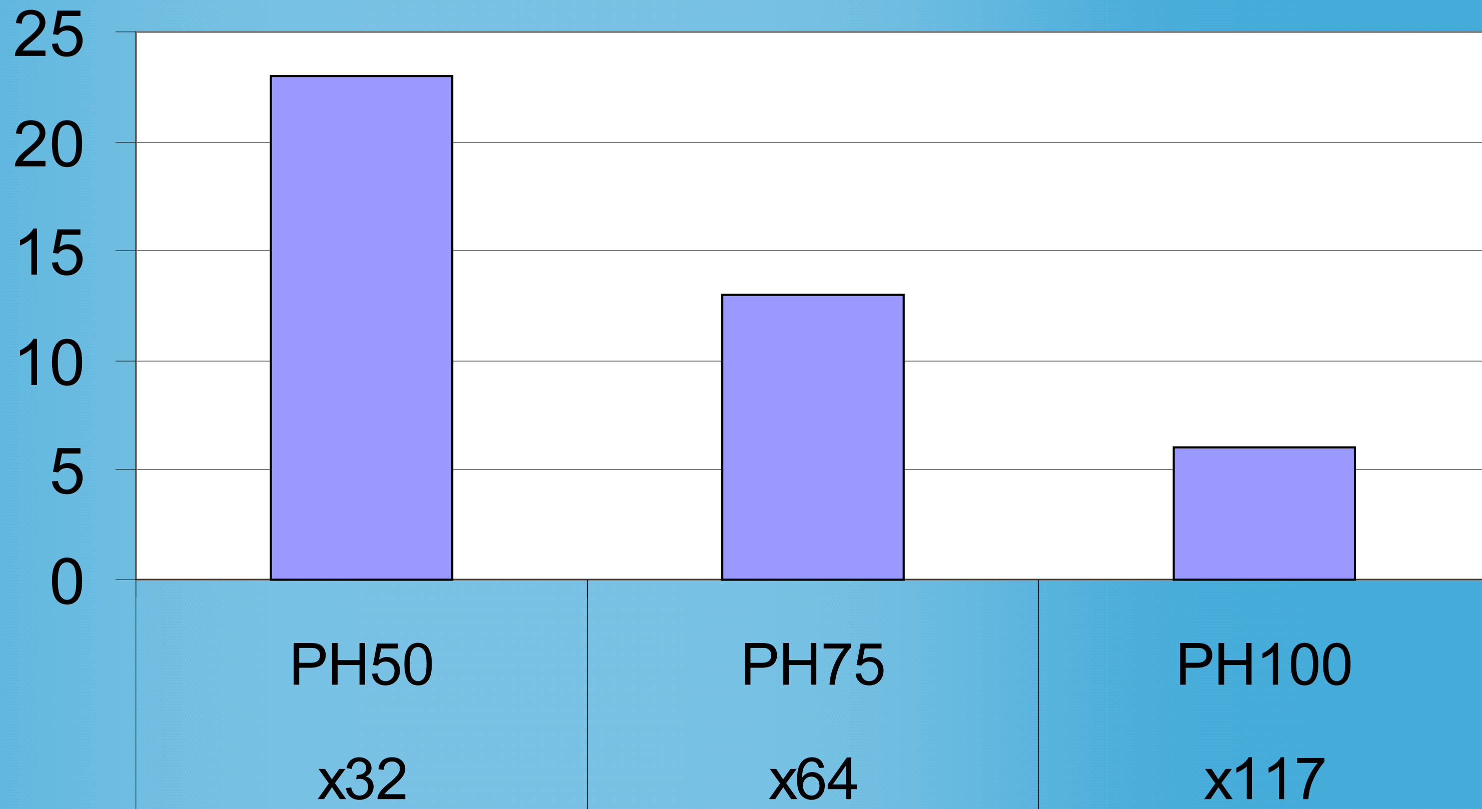
- Good Die Value = $4
- Die Size = $50mm^2$

Test time increases 15% per 2x test parallelism

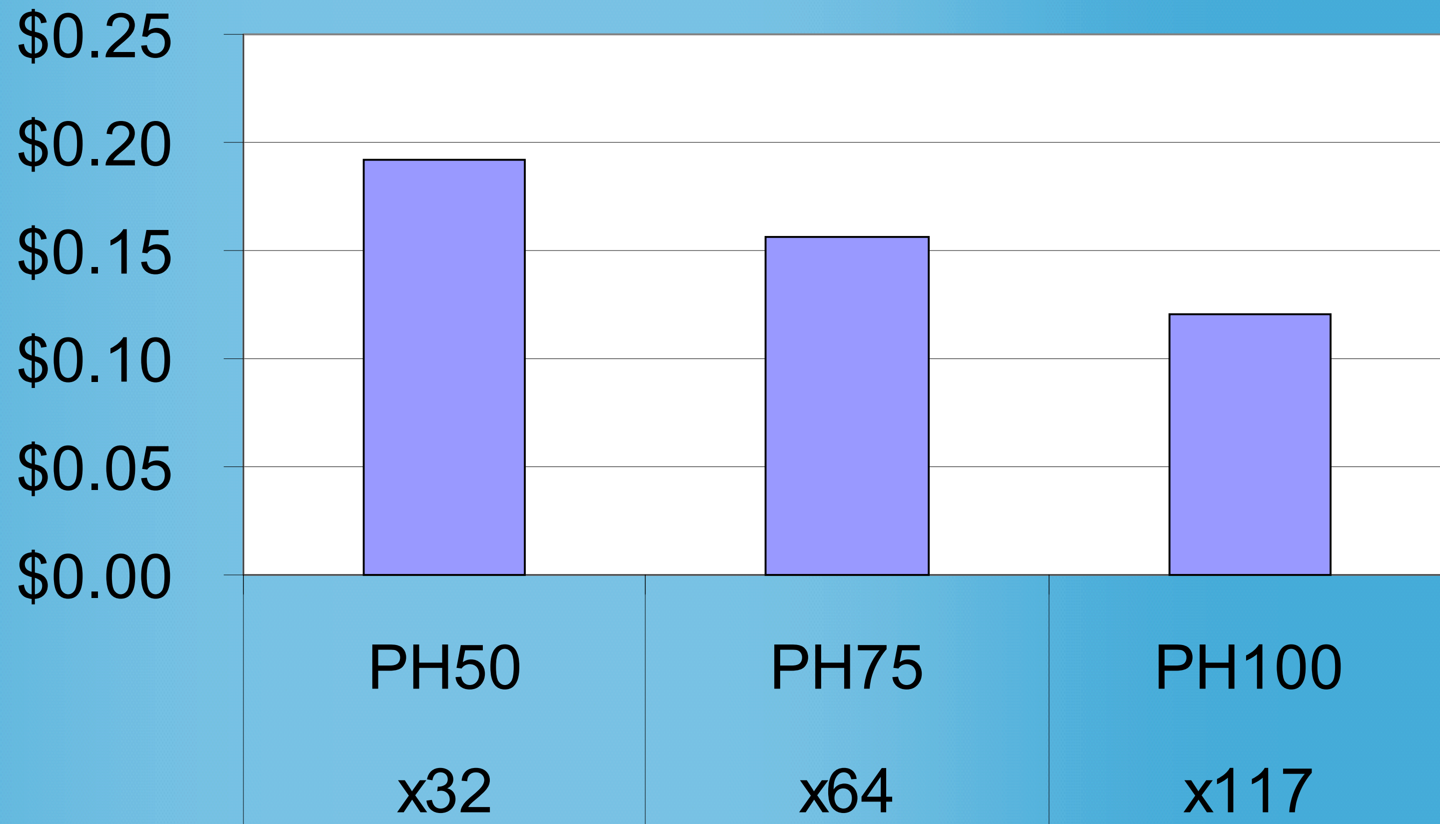
Compare the following situations:

Test Parallelism	32 DUT	64 DUT	117 DUT
Tester Cost	$1.8M	$2.2M	$3.5M

High Parallelism Probing – Reduces Touchdowns required



High Parallelism Probing – Reduces Test Cost per DUT



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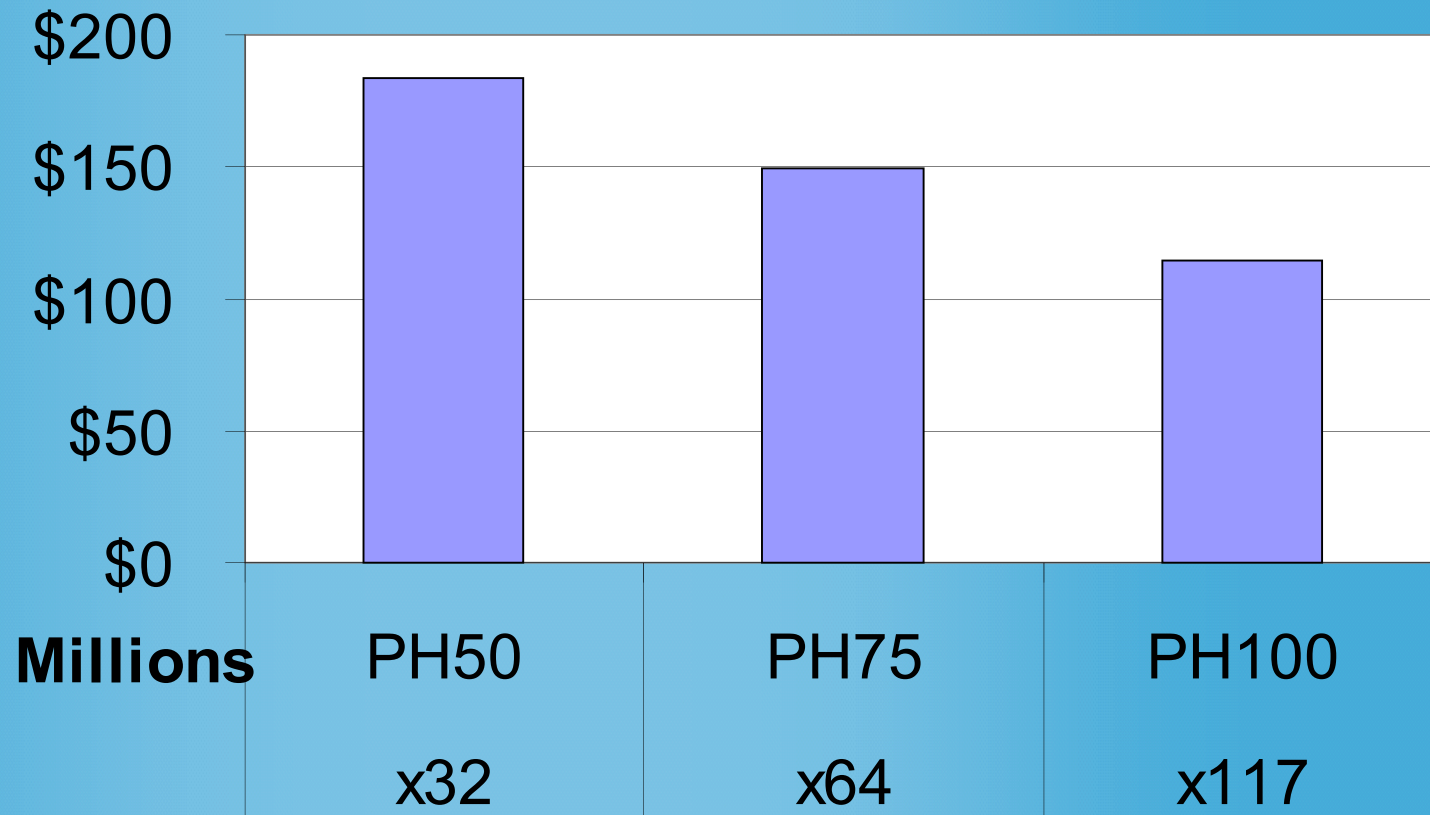
High Parallelism Probing – Delivers Overall Cost Savings



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PH100 - 4 Touchdown Solution:

Spring Technology and Active Area:

- T1 - 105 mm x 110 mm
- T2.1 – 112 mm array diagonal
- Planarity < 38 microns across array
- Both support:
  - Lead on center and edge pad designs
  - Odd # of rows and columns

FORMFACTOR

PH100 - 4 Touchdown Solution:

Probe Head:

- Multilayer ceramic
- 7544 I/O resources
- Supports maximum resources of Probe One and T5375
- x128 test parallelism possible

MicroSpring™ Test Interface System

Controlled impedance PCB

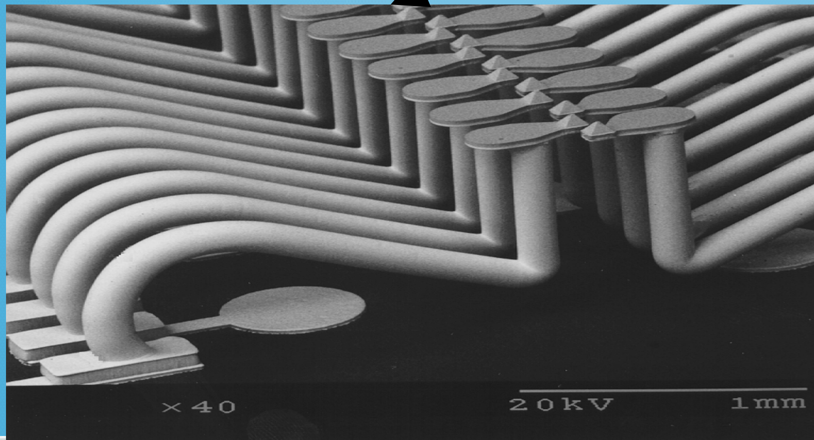
Planarizers

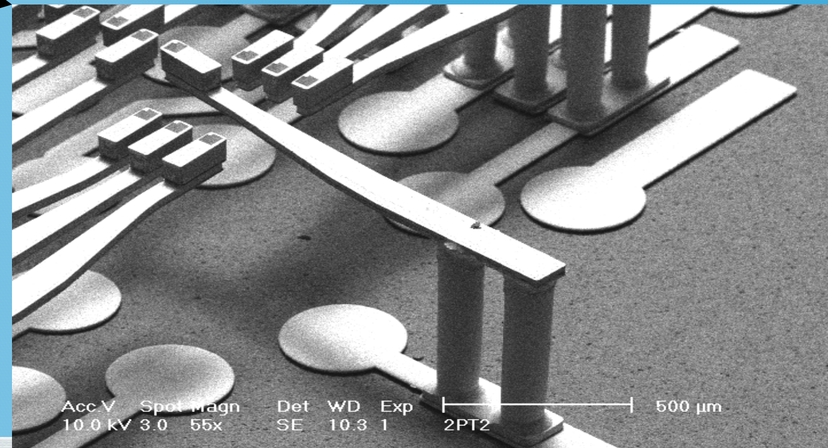
Resilient Microspring Interposer

Space transformer with Microspring™ probes

T1 Probe Array

T2.1 Probe Array





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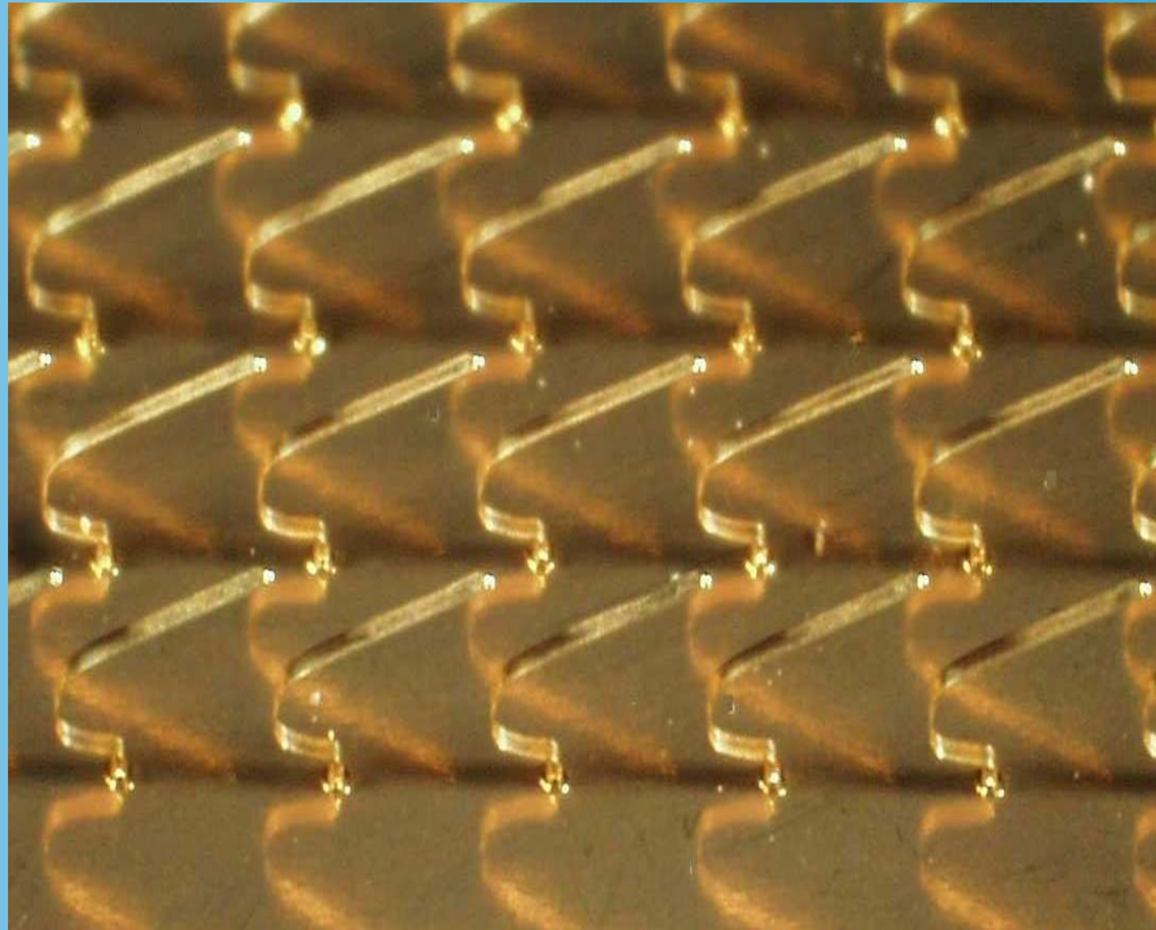
MicroSpring™ Interposer

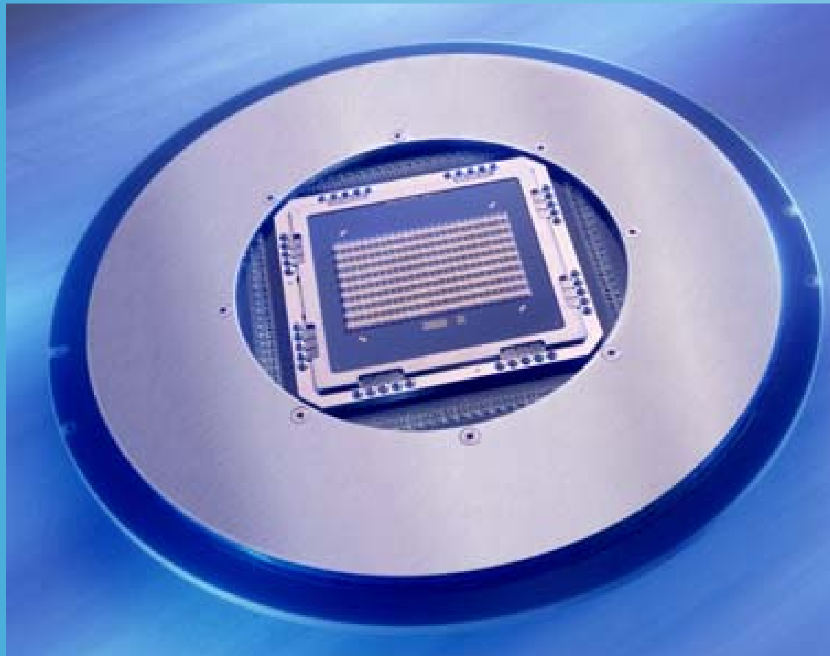
Printed circuit board to ceramic interface

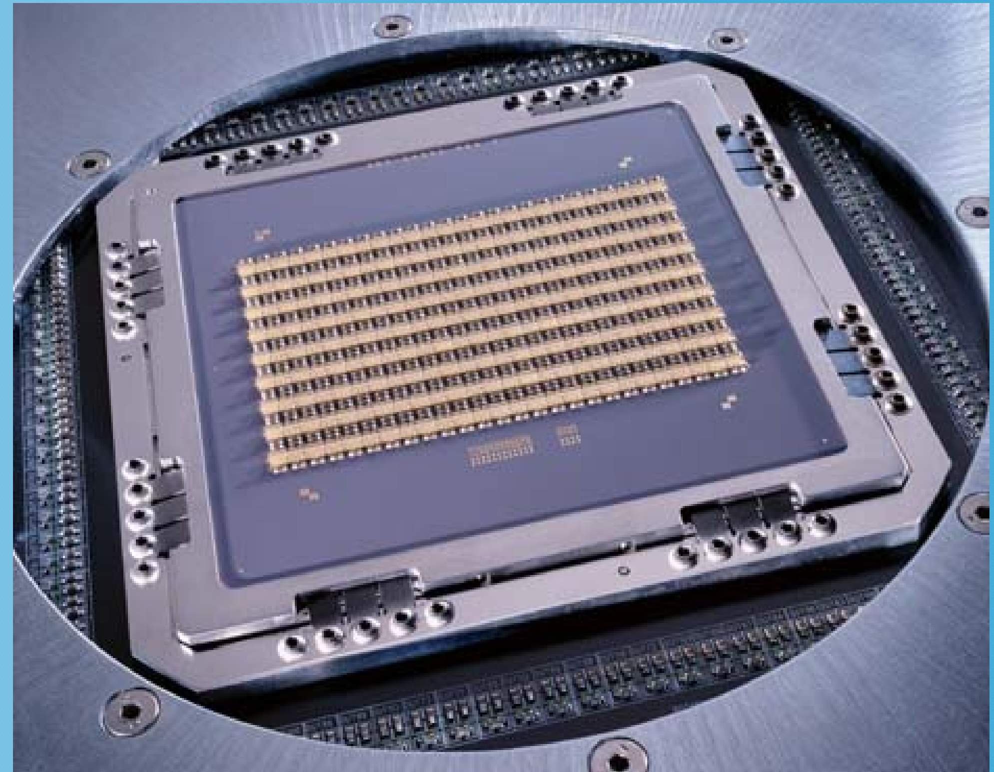
Wide range of compliance

Capable of 15 mil adjustment range



PH100 - 117 DUTs, 128M SDRAM





MicroSpring™ Array Performance

Measured on the API $PRVX_2$

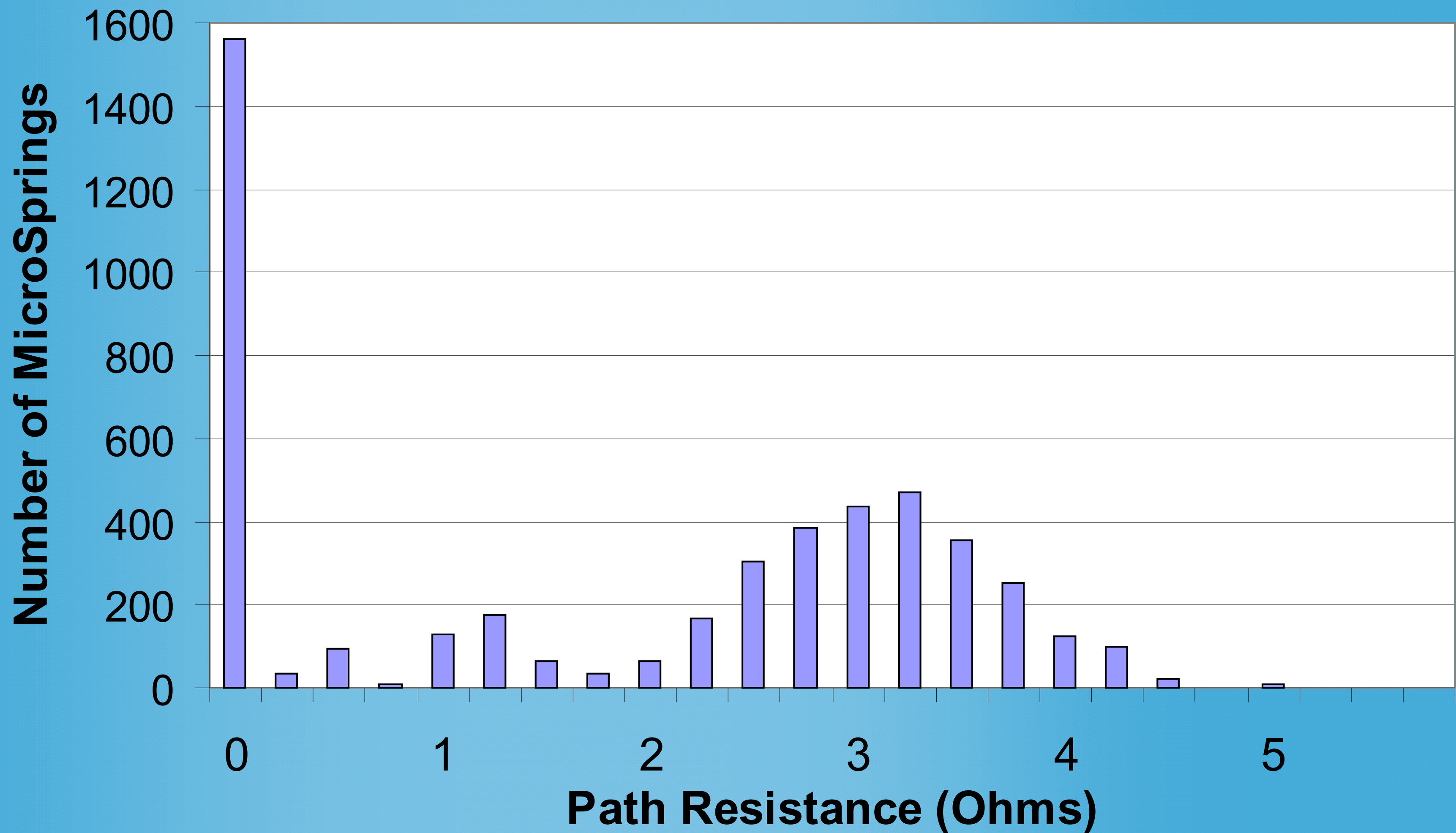
- Electrical Performance -C(res)
- Alignment and planarity of x117 array

Scrub Mark Verification on API wafer WoRx

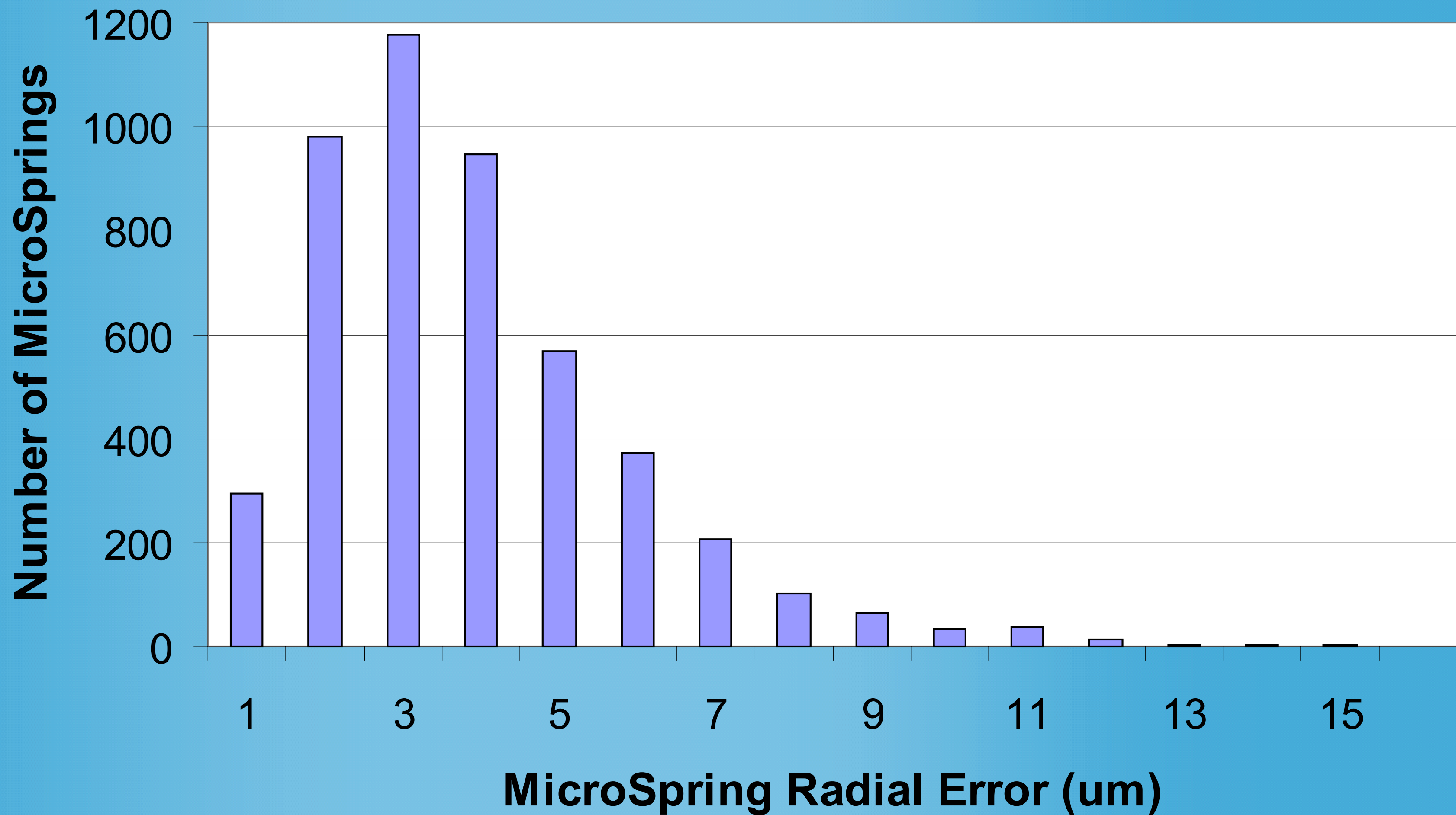
- Alignment across array at 25 and 88C

4797 MicroSprings were measured on API $PRVX_2$

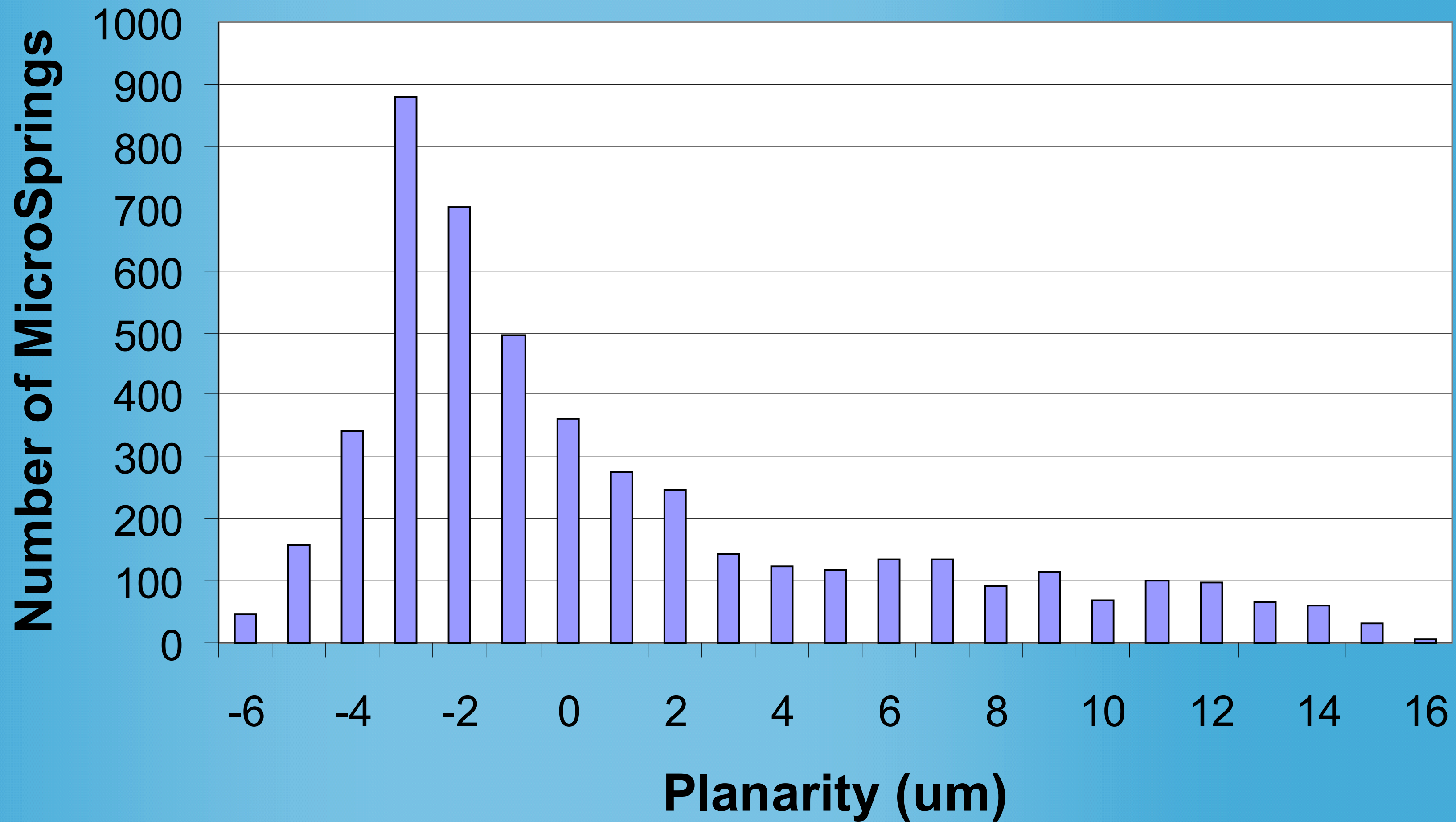
PH100 Path Resistance



PH100 Alignment Error from Pad Center



PH100 Planarity



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Scrub Alignment vs. Temperature

Scrub mark alignment

Distance from center of pad to center of scrub

API waferWorx:

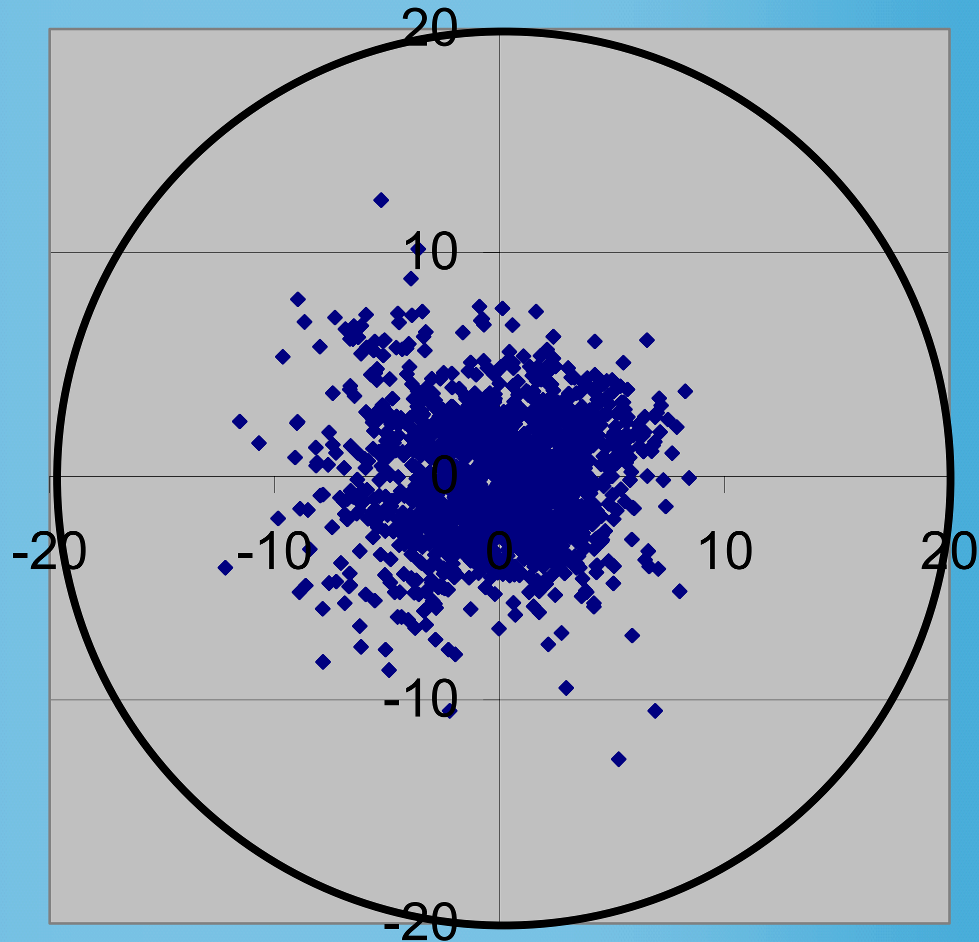
1170 Duts x 42 pads/DUT = 49,140 scrub marks

3 wafers probed at 25°C and 88°C

Delta scrub alignment 25°C vs. 88°C

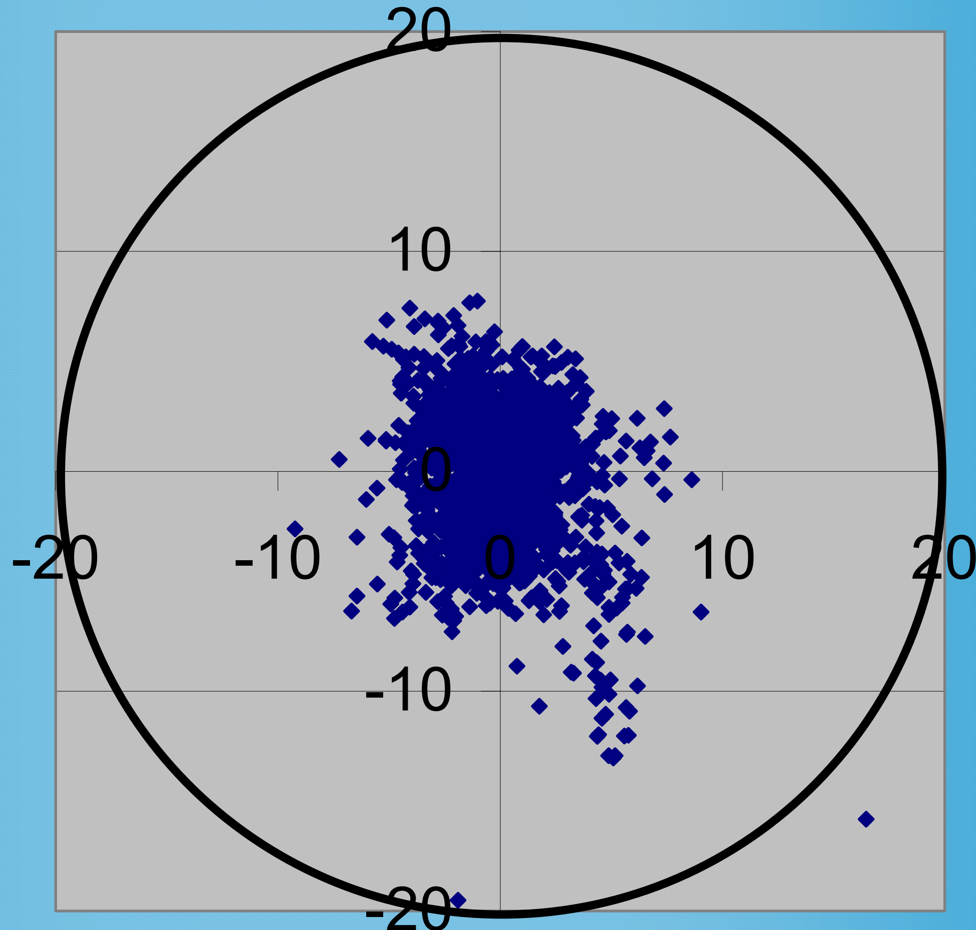
Scrub Alignment at 25°C

Scrub Position at Ambient - Prober Error Removed



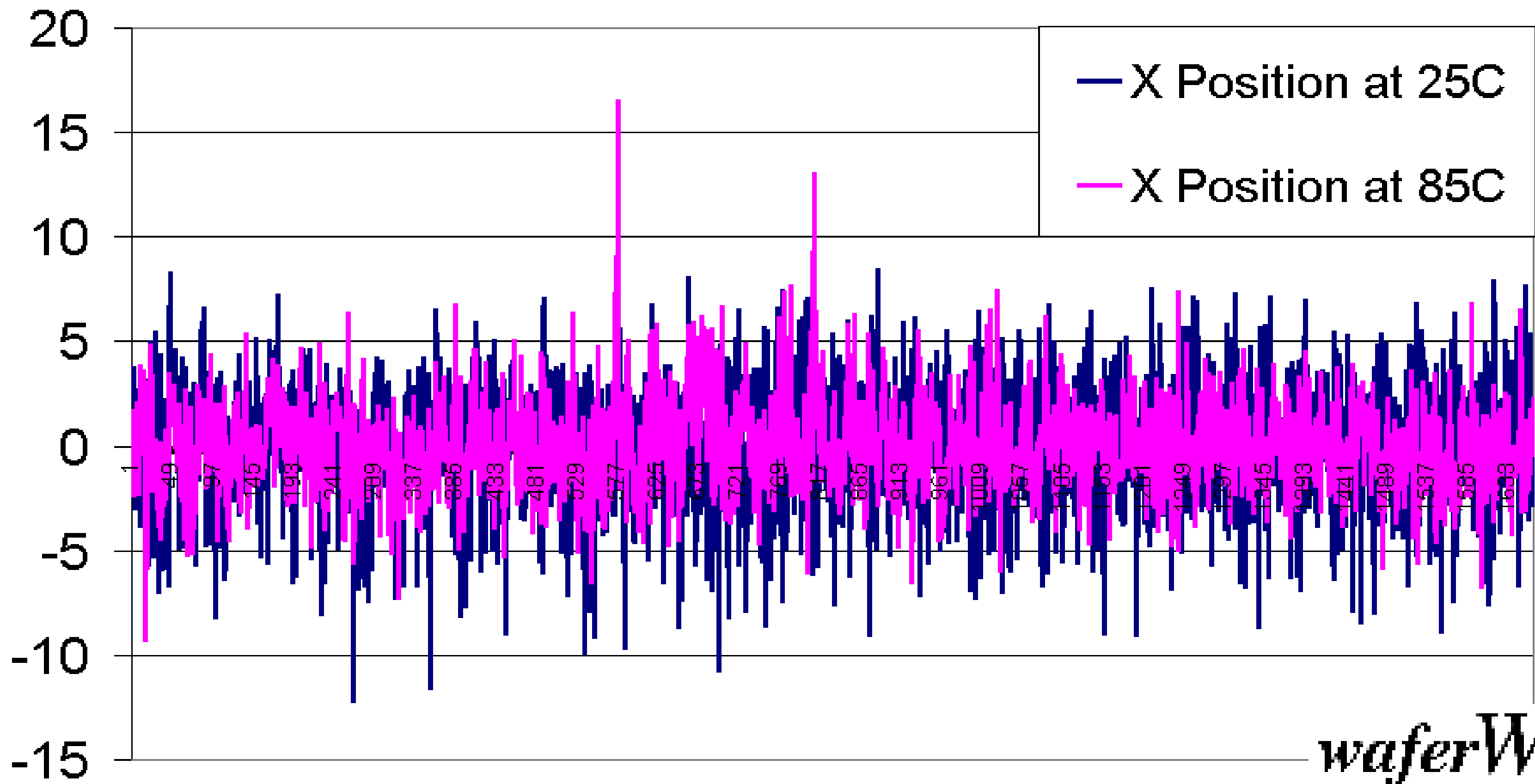
waferWoRx™

Scrub Alignment at 88°C



waferWoRx™

Delta Scrub Alignment 25°C to 88°C



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Summary and Conclusions

Increases in parallelism significantly reduce overall cost of test

MicroSpring™ technology is capable of supporting large, high pin count, array areas

FormFactor's PH100 will support the next generation of high parallelism probe arrays while maintaining stability over time and temperature

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Special Thanks

Alec Gomez – Teradyne

Touchdowns on x117 PC

John Strom – API

WaferWorx analysis

Chris Buckholtz – FormFactor

Experiment support