An integrated solution for KGD:
At-speed wafer-level testing
and
full-contact wafer-level burn-in
after flip chip bumping

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TD center
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Outline

• Purpose of the study
• ChipMOS KGD integrated solutions
• Cost issues
• Challenges
• Applications and future development
• Conclusion
Purpose of the study

• An integrated solution for KGD.
• The shortest process flow for IC backend processing.
• The lower total backend processing cost.
• Meet the demand of high speed/ high frequency and light, thin, short, and small hand-held applications.
• Meet the future trend of continuous process shrink and 300mm technologies.
Known Good Dies

- KGD are bare dies or “bumped dies” without any traditional packaging.
- KGD must
  - Pass all back-end testing.
  - Pass burn-in processes
  - After redundancy repair on memory IC.
  - Guarantee for “GOOD” functions
  - Ready for applications, such as MCP, MCM, FCOB, 3D CSP, SOP, …etc.
ChipMOS KGD solutions

- All testing after flip chip bumping
- At-speed wafer-level testing
- No probed mark testing
- Full-contact wafer-level burn-in
- Redundancy repair after flip chip bumping and wafer-level burn-in
- FCOB memory modules
Major process flow (1)

Bumping → WLBI → WLT1 → Laser → WLT2

Before bumping

Flip chip process flow:
• Design
• (1st passivation)
• Metal trace patterning
• Metal trace deposition
• 2nd passivation
• Bump base opening
• UBM deposition
• Bump patterning
• Bump deposition
• UBM etching
• Reflow

After bumping
Major process flow (2)

Bumping → WLBI → WLT1 → Laser → WLT2

Full contact wafer-level burn-in:

Resource: Courtesy of TEL.
Major process flow (3)

**Bumping** → **WLBI** → **WLT1** → **Laser** → **WLT2**

**Testing condition:**
- **WLT1:**
  - At-speed
  - High temp
  - MRA
- **WLT2:**
  - Room temp or cold temp

(Vertical Probe card)
(Bumped wafer)
(Chuck)
Major process flow (4)

Bumping → WLBI → WLT1 → Laser → WLT2

Before laser repair

During laser repair

(Bumped die)
All testing after flip chip bumping

<table>
<thead>
<tr>
<th>TSOP II</th>
<th>Flip chip</th>
<th>ChipMOS solutions</th>
</tr>
</thead>
<tbody>
<tr>
<td>* W/S 1</td>
<td>* W/S 1</td>
<td>* Bumping</td>
</tr>
<tr>
<td>* Laser repair</td>
<td>* Laser repair</td>
<td>* WLBI</td>
</tr>
<tr>
<td>* W/S 2</td>
<td>* W/S 2</td>
<td>* Die-level FT 1</td>
</tr>
<tr>
<td>* Assembly</td>
<td>* Bumping</td>
<td>* WLT 1</td>
</tr>
<tr>
<td>* FT 1</td>
<td>* Die-level FT 1</td>
<td>* Laser repair</td>
</tr>
<tr>
<td>* B/I</td>
<td>* Die-level B/I</td>
<td></td>
</tr>
<tr>
<td>* FT 2</td>
<td>* Die-level FT 2</td>
<td>* WLT 2</td>
</tr>
<tr>
<td>* Laser marking</td>
<td>* Laser marking</td>
<td>* Wafer saw</td>
</tr>
<tr>
<td>* FT 3</td>
<td>* Die-level FT 3</td>
<td>* Laser marking</td>
</tr>
<tr>
<td>* Inspect/reform</td>
<td>* Inspect/reflow</td>
<td>* Inspect</td>
</tr>
</tbody>
</table>

The shortest backend process flow!
All testing after flip chip bumping

• Benefits:
  – Shortest processes flow
  – Lower backend cost
    • No investment for FT1, FT2, and FT3.
  – Minimum turn around time for backend processes.
  – Reduce the impact of probe cards pitch limitation by I/O redistribution.
  – Lower backend cost for process shrink/ 300mm technologies.

Bumping >> WLBI >> WLT 1 >> Laser >> WLT 2
At-speed wafer-level testing

• Benefits:
  – Yield gain for laser repair

At lower speed:
  • Some G become R
  • Some G become B
  • Some R become B

Higher speed testing
  • Some G become R
  • Some G become B
  • Some R become B

WS1/ WLT1
At-speed testing
Final yield

Yield gain
Laser
At-speed wafer-level testing

• Benefits:
  – Higher throughput

Description:

• 64M SDRAM and 1 lot of wafers (25 wafers) was tested at 30 MHz, 50 MHz, and 100 MHz.

• Once the wafer tested, the package test was performed to compare the yield data.

• Customers see the improved throughput and yield when test speed is increased.

• Probe-One has scalable capture speed up to 250 MHz.
No probed marks testing

• Benefits:
  – No extra cost in making testing bumps.
  – No impact of probe marks on Al pads or flip chip bumps.
  – Reliability improvement in packages/ modules assembly.
Full-contact wafer-level burn-in

• Benefits:
  – More cost effective
    • for process shrink
    • for 300mm technologies

• Comparison:

<table>
<thead>
<tr>
<th>Items</th>
<th>Solutions</th>
<th>Advantages</th>
<th>Disadvantages</th>
</tr>
</thead>
<tbody>
<tr>
<td>Built-in circuit</td>
<td>Traditional probe card</td>
<td>Low cost</td>
<td>Extra wafer area for built-in circuits</td>
</tr>
<tr>
<td></td>
<td>Tester/prober</td>
<td>High throughput</td>
<td>B/I cells only</td>
</tr>
<tr>
<td>Full wafer contact</td>
<td>Special contact board</td>
<td>Good B/I quality</td>
<td>High cost</td>
</tr>
<tr>
<td></td>
<td>WLBI oven system</td>
<td>Cost effective</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Process shrink</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>300mm technologies</td>
<td></td>
</tr>
</tbody>
</table>
Redundancy repair after FCB/ WLBI

- Benefit:
  - Yield gain for laser repair

<table>
<thead>
<tr>
<th>During B/I</th>
<th>Laser before B/I</th>
<th>Laser after B/I</th>
</tr>
</thead>
<tbody>
<tr>
<td>● Passed &gt;&gt; Passed</td>
<td>● Passed</td>
<td>● Passed</td>
</tr>
<tr>
<td>● Passed &gt;&gt; Repairable</td>
<td>● Failed</td>
<td>● Passed</td>
</tr>
<tr>
<td>● Passed &gt;&gt; Failed</td>
<td>● Failed</td>
<td>● Failed</td>
</tr>
</tbody>
</table>
**Electrical simulation of FCOB**

**Condition:**
- **Software:** ANSOFT Maxwell Spicelink V4.5/ AutoCAD
- **Module:** Boundary Element Method Quick 3D Parameter Extractor
- **Method:** Quasi-TEM Method

**AutoCAD 2D Outline Drawing/ Maxwell 3D Package Module**

(A partial drawing showing the longest traces)

<table>
<thead>
<tr>
<th>Items</th>
<th>(L_s) (nH)</th>
<th>(L_m) (nH)</th>
<th>(C_L) (pF)</th>
<th>(C_m) (pF)</th>
<th>(R) (mΩ)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Max</td>
<td>Min</td>
<td>Max</td>
<td>Min</td>
<td>Max</td>
</tr>
<tr>
<td>TSOP II*</td>
<td>7.603</td>
<td>4.090</td>
<td>4.682</td>
<td>2.249</td>
<td>1.487</td>
</tr>
<tr>
<td>FCOB**</td>
<td>1.600</td>
<td>0.734</td>
<td>0.299</td>
<td>0.250</td>
<td>0.100</td>
</tr>
<tr>
<td>Ratio***</td>
<td>4.75</td>
<td>5.57</td>
<td>15.6</td>
<td>6.00</td>
<td>9.00</td>
</tr>
</tbody>
</table>

*: From pad to lead, including gold wire without considering the effect of the die.
**: From pad to bump including traces without considering the effect of the die.
***: FCOB as 1.
Footprint comparison of FCOB

• With same memory capacity:

<table>
<thead>
<tr>
<th>Items</th>
<th>Width (mm)</th>
<th>Length (mm)</th>
<th>Height (mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>TSOP II</td>
<td>11.76</td>
<td>22.23</td>
<td>1.2</td>
</tr>
<tr>
<td>Flip chip bumped die</td>
<td>4.83</td>
<td>9.25</td>
<td>0.737</td>
</tr>
</tbody>
</table>

Footprint ratio: **1 to 5.85**

• Same footprint (SO-DIMM):

**Memory capacity ratio:** **2 : 1**

Note: Use 0.20μm 64Mb SDRAM as examples.
Flip chip bumping vs. TSOP II

Flip chip bumping cost =
\[ f(\text{bumping, gross dies, wafer yield}) \]

**Assumptions:**
- Wafer yield: 90%
- Bumping: 200USD/ wafer
- Gross dies:

<table>
<thead>
<tr>
<th>Process(μm)</th>
<th>Gross die</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.25</td>
<td>500</td>
</tr>
<tr>
<td>0.20</td>
<td>600</td>
</tr>
<tr>
<td>0.17</td>
<td>1,000</td>
</tr>
</tbody>
</table>
Wafer-level testing vs. TSOP II

Wafer-level testing cost =
\[ f(\text{equipment, testing steps, throughput, wafer yield}) \]

Assumptions:
- Gross die: 600
- TSOP II:
  - W/S 1, W/S 2, FT 1/2/3
- WLT:
  - WLT1, WLT2
- Wafer yield: 90%
- Probing efficiency: 80%
- Cost per die: 5US$
- Throughput gain & yield gain:

<table>
<thead>
<tr>
<th>Testing speed</th>
<th>Throughput gain gain</th>
<th>Yield gain TSOP II</th>
<th>Flip chip</th>
</tr>
</thead>
<tbody>
<tr>
<td>30MHz</td>
<td>0%</td>
<td>0%</td>
<td>0%</td>
</tr>
<tr>
<td>50MHz</td>
<td>15%</td>
<td>0%</td>
<td>1.5%</td>
</tr>
<tr>
<td>100MHz</td>
<td>30%</td>
<td>0%</td>
<td>3.0%</td>
</tr>
</tbody>
</table>
Wafer-level B/I vs. TSOP II

Wafer-level burn-in cost =
\[ f(\text{equipment, gross dies, wafer yield, yield gain, die cost}) \]

Assumptions:
- Burn-in time: 24 hours
- Wafer yield: 90%
- Cost per die: 5 US$
- Oven capacity: 13 wafers
- Gross dies:

<table>
<thead>
<tr>
<th>Process (µm)</th>
<th>Gross die</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.25</td>
<td>500</td>
</tr>
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<td>0.20</td>
<td>600</td>
</tr>
<tr>
<td>0.17</td>
<td>1,000</td>
</tr>
</tbody>
</table>
Challenges (1)

- Flip chip bumping & I/O redistribution:
  - RLC for bumping and I/O redistribution design.
  - Possible defects caused by wafer saw

- At-speed wafer-level testing
  - Probe cards design for high speed applications.
  - Accuracy of tester during high speed testing.
  - Memory repair analysis during high-speed testing
Challenges (2)

- No probed mark testing
  - RLC effects of testing bumps and traces.
  - The impact of testing bumps during assembly.
- Full-contact wafer-level burn-in:
  - Number of contact points per wafer.
  - Contact quality
  - Contact coplanarity
  - CTE matching
  - Circuit isolation
Challenges (3)

• **Redundancy repair after FCB/ WLBI:**
  – Protection of fuses during FCB
  – Reliability of opened laser windows during package/module assembly

• **FCOB memory modules:**
  – KGD issues
  – Pitch limitation of module PCB.
  – Reliability of FCOB.
    • Warpage of PCB during module assembly.
    • Accuracy of die attach
    • Underfill processes on modules.
## Applications and future development

<table>
<thead>
<tr>
<th>Applications</th>
<th>Current</th>
<th>Phase 2</th>
<th>Phase 3</th>
<th>Phase 4</th>
<th>Phase 5</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>KGD type</strong></td>
<td>Bumped</td>
<td>Al pad</td>
<td>Cu pad</td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Devices</strong></td>
<td>High speed memory</td>
<td>Other memory</td>
<td>Logic</td>
<td>CPU</td>
<td>BIST</td>
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<tr>
<td></td>
<td></td>
<td></td>
<td>ASIC</td>
<td>DSP</td>
<td>Embedded</td>
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<td></td>
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<td></td>
<td></td>
<td>SOC</td>
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<tr>
<td><strong>Packaging</strong></td>
<td>MCP</td>
<td>3D CSP</td>
<td>SOP</td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Module assembly</strong></td>
<td>MCM</td>
<td>FCOB MCM</td>
<td>FCOB SOM</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Note:**
1. Current device/ packaging/ module: DDR SDRAM.
2. **SOP**: System On Package, the best alternative for SOC.
Conclusions

- ChipMOS KGD integrated solutions:

<table>
<thead>
<tr>
<th>Key factors</th>
<th>Wafer yield increase</th>
<th>Process shrink</th>
<th>200mm to 300mm</th>
<th>Throughput gain due to at-speed WLT</th>
<th>Yield gain due to at-speed WLT</th>
<th>Yield gain due to laser repair after FCB/WLBI</th>
<th>Yield gain due to better market prices</th>
</tr>
</thead>
<tbody>
<tr>
<td>Total backend cost per die</td>
<td></td>
<td></td>
<td></td>
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<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>TSOP II</td>
<td></td>
<td></td>
<td></td>
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<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>KGD</td>
<td></td>
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</tr>
</tbody>
</table>
Questions & discussions