An integrated solution for KGD:

At-speed wafer-level testing and full-contact wafer-level burn-in after flip chip bumping

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Outline

- Purpose of the study
- ChipMOS KGD integrated solutions
- Cost issues
- Challenges
- Applications and future development
- Conclusion

Purpose of the study

- An integrated solution for KGD.
- The shortest process flow for IC backend processing.
- The lower total backend processing cost.
- Meet the demand of high speed/ high frequency and light, thin, short, and small hand-held applications.
- Meet the future trend of continuous process shrink and 300mm technologies.

Known Good Dies

- KGD are bare dies or “bumped dies” without any traditional packaging.
- KGD must
  - Pass all back-end testing.
  - Pass burn-in processes
  - After redundancy repair on memory IC.
  - Guarantee for “GOOD” functions
  - Ready for applications, such as MCP, MCM, FCOB, 3D CSP, SOP, …etc.

ChipMOS KGD solutions

- All testing after flip chip bumping
- At-speed wafer-level testing
- No probed mark testing
- Full-contact wafer-level burn-in
- Redundancy repair after flip chip bumping and wafer-level burn-in
- FCOB memory modules

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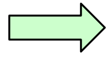
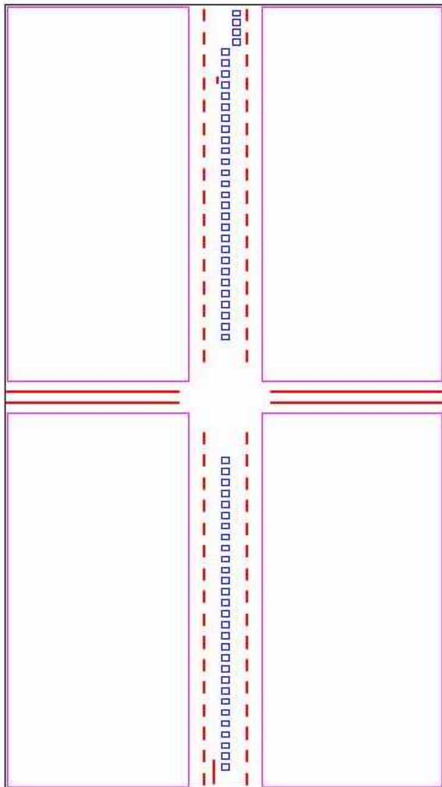
Major process flow (1)

Bumping  WLBI WLT1 Laser WLT2

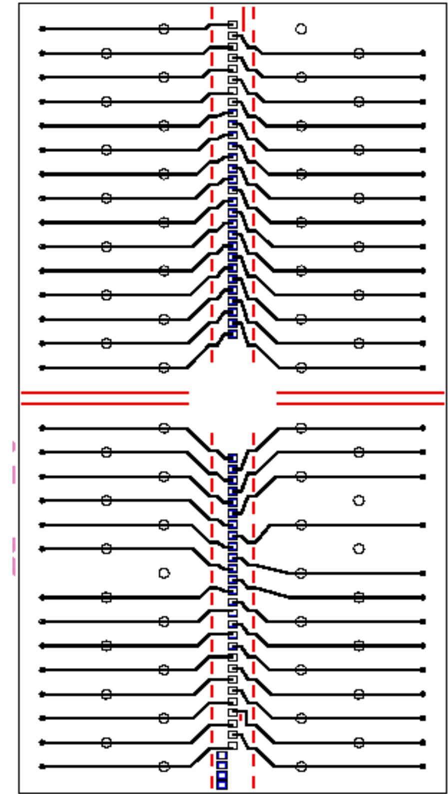
Before bumping



Flip chip process flow:

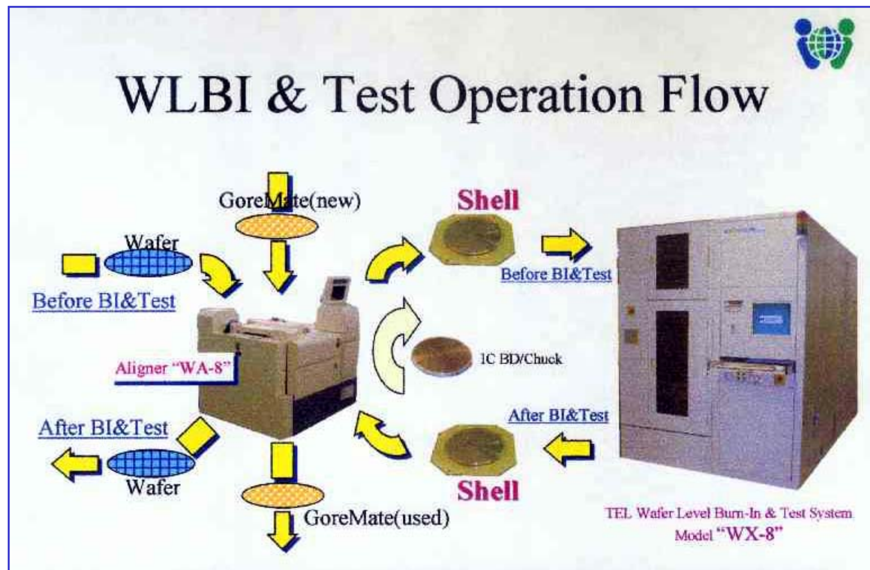
- Design
- (1st passivation)
- Metal trace patterning
- Metal trace deposition
- 2nd passivation
- Bump base opening
- UBM deposition
- Bump patterning
- Bump deposition
- UBM etching
- Reflow

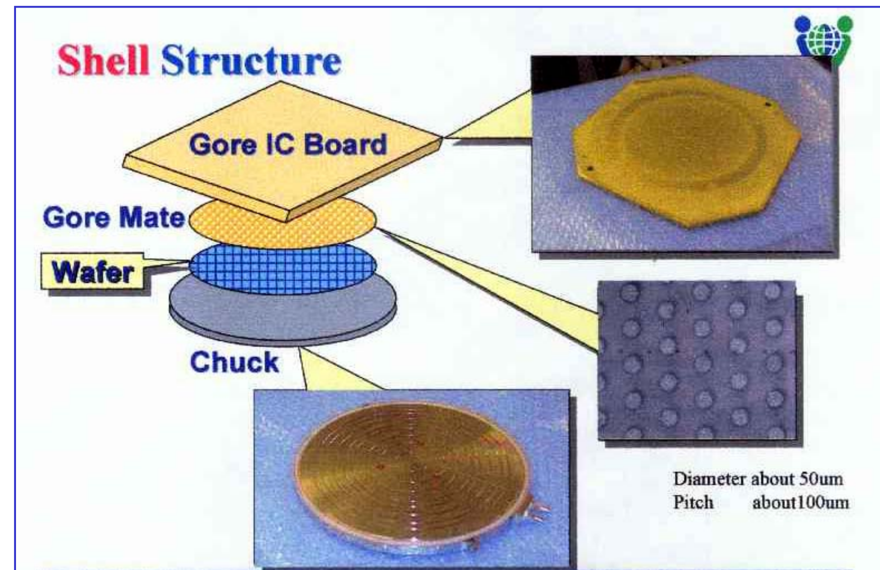
After bumping



Major process flow (2)

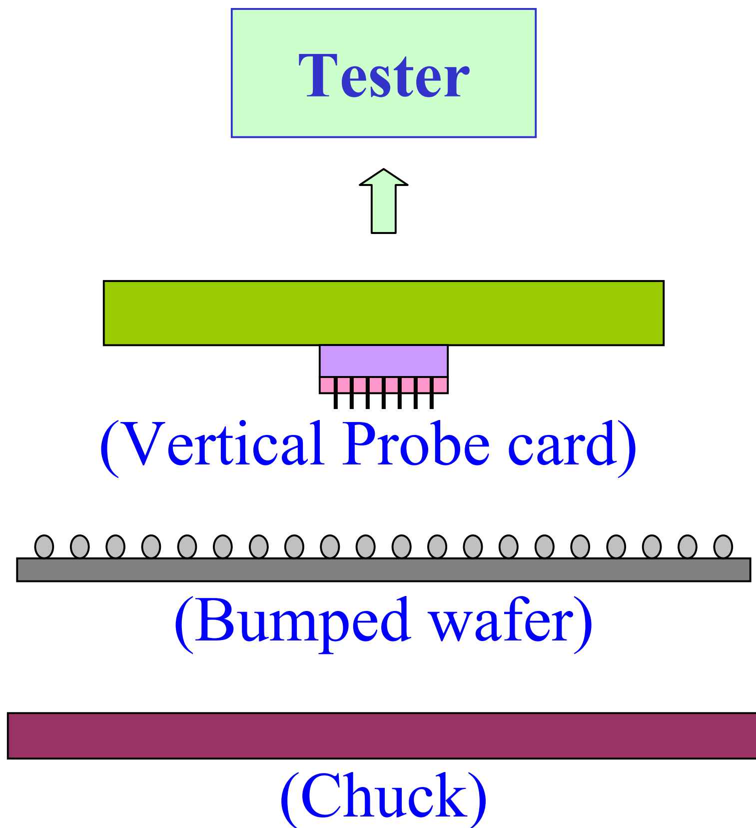
Full contact wafer-level burn-in:





Resource: Courtesy of TEL.

Major process flow (3)



Testing condition:

- WLT1:
  - At-speed
  - High temp
  - MRA
- WLT2:
  - Room temp or cold temp

Major process flow (4)

Before laser repair

During laser repair

(Bumped die)

(Bumped die)

All testing after flip chip bumping

TSOP II	Flip chip	ChipMOS solutions
• *W/S 1*	• *W/S 1*	
• *Laser repair*	• *Laser repair*	
• *W/S 2*	• *W/S 2*	
• Assembly	• Bumping	• Bumping
		• WLBI
• FT 1	• Die-level FT 1	• WLT 1
		• Laser repair
• B/I	• Die-level B/I	
• FT 2	• Die-level FT 2	• WLT 2
		• Wafer saw
• Laser marking	• Laser marking	• Laser marking
• FT 3	• Die-level FT 3	
• Inspect/ reform	• Inspect/ reflow	• Inspect

The shortest backend process flow!

All testing after flip chip bumping

- Benefits:
  - Shortest processes flow

Bumping >> WLBI >> WLT 1 >> Laser >> WLT 2

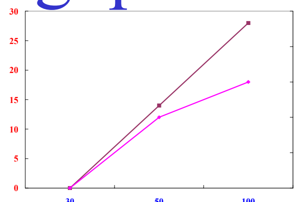
  - Lower backend cost
    - No investment for FT1, FT2, and FT3.
  - Minimum turn around time for backend processes.
  - Reduce the impact of probe cards pitch limitation by I/O redistribution.
  - Lower backend cost for process shrink/ 300mm technologies.

At-speed wafer-level testing

- Benefits:
  - Yield gain for laser repair

At-speed wafer-level testing

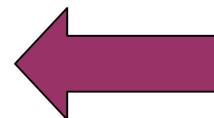
- Benefits:
  - Higher throughput

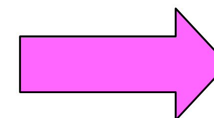


Description:

- **64M SDRAM and 1 lot of wafers(25wafers) was tested at 30 MHz, 50 MHz, and 100 MHz.**
- **Once the wafer tested, the package test was performed to compare the yield data.**
- **Customers see the improved throughput and yield when test speed is increased.**
- **Probe-One has scalable capture speed up to 250MHz.**

Throughput gain (%)





Yield gain for laser(%)

Testing frequency

Resource: Courtesy of Teradyne

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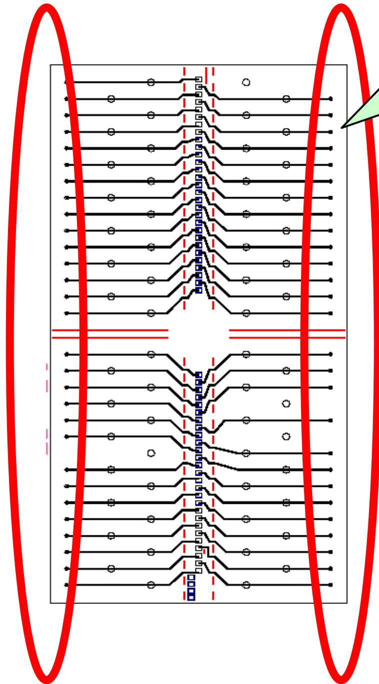
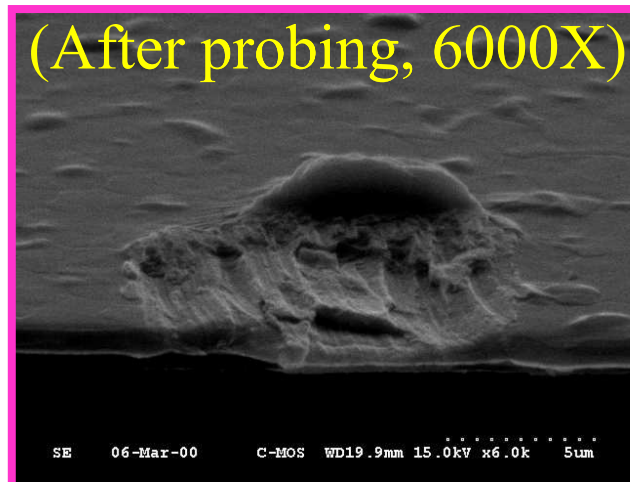
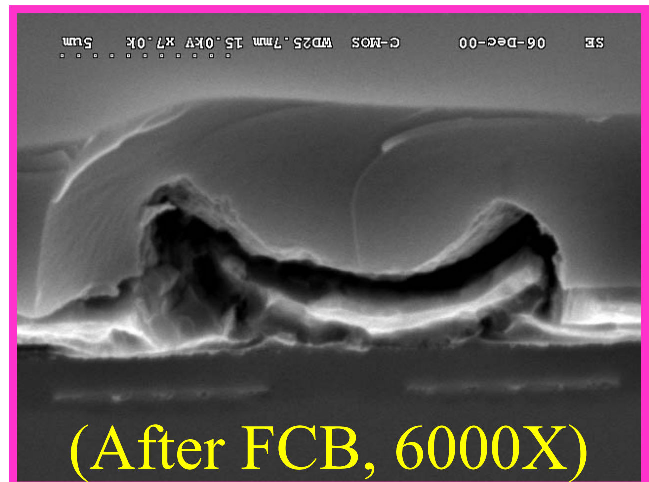
No probed marks testing

- Benefits:
  - No extra cost in making testing bumps.
  - No impact of probe marks on Al pads or flip chip bumps.
  - Reliability improvement in packages/ modules assembly.

Testing bumps on dies or on scribe lines.







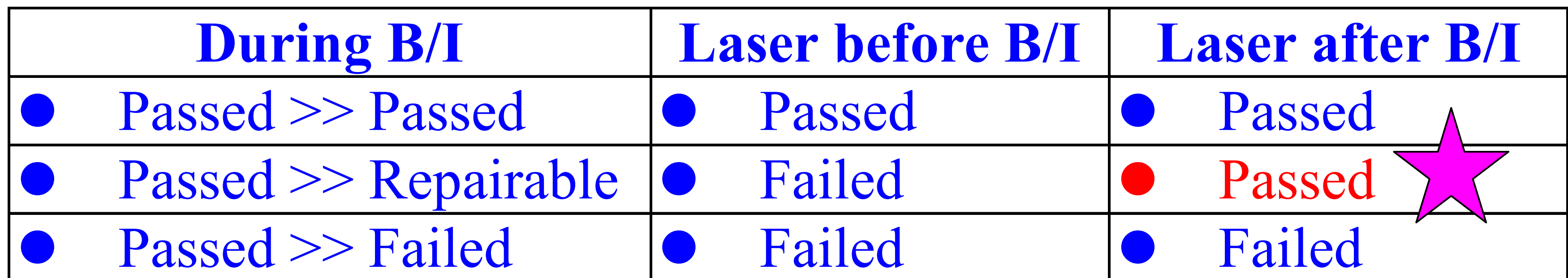
Full-contact wafer-level burn-in

- Benefits:
  - More cost effective
    - for process shrink
    - for 300mm technologies
- Comparison:

Items	Solutions	Advantages	Disadvantages
Built-in circuit	● Traditional probe card ● Tester/ prober	● Low cost ● High throughput	● Extra wafer area for built-in circuits ● B/I cells only
Full wafer contact	● Special contact board ● WLBI oven system	● Good B/I quality ● Cost effective ● Process shrink ● 300mm technologies	● High cost

Redundancy repair after FCB/ WLBI

- Benefit:
  - Yield gain for laser repair



During B/I	Laser before B/I	Laser after B/I
● Passed >> Passed	● Passed	● Passed
● Passed >> Repairable	● Failed	● Passed
● Passed >> Failed	● Failed	● Failed

Electrical simulation of FCOB

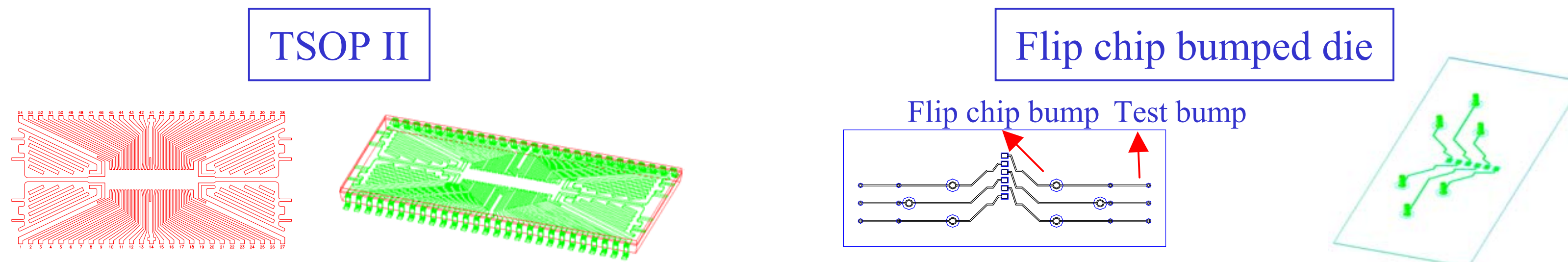
Condition:

•Software: ANSOFT Maxwell Spicelink V4.5/ AutoCAD

•Module: Boundary Element Method Quick 3D Parameter Extractor

•Method: Quasi-TEM Method

AutoCAD 2D Outline Drawing/ Maxwell 3D Package Module



(A partial drawing showing the longest traces)

Results:

Items	Ls(nH)		Lm(nH)		Cl(pF)		Cm(pF)		R(mΩ)	
	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min
TSOP II*	7.603	4.090	4.682	2.249	1.487	0.986	0.569	0.358	107.65	76.92
FCOB**	1.600	0.734	0.299	0.250	0.100	0.067	0.024	0.021	125.65	66.04
Ratio***	4.75	5.57	15.66	9.00	14.87	14.72	23.71	17.05	0.86	1.16

*: From pad to lead, including gold wire without considering the effect of the die.
**: From pad to bump including traces without considering the effect of the die.
***: FCOB as 1.

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Footprint comparison of FCOB

•With same memory capacity:

Flip chip bumped die

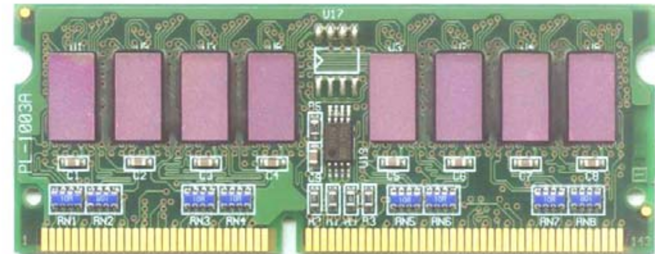
TSOP II

Items	Width (mm)	Length (mm)	Height (mm)
TSOP II	11.76	22.23	1.2
Flip chip bumped die	4.83	9.25	0.737

Footprint ratio: **1 to 5.85**

•Same footprint (SO-DIMM):

TSOP II 54L on a SO-DIMM



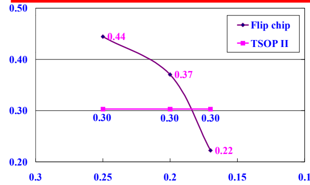
Flip chip bumped dies on a SO-DIMM

Memory capacity ratio:
2 : 1

Note: Use 0.20µm 64Mb SDRAM as examples.

Flip chip bumping vs. TSOP II

Flip chip bumping cost = f(bumping, gross dies, wafer yield)



Cost (US$)

Process(µm)

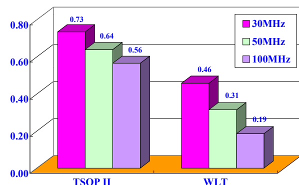
Assumptions:

- Wafer yield: 90%
- Bumping: 200USD/ wafer
- Gross dies:

Process(µm)	Gross die
0.25	500
0.20	600
0.17	1,000

Wafer-level testing vs. TSOP II

Wafer-level testing cost =
f(equipment, testing steps, throughput, wafer yield)



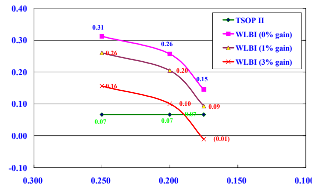
Assumptions:

- Gross die: 600
- TSOP II:
  W/S 1, W/S 2, FT 1/ 2/ 3
- WLT:
  WLT1, WLT2
- Wafer yield: 90%
- Probing efficiency: 80%
- Cost per die: 5US$
- Throughput gain & yield gain:

Testing speed	Throughput gain	Yield gain	
		TSOP II	Flip chip
30MHz	0%	0%	0%
50MHz	15%	0%	1.5%
100MHz	30%	0%	3.0%

Wafer-level B/I vs. TSOP II

Wafer-level burn-in cost =
f(equipment, gross dies, wafer yield, yield gain, die cost)



Cost (US$)

Process(µm)

Assumptions:

- Burn-in time: 24hours
- Wafer yield: 90%
- Cost per die: 5US$
- Oven capacity: 13 wafers
- Gross dies:

Process(µm)	Gross die
0.25	500
0.20	600
0.17	1,000

Challenges (1)

- Flip chip bumping & I/O redistribution:
  - RLC for bumping and I/O redistribution design.
  - Possible defects caused by wafer saw
- At-speed wafer-level testing
  - Probe cards design for high speed applications.
  - Accuracy of tester during high speed testing.
  - Memory repair analysis during high-speed testing

Challenges (2)

- No probed mark testing
  - RLC effects of testing bumps and traces.
  - The impact of testing bumps during assembly.
- Full-contact wafer-level burn-in:
  - Number of contact points per wafer.
  - Contact quality
  - Contact coplanarity
  - CTE matching
  - Circuit isolation

Challenges (3)

- Redundancy repair after FCB/ WLBI:
  - Protection of fuses during FCB
  - Reliability of opened laser windows during package/ module assembly
- FCOB memory modules:
  - KGD issues
  - Pitch limitation of module PCB.
  - Reliability of FCOB.
    - Warpage of PCB during module assembly.
    - Accuracy of die attach
    - Underfill processes on modules.

Applications and future development

Applications	Current	Phase 2	Phase 3	Phase 4	Phase 5
KGD type	● Bumped	● Al pad	● Cu pad		
Devices	● High speed memory	● Other memory	● Logic ● ASIC	● CPU ● DSP	● BIST ● Embedded ● SOC
Packaging	● MCP	● 3D CSP	● SOP		
Module assembly	● MCM	● FCOB MCM	● FCOB SOM		

Note:

1. Current device/ packaging/ module: DDR SDRAM.
2. SOP: System On Package, **the best alternative for SOC**.

Conclusions

- ChipMOS KGD integrated solutions:

	Key factors						
	Wafer yield increase	Process shrink	200mm to 300mm	Throughput gain due to at-speed WLT	Yield gain due to at-speed WLT	Yield gain due to laser repair after FCB/ WLBI	Yield gain due to better market prices
	Total backend cost per die						
TSOP II							
KGD							

Questions & discussions