

PRISMARK PRESENTATION

PREPARED FOR:

SOUTHWEST TEST WORKSHOP

June 13, 2002

DEVICE TESTING,

“ WHEN THE BACK END MEETS THE FRONT END”

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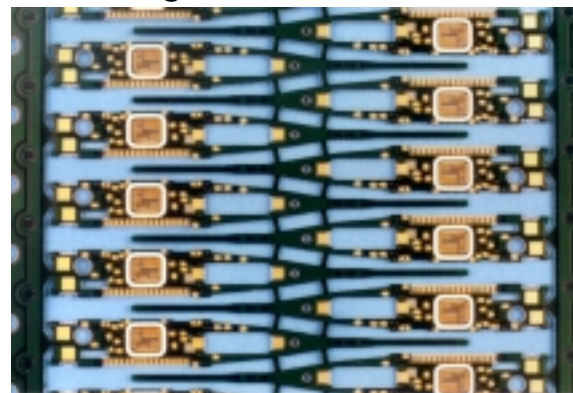


DEVICE TESTING

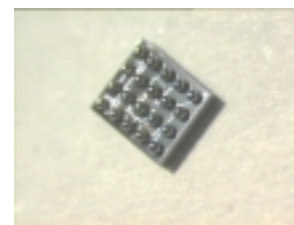
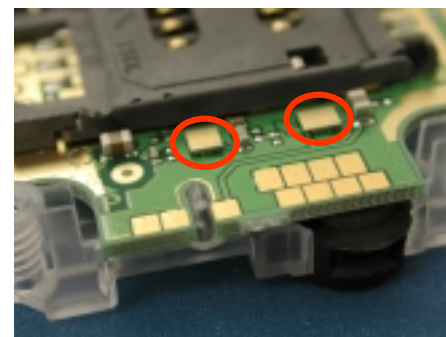
WHEN THE BACK END MEETS THE FRONT END

- Traditionally large numbers of low complexity bare die have been incorporated in hybrids and modules.
- Testing has been nominal probing and functional test at the module level.
- “Known Good Die” for higher functionality, higher complexity die has languished because:
 - The test socket amortization often costs more than packaging each die
 - There are not standard body sizes or pad outs to provide a consistent test interface
- Today Wafer Level Chip Scale Packages provide a standard probe and interconnect pitch that can be economically accessed at the device and wafer level.
- The back end is moving into direct contact with the front end, potentially enabling test and burn in to be done without packaging.

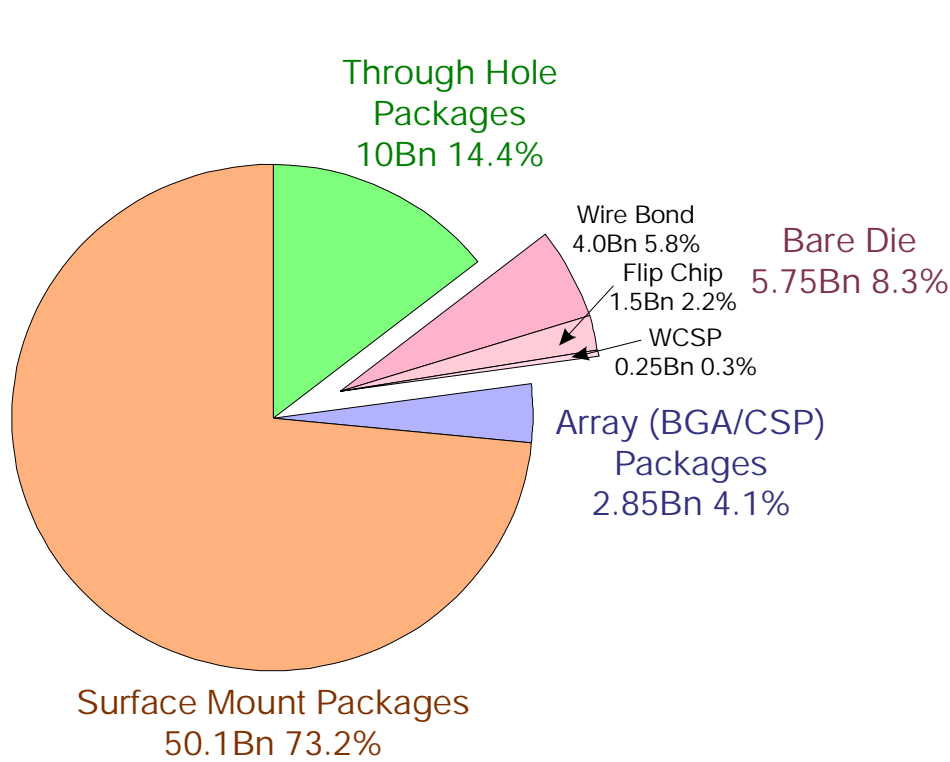
Wire Bonded Bare Die
in Digital Thermometer



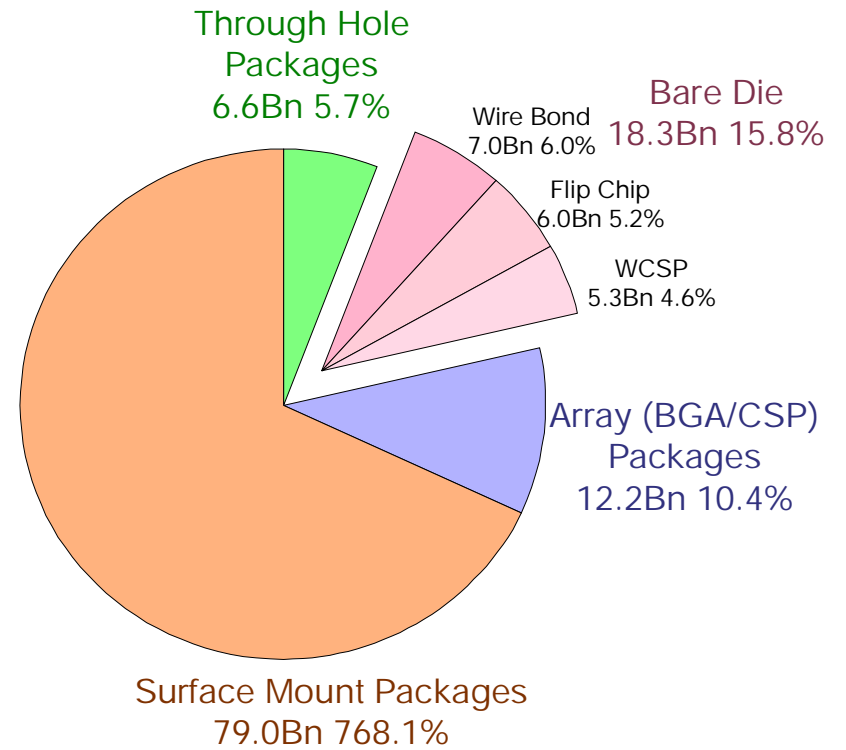
Wafer CSP in Ericsson Cell Phone



BARE DIE CONTENT OF TOTAL INTEGRATED CIRCUIT POPULATION INCREASES DUE TO SOLDERABLE DEVICES M52.123cII



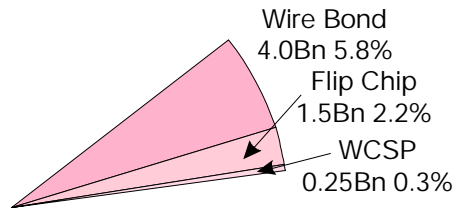
69 Billion Devices in 2001



116 Billion Devices in 2006

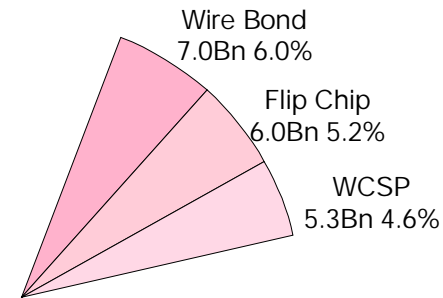
SOLDERABLE INTERFACE AND DIE COMPLEXITY INCREASE

2001



Solder Interface Content:
1.75Billion die 30%

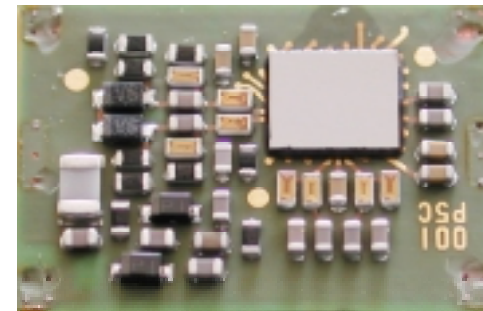
2006



Solder Interface Content:
11.3Billion die 62%

Driving Applications

- Wireless RF modules
- High performance memory
- Stacked die packages
- RFID tags and smart cards
- Power management modules
- Optoelectronic modules



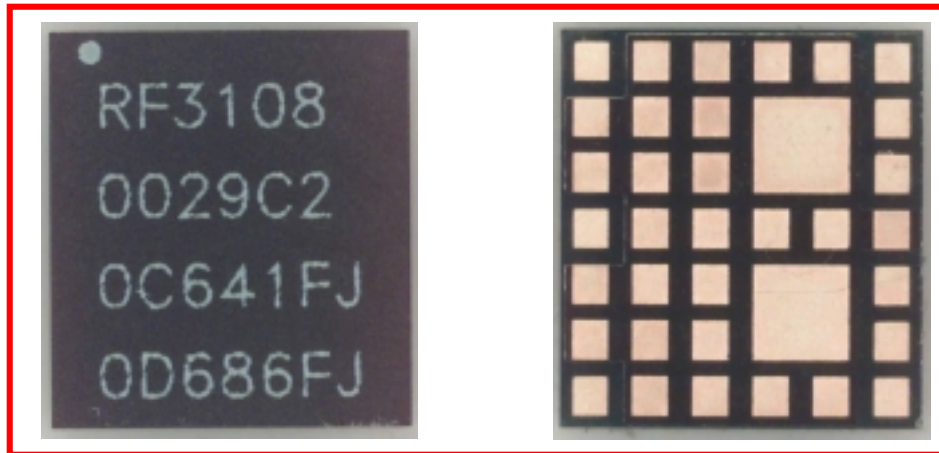
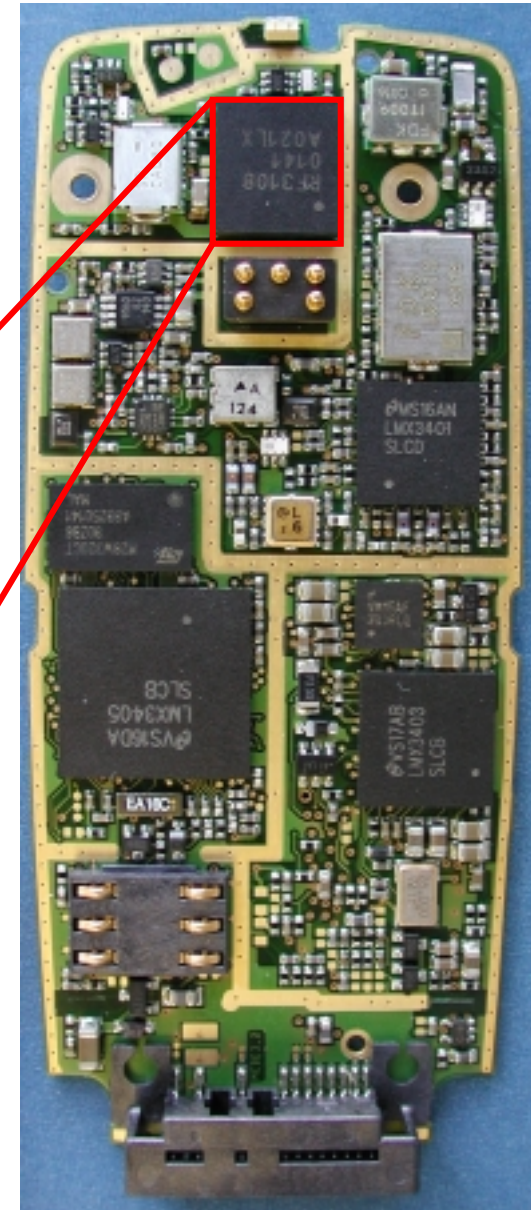
SOLDERED FLIP CHIP IN MODULE

WIRELESS RF MODULES

52.132mvc

- Most RF systems such as cellphones, wireless LANs and other radios are initially implemented with discrete RF integrated circuits
- Increasingly, the RF front end of these systems is being implemented in bare die modules
- Shown here is a triband (900/1800/1900 MHz) power amplifier from RF Micro Devices
- Further integration with SAW filters and integrated passives will continue with all of these devices requiring wafer level test

ERICSSON T66 PHONE



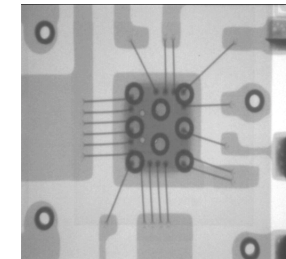
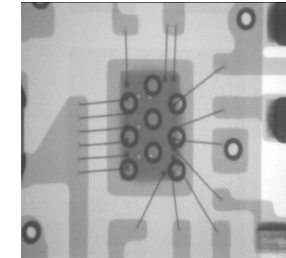
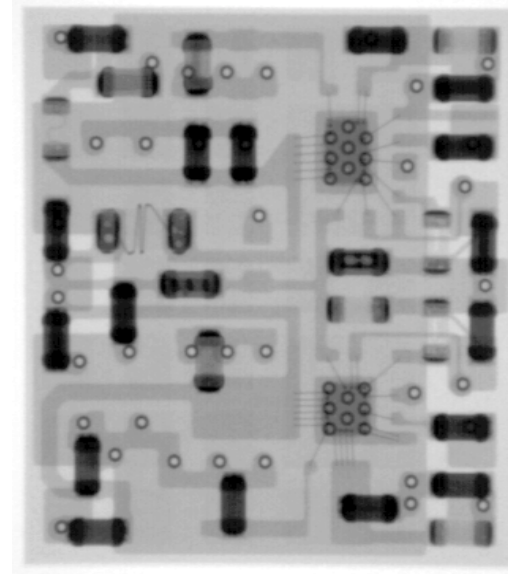
FRONT

BACK

RFMD TRIBAND PA MODULE

52.132mvc

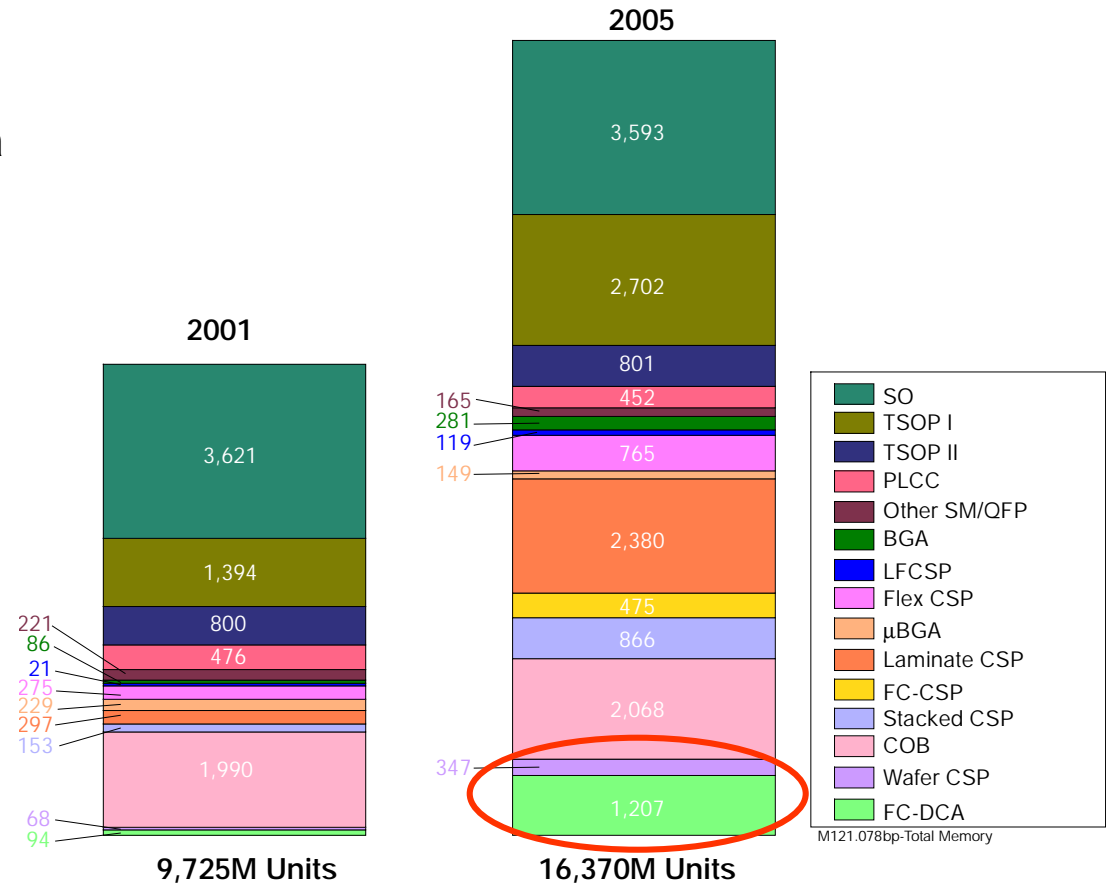
- Die 1: GaAs HBT
 - 1190 x 735 μ m
 - 90 μ m thick
 - 12 μ m thick die attach material
 - 16 wire bonds, Au
 - 9 thermal vias
- Die 2: GaAs HBT
 - 935 x 935 μ m
 - 90 μ m thick
 - 12 μ m thick die attach material
 - 19 wire bonds, Au
 - 8 thermal vias
- 29 Passives
 - 23C, 0402
 - 5 L, 0402
 - 1 L, 0603
- Moving to flip chip die in other parts of the RF chain and wafer level passives



Source: Prismark/IEEC.

WAFER CSPs FOR HIGH PERFORMANCE MEMORY

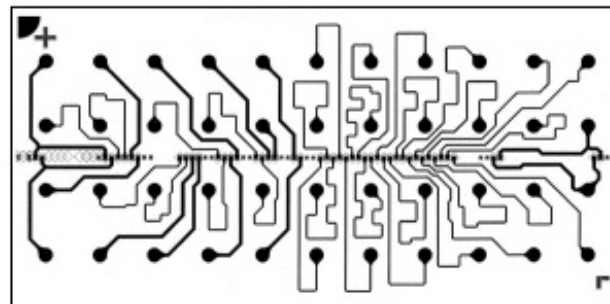
- Memory is the big one. Big numbers, big die.
- Memory is currently packaged in a wide range of low cost legacy packages.
- Memory is moving from leadframe to center wire bond BGA to Wafer CSP and Flip Chip Direct Chip Attach, as access speeds rise.
- Wafer Level Chip Scale Memory products are in production today for low bit count, and high-level integration products have been announced.



1.5Bn memory devices out of 13.4Bn (12%) will be Wafer CSP or FC DCA

MICRON 256MB SDRAM, THE FIRST PERFORMANCE MEMORY PRODUCT IN A WAFER LEVEL, CHIP SCALE PACKAGE

- Current WL-CSP production in high volume for 1M to 4M devices.
- High performance, high capacity WL-CSP memory emerging for graphics, server modules, and wireless applications.
- Center wire bond design brought out to 0.8/0.5mm pitch with additional redistribution layer (RDL).
- RDL based on Dow Chemical's BCB resin with copper traces (note delay lines and wider power ground traces)
- Greatly facilitates test access at a wafer level and burn in or high temp. speed sort.
- The preferred future "package" for high-speed memory.



Micron 256Mb SDRAM WLCSP

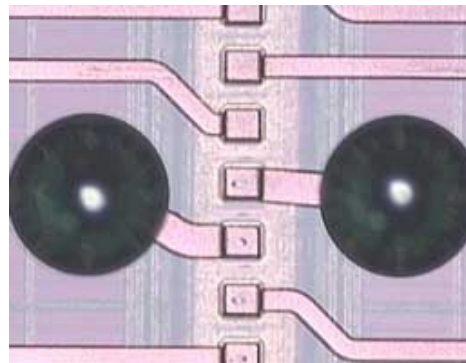
64M DRAM WLCSP

Die Size: 6.9 x 14.3mm

68 Bumps

Pitch: 0.8mm

Bump Dia.: 0.4mm

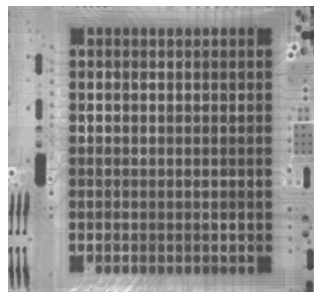


Development Product for
Undisclosed Memory Maker

PANASONIC 3G BASEBAND STACKED CSP

52.105mvc

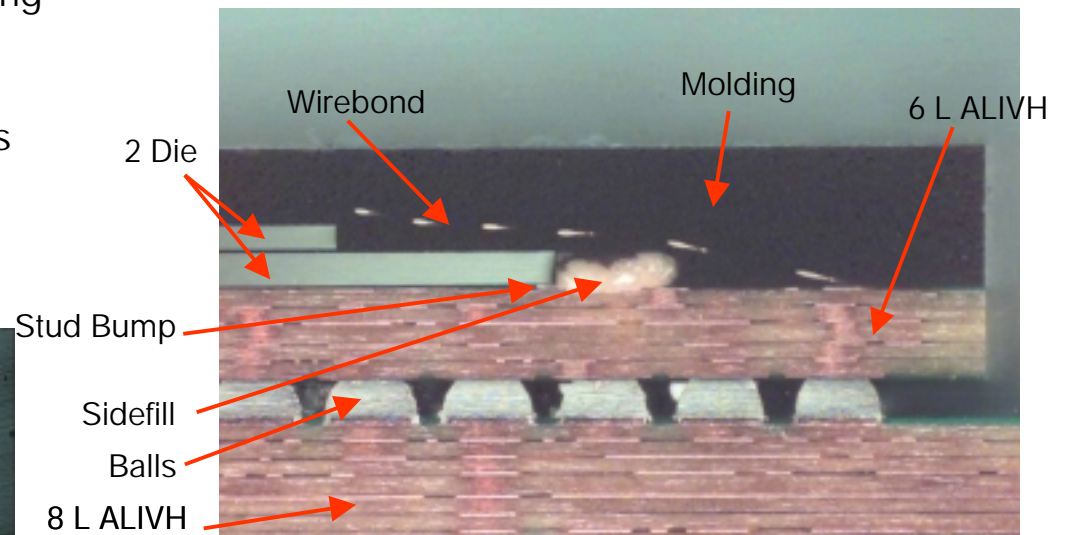
- Baseband for 3G WCDMA Phone
 - Two stacked die
 - 16 x 16mm, 1.6mm mounted height
 - 512 balls, 0.65mm pitch, full array
- Bottom Die: 11 x 11mm, 175 μ m thick
 - ~400 peripheral stud bumps (60 μ m diameter, 25 μ m height) 100 μ m pitch
 - Side fill enhances reliability
 - Stud bump on Ni/Au plated pad. No conductive adhesive. Uses TCB
- Top Die: 8.5 x 8.5mm, 140 μ m thick
 - ~300 wirebonds, 100 μ m pitch, >2 mm long
 - 430 μ m molding clearance over top die
- 6-Layer ALIVH CSP Carrier
 - 550 μ m thick, 120 μ m filled vias, 30 μ m lines
 - Soldermask defined balls
 - Assembled as array, then sawed



Source: Prismark/IEEC.



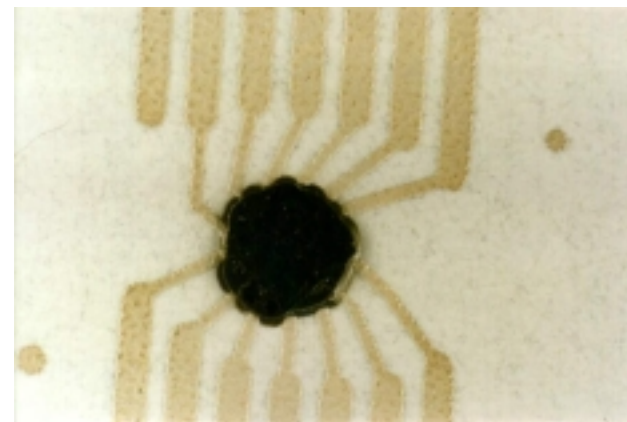
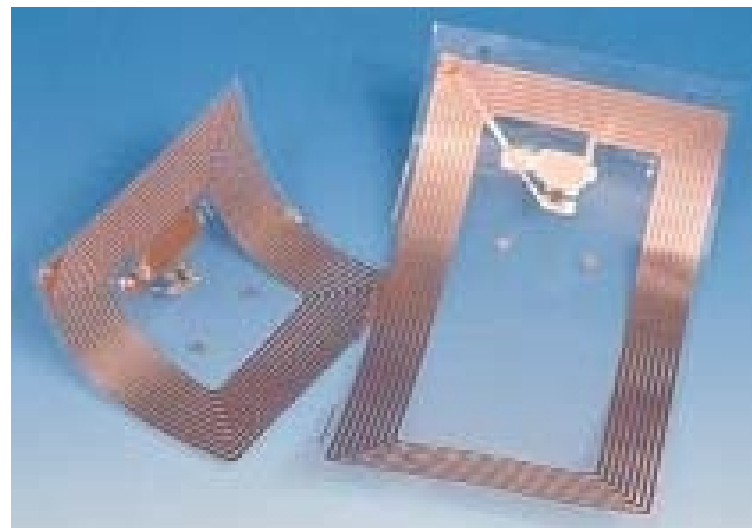
Source: Prismark/IEEC.



Source: Prismark/IEEC.

RFID TAGS AND SMART CARDS

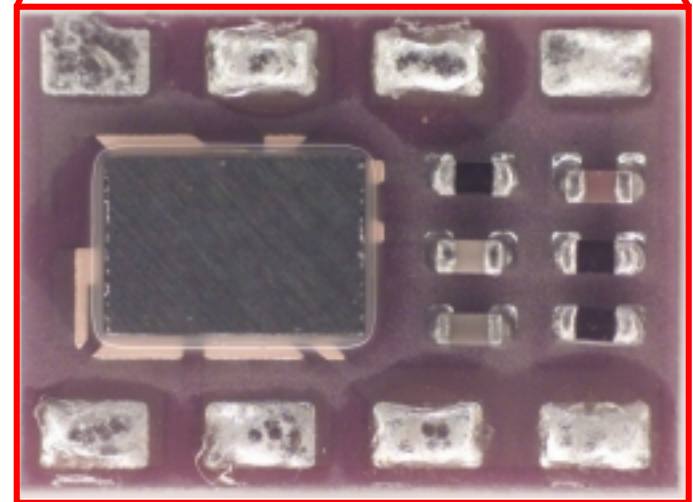
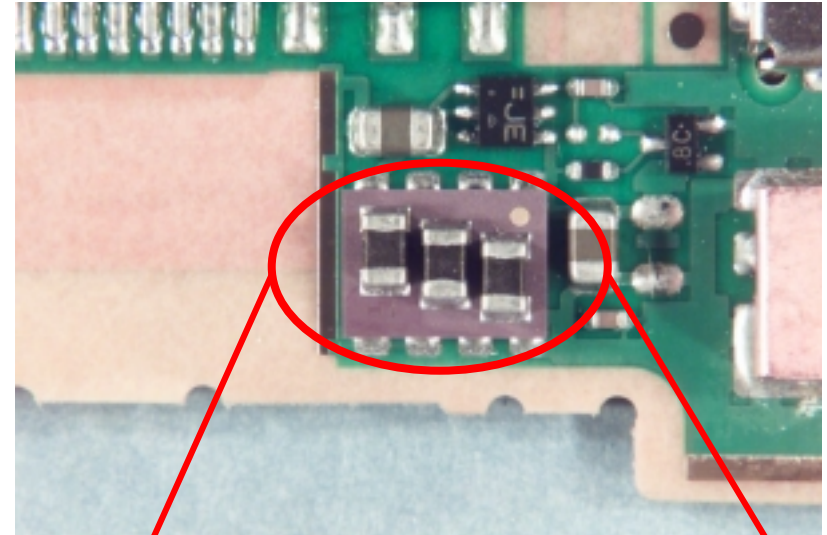
- An RFID tag is a die that is bonded to an antenna in the form of a thin “label.”
- It can record multiple unique transactions. For example, the various flight segments that a passenger’s item of luggage may pass through.
- Memory may be up to 256K and transmitting frequency up to 2.44GHz. Flip chip devices are used for size, cost, and frequency.
- Trillions of bar codes and billions of passive RF labels are read each year. RFID systems allow multiple active transactions to be recorded and interrogated.
- The back end is moving into direct contact with the front end. Is it cheaper to test the wafer or the label?



POWER MANAGEMENT MODULES

52.079cII

- Portable personal electronics require highly efficient power supplies in a small physical space with multiple output voltages
- This surface mounted micro DC/DC converter from Taiyo Yuden in a 3G phone uses a flip chip device and 0201 passives
- It works off a 3.0 to 5.5V input and provides adjustable outputs from 0.8V to 3.0V, extending transmission time of the Panasonic unit by 39%

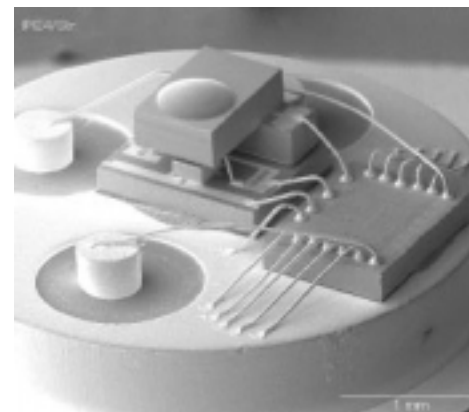
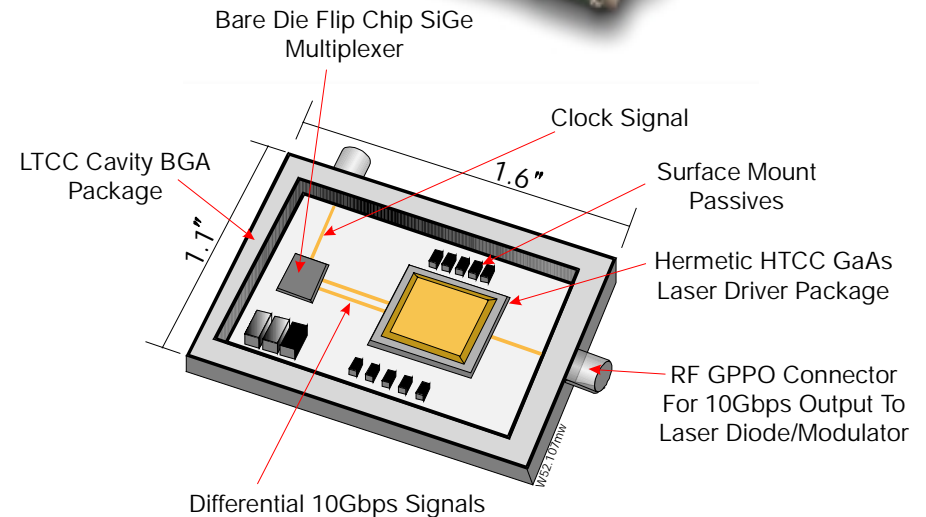
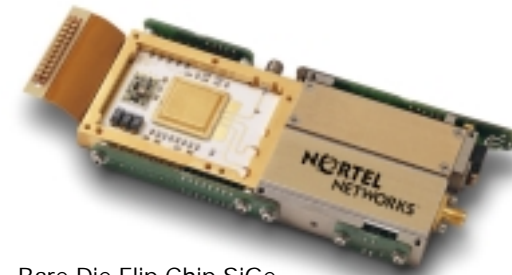


Die is 2.2mm x 1.3mm and contains MOSFETs and a diode

BARE DIE IN OPTOELECTRONIC MODULES

52.123cll

- The highest volume optoelectronic modules are transmitters and receivers. They take low speed electronic signals, multiplex them together, amplify them, and drive the laser diode to emit light into the fiber (or vice versa for the receiver).
- In longer distance modules, packages are giving way to bare die flip chip devices for 10 Gb/sec and higher data ranges.
- Shorter distance LAN transceivers (or parallel VCSEL arrays) mainly use bare die wire bonded devices today. They may use wafer CSP configurations in future.
- Small scale wafer level probing of GaAs, InP devices is practiced today.



INFINEON MICROBENCH

DEVICE TESTING WHEN THE BACK END MEETS THE FRONT END

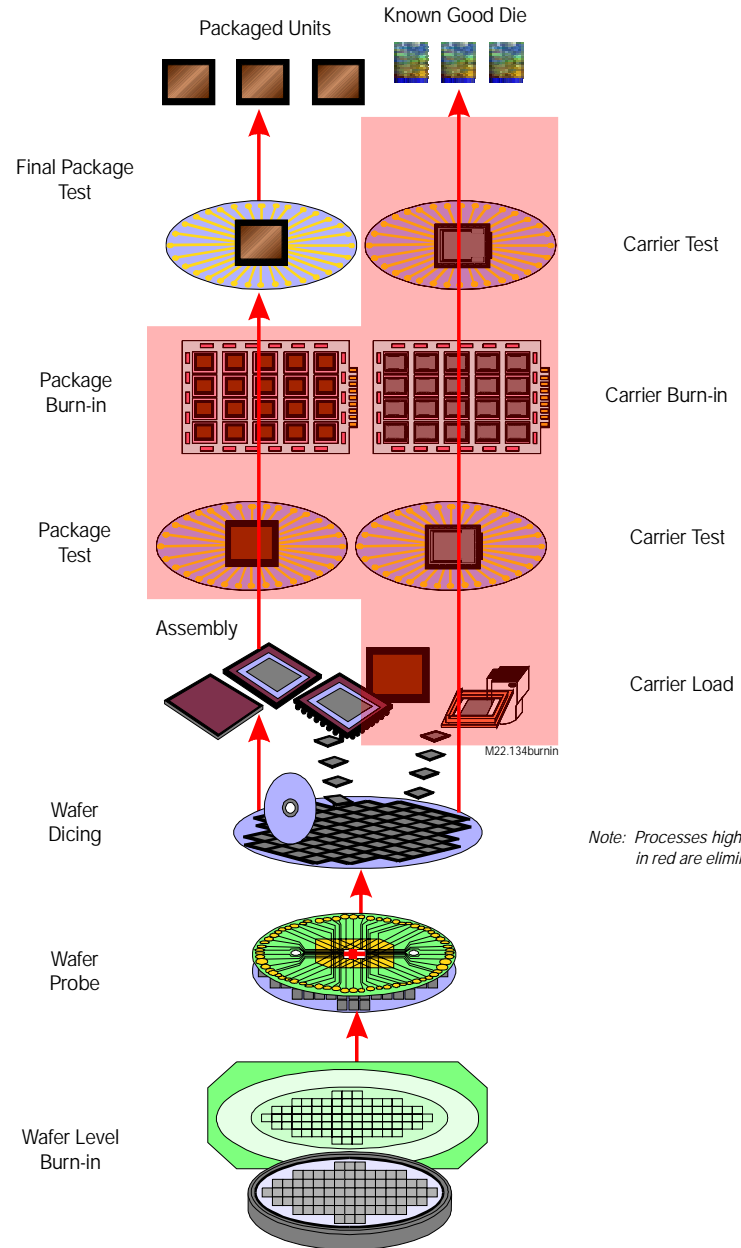
Summary of Trends

- An increase in the proportion of bare die that have higher complexity and speed, particularly in wireless, wireline, and fast digital subsystems.
- A corresponding increase in the complexity of test for these die and a continuing trade off between the economics of wafer level test and module test.
- Devices increasingly ready for final assembly while still in wafer form (redistribution, solder balls, standard pitches from flip chip to chip scale (e.g., 0.25mm – 0.5mm)).
- Increasing use of supporting functions in wafer level format (integrated passives, saw filters, RF MEMS switches).
- Build out of fine pitch array infrastructure (low cost fine pitch PCBs, strip testing).

ENCOURAGING GREATER USE OF WAFER LEVEL TEST (AND BURN IN)
OF READY-TO-ASSEMBLY WAFER LEVEL DEVICES.



WAFER LEVEL BURN-IN MANUFACTURING FLOW



DEVICE TESTING WHEN THE BACK END MEETS THE FRONT END

- Testing is always a complex, and device specific, activity
- The elimination of the package and its replacement with a WL-CSP or a flip chip die in a module increases the complexity of test economics, but it also opens up the opportunity to carry out final test at a wafer level
- Implementation of wafer level, versus module level, test strategies – or some combination – must be carried out on a device by device basis, in full knowledge of subsequent packaging, or lack thereof