Semiconductor Test DFT News Trends Technology Commentary

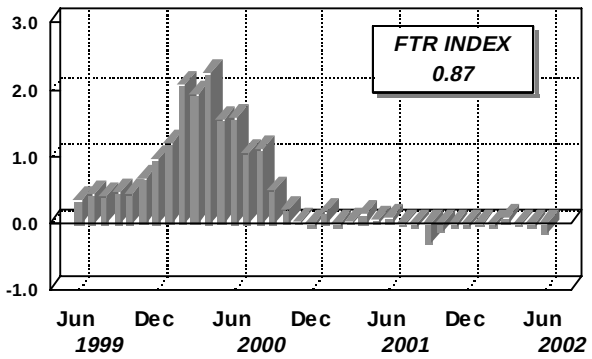
FTR THE FINAL TEST REPORT

Vol. 13 No. 07 July 2002

Intel Exec. Asks for Single-Sourced Test Tooling, But Multi-Sourced ATE

In what should have been the "Key Note" address at last month's *SouthWest Test Workshop* – or *International Wafer Test Workshop* as it should be known – Steven Strauss presented Intel's outlook on test tooling problems. Strauss is Intel's Tooling Operations manager – located in Chandler, AZ. In addition to making a pitch for single-sourcing, shorter lead times and lower pricing of test tools, he also called for open architecture VLSI ATE testers. Strauss pointed out that Intel is spending less on capital equipment (testers, probers, handlers) every year (as shown in the graph as the bottom of p. 3 of this issue.), but is spending more on tooling – making it a bigger percentage of the cost-of-test. Strauss defined "test tooling" as anything that "provides a temporary thermal, mechanical and/or electrical interface to the DUT, eg. probe cards, sockets, DUT bds., etc. – all of which must be customized for packaging form factors, electrical and thermal requirements and device function"

Steve Strauss



FTR's index of ATE, chipmakers, and PC makers vs. the Dow-30, fell as investors were even more wary of tech stocks than stocks in general last month.

It was a major change in Intel's complaints about test costs. In the past it has riled against the chip tester vendors for the cost/complexity/non-reliability of testers. Now, Intel apparently feels that those complaints have been acted on has turned its attention to non-capital tooling.

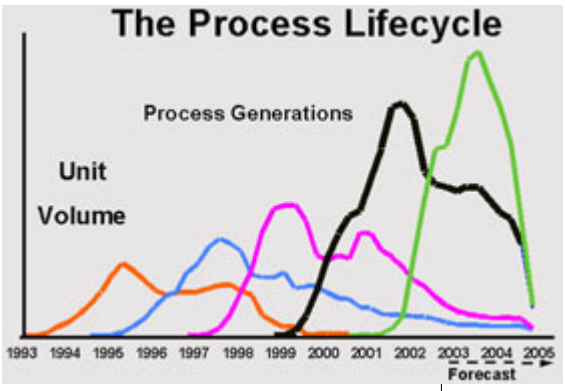
Strauss called for a *Revolution in Test Tooling,* saying that the tooling suppliers "have not changed with the times to meet customers' needs" – and implied that this situation is not limited to Intel. He said all chipmakers are looking for more comprehensive solutions, lower cost, shorter lead times and better capability than they are presently getting from their socket, board and probe suppliers.

He pointed out that chip sales have grown at a compound annual rated (CAGR) of about 15 percent since 1958 and were expected to at least maintain that rate through 2006.

Continued on page 2

iNSIDE iNFO

 Editor: J. Mulady
THE FINAL TEST REPORT is published by IKONIX Corporation, P.O. Box 1938, Lafayette, CA 94549 USA. Tel:925-939-7909 Fax: 925-906-9427 e:mail: ftr@ikonix.com. Subscription rates and a sample issue are available upon request.



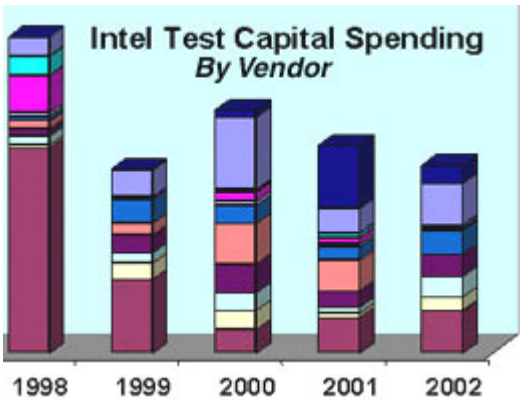
Continued from page 1

He said that forecast will hold despite last year's drop in chip sales of almost 40 percent.

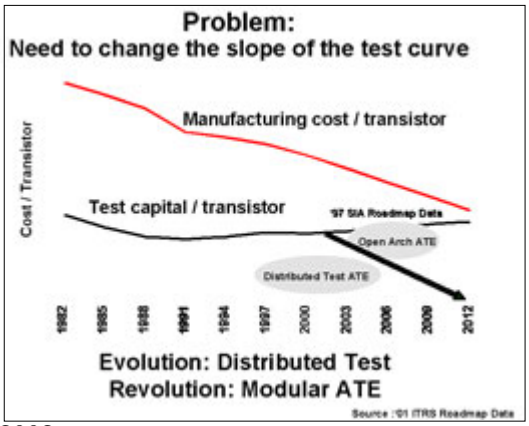
Even more important for test tooling, according to Strauss, process cycles have continued to ramp up faster and fall faster as well. Strauss pointed out that 130-nm process technology took just four quarters to go from development to high-volume manufacturing (HVM) at Intel– arguing that there is "no time for mistakes" – prototypes and HVM are now "one and the same."

In addition, speed improvements, yield improvements, packaging and other changes now result in an effective product cycle of 3 to 6 months – an thus new tooling – including probe cards, sockets, DUT boards and burn-in boards – must be designed, manufactured and installed in production quantities, in that same time-frame. Tooling is, according to Strauss, "a technology, development and HVM enabler!"

As he was talking to mainly probe card suppliers at this conference, Strauss chose to use probe cards as an example.



(He had given a similar presentation in March at the BiTS conference, where he focussed on test sockets.) He noted that the number of different probe cards required by Intel are increasing. New designs grew 22 percent between 2000 and 2001 and by 38 percent from 2001 to 2002. Until 2001, Intel had designed all SIU's (Sort Interface Units in Intel's parlence) in-house, but then changed its strategy to "enable" outsourcing of those designs.



Intel expects to outsource about one-third of all such designs this year. However, while Intel 'enabled' suppliers to do these designs, those same suppliers could not provide total solutions – only designs. As a result, "lead time reduction showed only marginal improvement in 2 years" he said

The problem, according to Strauss, is that a typical tooling supply chain contains 2- 4 "poorly synchronized suppliers." As an example he cited a vertical probe card, one supplier supplies the design, another the PCB/ space transformer and a third supplies the probe and integration and – the 'customer' ends up being responsible for its functionality.

What is needed, he said, is "turn key tooling suppliers" a single supplier which can provide the design, all of the components and volume production. A single supplier who can:

- Enable fungible designs that last multiple product generations
- Is synchronized with the specific technologies of the customers
- Provides complete turn key solutions – allowing the customer to be able to negotiate with a single supplier.
- Has 2 - 4 weak lead times, and finds innovative ways to continue to drive costs down.

According to Strauss "What it takes is *Revolution – Evolution* will not yield these goals!

He used the example of LSI ATE equipment as having gone through such a "Revolution."

That industry, he said has implemented testers which allow the use of advanced DFT to manage test complexity and has produced "Distributed Test" capability – eg. partitioning test capability by socket, allowing chipmakers to move a significant percentage of test content to less expensive DFT based structural testers. It is also moving to provide parallel test capability for complex chips.

The result is simplified tester hardware designs, while maintaining state-of-the-art capabilities and reducing capital expenditures.

But the ultimate tester solution, according to Strauss, is "open architecture" VLSI ATE. (See *Opinion* column on p. 3 of this issue for a detailed discussion and the industry's reaction to that idea – and *FTR*'s comments on such a development.)

Returning to the problems of test tooling – and particularly the probe card suppliers in the audience. Strauss asked "Can you do this [be part of a revolution and not just an evolution]? He said, "If not you won't survive!. He then offered the audience the following

Strauss's Prediction **:**
About one-half of you will not be around in 2 years!

He then asked "Will you be one of them?

IN FTR'S OPINION

In what Intel's Steve Strauss himself admits "appeared to be some thing of a contradiction" in his presentation at last months' SWTW gathering in Long Beach, CA – he called for "single-sourced" test tooling, while at the same time asking for 'multi-sourced' testers. As we described in this issue's cover story, he believes that the chip industry would greatly benefit from a 'consolidation' of tooling (probe cards, sockets, DUT boards, burn-in boards, etc.) supplier, giving chipmakers 'turnkey' solutions to their tooling needs.

However, he took quite a different tact, in that same presentation, calling for "open architecture" VLSI ATE. (Intel has been promoting this approach to its vendors for some time, but this was one of the first 'public' presentation of the idea beyond several papers at recent ITC meetings.)

While Strauss said that the latest "modular" testers are an "evolutionary" (although one slide, top of p.2) called them "revolutionary") improvement over conventional testers – they are not sufficiently so. He said that 'conventional" testers, with their custom infrastructure are too difficult to support and improvements are only 'generational. And, they are available from only a single supplier.

Modular or "Tester-on-a-Board" systems provide more flexible configurations, but are still a "closed architecture" and still are available from only a single supplier.

Strauss is asking for a "revolutionary' change – to truly "open architecture" testers – by the ATE industry. Such an architecture would allow chip makers to purchase tester main frames, test heads, and modules from different suppliers. He likens it to a PC maker which has a wide choice of suppliers for each of the components in its products.

The result, in Strauss' opinion, would be test equipment which truly "scale across price, performance, pin count and application requirements".

He recognizes that such a "revolution" would require 'disruptive" changes in the ATE industry. It would require the development of official or at least defacto industry standards for every tester component interface – and inevitably, standard software, along the line of Microsoft *Windows*.

All of that would represent a 180-degree turn in ATE industry thinking – which since its beginnings more than 35 years ago has been based solely on proprietary tester architectures and software.

This writer has had some relatively recent experience with the industry's refusal to change that mind set. In 1994 we began an effort to work with SEMI and equipment makers to develop 'standards' for chip testers and related equipment. After four years of frustration – with both SEMI's lack of interest in 'back-end" standards and ATE makers' almost total indifference, *FTR* abandoned the effort. (It has been continued – led by Xandex's Roger Sinsheimer – but with limited results.)

However, in recent months, at least two new efforts to develop standards for an "open architecture" have been quietly created.

One is reportedly being led by Schlumberger CTO, Bernie West and the other by Advantest VP, Sergio Perez. Each group is attempting to develop a 'consensus' open architecture, but doing it outside of industry groups such as SEMI and IEEE.

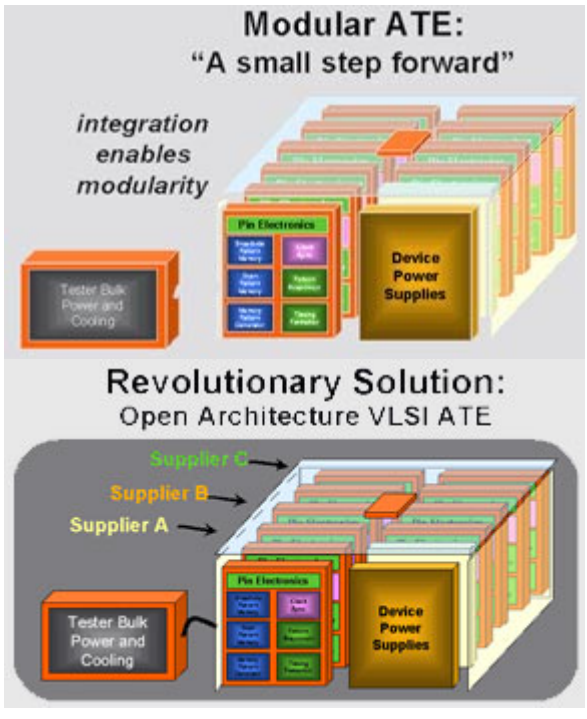
Teradyne reportedly has not joined either group, but is already embracing ithe concept.

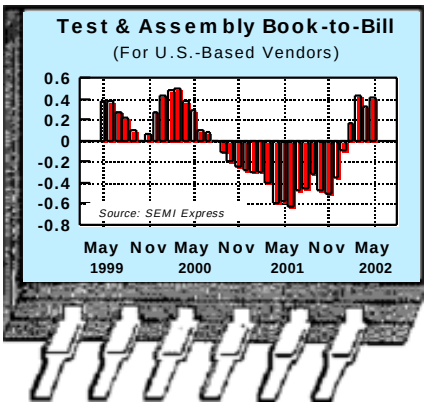
In May it announced the creation of an *Open Architecture Initiative* for its newly introduced Integra FLEX test system. "This initiative enables third parties to both cooperatively and independently develop and market instrumentation options for the FLEX system. It will provide our customers with access to a wider range of instrumentation on the FLEX platform with an accelerated time to market," said Mark Jagiela, VP/GM of Teradyne's Semiconductor Test Group.

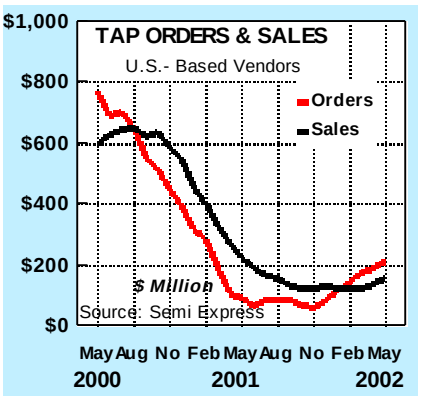
You can look for both groups – or perhaps a merged "consortium" – to surface publicly at SEMICON/West next month and at ITC in October.

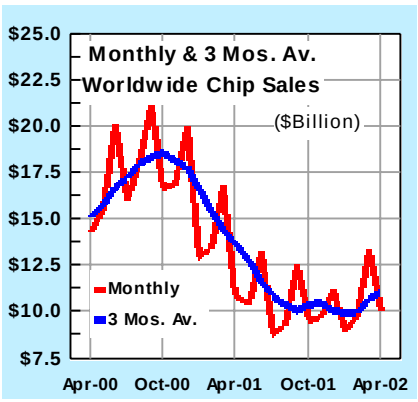
Given the present distress of the ATE industry – where most companies have little except price cuts to close orders – the time may just be right for the required mind set change.

That's my opinion,









SEMI reported that No. American chip equipment vendors saw an upturn in their bookings for the sixth consecutive month in May.

Total net new orders were $1,084 million in May (three-month rolling-average) - about 9 percent above the April figure of $995.6 million, and about 50 percent above the level of May 2001. Billings were $861.7 million, a 6 percent increase over April, but still more than 40 percent below May 2001. The book-to-bill was 1.26, up from the 1.22 (revised) in April.

Front-end orders in May were $861.8 million, a 7 percent sequentially, and 37.3 percent higher than in May of last year. Billings totaled $704 million, a 5 percent improvement over April, but about 43 percent below billings in May of last year.

The resulting book-to-bill ratio for front-end equipment was 1.22.

TAP (Test, Assembly, Packaging) orders were $222.2 million, more than double the level of May 2001 when TAP orders reached only $95.7 million.

TAP billings rose just over 10 percent MOM, reaching $157.7 million, but YOY TAP billings are still down about 31 percent. The book-to-bill for TAP equipment was 1.41.

May '02 TAP Book-to-Bill

	Apr'02	May'02	May-01
Book	$190.3	$222.2	$95.7
Bill	$143.0	$157.7	$228.0
B/B	1.33	1.41	0.42

April '02 Global Chip Billings Report

The SIA reported that worldwide chip sales (3-month average) totaled $11.07 billion in April, a 3.1 percent increase from the $10.73 billion level reached in March, with all four geographic regions reporting growth for the second month in a row. **George Scalise**, SIA president said: "Semiconductor sales in April are continuing the steady growth exhibited in the first quarter of this year, another sign that the industry is rebounding from 2001. We expect the modest growth we are experiencing in the first half of the year to continue throughout the remainder of 2002," stated . He added, "April's growth was led by an increase in sales in the wireless sector."

(US$Billions)

Market	Mar'02	Apr'02	Change	Apr'01	Change
Americas	2.61	2.62	0.2%	3.76	-30.5%
Europe	2.26	2.28	1.1%	3.08	-25.8%
Japan	2.11	2.20	4.4%	3.36	-34.5%
Asia Pacific	3.76	3.97	5.7%	3.54	12.1%
Total	10.73	11.07	3.1%	13.74	-19.4%

WW Chip Sales Fell 24.8% in April

According to preliminary data released by the SIA the dollar value of worldwide chip sales fell 24.8 percent between March and April to $10.03 billion. This drop is typical of the first month of a new quarter .

But, the YOY trend remains worrisome, as sales for the first four months of 2002 were about 22 percent below the same period in 2001.

Things have improved in recent months: last April chip sales were down over 24.8 percent YOY, while this year that figure has fallen to just 8.2 percent. Last September, worldwide chip sales were trailing the year-earlier total by 44.4 percent, so the April 2002 vs. April 2001 comparison shows real improvement over the dismal late-2001 state of the industry.

Nevertheless, when semiconductor sales are viewed in a larger historical perspective there is still reason for concern: at the end of 2000, sales on a three-month-average basis were growing at an annualized rate of almost 22 percent, but during the first quarter of this year chip sales were declining at a 33.9 percent annualized rate.

April 2002 Chip Sales

	MOM	YOY
Americas	-30.0%	-13.5%
Europe	-36.9%	-24.4%
Japan	-11.3%	-25.1%
Asia-Pacific	-22.0%	+23.9%
Total	-24.8%	-8.2%

2002 10 BEST Chip Equipment Suppliers

This year, VLSI Research added two overall categories to its *10 BEST Customer Satisfaction* awards.

• *Focused Suppliers* – companies who focus on Individual segments.

• *Large Suppliers* of chipmaking equipment – companies who rank among the top fifteen in revenues.

Focused Suppliers

Rank	Company	Rating
1	Tegal	8.26
2	Datacon	8.23
3	Universal	8.21
4	Orthodyne	8.10
5	Alphasem	8.06
6	EBARA	8.03
7	SUSS Micro	7.78
8	Multitest	7.69
9	Disco	7.68
10	Axcelis	7.68
Other TAP Companies		
11	SZ Test	7.65
12	Credence	7.47
14	Schlumberger	7.42
15	TSK	7.41
19	Electroglas	7.21
21	Shinkawa	7.11
23	K & S	6.95
27	Yokogawa	6.49
30	Ando	6.36

Large Suppliers

Rank	Company	Rating
1	ASM	7.90
2	Varian	7.89
3	Agilent	7.38
4	Teradyne,	7.35
5	Nikon	7.31
6	Novellus	7.29
7	Advantest	7.01
8	Canon	7.00
9	Hitachi	6.95
10	TEL	6.93

TAP Sales

Agilent Technologies

Said **Progate** (Taiwan) had selected its 93000 SOC Series test system.

Said **Galileo Technology (**Manof, Israel) has chosen the Agilent 93000 SOC for engineering testing

Aetrium

Reported its first order for its Model 55V6 gravity feed tri-temp handler.

inTEST

Reported $2.8 million in orders for wafer-probing interfaces and related test equipment **Agilent** in Q2.

Credence Systems

Said that **Macronix** purchased "multiple" Kalos memory test systems.

Electroglas

Said **LSI Logic** has selected its EG5/300 ARGOS wafer probe system.

Said **Seiko Epson** has qualified its QuickSilver IIe* inspection system for LCD driver circuit production.

Kulicke & Soffa

Said that **Siliconware Precision** has placed an order for 120 Maxum ball bonders.

Teradyne

Said that **MediaTek (**Taipei, Taiwan), has selected its Catalyst SOC test systems. Media Tek said that it has "specified its subcontractors to purchase multiple systems."

ATE STOCKS

COMPANY	Ticker	Close 06/28	Change Month	52 Week High	52 Week Low
Aehr Test	AEHR	$5.46	-8.2%	$5.94	$3.30
Aetrium	ATRM	$1.25	-42.4%	$2.96	$0.71
Advantest	ATE	$15.65	-9.5%	$23.00	$9.95
Agilent	A	$23.65	-10.3%	$38.00	$18.00
Cohu	COHU	$17.28	-29.5%	$30.65	$13.05
Credence	CMOS	$17.76	-6.3%	$25.33	$10.95
Electroglas	EGLS	$10.01	-28.7%	$18.35	$9.21
ESI	ESIO	$24.30	-7.8%	$36.90	$19.42
InTest	INTT	$6.67	-6.1%	$8.59	$2.44
K & S	KLIC	$11.80	-19.2%	$21.67	$8.16
LTX	LTXX	$14.28	-14.8%	$28.22	$10.36
MCT	MCTI	$2.50	-20.7%	$4.47	$1.46
Mosaid $C	MSD	$7.05	-19.9%	$61.00	$6.10
Photon	PHTN	$29.99	-25.5%	$54.50	$20.00
Teradyne	TER	$23.50	-13.2%	$40.20	$18.43
Average Change during June			-17.5%		

April Global Eqpt. Sales Dn. 41.9% YOY

SEMI reported that global sales of chipmaking equipment fell 41.9 percent YOY in April the smallest drop in 11 months. Worldwide sales totaled US$1.69 billion in April it said.

The data showed strength in Taiwan where sales rose 5.1 percent YOY to US$387.6 million and in Korea where sales were down just 9.2 percent YOY.

On a brighter note No. American equipment suppliers said net new orders were up 9 percent and Japanese equipment makers reported orders up 48.9 percent YOY in May.

April 2002 Chip Equipment Sales By Product Segment (US$M)

Type	Amount
Mask	$53.81
Wafer Fab	$1281.24
Packaging	$62.07
Testing	$215.00
Related	$57.57
Total	**$1,669.00**

April '02 Chip Equipment Sales By Geographical Region

Region	Sales	YOY
No. America	$483.6	-44.9%
Europe	$204.0	-48.5%
Japan	$208.5	-71.1%
Korea	$180.7	- 9.2%
Taiwan	$387.6	+5.1%
Other	$204.6	-82.9%
TOTAL	**$1,669.0**	**-41.9%**

FINANCIAL REPORTS

MOSAID Technologies

Q4 Ending April 26 : C$000

Figures in Canadian dollars

	2001	2002
Sales	C$9,762	C$24,292
Net	(3,186)	2,175
Per Shr.	(0.31)	0.22

Yr. Ending April 26 : C$000

	2001	2002
Sales	C$51,861	C$82,926
Net	(24,686)	7,002
Per Shr.	(2.45)	0.72

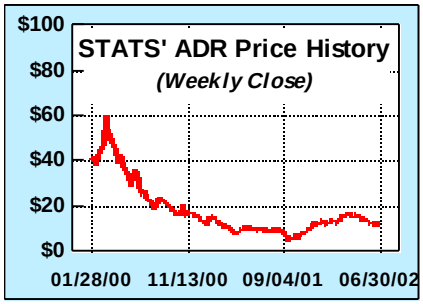
FOCUS ON STATS/FastRamp

ST Assembly Test Services (STATS) is a supplier of complete back-end turnkey services from wafer sort, test, assembly to drop shipment, with particular focus on mixed-signal testing. STATS is headquartered in Singapore with worldwide offices in the United States, United Kingdom, Germany, Japan and Taiwan. Its main manufacturing plants are located in Singapore and Taiwan, with operational space of 300,000 square feet and 220,000 square feet respectively. It also has test development centers in Singapore, the U.S. and the U.K and has approximately 2, 500 employees – half of them technical professionals – worldwide.

STATS began operations in January 1995, and has been listed on the U.S. Nasdaq (STTS) since January 2000. As was the case for most semiconductor-related companies, 2001 was a tough year for STATS – as reflected in its ADR price. It had revenues of $145.9 million – down from $333.3 million in 2000 – and a loss of $133.9 million.

In its various manufacturing facilities it has a large portfolio of state-of-the-art testers including platforms servicing digital, mixed signal, Radio Frequency (RF) and Bluetooth test requirements.

In the area of advanced packaging, STATS offers an extensive range of packages and options including BGAs, QFPs, PLCCs, near CSP packages, Stacked Die Ball Grid Array and lead-free packaging targeted at mid- to high-end packaging applications.



In February of this year – in an aggressive bid to strengthen its global presence – STATS opened its FastRamp Test Services facility – a high-end engineering and production test laboratory which focuses on providing engineering and pre-production test services — in Milpitas, CA.

According to FastRamp GM, Mark Kelly, the company had looked at purchasing one of the available existing test centers in Silicon Valley – but finally decided to build its own facility.


Mark Kelley

For the new 34,000 sq. ft. facility, an initial investment of $10 million has already been made and it plans a total capital outlay totaling $20 million. Much of the investment was allocated to the development of a premier test engineering area to meet the demands of fabless companies looking for solutions for testing the products they are rushing to market.

A unique feature of the facility is that the test floor is surrounded by large, comfortable customer offices which offer a full view of the tester in operation. The offices are fully equipped for operation of the testers and for data collection. It also provides catered meals for customers who work through lunch/dinner.

In addition, personnel, test equipment and processes are aligned to help customers launch new products, and meet volume ramps and production cost targets

It has begun equipping FastRamp so that it 'mirrors the test hardware and tester configurations of those at its main facility in Singapore. Testers already installed include: Teradyne Tiger, Catalyst, and J750, Agilent 93000 and 83000, Credence Quartet and Duo, and LTX Fusion. According to Kelly, a second Agilent 93000 will "arrive soon."

Many of the testers were transferred from STATS' Singapore facility to FastRamp, and STATS Singapore's technical staff and engineers provided training on each of the systems and aided in the launch of FastRamp's operation. According to Kelley, "technical and technology knowledge is shared between STATS and FastRamp, with the regular cross-training of technical staff."

The goal of FastRamp is to provide test engineering solutions which include lab-to-factory compatibility for transition from development to production. When the customer is ready for transition to volume production, FastRamp will provide production off-loads and capacity coordination in STATS' manufacturing facilities in Singapore and Taiwan.

Kelley said, "Customers who use STATS' testers and platforms for development work can now easily transfer their devices to volume production."


FastRamp Test Floor and User Offices

Device Tracking for Strip & Matrix Test

The following article was written for FTR by Dave Huntley, president of KINESYS Software, Petaluma, CA.

Significant cost savings can be achieved in semiconductor TAP (test, assembly and packaging) factories by using matrix (strips) substrates in conjunction with parallel unit strip testing instead of conventional singulated unit testing. These savings apply not only to test, but also to the actual assembly of the packages themselves. These savings are made possible by the existence of a strip map, an electronic representation of the devices on the strip. The strip map presents the possibility for traceability in the event of a failure, in reverse order, to the individual device, the individual piece of assembly equipment and the individual equipment and to the wafer.

This article will explore the cost-saving opportunities and what it takes for TAP manufacturers and subcontractors to realize them.

Strip Test

Strip test is the testing of the device before singulation into individual semiconductor components, while it is still mounted on the matrix (strip) substrate (ceramic, leadframe, laminate or tape). It is much easier for human operators to handle the strip as opposed to individual devices, particularly when the devices are small, light and/or thin.

A factory can standardize on a strip size and handler and perform parallel test on several different devices at once with high pincount testers. The improved utilization of the tester and reduction in material handling errors can lower test costs significantly.

For example, Amkor invested $50 million to be able to carry out strip testing on-line. The company, the world's leading independent supplier of outsourced packaging and test semiconductor interconnect services, is now reporting test cost savings of as much as 80 percent.

Traceability

Welcome by-products of strip test are strip mapping and traceability. When a device is singulated, its connection to the strip is severed both physically and logically. When devices are tested on the strip, the result is a strip map - a computerized representation of electrical test specific to each individual strip as identified by the strip designator. With the strip map, it is possible to analyze failure patterns with regard to the strip geometry. Perhaps more important, in the event of device electrical failures, and assuming a strip tracking system is in place, then it is possible to identify potential causes of the failure and implement correction plans within the factory as needed.

If the devices are marked, the device identifier can be correlated with the device's location on the strip. If a marked device fails in the field, its history can be traced via the strip it came from and the factory equipment on which it was processed.

Using strip mapping and traceability to identify and correct process problems is in its infancy and cost reduction figures are not yet available. However, initial results look promising.

Substrate Tracking

Today, matrix (strip) substrate tracking and the failure analysis is largely manual. TAP factories typically rely on the operator to manually read the magazine or scan a bar code on the magazine. Since only the magazine is tracked, traceability is lost if strips are transferred to another magazine (for example as a result of lot split or merge). A better approach to substrate tracking is to mark each strip with a 2D matrix that uniquely identifies it. The 2D matrix cannot be read by human operators and scanning every strip by hand would not be cost-effective. To track strips individually, the equipment must read and report the strip identifier.

There is now a standard for substrate tracking (SEMI E90) that is being widely implemented in 300-mm wafer processing plants.

Feed Forward Map Data

There is also now a standard for exchanging strip map information with equipment (SEMI E84). If this standard was implemented in die-attach equipment, traceability from wafer to strip could become a reality. Subsequent equipment (for example, inspection) supporting this standard could modify the map so that any further yield loss could be recorded and skipped at strip test.

With wafer map data being fed forward in the TAP factory, it becomes possible to correlate wafer and strip test results in real-time to look for early indications of process drift.

Device Tracking

Once the link is made from wafer to strip at die attach, it becomes possible to trace an individual device that has proven defective in the field right back to the wafer. The wafer identifier can be used to zero in on the wafer processing equipment responsible for the failure. If the device location on the wafer is tracked, then it becomes possible to analyze failure patterns with regards to the wafer geometry.

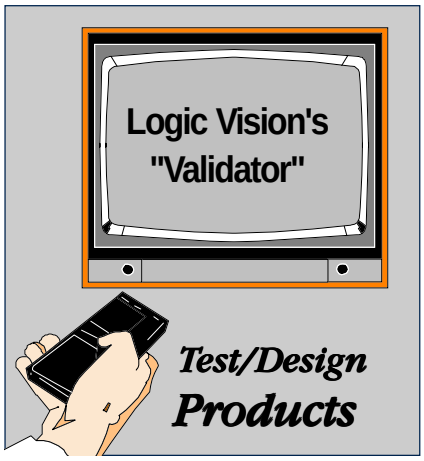
Conclusion

Although yields are typically high in TAP factories, the cost of failures is also high since the devices are at their maximum value and profit margins are at their slimmest at this point in the semiconductor manufacturing process.

Integrating strip mapping with die attach is the key to enable feed-forward and feed-back control of the TAP process as well as deliver critical failure data back to the wafer processing plant.

All failure patterns can be analyzed with respect to the strip, the assembly equipment, the wafer and the wafer processing equipment.

Automated map data collection and substrate tracking coupled with failure analysis software can offer real-time process correction. There are standards now in place for traceability and substrate tracking. It will take time for these standards to become widely accepted.



LogicVision Unveils Hdw. IC Debug tool

LogicVision has entered the hardware arena with its *Validator* – composed of software, intellectual property (IP) and hardware – which it describes as "the industry's fastest software and hardware solution for silicon debugging. It is targeted at the broad range of chips for consumer, computer, communications and other applications, said the San Jose, CA-based supplier of built-in-self-test (BIST) software and hardware.

LogicVision claims that in beta trials, the Validator has cut silicon debugging times by more than 100 times over traditional methods. It said that in one case, the first silicon consisting of 10 million gates on 0.13-micron technology, the at-speed test was successfully completed within 45 minutes after the first silicon was received. It also claims that it "eliminates dependence on test vectors, test programs, and hard to access test equipment."

The Validator will be available in Q3 of this year, the company said.

LogicVision's Validator

Validator Specifications	
Clocks	2 or 4 – 3.8V Max
Clock Freq.	0 – 330MHz
Power supplies	
Programmable voltage ranges	
Option1	0 – 8 Volts
Option2	0 – 20 Volts
Max Current	30A @8Volts
Debug Data Interfaces:	
Chip	JTAG, 9 In, 4 Out
Board	1 - JTAG
Voltage	2.5V – 5.0V
CPU 1	
SUN SPARC – 500MHz	
RAM	512MB
Storage	80GB
CPU 2	
Intel Pentium 3 – 1.1GHz	
RAM	256MB
Storage	80GB
Dimensions	21"W x 14"H x 28"D

Aehr Gets Full Wafer Test/BI Contract

Aehr Test Systems said that it has received an order – from an undisclosed source – totaling over $2 million for engineering development of a full wafer contact test system. The system will be developed using proprietary interconnect and parallel test technology currently utilized its full wafer contact FOX product line.

The full wafer contact system is expected to parallel test 200-mm and 300-mm wafers, and will include individual DUT power supplies using Aehr's MTX test technology.

C.J. Meurell, president of Aehr Test said, "A DFT or JTAG test strategy eliminates many of the barriers to full wafer contact and allows for an extremely cost effective test solution. Testing an entire wafer of die at the same time certainly changes the dynamics of manufacturing test costs and throughput improvements."

Aehr's FOX full wafer contact burn-in and test systems contacts, burns-in and tests up to 14 wafers simultaneously, with more than 30,000 contact-point capability per wafer.

The FOX systems use full algorithmic test (N, N2, N3/2) for memories, and a vector pattern generator for devices using BIST.

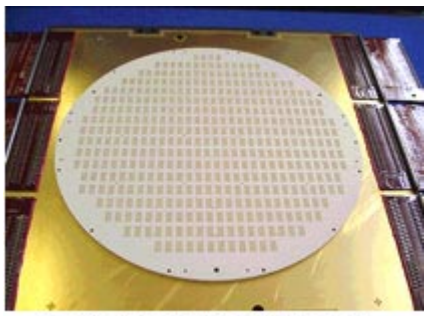
Aehr's contact system utilizes micro pogo spring contacts, which the company claims provide a high touchdown life, high compliance and works with most pad metalurgies.

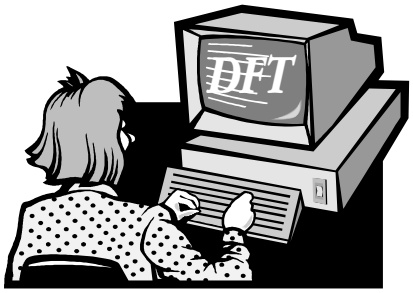
However, as Steve Steps of Aehr pointed out in his presentation at SWTW last month, contact pressure requirements are substantial. In his example an 8" SDRAM wafer, with 500 die and 50 pads/die requires a 25,000 pin contactor and at 10 grams /pin requires about 250kg (about 550 pounds.) A major challenge is to maintain planarity to within a few microns at such force levels.

Wafer alignment is accomplished off-line – using Electroglas equipment – in wafer/PWB cassettes held together with air pressure.

Aehr admits that the development of the FOX system has taken considerably longer than it expected, due to the number of thermal, mechanical and electrical barriers which must be dealt with. The company would not provide specific information about existing installations of its FOX system, but reportedly does have at least one customer which is using it for laser diode burn-in. In addition, the system is said to be under evaluation by "several' memory device makers.

This development contract includes performance milestones which are scheduled to be completed during calendar 2002 and 2003. Non-recurring engineering (NRE) revenue will be recorded as earned, upon milestone completion, Aehr said.


Aehr's Micro Pogo Contactor



Teradyne/Test Insight Test-to-EDA Tool

Teradyne has partnered with Israel-based Test Insight to provide that company's *WaveWizard* test development product for design-to-test solutions. WaveWizard enables test engineers to create test programs for Teradyne's J973, Integra and Catalyst testers, utilizing EDA software design data. Teradyne's Test Assistance Group (TAG) will standardize on the WaveWizard tool set for test generation solutions. TAG's standardization provides the foundation for worldwide applications support and training for all Teradyne and Test Insight customers, establishing "the first industry-wide accessible solution for easily moving design information into test," according to the companies.

The WaveWizard productivity tool facilitates an efficient transition from EDA software into fully functioning ATE test programs, complete with patterns, timings, levels, and pin configurations. With WaveWizard, test and design engineers can emulate device timing architecture and design, removing the constraints of cycle-based methods typically found in EDA-to-test conversion products.

Teradyne has benchmarked Wave Wizard against several commercially available tools and selected it for its ease of use, graphical display, faster code development, debug, and characterization capability, and flexible, intelligent timing generation.

"The intuitive approach to device timing, combined with WaveWizard's ease of use, shortens customers' test program development cycle and reduces errors," explains Meir Gellis, CEO of Test Insight.

EDA Finally Getting Some Respect?

When the *Design Automation Conference* (DAC) returned to New Orleans last month, it was not just be the city that was heating up. At one panel – led by Synopsys' CEO Aart de Geus, a "Man on the Street" video was presented. Shot in New York, an interviewer asked passersby whether they thought investing in EDA or pork bellies was more lucrative. When people got a definition of EDA from the interviewer, they overwhelmingly voted for pork bellies. A closing question to a passing woman: "Would you vote for Wally Rhines?" "Never heard of him," came the reply,

However, de Geus pointed out in his presentation that while Nasdaq spiked during the boom years of the dot-com craze, EDA stocks have remained a remarkably stable investment "even though people don't understand what we do." Others argued that from an investment perspective, EDA can be extremely attractive, especially in uncertain times.

EDA growth is stable and comparatively predictable and only goes one direction—up. You can count on the EDA industry to deliver positive growth at a compounded annual rate of about 12 percent to 15 percent over the long haul, and EDA has never had a down year.

Also, EDA companies, even those that sell some hardware, usually have "software-like" business models in the sense that there's little physical inventory and the margins are high.

The aggregate gross margins of the 15 publicly traded EDA companies last year totaled 81 percent. Operating margins ranged from 10 percent to 30 percent, with an aggregate of 15 percent operating income last year.

This was a very attractive financial profile for a single equity—not to mention an entire industry—in troubled 2001.

EDA Industry Still Consolidating

And, [EDA] willows down, to a precious few: A spate of acquisitions of publicly held EDA companies by the three industry leaders, Cadence, Synopsys and Mentor over the last couple of months has further increased the domination of EDA industry by those three companies.

- Cadence Design acquired Simplex Solutions as of June 27 for $3.95/share or about $165 million. Simplex had revenues of about $48 million for the last four quarters.
- Mentor Graphics is acquiring Innoveda at $3.95/share or about $160 million. That company had revenues of about $80 million for its last four quarters as an independent company. Mentor also acquired IKOS Systems in late April, at $11.00 per share or about $135 million. IKOS had revenues of $53.3 million for the previous four quarters.
- Synopsys' acquisition of Avant! was completed on June 7 at about $18.36/share – about $730 million – well above their 52-week low of $2.62 on Sept. 27, 2001 but below the 52-week high of $21.23 reached on Jan. 9 of this year. Avanti reported 2001 revenue of $398.7 million.

Although these three companies claim to represent over three quarters of worldwide EDA revenues, there are a total of about 145 other companies which classify themselves as EDA companies.

(Avanti, Innoveda and IKOS had previously been 'tracked' by *FTR*, but now have been removed from our weekly and monthly charts. We are presently evaluating other public companies to replace them.)

EDA STOCKS

COMPANY	Ticker	Close 06/28	Change Month	52 Week High	52 Week Low
Cadence	CDN	$16.12	-16.3%	$24.94	$14.10
LogicVision	LGVN	$12.75	0.0%	$15.45	$3.97
Mentor	MENT	$14.23	-12.4%	$27.15	$12.84
Synopsys	SNPS	$55.48	8.9%	$61.00	$36.15
Average Change during June			-5.0%		

Japan Eqpt. Orders up 48% YOY in May

Worldwide orders for Japan-made chip equipment grew 48.9 percent YOY in May, to Y112.06 billion ($940 million), the third month of YOY increase and the highest level since January 2001. May's WW orders represented a 32 percent rise from April, according to the SEAJ. However orders placed by Japan's chipmakers to both Japanese and foreign firms in May decreased 17 percent YOY to Y35.57 billion ($297.4 million), down 5.2 percent from April, it said.

Worldwide sales of Japan-made equipment declined 50.2 percent YOY in May, to Y46.14 billion ($38.6 million). Domestic sales of chip equipment made by both Japanese and foreign firms dropped 53.0 percent YOY to Y25.10 billion ($210 million) in the month,

The global book-to-bill ratio for Japanese equipment climbed to 1.61 in May from 1.26 in April. That ratio topped the key 1.00-mark in April for the first time since January 2001

The book-to-bill for Japanese equipment was 0.98 in March and 0.74 in February, according to the SEAJ .

JAPANESE ATE STOCKS

INDEX	Ticker	Close 06/28	Change Month
NIKKEI 225	N225	10,622	-9.7%
Advantest	6857	7,460	-12.2%
Ando	6847	480	-15.5%
JEM	6855	1,160	-5.7%
MJC	6871	910	-14.2%
TEL	8035	7,810	-6.8%
TSK	7729	4,070	-14.0%
Yokogawa	6841	930	-14.3%

The data shows chipmakers, particularly in Asia, are increasing capital spending as global chip demand improves, the SEAJ noted.

However, industry observers say "Japanese chip-manufacturing equipment makers shouldn't get their hopes up too much as the order outlook remains uncertain. A recovery in the global chip market still looks fragile in the absence of strong demand for finished products", they said.

Furthermore, the industry can't count on a rise in orders from Japanese chip makers, who remain hesitant to boost capital spending after sinking deeply into the red last fiscal year, ended March 31 .

Tough Times Test Japan's Chipmakers

Japan's IC industry is under intense pressure and scrambling for answers. Saddled with billions of dollars in fresh losses. Toshiba's IC operations in the business year ended March 31 were $1.32 billion; Hitachi's semiconductor business lost $1.28 billion; NEC's Electron Devices fell $1.14 billion into the red; and Mitsubishi Electric's chip division posted a $615 million operating loss.

Now, chipmakers there appear to be responding by dismantling the strategies that just a decade ago appeared to make them invincible. NEC has moved to spin off almost all its semiconductor and flat-panel-display operations into a series of subsidiaries and joint ventures that will essentially eliminate its Electron Devices group. Hitachi has already spun off its DRAM design and marketing business into the Elpida Memory joint venture with NEC, and is apparently planning to merge its remaining microcontroller and logic-IC operations into a joint venture with Mitsubishi.

Japanese chipmakers controlled 51 percent of the worldwide market in 1988, but that slipped to just 23 percent in 2001 while the U.S. chip industry now controls 52 percent of the global market.

Most industry observers believe that the decline was guaranteed during the 1997-98 chip recession, when Japan' chipmakers cut their CAPEX by 40 percent YOY, to a collective $5.3. They increased their spending in 1999, but, then cut them again in 2000, and again in 2001 by 63 percent YOY. According to IC Insights, since 1992, Japan's chipmakers have steadily falling behind their foreign rivals when capital expenditures are measured as a percentage of IC sales. Last year capital spending for the average Japanese semiconductor company was 19 percent of sales, far from the 27 percent global average, according to IC Insights.

Japan is already depending on both foundries and test/assembly contractors to provide the capacity they are unwilling-or unable-to provide for themselves. Most observers believe that within a few years, many of Japan's large chip companies will become essentially fabless. Most won't build new fabs and instead will turn to foundries to make their leading-edge chip designs.

Japanese chipmakers are also expanding production in China, attempting to take advantage of China's low costs to boost their competitiveness in its semiconductor market.

Toshiba plans to increase monthly production capacity at its IC packaging and testing plant in Wuxi, Jiangsu Province from the current three million units to 30 million units and Mitsubishi Electric plans to boost monthly production capacity at its Beijing plant from the current 16 million units to 20 million units by year-end and to 35 million units by March 2004. In addition,. Sony is expected to build its first IC packaging and testing plant next to its notebook computer plant in China.

Of the dozen or so Japanese DRAM makers, Elpida remains the only one wholly committed to the sector, making about 20 million 128-M DRAM equivalents a month. However, Elpida is now Japan's No. 2 DRAM maker-behind Micron Technology's, plant in Kobe, Japan.,

The annual *SouthWest Test Workshop* (SWTW) moved – over the objections of many of its long-time attenders – from its previous venue at Paradise Point in San Diego, CA to Long Beach, CA's convention center area. The new venue was generally viewed as adequate, but little more.

The workshop had 282 advanced registrants before early registration was cut off a week before the conference and 62 more registered on-site, for a total of 345, up slightly from 330 in 2001. About one-third were first time attendees, and the mix of vendors and users was substantially better than at last year's version – when relatively few users attended.

As usual, this workshop – which as we repeatedly say, should be renamed the *International Wafer Probe Conference* (or *Workshop*) – provided a good mix of presentations including 'hands-on' problem descriptions and solutions for those who are directly involved in wafer probing on a day-to-day basis.

SWTW Chair,Bill Mann, trying to buy a Coke at Tuesday's BYOB Bar

It also offered more general presentations on the future of wafer test.

SWTW began on Sunday afternoon with a first-class description of the state of *Wafer Level Burn-in*. A very detailed description of the status of chip burn-in and various companies efforts at both in-house and commercial equipment to accomplish full-wafer burn-in was presented by Bill Mann, General Chair of SWTW.

His presentation was followed by Teresa McKenzie, a Motorola engineer who described her company's work with sacrificial metal wafer-level burn-in and test methodology (As *FTR* described in the Jan. '02 issue, p.7).

McKenzie was followed by Steve Steps' of Aehr presentation of *Solutions to Technical Challenges for WLBI*. He struck a solid note when he said "There are "only three major technical challenges in developing a full-wafer test and burn-in system – thermal, mechanical, and electrical. (See p. 8 of this issue for a description of Aehr's "FOX" test system.)

The main workshop produced a wide variety of offerings: from high-power probing to RF and parametric probing. Safe to say, anyone involved in wafer test would have found something of value during the two and one-half days of the workshop.

The award for *Best Overall Presentation* went to Brett Grossman and Tim Swettlen of Intel for their presentation titled: **Modeling Distributed Power Delivery Effects in High Performance Sort Interface Units.**

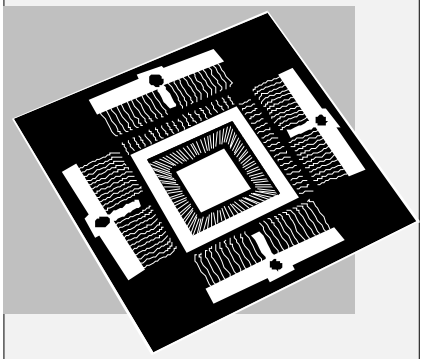
The award for which this conference is famous – the *Golden Wheelbarrow Full of Crap*, for the most poorly disguised sales pitch - for the first time ever, was awarded to a company – rather than to individual presenters – JEM America's two papers; the *HAWK: High Parallel Hybrid Probe Card for Memory Devices* and *VSCC: Vertical Spring Contact Card for Bump Probing"* by Phill Mai, et al and Patrick Mui, et al respectively. (How those papers got past the SWTW program committee, will forever remain a mystery.)

On Monday evening Steve Strauss of Intel gave what should have been the Keynote Address and to which we have devoted a substantial part of this issue of *FTR*. (The actual Keynote, titled *Wafer Testing – Where Back-End Meets the Front-End* and given by Neil Moskowitz of Prismark Partners. While it was interesting, it seemed off-the subject of this conference.)

In addition to the presentations – in the long-time tradition of this gathering – long breaks and a number of social gatherings provided lots of opportunity for networking and discussions. All in all, this is one conference where you do get your money' worth – in information, food and booze.

In summary, in a very difficult year for technical conferences and exhibitions – due to tight travel budgets – This year's *SouthWest Test Workshop* has to rated a substantial success.

ATE/DFT MEETINGS



July '2002
17-19 SEMICON/West
Test, Assembly & Packaging
San Jose, CA Convention Ctr
www.semi.org

September, 2002
16-18 SEMICON Taiwan 2002
www.semi.org

October '2002
8 - 10- Intl. Test Conference
Baltimore, MD Convention Ctr.
ITC@courtesyassoc.com.

15-16 SEMICON Southwest 2002
Austin, TX Convention Ctr.
www.semi.org

FREDDY'S TEST REPORT

INDUSTRY

The SIA released its 2002 mid-year forecast last month, outlining its view that an industry-wide recovery is now under way. The SIA expects semiconductor sales to increase by 3.1% in 2002, with the growth rate accelerating to 23.2% in 2003 and 20.9% in 2004.

VLSI Research expects that chip equipment sales will reach $100 billion in 2007 – a compound annual growth of 22% from $36.8 billion in 2002. Though this forecast seems high considering the industry's recent woes, VLSI notes that when the figure is calculated as a CAGR from the high point of $60 billion in 2000, it translates to only 8% per year.

SEMI said that its office in Washington, D.C. will become the headquarters for SEMI North America, and **Victoria Hadfield** has been name president of its North American operations. Hadfield, had been VP for industry advocacy for SEMI.. She replaces **Bobby Greenberg**, who has resigned 'to pursue other interests."

COMPANIES

MCT has received notification from the **Nasdaq Stock Market**, that it does not meet the $50,000,000 market capitalization required for continued listing on the Nasdaq National Market. It said it will appeal it to *Nasdaq Listing Qualifications Panel* .

LogicVision said **Agere Systems** has licensed its Embedded Test 4.0 for design, debug and production test.

Morgan Stanley's chip equipment analyst in Japan, **Noriko Oki**, said he expects **Advantest** to miss its F2002 (ending March, 2003) sales target

Credence Systems will fund a Masters of Science (MS) level fellowship program in electrical and computer engineering at **Portland State University**. **Electroglas** has donated an EG4|200e parametric wafer prober to that same school's new IC Design and Test Laboratory.

Kulicke & Soffa will revise the wafer test portion of its chip test tooling business, by consolidating multiple U.S.-based probe card manufacturing facilities in Gilbert, AZ, Austin, TX and San Jose, CA facilities, followed by consolidation of Taiwan-based manufacturing operations into the Hsin Chu location. No changes are expected in European operations at this time.

PEOPLE

David Tacelli was named president and COO of **LTX.** He had been an Exec. VP of the company since 1999.

Jim Healy has resigned his positions as president of **ASAT** USA and Sr. VP of worldwide sales and marketing for ASAT. Sales and marketing will report to **Harry Rozakis**, ASAT's new CEO.

Bryan Hoadley has been named STM Worldwide Account Manager for **Credence Systems** – based in Grenoble, France. He had been Sr. Manager of Field Operations for that company. **Todd Delvecchio** will assume Hoadley's previous position.

Dennis Bibeau has joined **LogicVision** as Sales Manager. **Bibeau** had been with **Symtx**, in Austin, TX and prior to that **LTX** in Boston.

Ray Sites has rejoined **LTX** as Account Manager for the Western Region. Sites also comes from **Symtx**.

Chin Koon Koh has been named GM of Asian manufacturing operations for **Electroglas**.

Tan Lay Koon has been name President/CEO of **STATS,** replacing **Harry Davoody**, who resigned after just six months in that position, "to pursue interests in the United States", according to the company.