Modeling Distributed Power Delivery Effects in High Performance Sort Interface Units

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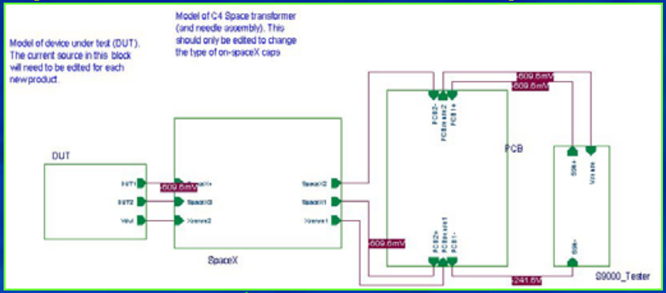
Power Modeling: A look back

Menu based:

<u>Decoupling:</u>

- •Standard (1.0uF, 0.1uF, 0.01uF):
- •Other (custom):

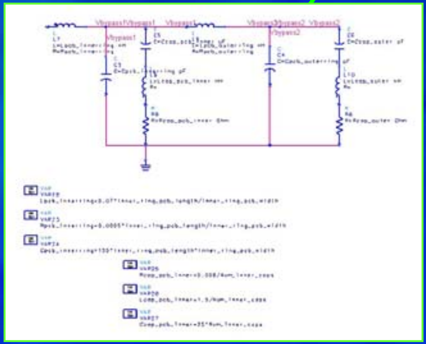
Spice Based:
(lumped time domain)



1990 — time — **Today**

PRODUCT:	USES: Vnoise = Iccmax	
(note: fill in grey squares with product specific da	X	Y
Die Size, approximate (mils)	443.0	506.0
Clock frequency **Fmax** (MHz)		300
Assumed contact resistance (Ohms)		0.50
Power supply name:	**DPS1**	**DPS0**
Assigned function:	**Periphery**	**Core**
Allowable Vcc + Vss noise, as percent of Vcc	10.0%	12.5%
Vcc (volts)	2.750	2.750
Iccmax (Amps)	1.00	13.00
di - Maximum change in Icc (Amps) = 2 * Iccma:	1.00	26.00
Assumed **dt** (seconds) - uses 1/4 of 1/**Fmax**)	1.00E-9	833.33E-12

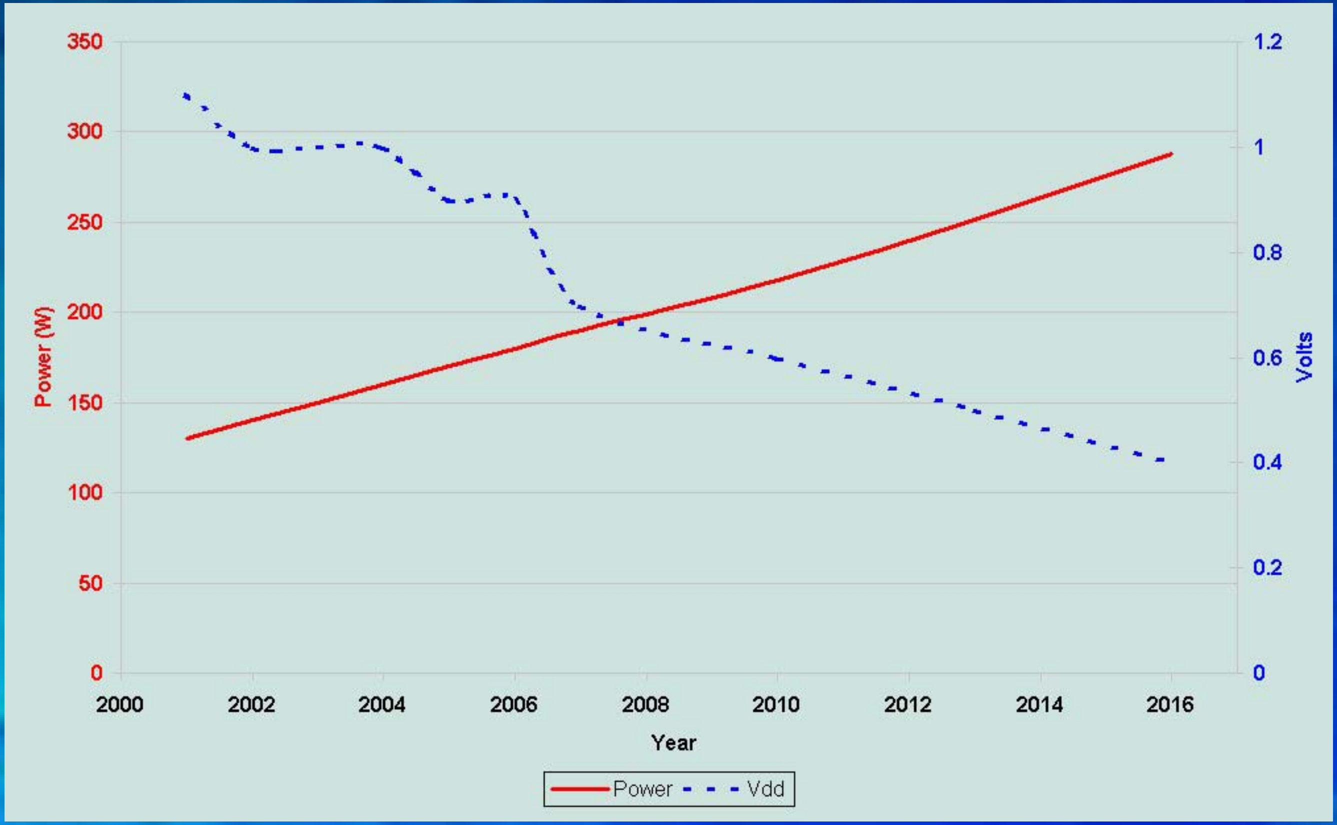
Spreadsheet based:
(lumped freq. Domain)



ADS Based:
(lumped time/freq domain)

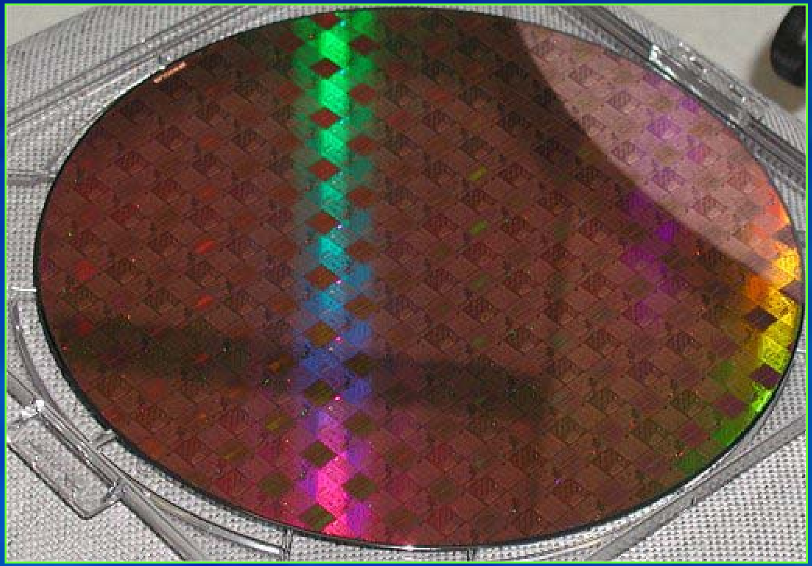
Power Modeling: A look forward

- Continuing growth in power demand drives the need for refinements in modeling power delivery



Source: 2001 ITRS Roadmap

What is 100A?



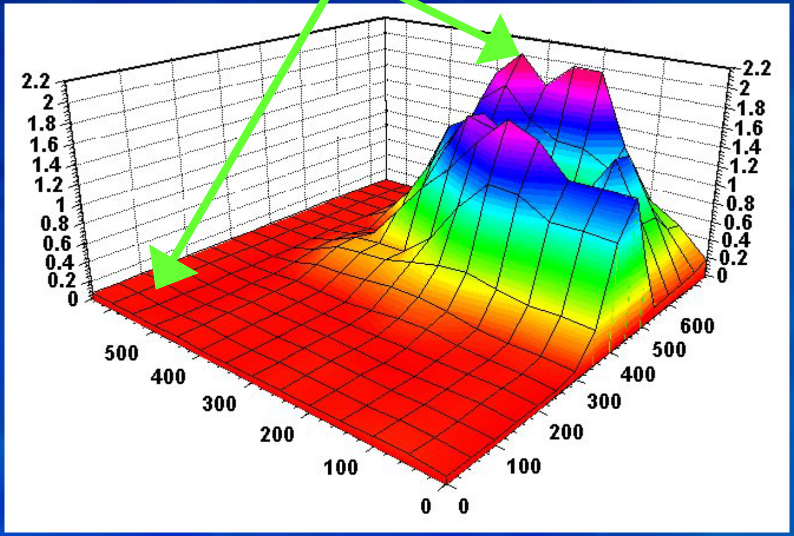
Different viewpoints of 100 Amps

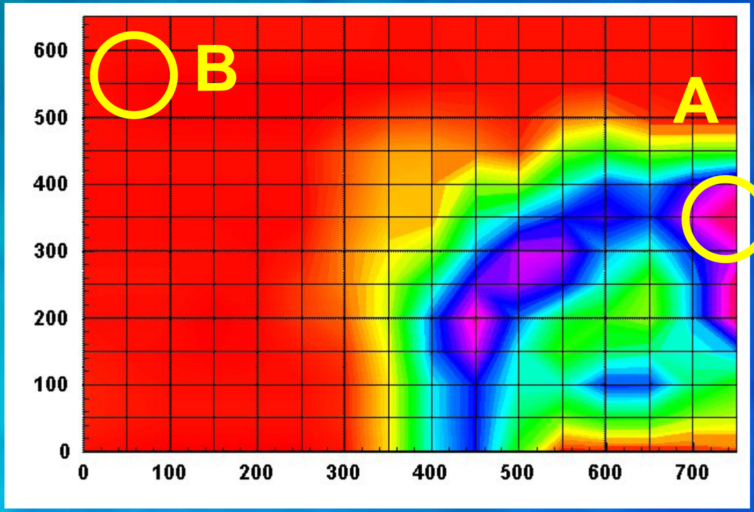
- What might it look like if ½ the DUT were idle?

The Problem

- Device current demand
  - ❑ Varies with device state
  - ❑ Varies with time
  - ❑ Varies with X-Y position

Power Δ >10x

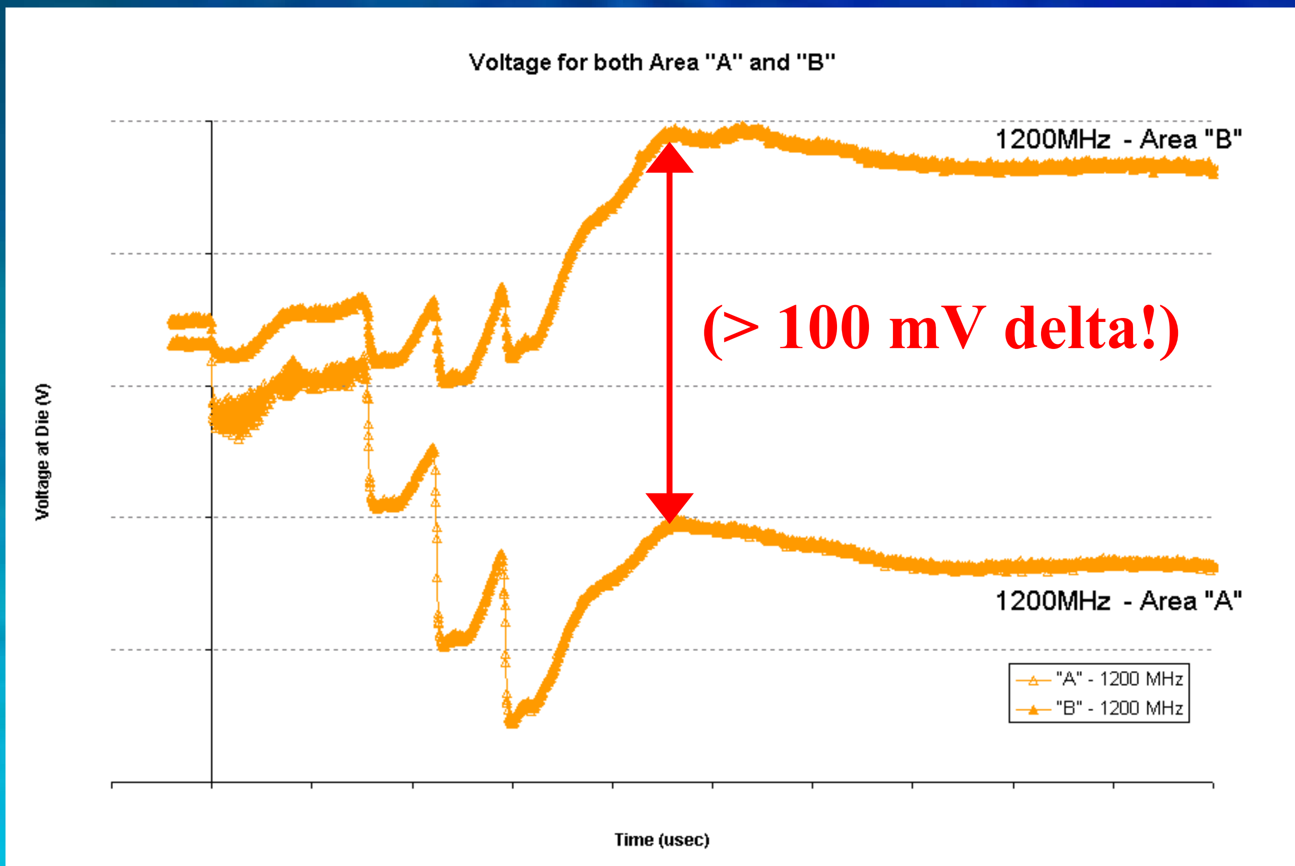




- What is the impact:
  - ❑ Of probe or capacitor placement?
  - ❑ Of measuring Voltage at points A & B?
  - ❑ Of locating supply sense at points A & B?

The Impact

- Example :
  - ❑ Measured droop voltages at two die locations (A&B)



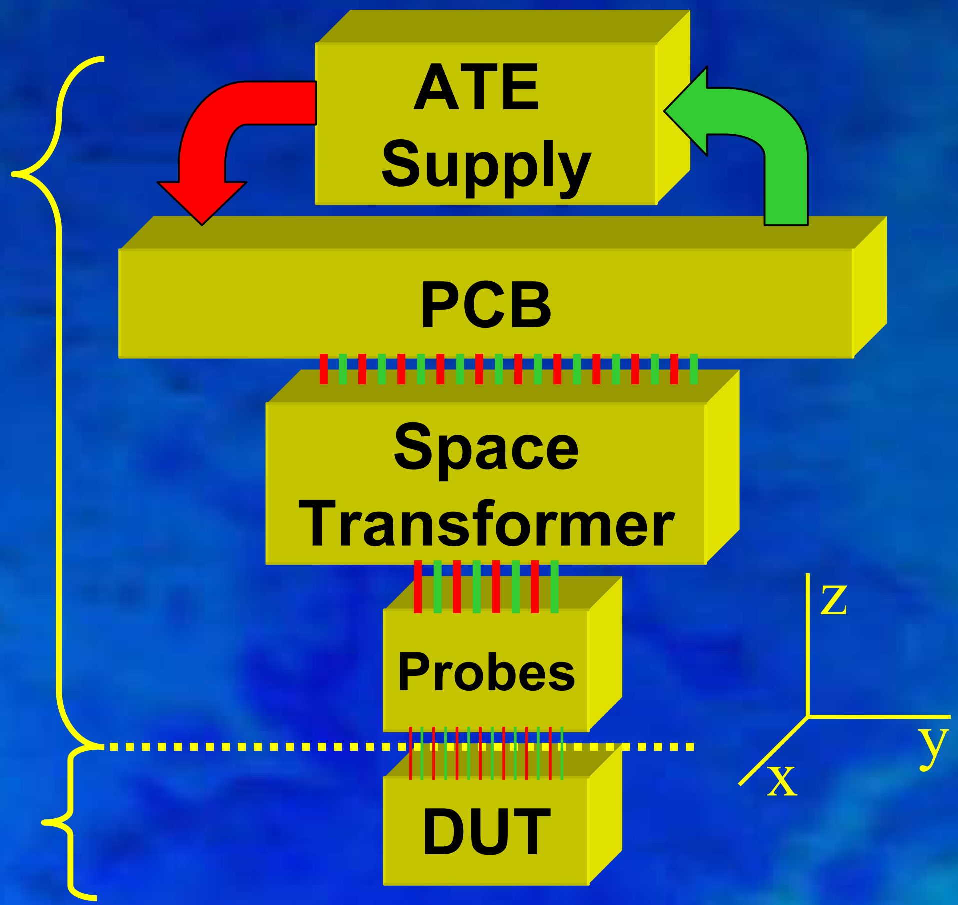
Device running 80% max speed executing reset sequence. Voltages measured at the DUT/probe interface.

Power Delivery System (PDS)

PDS
- Uniform design
  - ❑ Probes, decoupling, etc.
- Modeling only represents lumped components
  - ❑ No (X,Y) understanding

DUT
- Non uniform demand
- Non uniform decoupling
- Non-uniform parasitics

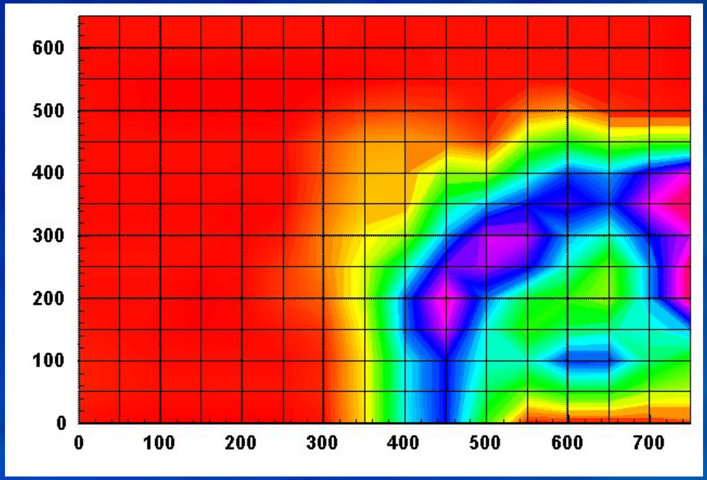
Simplified Block Diagram



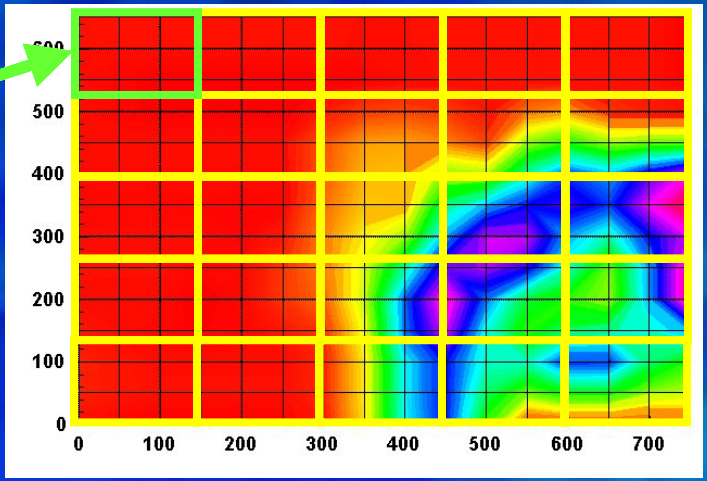
Vdroop
- Performance metric for PDS
- Measure of voltage change to an applied current

Understanding a solution – DUT level

- DUT non-uniform elements
  - ❑ I source
  - ❑ RLC elements
  - ❑ All data from DUT simulations
- Approach to issue:
  - ❑ Discretize die area
    - ➢ Mesh size is a function of transient frequency
  - ❑ Model components with spatial variance
    - ➢ Power demand
    - ➢ device decoupling
    - ➢ metal grid parasitics



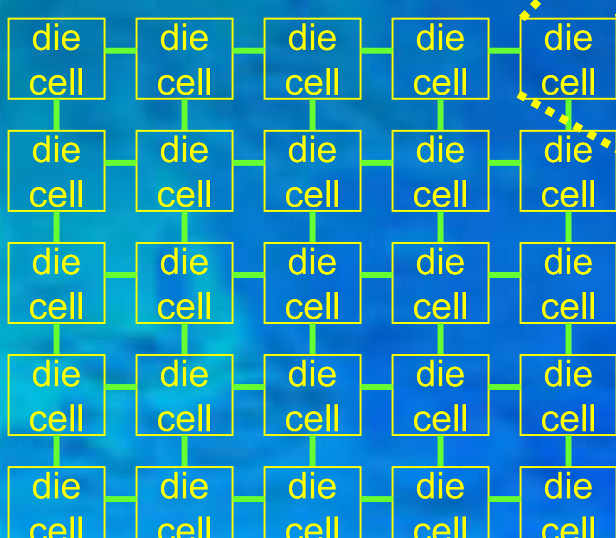
XY power map

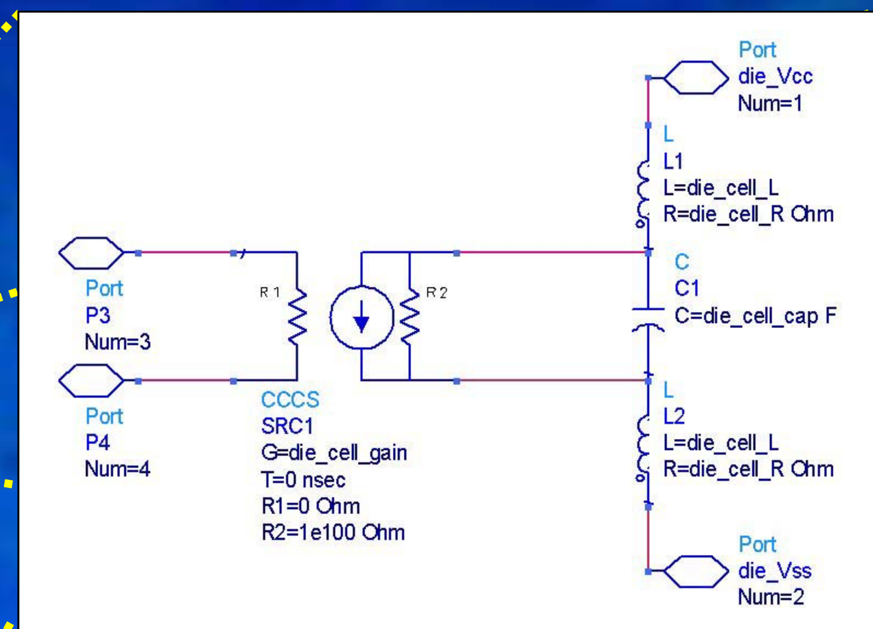


Discretized power map

Die cell model

- Typical model
  - ❑ Controlled Current Source
  - ❑ 'constant' current ramp
  - ❑ RLC parasitics
    - ➢ metal grid parasitics
    - ➢ decoupling

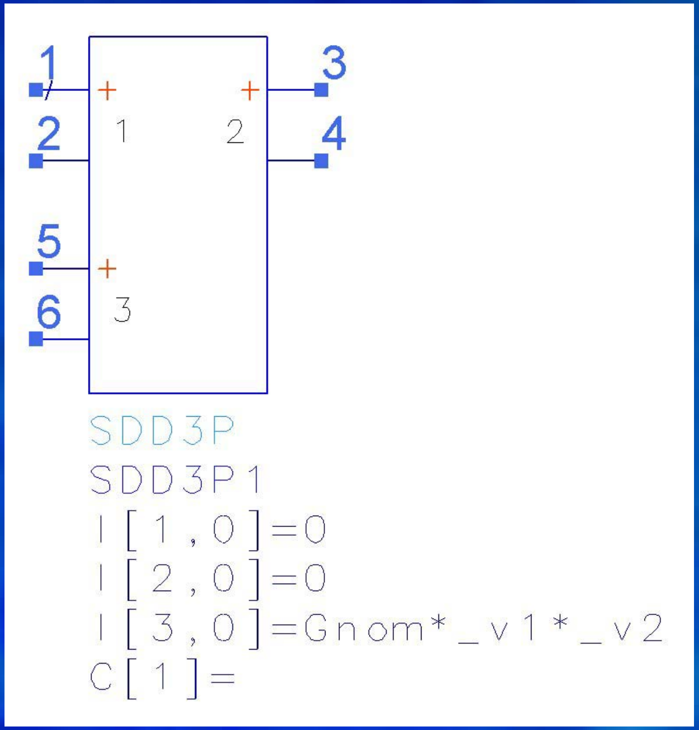




m x n array of die cells

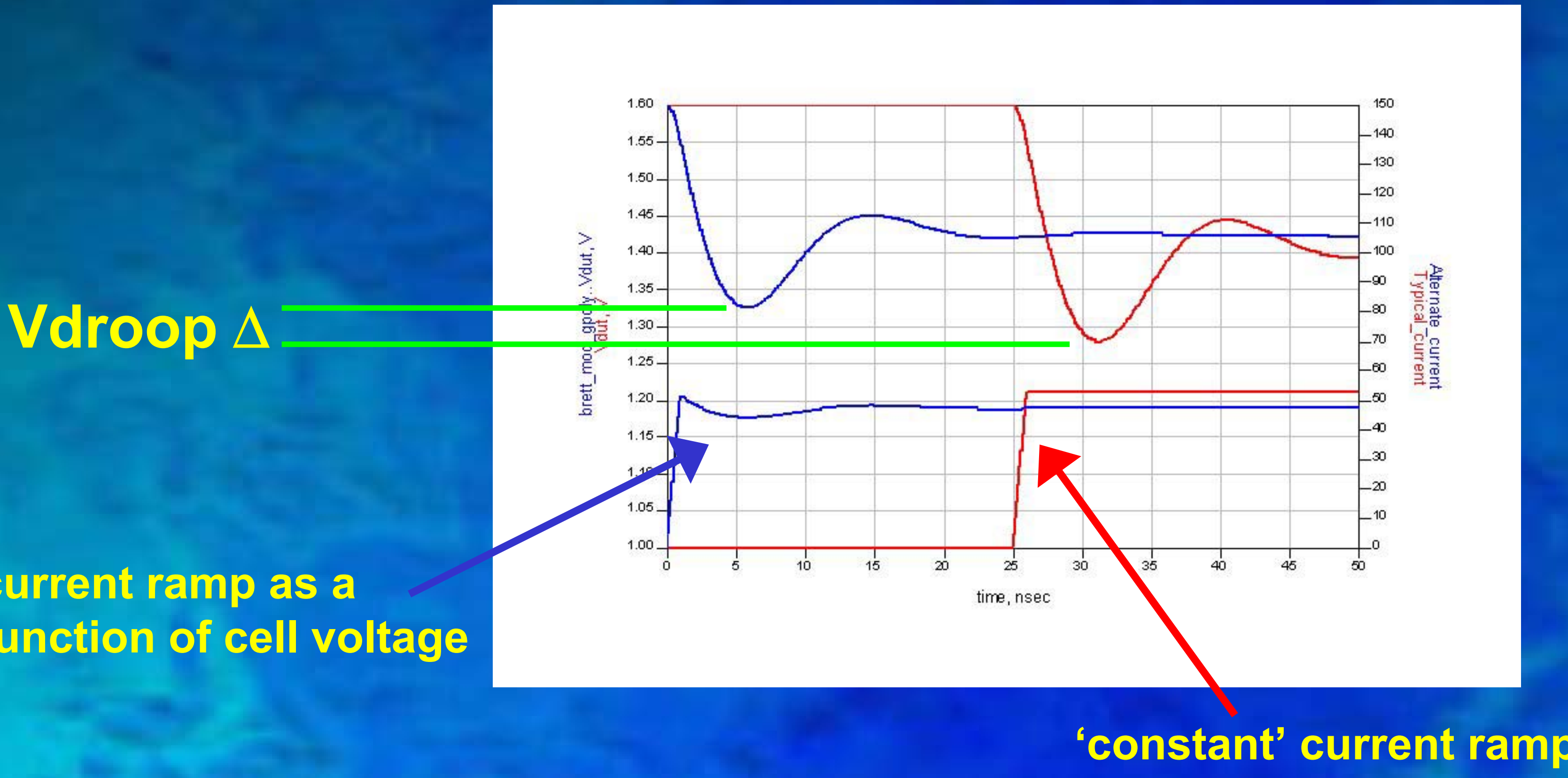
Die cell model

- Alternate model
  - Controlled current source
    - Control voltage into port 1
    - DUT voltage into port 2
  - RLC parasitics
    - still included though not illustrated here
  - Current ramp (port 3) is now a function of the instantaneous voltage across the cell



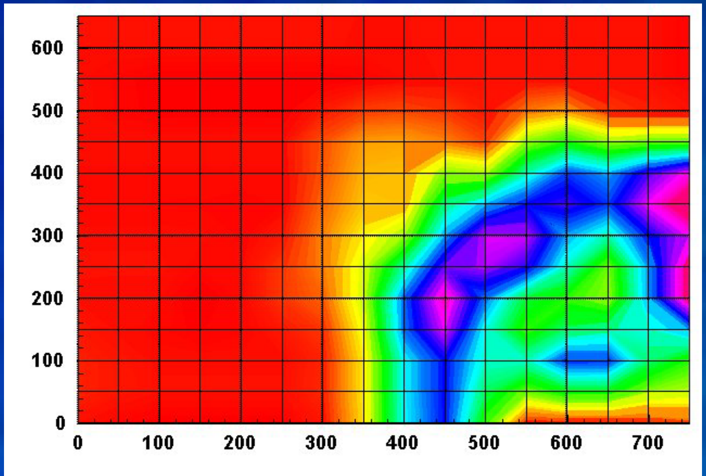
Die cell model

- Typical vs. Alternate model response

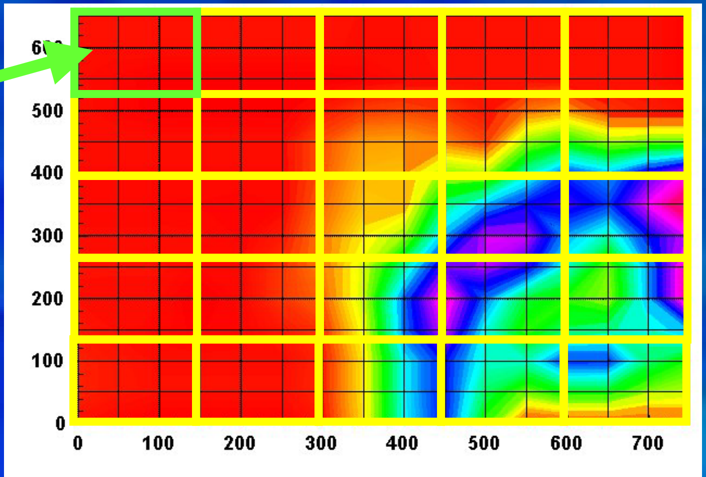


Understanding a solution – Probe level

- Probe cell definition
  - Meshed similar to the DUT
  - Cell modeled as probe pair w/ coupling
- Considerations:
  - Take advantage of fewer probes in low power area
  - Allow for increased probes in areas of high demand



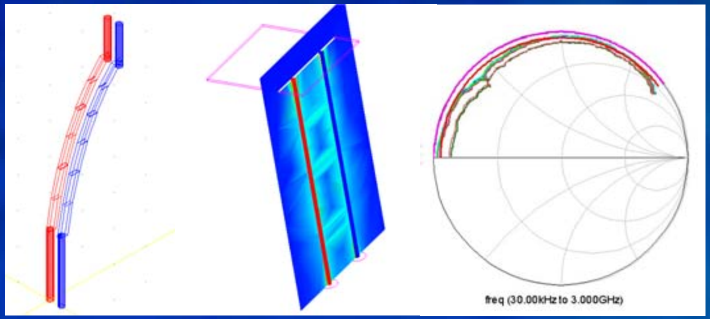
XY power map

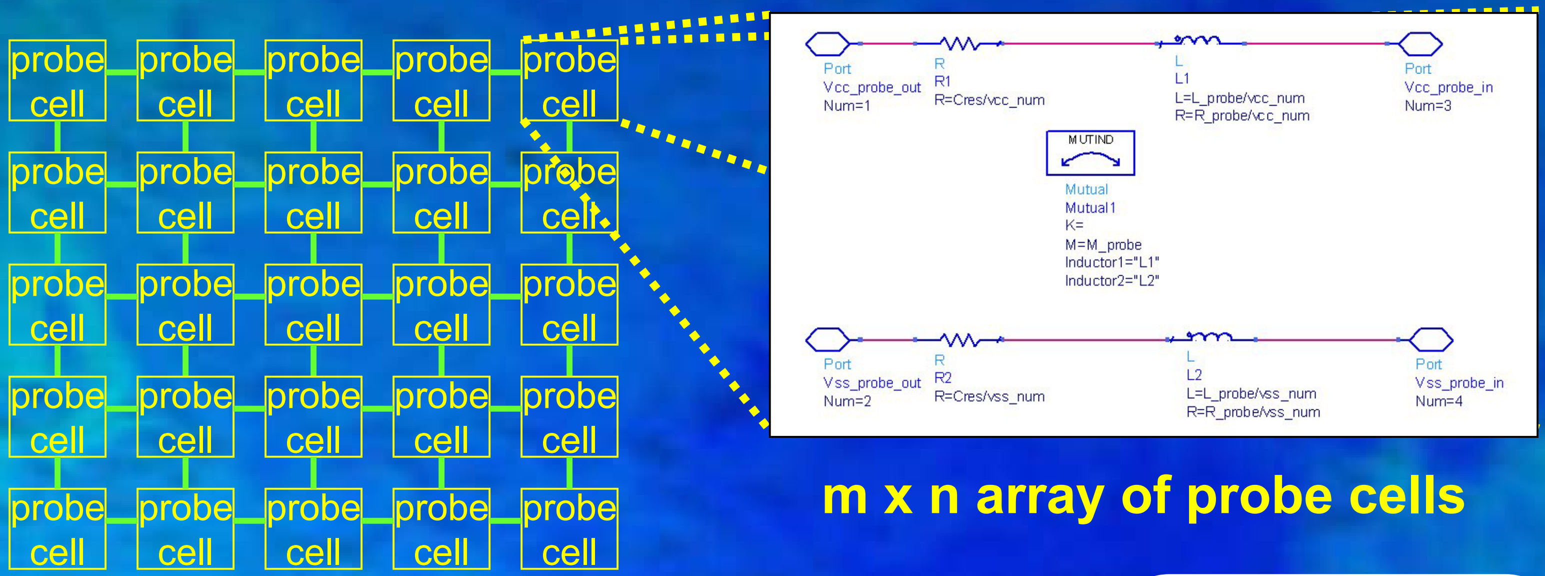


Discretized power map

Probe cell model

- Probe models
  - Probe styles fully characterized
    - Agilent 8753 VNA
    - 0.050 - 5.05 GHz
    - Custom fixturing

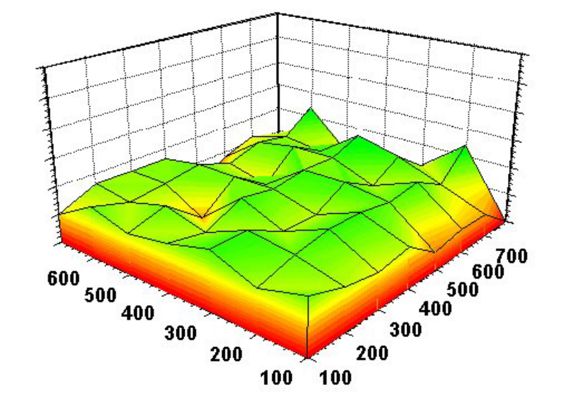




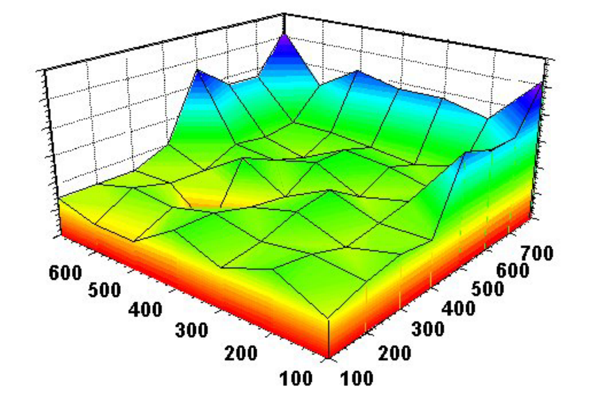
m x n array of probe cells

Probe cell model

- Probe uniformity
  - Currently do not probe every bump
    - 1 of 3, 1 of 5, 1 of 7…
  - Currently maintain a uniform probe array



Vcc probe distribution

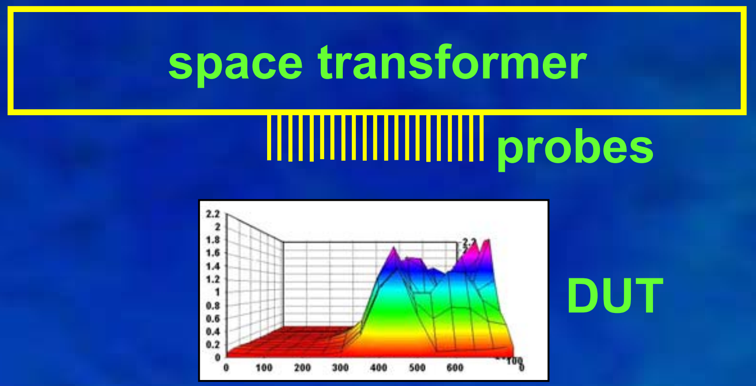


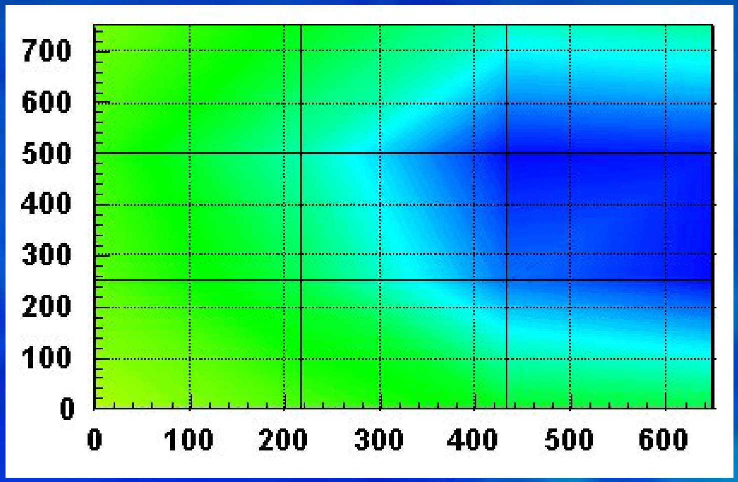
Vss probe distribution

  - Limits our ability to meet Vdroop targets
    - Increased resolution required

Understanding a solution – ST level

- Space Transformer
  - ❑ Space transformer expands the X-Y plane
  - ❑ It also serves to further distribute the effects of the current load
- Considerations
  - ❑ Internal power architecture
  - ❑ Decoupling capacitor placement

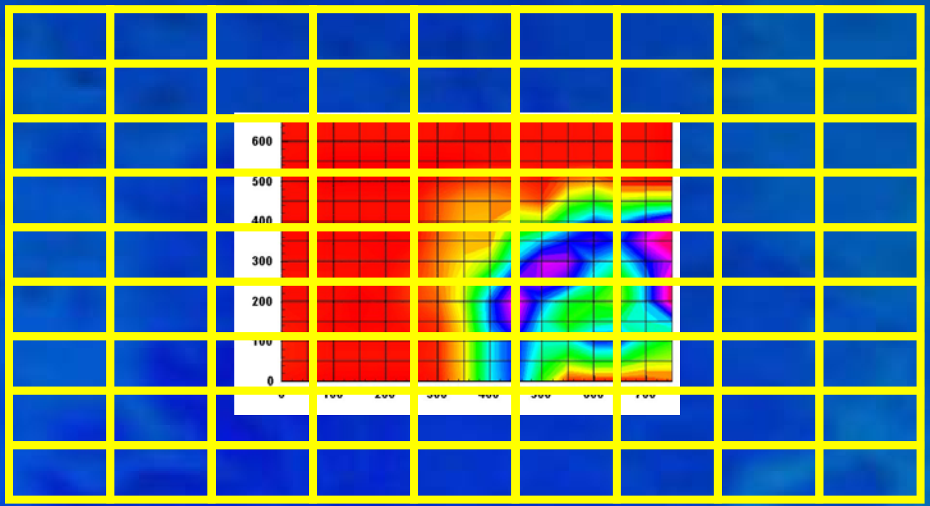




Space Transformer XY power map

Space Transformer cell model

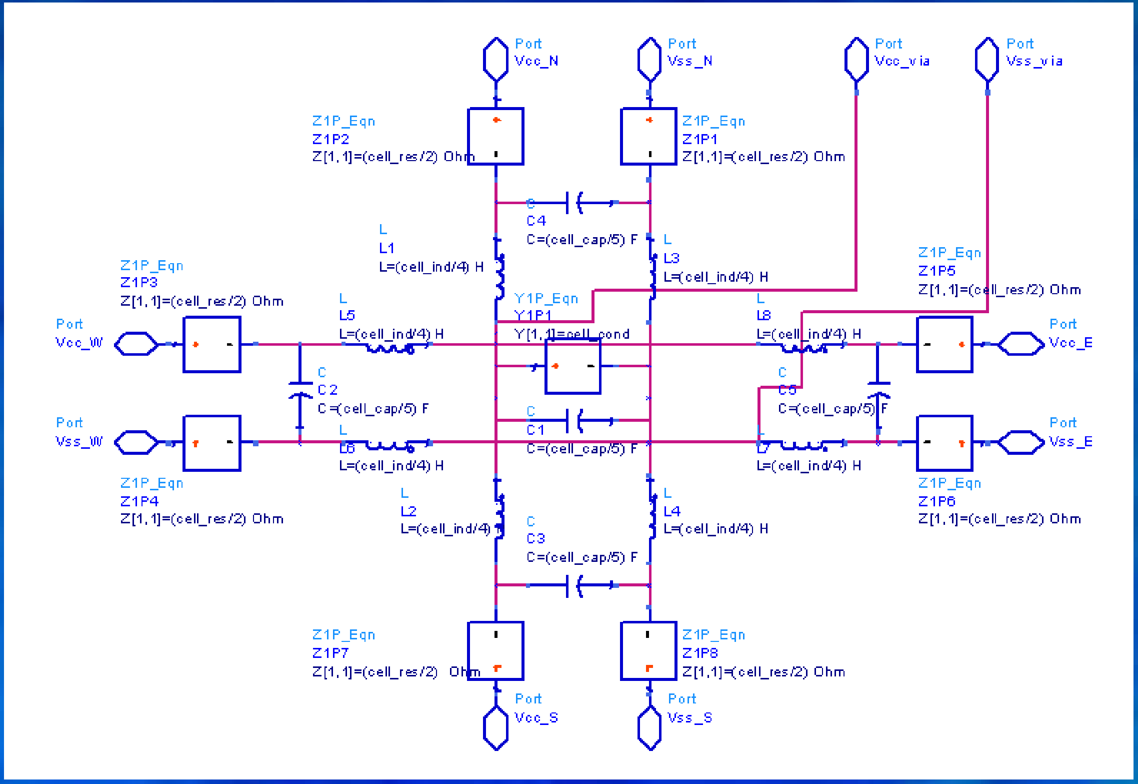
- ST Mesh
  - Mesh area is no longer confined to the die area
  - Continuing the same mesh as the die would produce a huge array
- Mesh size
  - Again determined as a function of transient frequency
  - Model reduction



Discretized power map

Space Transformer cell model

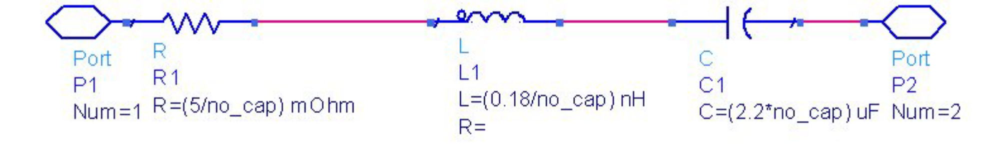
- **Plane cell model**
  - ❑ **Common RLC terms**
  - ❑ **Also includes freq. Dependent losses**
    - ➢ Skin effect
    - ➢ dielectric loss
  - ❑ **Don't forget the vias!**



- **Model elements**
  - ❑ **Validated with test vehicles**

Understanding a solution – other

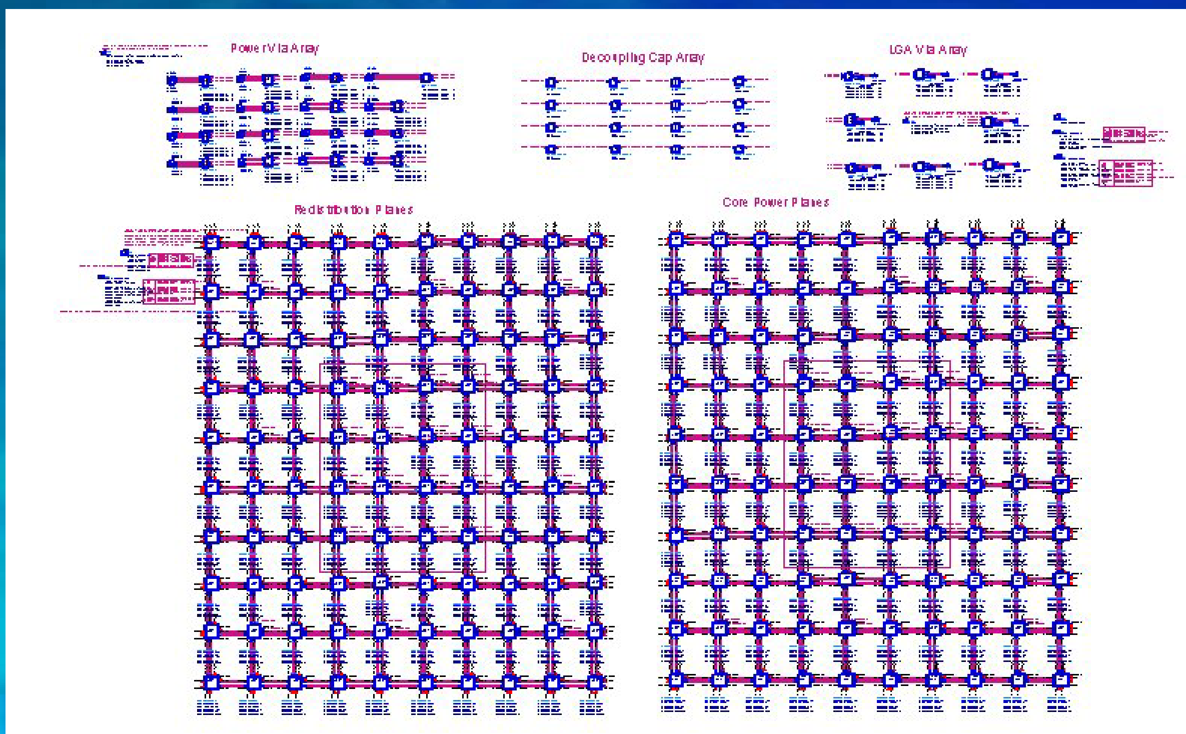
- Decoupling capacitors
  - ❑ Library of fully characterized parts
- PCB
  - ❑ Lumped model

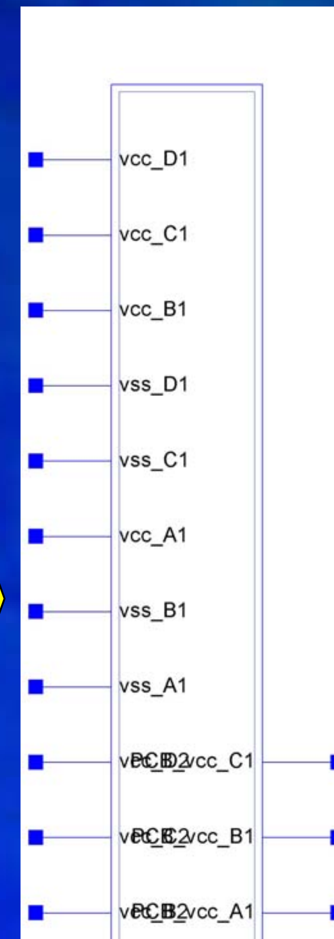


- ATE supply
  - ❑ Vendor provided model
  - ❑ Custom model

Bringing the model together

- Model assembly
  - Hierarchical
  - Large number of components in fully assembled model

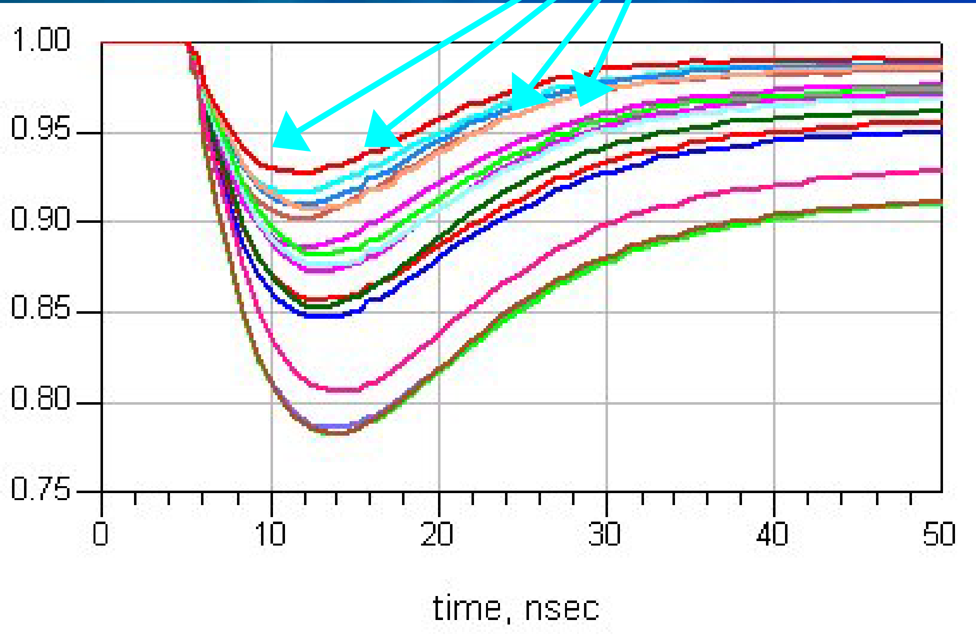


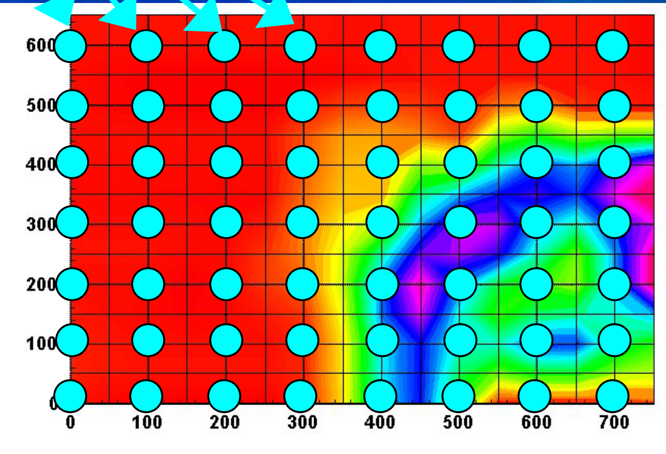


Distributed droop simulations

- Simulated Vdroop response

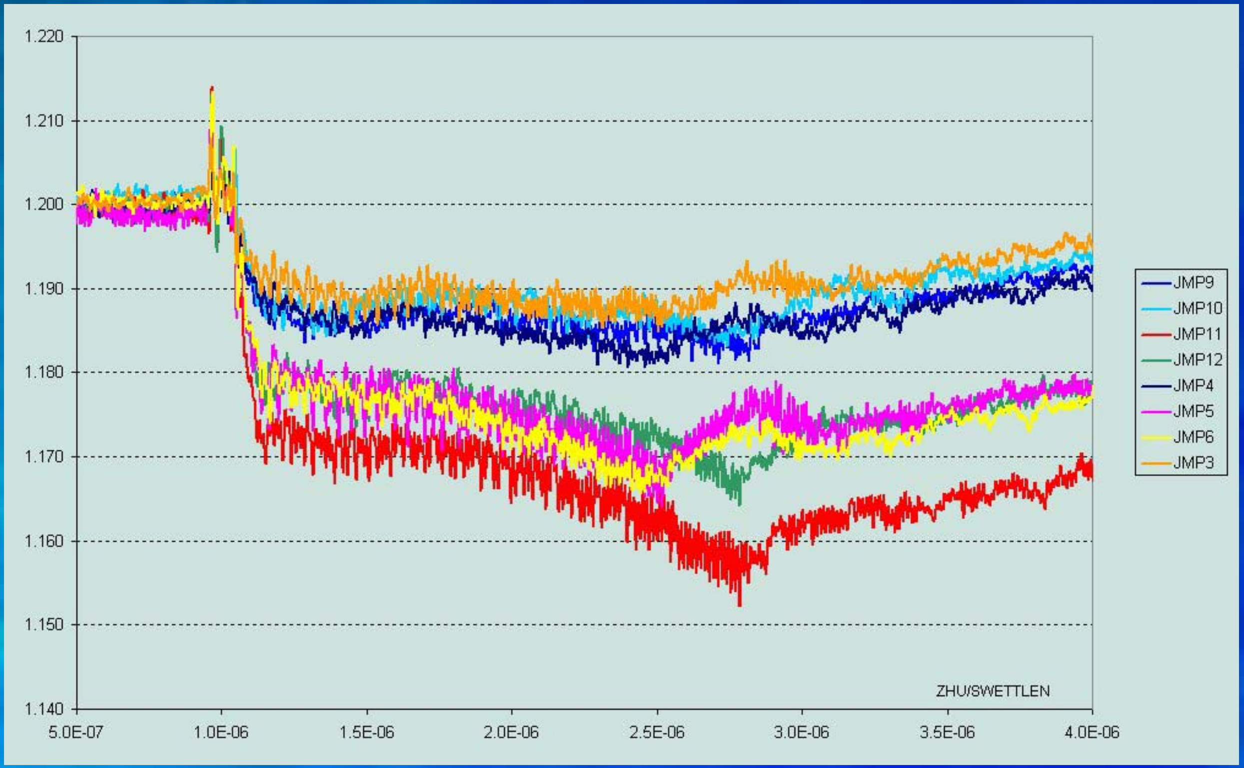
Response at m x n points across the array





Next Steps

- Improved model management
- Continued refinement
- Extending the model to multi-die applications



Summary

- Shrinking margins continue to drive refinements in power modeling accuracy
- Non-uniform power demand will further exacerbate this concern
- Question model assumptions, create measurement based models
- Distribute model elements in three dimensions

Acknowledgement

- We would like to recognize our colleagues Kevin Zhu and Sayed Mobin for their contributions to this project

References

- K. Lee and A. Barber, “Modeling and Analysis of Multichip Module Power Supply Planes”, IEEE Trans. on Components Packaging and Manufacturing Technology, Part B, Vol. 18, No. 4, Nov. 1995, pp. 628-639
- Henry Wu, Jeffery Meyer, Ken Lee, Alan Barber, “Accurate Power Supply and Ground plane pair models”, Proceedings of the 1998 Topical Meeting on Electrical Performance of Electronic Packaging, Oct. 1998, pp. 163-166
- M.A. Schmitt, K. Lam, L.E. Mosely, G. Choksi, and K. Bhattacharyya, “Current Distribution on Power and Ground Planes of a Multilayer Pin Grid Package”, Proceedings International Electronics Packaging Society, 1988, pp. 467-475
- Larry Smith, Tanmoy Roy, Raymond Anderson, “Power Plane Spice Models for Frequency and Time Domain”, Proceedings of the 9th Topical Meeting on Electrical Performance of Electronic Packaging, Oct. 2000, pp. 51-54