Enabling Parallel Testing at Sort for High Power Products

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Agenda

- Background
- Goals:
  - Interchangeability between a 1X and 2X SIU
  - Equivalent performance between a 1X SIU and a 2X SIU
  - Equivalent performance between "test site 1" and "test site 2" on the 2X SIU
- Challenges
  - Spatial Location of 2 DUTs
  - Space Transformer
  - Printed Circuit Board (PCB)
  - Interconnect and stiffening Hardware
- Results
- Minimal Deflections
- Power delivery
- Signal Integrity
- Summary

Background

- Parallel Testing is a manufacturing capability that allows multiple devices to be tested simultaneously.
- Parallel testing allows the user to improve output capacity of each test module by reducing the average test time
- Capability has existed at Intel for Flash Memory products since 1989.
- For High Power CPUs parallel testing (2X) aims to test 2 die at a time.
- Testing 2 CPUs at one time has been more challenging due to the high power demand and the complexity of the probe card design
- This presentation focuses on the work done to demonstrate the 2X probe card capability being applied to microprocessors

Project Goal

- GOAL:
  - To develop a robust 2X Sort Interface Unit (SIU) capable of intercepting high power microprocessors

- Fundamental criteria:

  Interchangeability and equivalent performance between the 1X and the 2X SIU

  - To eliminate the need to segregate test modules
  - To increase cost savings

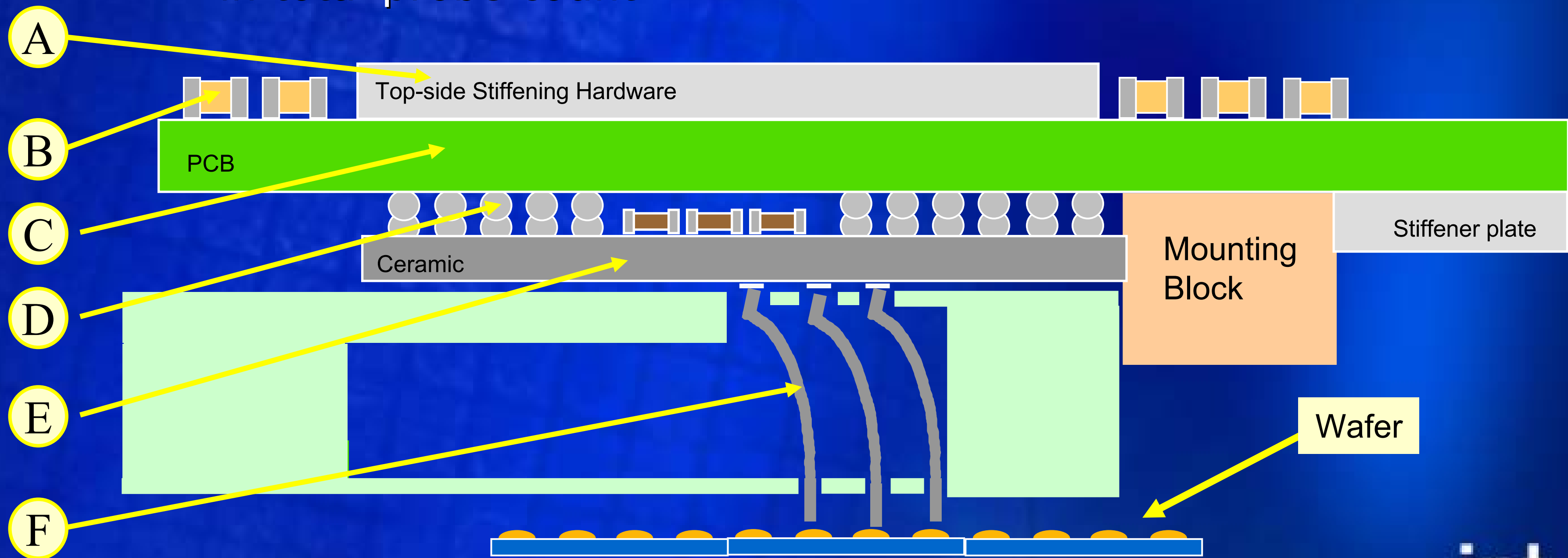
  Equivalent performance between “test site 1” and “test site 2” on the 2X SIU

  - To reduce test pattern development

- Boundary conditions
  - Similar shape, size and functionality of the probe card
  - Equivalent power delivery and routing integrity

Challenges

Magnitude of change	
Minor	A. New Stiffener: To accommodate larger MLC
Minor	B. Bulk decoupling: New location and improved components
Mix	C. PCB: Split power planes for isolation
Major	D. Interconnect: Increase in physical size and LGA count
Major	E. Space Transformer: Split plans, new stack, larger in size
Minor	F. Probes: Same as current probe selection, but marginal increase in total probe count



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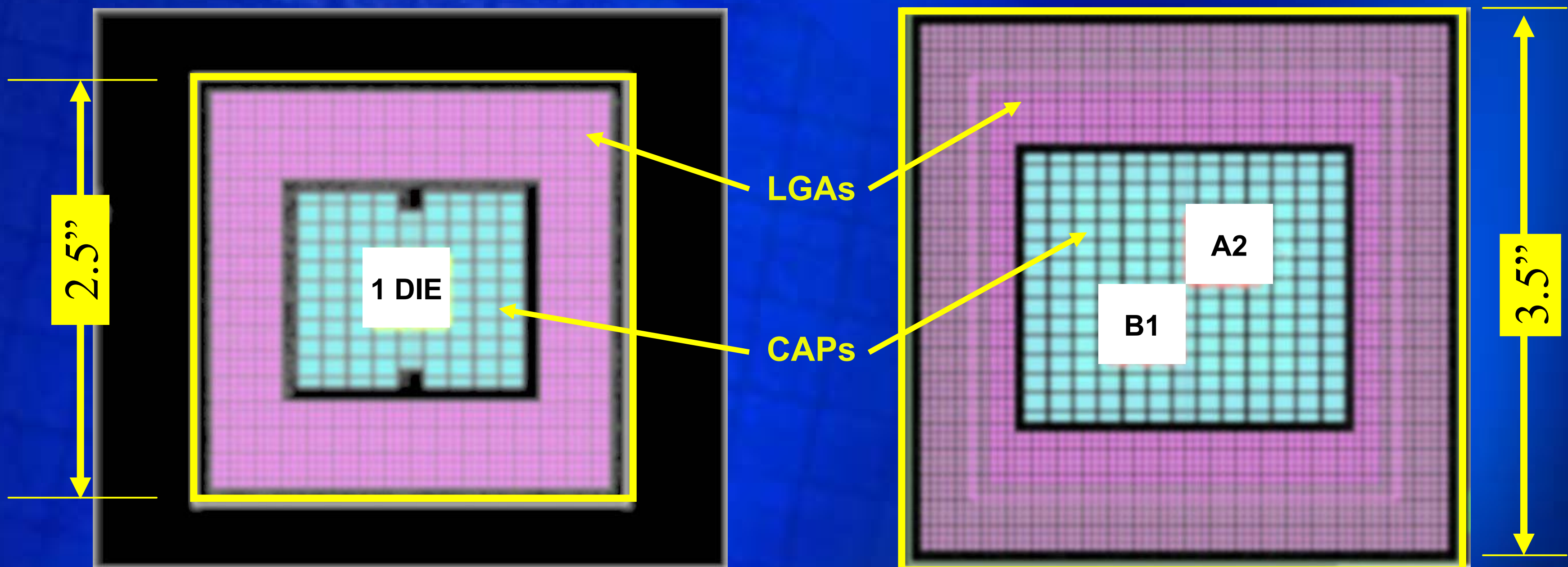
Comparison of noted 1X and 2X SIU differences

Noted Differences Short list	**1X Configuration**	**2X Configuration**	**1X Envelope**
Wafer Level contacts • # of contacts	 ~ 1600 total	 ~ 3200 total	 ~ 3000 total
Glass Ceramic ST • # of I/Os •Routing Technology •Dimensions •Decoupling	 ~ 125 total 2 layers ceramic 2.5 x 2.5 x 0.150” ~ 90 caps total	 ~ 250 total 1 layer Thin Film 3.5 x 3.5 x 0.150” ~ 180 caps total	 ~ 300 total Mixed 2.5 x 2.5 x 0.150” ~ 90 caps
Printed Circuit Board • # of layers • Thickness • LGA	 22 0.187” ~ 1300 total	 24 0.187” > 2500 total	 22 0.187” > 2500 total

Thin Film Space Transformer

- Equivalent performance challenges most pronounced in ST
- Power delivery of ~ 60 W per DUT
  - Larger space to allow adequate decoupling and power plane area.
- Signal routing: escape routing of 128 channels per design
  - Thin Film allows fine line widths to be fabricated.
- A2/B1 alternatives: More space w/ constraints: scribe width, planarity



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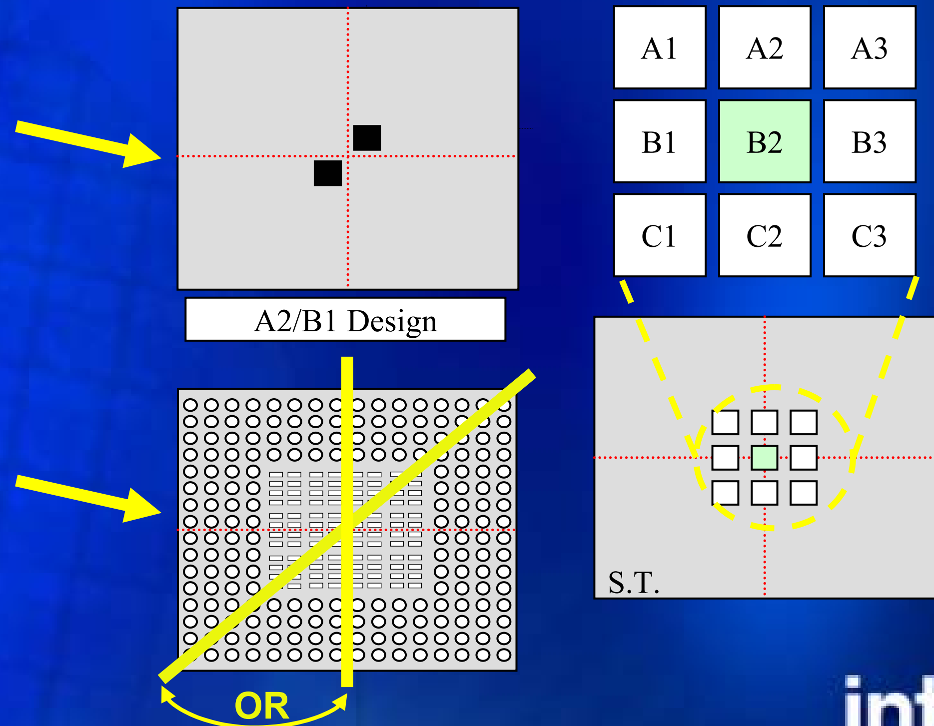
Interconnect and Space Transformer (ST)

- ST area would be increased by ~80%
  - Increased LGA count to >2500 at the PCB interface
    - Required development of an interconnect solution
- ST would need to provide independent power delivery systems
  - No shared power planes
  - No shared reference (Ground) planes
  - Routing rules needed to be defined to maintain Signal integrity
  - Increased # of decoupling capacitors, locations not as ideal
- Location of two DUT arrays given the above constraints
  - Where to locate the two arrays with respect to each other

Spatial Location of the two DUT's

- Flexibility in choice
  - A 3x3 maximum array area was assumed possible
- Trade off analysis: SIU manufacturing, routing, power delivery, die isolation, heat dissipation and a sort de-rating study that considered wafer stepping impacts with different patterns
- A diagonal side-by-side pattern was considered to be the best solution to all constraints
  - Sites A2/B1
- Splitting the power planes
  - Consider power delivery
  - Consider decoupling



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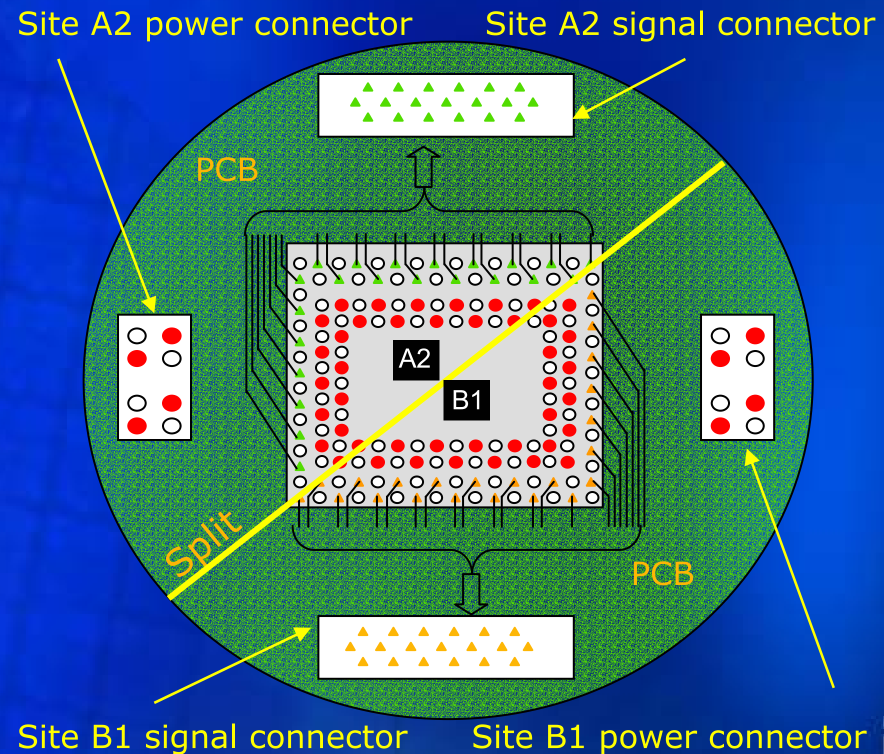
Printed Circuit Board

- Interchangeability with the 1X SIU: Same PCB thickness
- Power delivery: Two more power planes (Vcc) required.
  - Modified the PCB stack-up by decreasing dielectric layer's thickness to add two planes.
- Signal Routing: 128 per DUT in 6 layers required
  - Orientation site A2/B1 to its appropriate tester Connectors
  - Forcing signals to the outer rows of the LGA pattern of the S.T. helped ease the routing



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Interconnect Solution Selection

- Trade off analysis: Reflow Heat, CTE mismatch, planarity and thinner ST

Interconnect	Button Interposer	BGA	PGA
What it is	Pogo interposer	Ball Grid Array of Pb/Sn solder balls	Pin Grid Array of gold plated Kovar pins
Heat to attach pins/balls	N/A	Up to 225 C	Up to 800 C
Planarity improvement	< 2.0 mils	< 2.0 mils	< 2.0 mils
Compatibility w/thinner ST	No	Yes	Yes
50 mil pitch achievable	Yes	Yes	No

PCB Mechanical stiffener

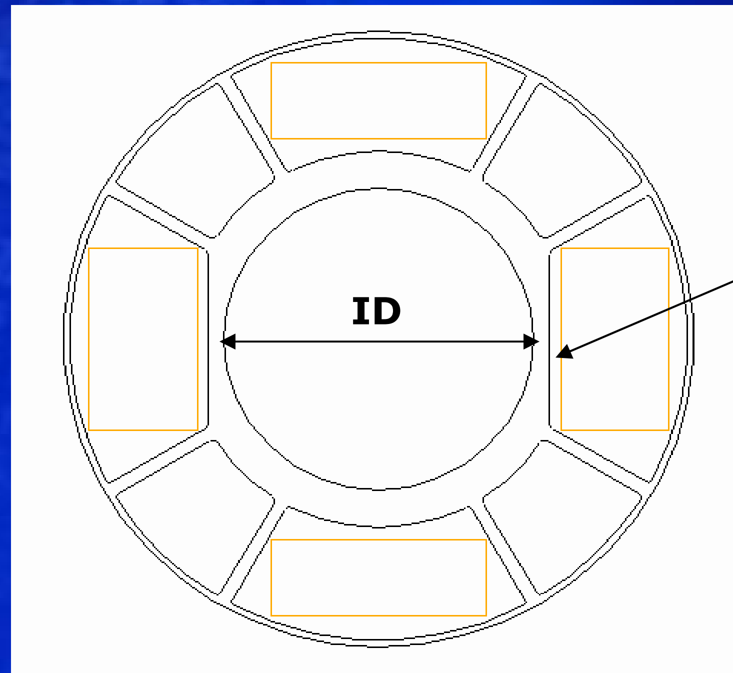
Requirements to meet:

-Fit in a larger ST

-Increase ID of mounting hardware keep out zone

-Limit 2X stiffener thickness changes to control/reduce deflection

-Maintain clearance for tester cable connections.



Clearance

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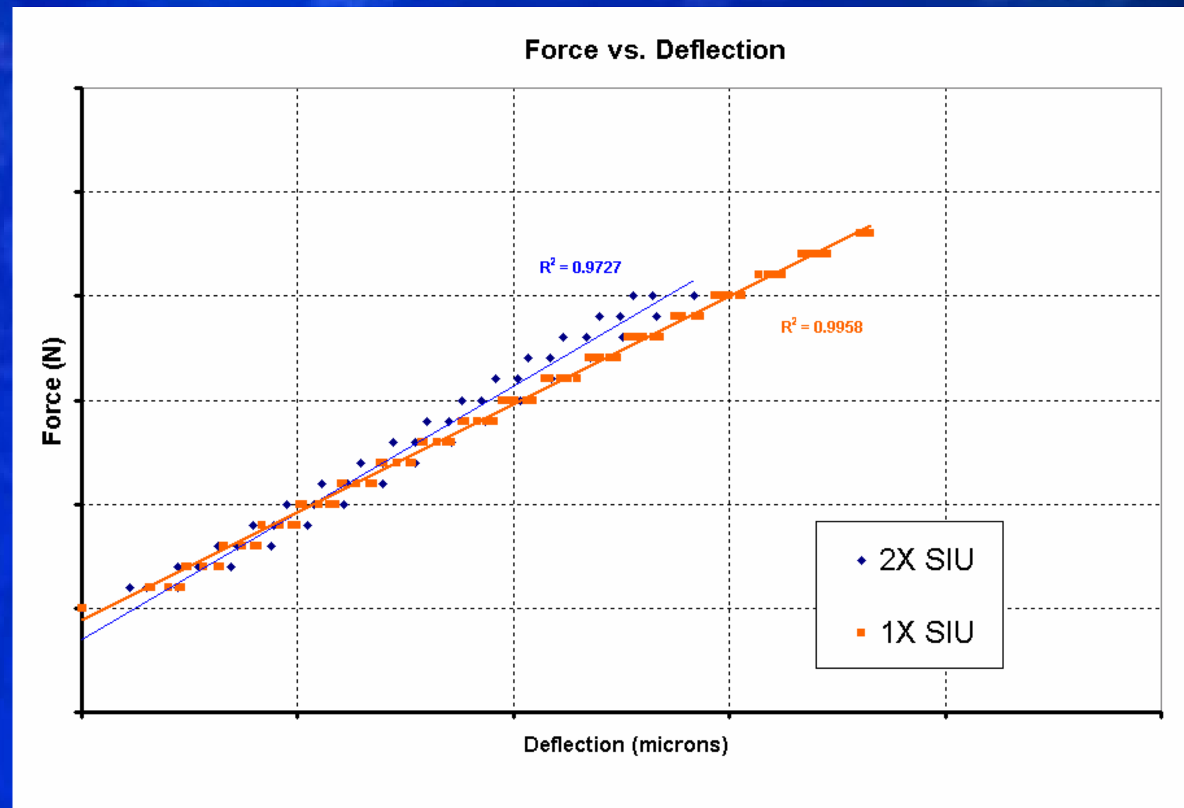
Deflection Data

- Preliminary data collected on 1 tool, using a deflection measurement system, show signs of reduced deflection.

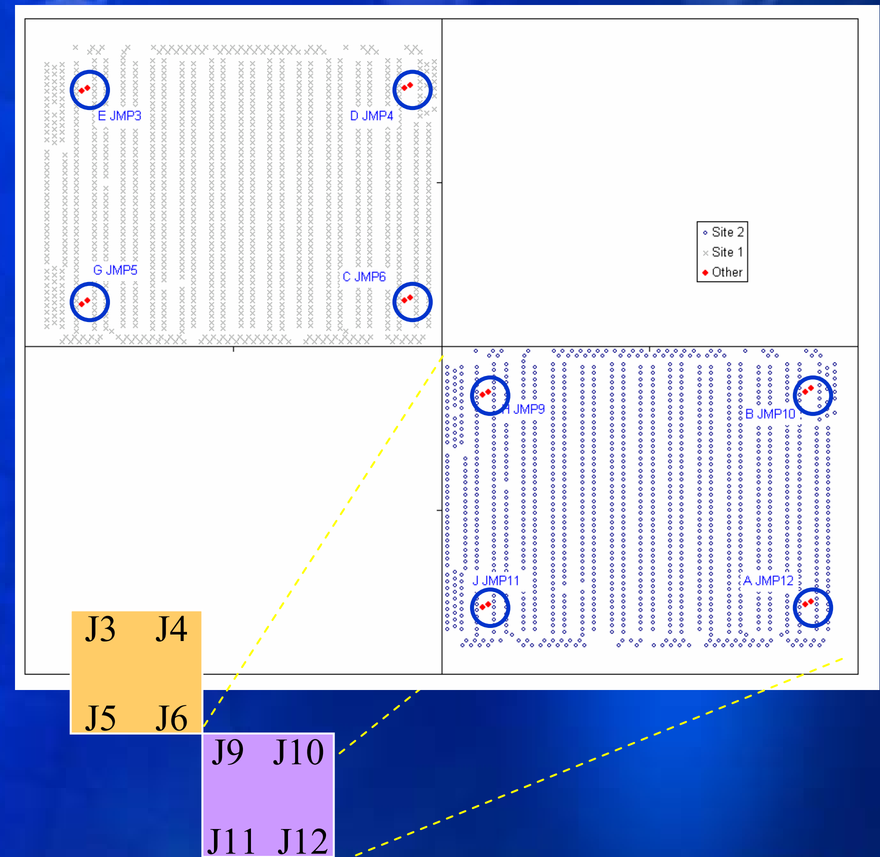
- More data needed to improve accuracy of best fit line (R^2) and to better assess repeatability and reproducibility



The Measurements… what we did

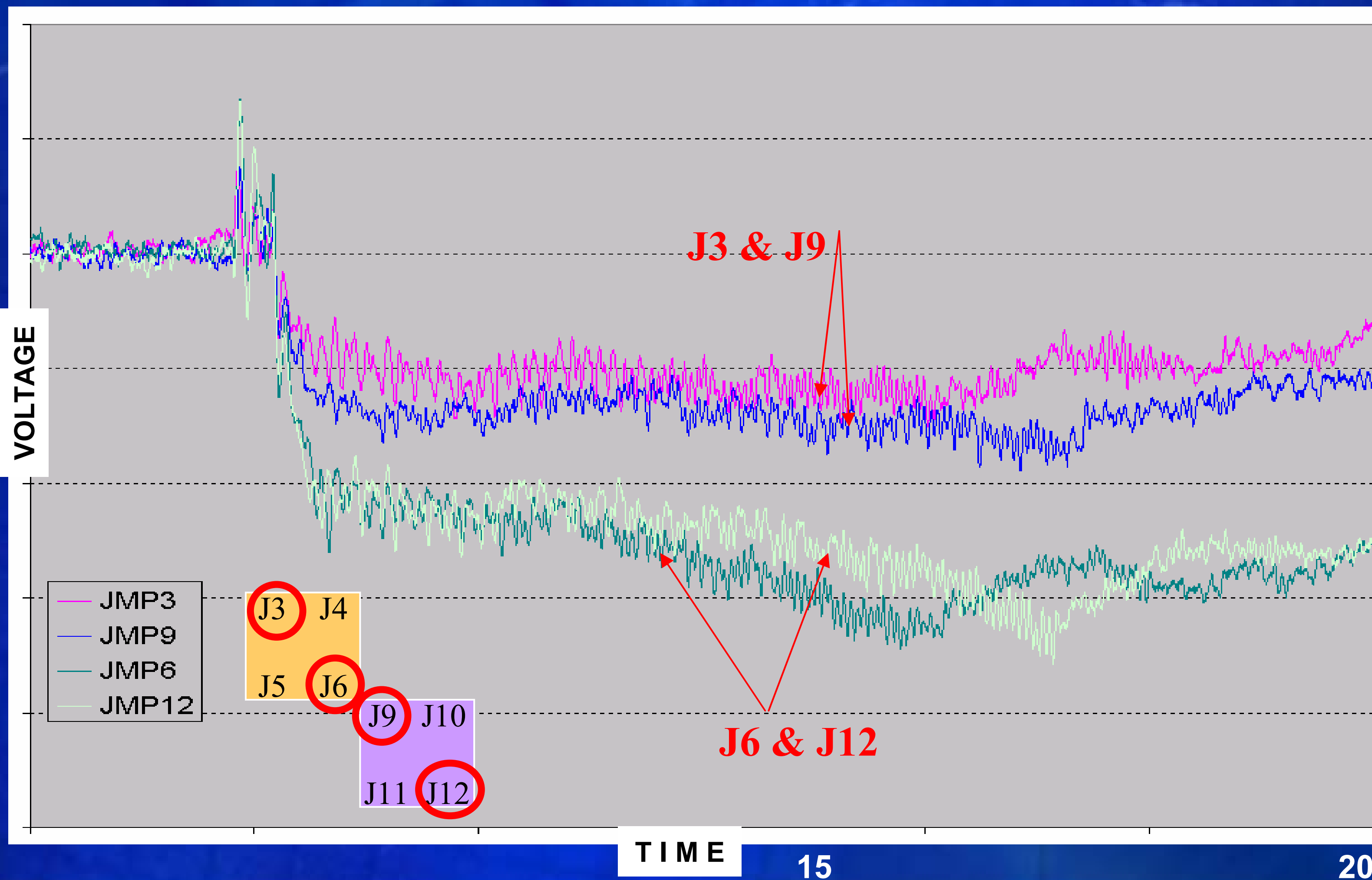
- 8 measurement points
  - 4 per DUT
  - Measure voltage at the DUT
  - Provide ability to block non-uniform demand of the DUT

- Measured with
  - Site 1 “ON” and Site 2 “ON”
  - Site 1 “ON” and Site 2 “OFF”
  - Site 1 “OFF” and Site 2 “ON”



Performance Results

- Within site a large variance, but site to site well matched



Site 1 = “ON”
Site 2 = “ON”

DUT running
> 1.0 GHz

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Performance Results, Cross talk

- No measurable coupling of energy between sites

J11 J9

yyJMP11
yyJMP9
yyJMP6

0.06
0.05
0.04
0.03
0.02
0.01
0
-0.01
-0.02

VOLTAGE

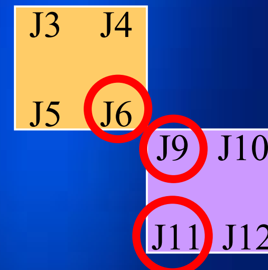
TIME

J6
Plotted on Right scale

Site 1 = "OFF"
Site 2 = "ON"

DUT running
> 1.0 GHz

0 V; no energy coupled site to site



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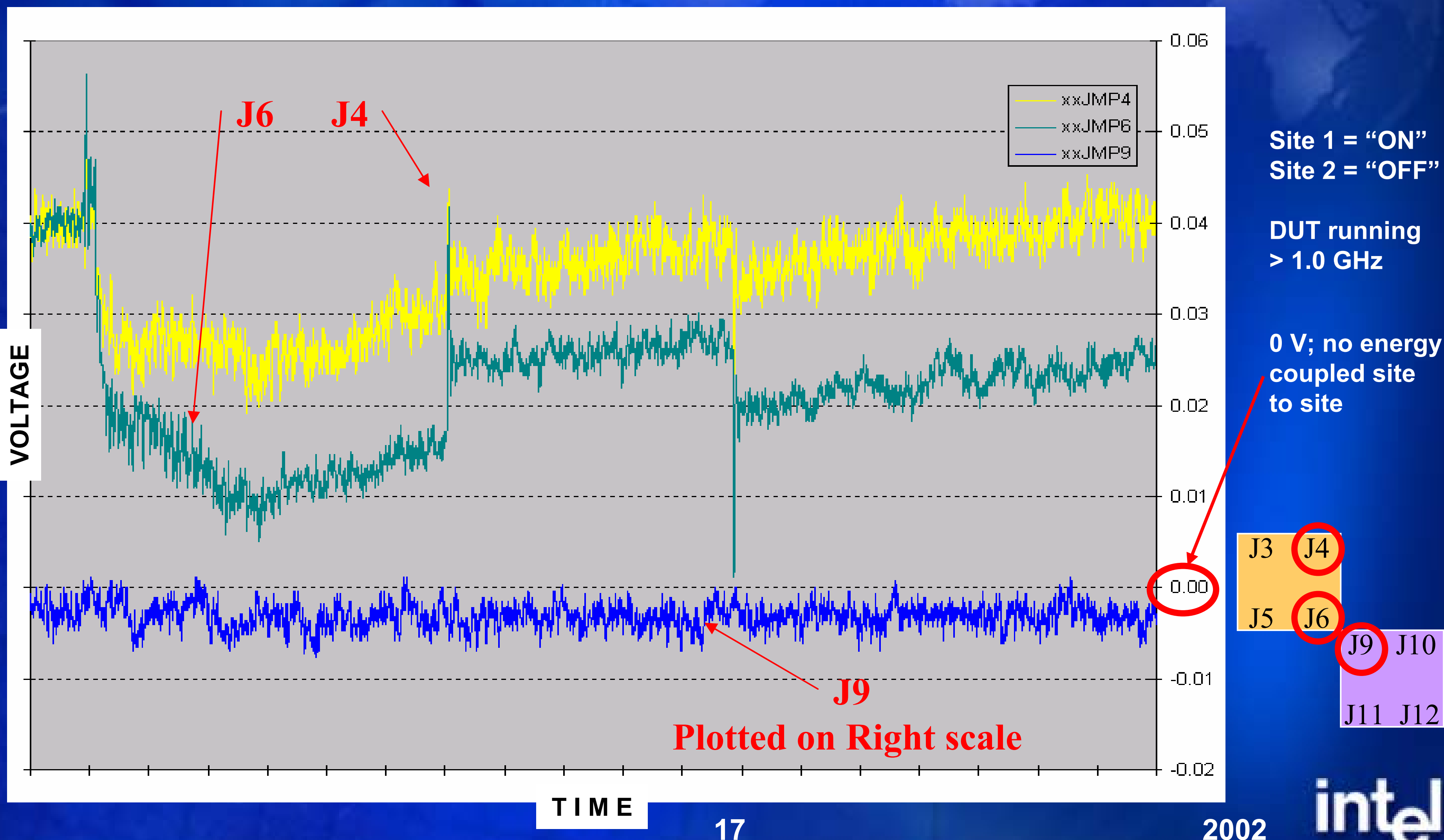
Performance Results, Cross talk

- No measurable coupling of energy between sites



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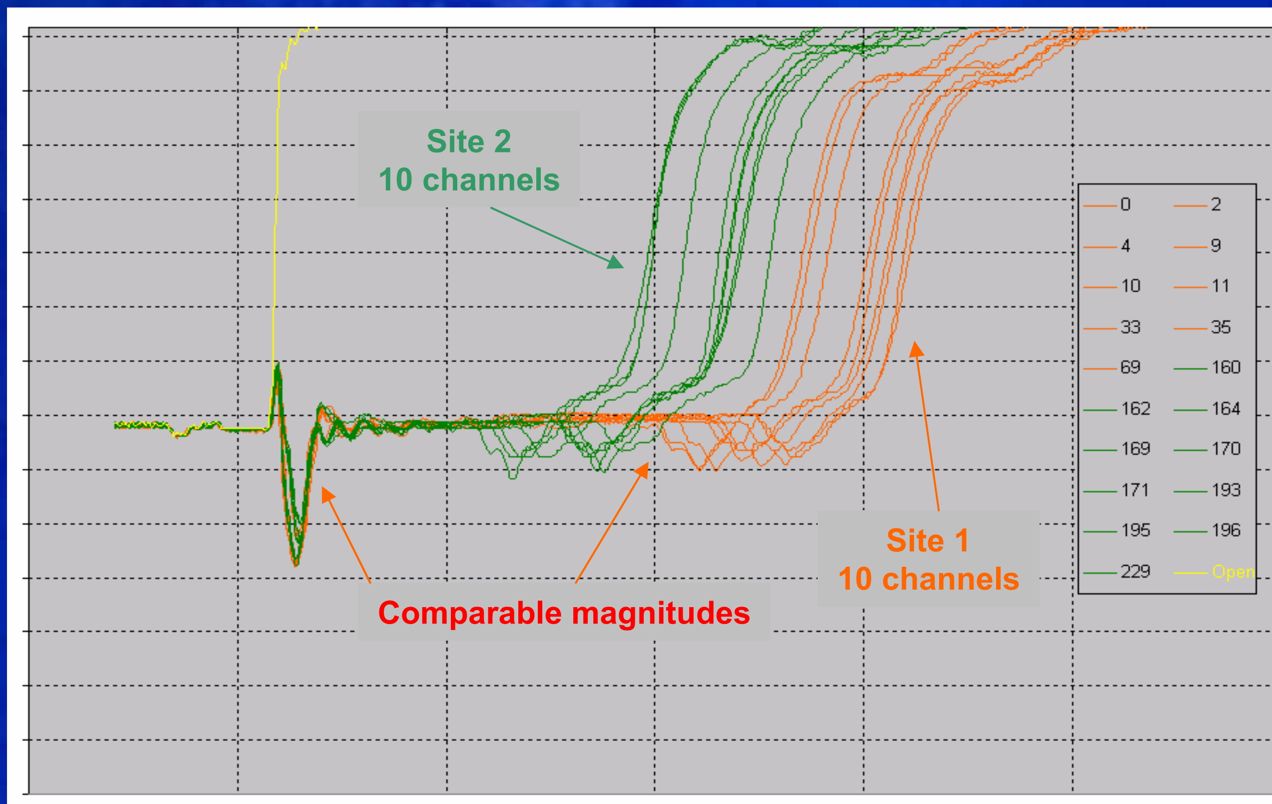
Signal integrity between sites

- TDR of 10 traces on both sites
  - Lengths are different, but this is compensated by the ATE
    - Worst channels shown



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Summary

- To date the 2X SIU development is progressing at or beyond expectations
  - Metrology system check out passed with no issues
  - Sort performance data shows 2X card progressing well
    - Small "hick-ups" still need to be worked on
  - Improvements to the SI path planned, but not critical (yet)
  - More characterization work to be completed
  - Progressing well against slide four goals

Acknowledgement

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Thank YOU!