### Presentation to Southwest Test Workshop 2002

### Using MLOs to Build Vertical Technology Space Transformers

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### Overview

- 1. Terminology
- 2. Benefits of MLOs vs MLCs
- 3. MLO Basics
- 4. MLO Variables
- 5. MLO Manufacturing Challenges
- 6. Processing MLO for Use as Space Transformer
- 7. Test Verification
- 8. Reliability
- 9. Performance Data
- 10. Conclusions

# Terminology/Acronyms

- 1. ST Space Transformer
- 2. MLO Multi Layered Organic
- 3. MLC Multi Layered Ceramic
- 4. BGA Ball Grid Array
- 5. FR4 Fiber Glass
- 6. ePTFE Expanded Polyetraflouroethylene
- 7. C<sub>RES</sub> Contact Resistance
- 8. C4 Controlled-Collapse Chip Connection
- 9. CTE Coefficient of Thermal Expansion

10. OSP – Organic Solderability Perservative

# **Benefits of MLO vs MLC**

- 1. Design/Manufacturing Time
  - i. MLO customer supplied at time of order
  - ii. MLC lead time of up to three months

# **Benefits of MLO vs MLC**

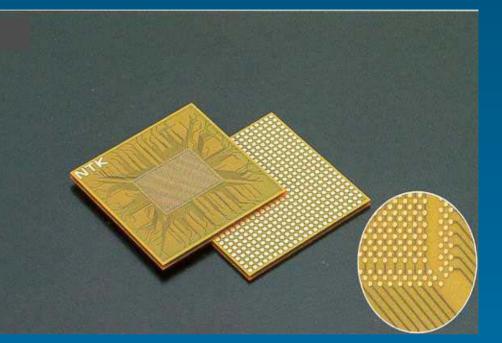
#### 2. Cost

- i. Typical MLO package \$15 \$50
- ii. Custom designed MLC NRE \$10,000 -\$15,000, \$5,000 – \$10,000 each (10 piece minimum)
- 3. Tighter Pitches (BGA side)
  - i. Minimum pitch MLC 1.0 mm (typical)
  - ii. Minimum pitch MLO 0.6 mm (typical)

### **MLO Basics**

### Application "Flip Chip" Packaging for

- 1. Microprocessors
- 2. ASICs
- 3. DSPs
- 4. Memory Flash and DRAM



### **MLO Basics**

- 1. Design: Determined by customer's packaging group
- 2. Vendors
  - i. 3M (W.L. Gore)
  - ii. IBM
  - iii. Fujitsu
  - iv. Ibiden
  - v. Kyocera
  - vi. NTK

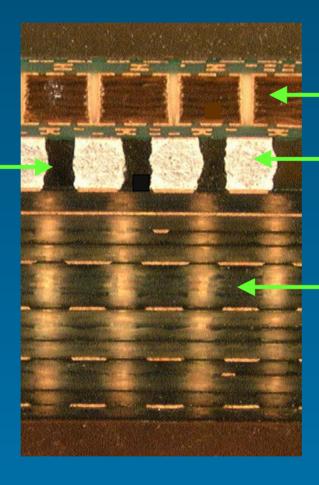


### 3. Composition

- i. FR4 most commonly used fiberglass-type material
- ii. ePTFE newer material
  - 1. resin composite uniform structure throughout
  - 2. better machinability with laser
  - 3. better CTE matching
  - 4. ideal for dense arrays, tighter pitch size device side

### **Typical MLO Assembly**

#### Underfill



# MLO Solder paste and spheres

PCB

### **MLO Variables**

- 1. Thickness
- 2. BGA Pitch
- 3. Pad Composition
- 4. Solder Mask Opening
- 5. Metal Stiffener Rings
- 6. C4 Pitch
- 7. Flatness

#### Structural integrity

- Problem BGA pattern voids under C4 area
- Solution Underfill on BGA side

### **BGA** Pitch

- Problem Accommodate smaller pitch requirements
  - 1.27 mm past
  - 1.00 mm today
  - 0.80 mm soon
  - 0.60 mm future
- Solution Create custom fine pitch solder stencils

#### Pad Composition

- Problem OSP and solder on pads
- Solution Remove and plate with nickel and gold

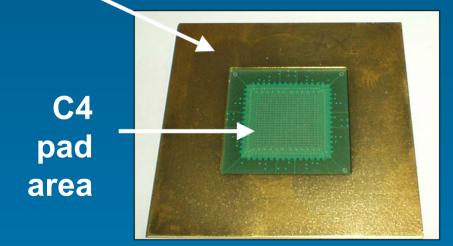
#### Solder Mask Opening

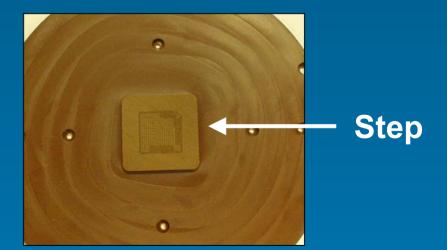
- Problem Solder mask opening too small
- Solution Remove solder mask (proprietary process)

#### Metal Stiffener Ring

- Problem C4 pads recessed below stiffener
- Solution Stepped Cobra® head

#### Stiffener





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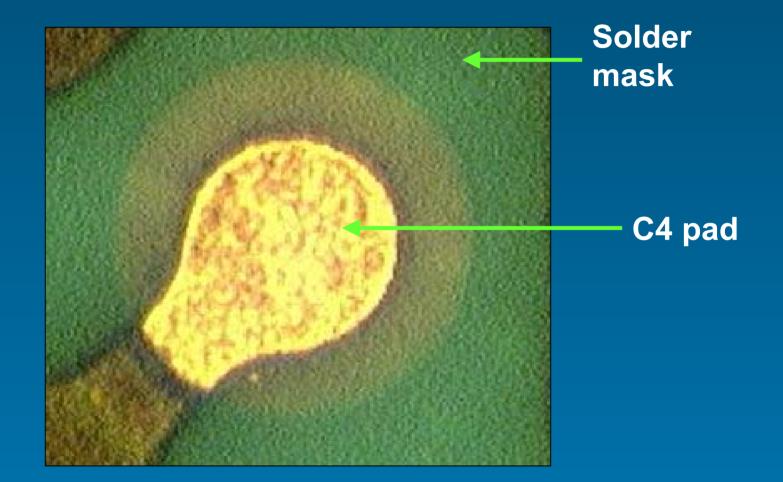
#### C4 Pitch

No issue with current fine pitch contact technology

#### Flatness

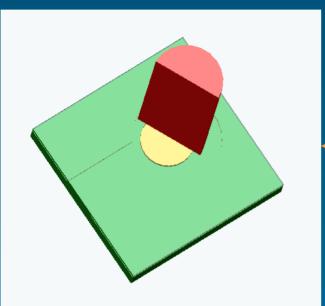
- Problem Warping of extra-thin MLOs
- Solution Custom lap at assembly

### **Processed C4 Pad**



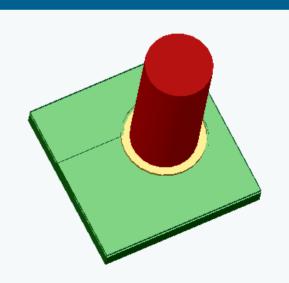


### **MLO Processing**



#### Unprocessed MLO – soldermask still on pad area

Processed MLO – solder mask cleared from PAD area



### **MLO Processing**



Remove solder mask exposing pad
 Nickel and gold plate

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### **Post-Processing Inspection**

- 1. Visually inspect C4 pads for damage
- 2. Verify alignment of C4 pads within .0003" in true position
- 3. Measure flatness of C4 area .0005"or less
- 4. Measure flatness on entire MLO .0015" or less
- 5. Test for allowable leakage <5 nA @5VDC

# **Bonding MLO on Probe Card**

### **BGA** Attach

- 1. Equipment:
  - i. Solder Stencil Printer apply solder to BGA pads
  - ii. Programmable Reflow Oven



Fixturing:
i. BGA Alignment
Placement Tool
align and place
MLO to PCB



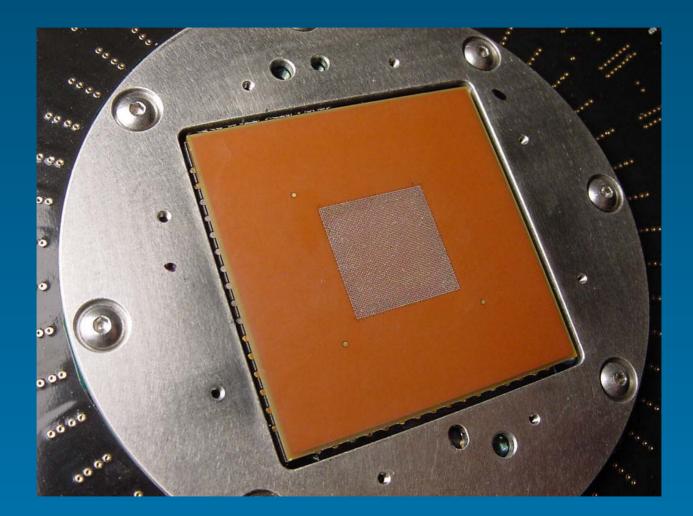


# **Bonding MLO on Probe Card**

### **BGA Attach Techniques**

- Apply solder paste and solder spheres to BGA pads
- 2. Reflow solder
- 3. Apply solder paste to PCB
- 4. MLO aligned and placed on PCB
- 5. Reflow the assembly in programmable oven
- 6. Apply underfill to MLO
- 7. Inspect

### **Completed Space Transformer**





# **Verification of Probe Card**

### **Final Assembly Test**

- 1. Leakage
- 2. Bulk Planarity
- 3. Overdrive leakage
- 4. Alignment
- 5. Full planarity & CRES
- 6. Wire Check
- 7. Components

### **Performance Data**

#### **Typical Pad Wear**

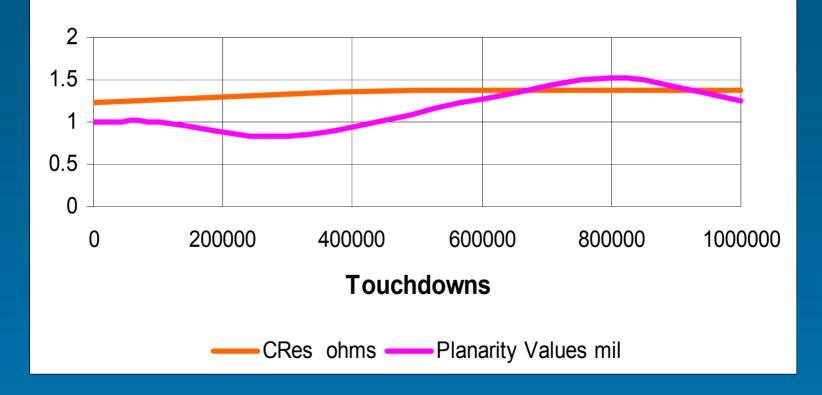
#### 1 million touchdowns

Initial-



### **Performance Data**

MLO Lifetime Performance as Measured by Path Resistance and Planarity



# Conclusion

#### MLO/ST technology benefits:

- 1. Fast turnaround as compared to customdesigned MLC
- 2. Lower cost probe card cost due to lower ST costs
- 3. Closer match to actual "real world" application due to similarity of materials
- 4. Performance equal to more expensive MLCs
- 5. Ideal, cost-effective solution for short-runs of ASICs and other specialty devices