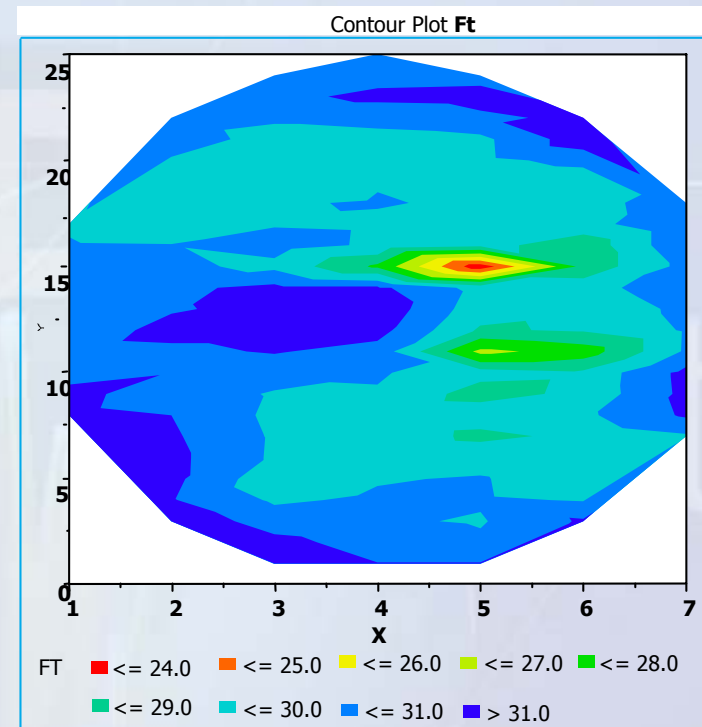




RF S-Parameter Wafer Probing – A Production Solution

Bill Knauer
Keithley Instruments
Tel: 440-498-3053
Email: knauer_bill@keithley.com



Agenda

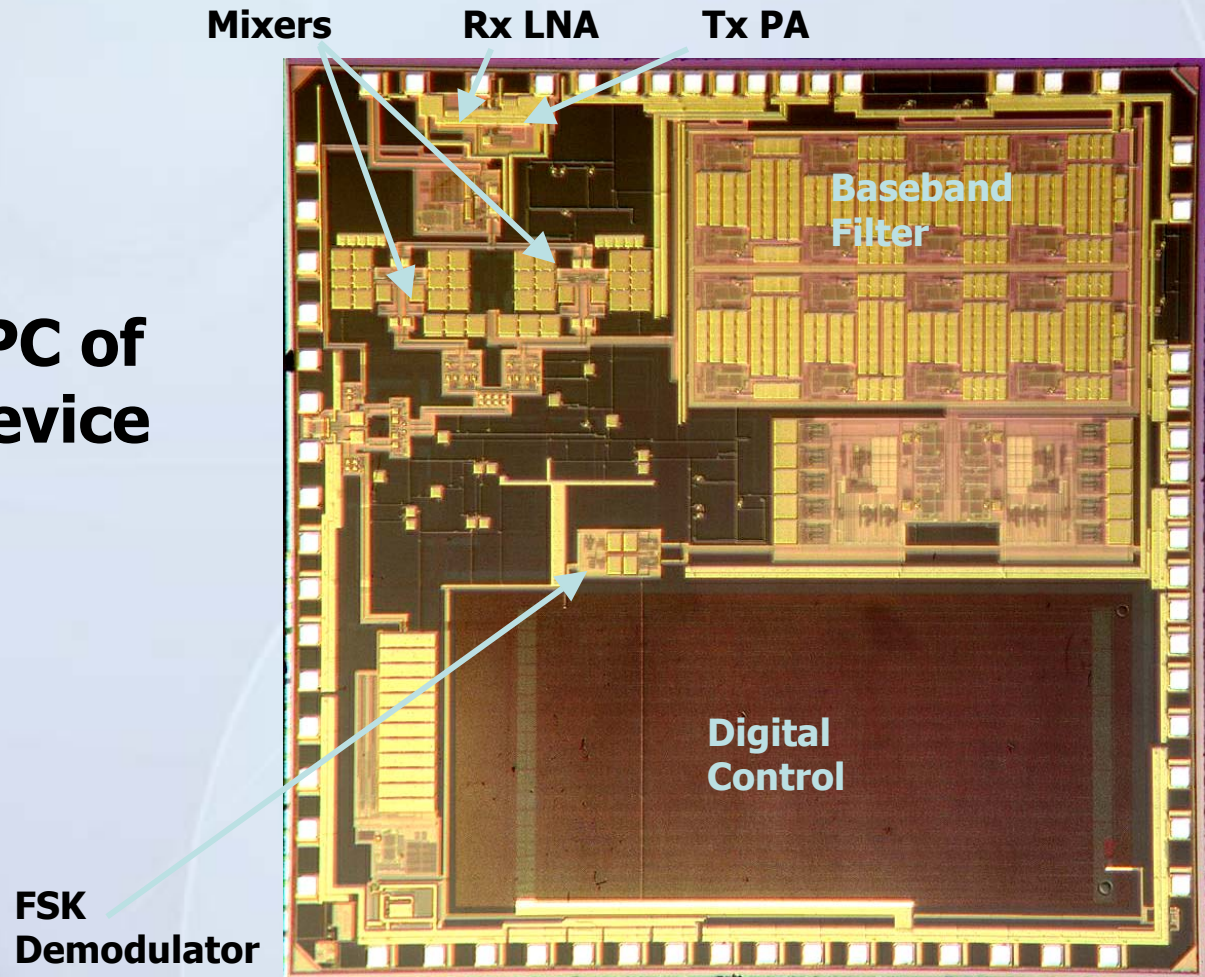


- **The Need for Fully Automated, On-Wafer S-Parameter Measurement**
- **Test System Requirements**
- **System Calibration / Diagnostics**
- **Device Layout Considerations / De-Embedding**
- **Considerations for Probe Selection**
- **Probe Cleaning**
- **Data Extraction Techniques**

The Need for Fully Automated S-Parameter Measurement

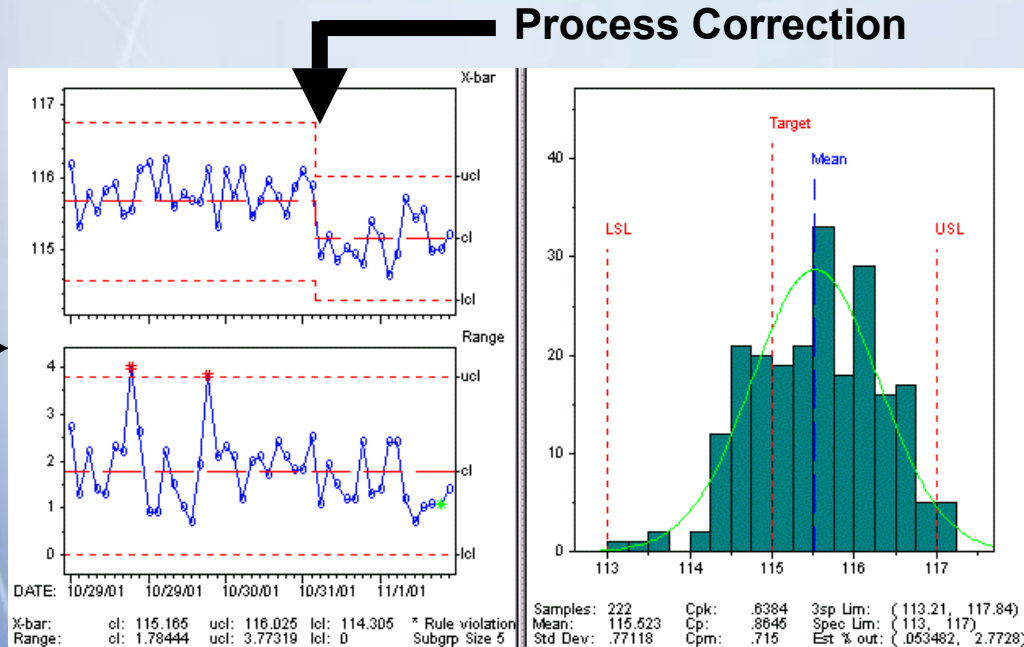


- **Statistical Model Generation**
- **Manufacturing SPC of high frequency device characteristic**
- **Yield Analysis**



Need – Statistical Process Control

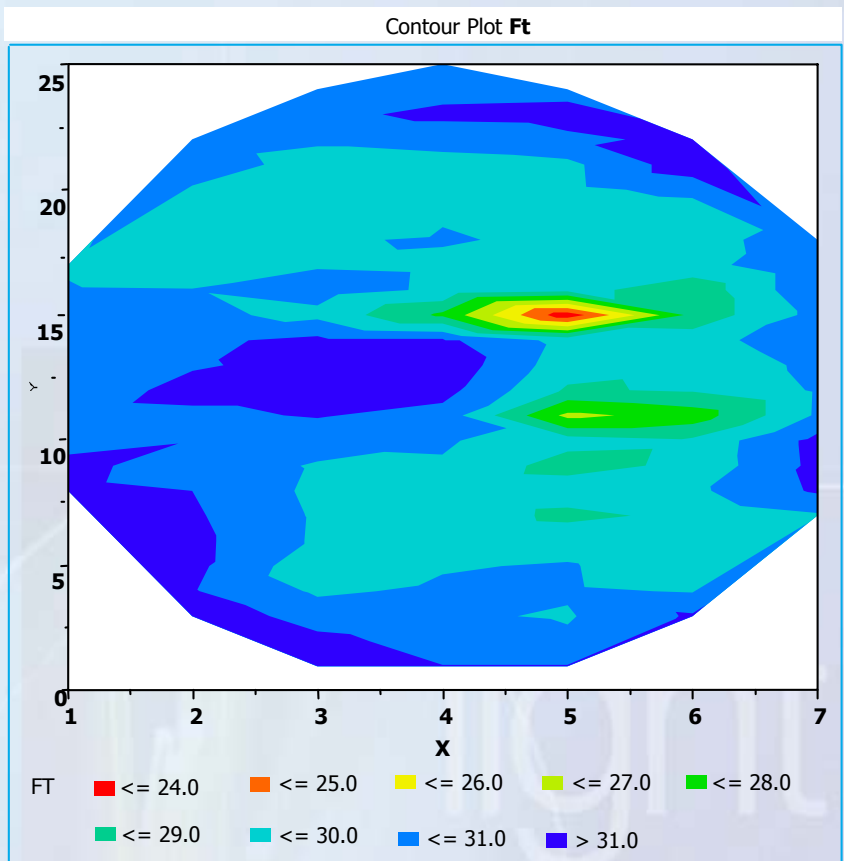
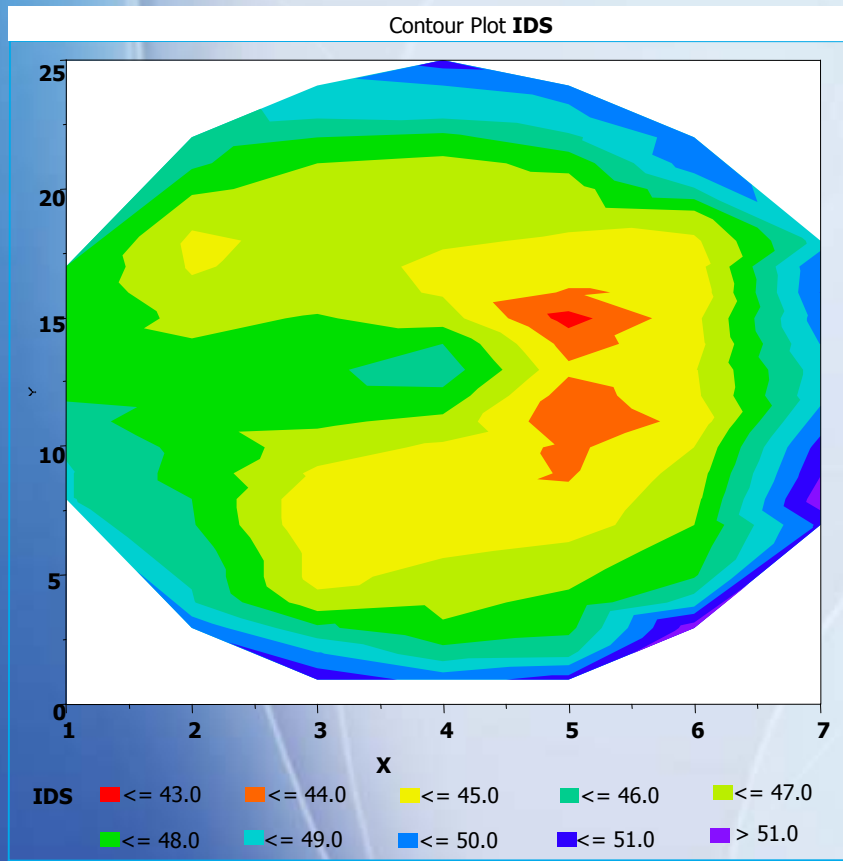
RF SPC Data



RF Product Performance Improves

DC is Necessary but not Sufficient.

Need – Yield Analysis

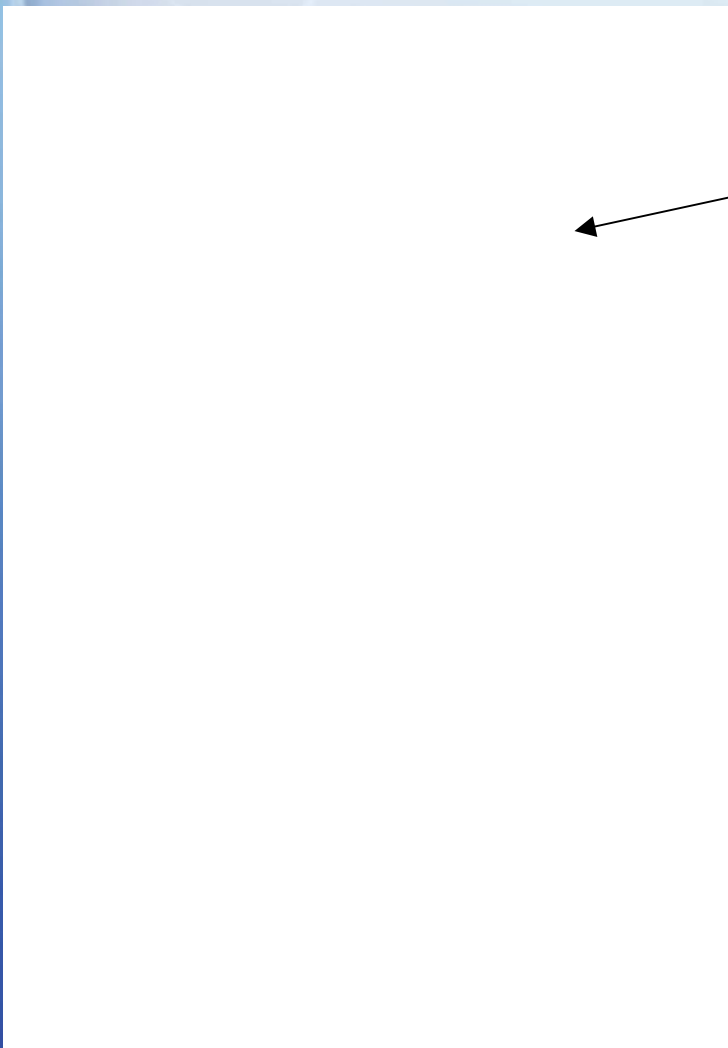


Overlay of DC and RF Wafer Maps Makes Systematic Defects Visible.



A GREATER MEASURE OF CONFIDENCE

Three Main Aspect of Requirements



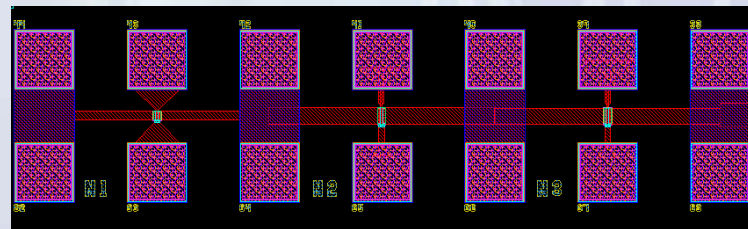
**Vector Network Analyzer (VNA),
Cable and Connector calibration**



**Probe Card
Stability**



**Wafer Test Structures
and De-embedding**



System



Parametric tester with
DC and RF interconnect
To a automatic prober



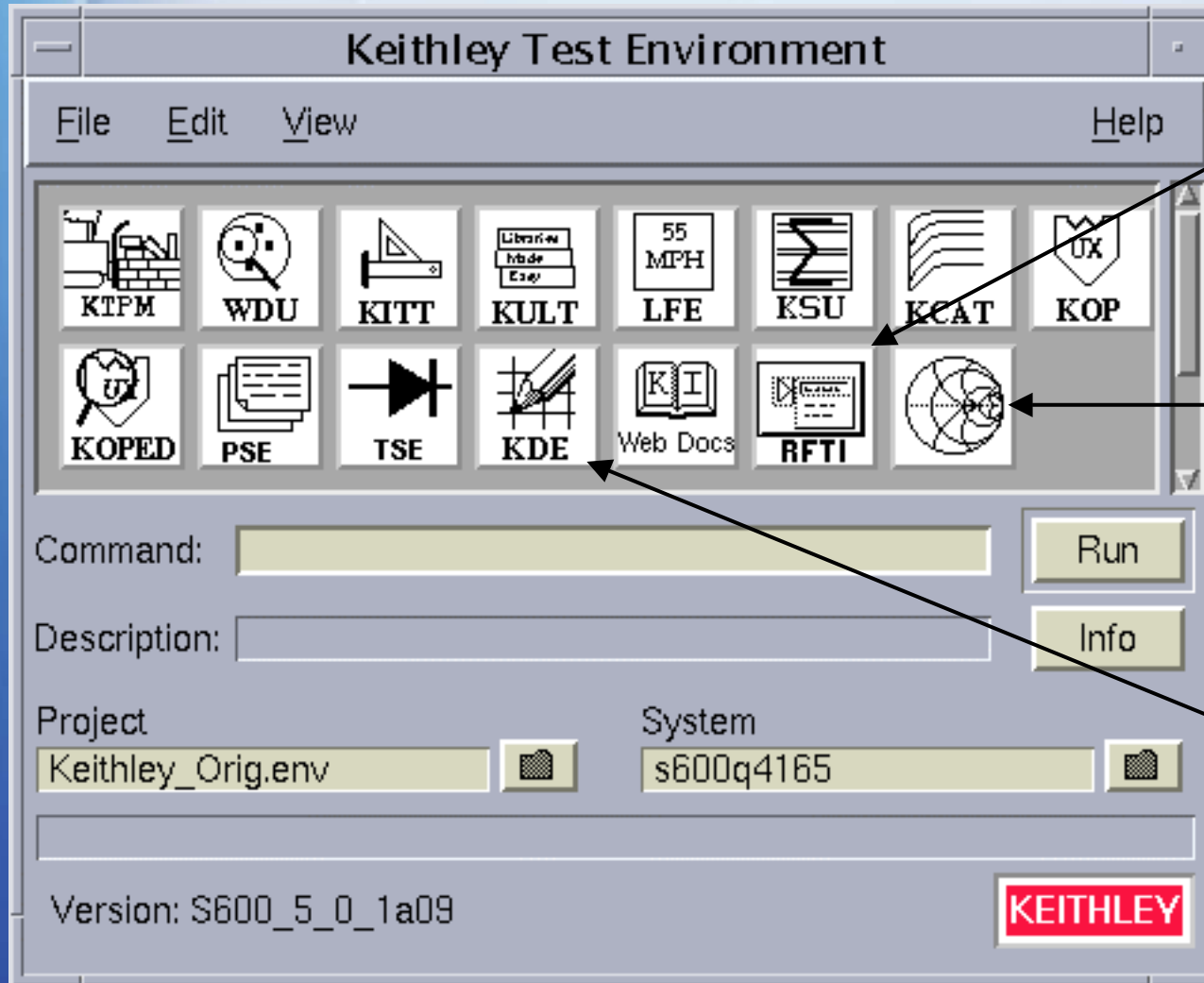
Probe Card And Prober



System interconnect showing cables, bias tees, probe card interconnect, and probe card adapter mounted in an automatic prober.



RF Test GUI



RF Test Setup

RF Data Display

Global Data Entry

Global Data Entry



Global Data : rfcal1.gdf [Local - RW]

File Options Version Control Help

Global Data Editor Probe Card Editor Pre-Defined Identifiers

Data Name	Type	Value
ManualWaferLoad	int	1
rf_cal_verify_logging	int	1
ktxe_min_SS_touch	int	0
enable_chuck_control	int	1

Ok Apply Add Delete Cancel

- **Control Wafer Loading**
- **Optimize Probe Contact**
- **Verify Contact Resistance**
- **Minimize Probe Wear**
- **Set Control limits by technology**
- **Log all events and associate with data**
- **Enable Tester SPC**

RF SETUP - VNA



RF SETUP --- /opt/kiS600/dat/rfcal/rf_cal_file.rfi

File About

VNA | Signals | Calibration | Auto-Z | Limits | SOLT | LRM

Measurement

512 Number of points to average

1e3 IF Band, Hz

Frequency

Frequency Set Label freqName

Start, Hz Stop, Hz Number of Freq

Start, Hz Stop, Hz Number of Freq

Subset 1 1e8 1e9 2e9 3e9 4e9 5e9 6e9 7e9 8e9

Subset 2 10e9 15e9 20e9

Subset 3



RF SETUP - Signals

RF SETUP --- /opt/kiS600/dat/rfcal/rf_cal_file.rfi

File About

VNA | **Signals** | Calibration | Auto-Z | Limits | SOLT | LRM

2 Number of Signal Levels

Signal Set

Label	Port1 Attn	Port1 Power	Port2 Attn	Port2 Power
s1:	20	-1	30	-7
s2:	10	-10	10	0



RF SETUP - Calibration

RF SETUP --- /opt/kiS600/dat/rfcal/rf_cal_file.rfi

File About

VNA | Signals | Calibration | Auto-Z | Limits | SOLT | LRM

\$KILOG/rfcal.log Cal Log File in \$KILOG

rf_card Probe Card Label

Use Manual Prober

Use Cal Kit

SOLT

Site_2

Pin Pair 1

25	Port1 DC pin
26	Port2 DC Pin

RF SETUP— Auto-Z



RF SETUP --- /opt/kiS600/dat/rfcal/rf_cal_file.rfi

File About

VNA | Signals | Calibration | Auto-Z | Limits | SOLT | LRM

Enable Auto-Z

1 Pin pair used for AUTO-Z test

16.0 Contact trigger value, Ohms

auto_z Subsite Name from WDU

2 Subsite Index

5.0 Increment step for a contact

25.0 Additional Overdrive

RFCALSUP KULT Library

rfcalsup_t KULT Function

190.0 Maximum Travel. PLEASE USE CAUTION WHEN SETTING!

RF SETUP— Limits



RF SETUP — /opt/kiS600/dat/rfcal/rf_cal_file.rfi

File About

VNA | Signals | Calibration | Auto-Z | Limits | SOLT | LRM

Contact Test Limits

1e-6	Leakage on OPEN, Amp
60	Resistance on MATCH, Ohms
8.0	Resistance on SHORT, Ohms
16	Resistance on THRU, Ohms

S-Parameter Verify Limits

OPEN		SHORT	
1e-1	S11	0.01	S11
1e-1	S12	0.01	S12
1e-1	S21	0.01	S21
1e-1	S22	0.01	S22

RF SETUP— SOLT



RF SETUP --- /opt/kiS600/dat/rfcal/rf_cal_file.rfi

File About

VNA | Signals | Calibration | Auto-Z | Limits | SOLT | LRM

OPEN

C0, F

Length, m

LOAD

Inductance, H

Impedance, Ohm

THRU

Length, m

Impedance, Ohm

SHORT

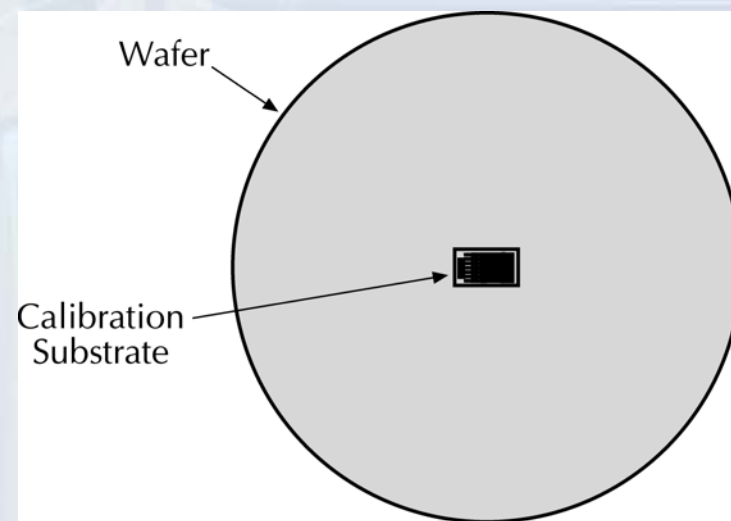
L0, H

Length, m

Requirements - VNA Calibration

- **Calibration is required to correct for systematic errors in the VNA and cabling.**
- **The fixed probe spacing of a production probe card limits the choice error correction methods to SOLT (two port, 12 term error corrected).**
- **Automatic calibration is performed by inserting a calibration standard onto a silicon wafer.**

A Calibration Substrate has gold test structures on alumina substrate.



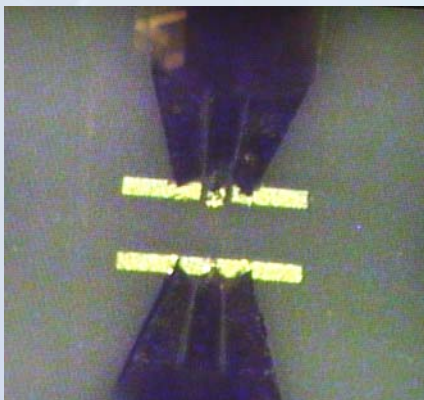
VNA Calibration SOLT

Measurement

Structure

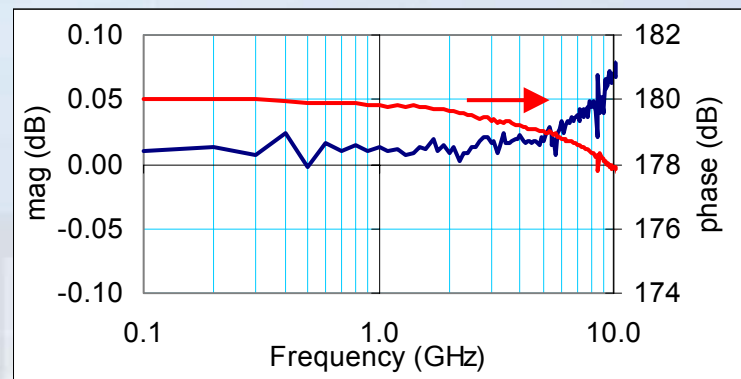
Response

Short



S_{xx}

Ideal: Unity Reflection(0dB), 180 Phase Shift

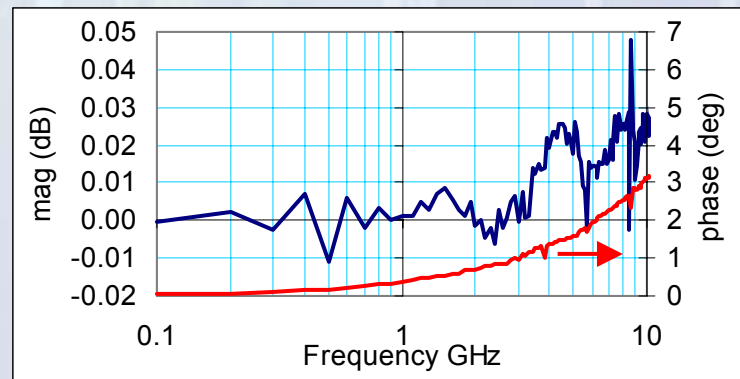


Open



S_{xx}

Ideal: Unity Reflection(0dB), 0 Phase Shift



VNA Calibration SOLT (cont.)

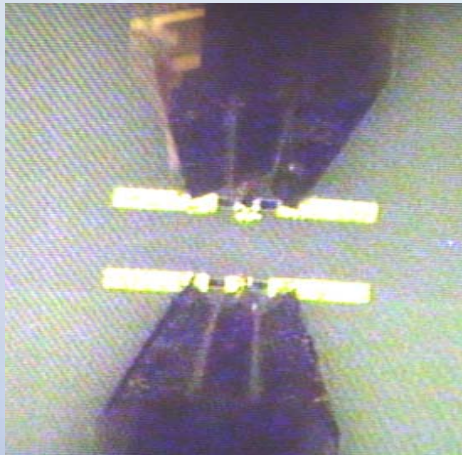


Measurement

Structure

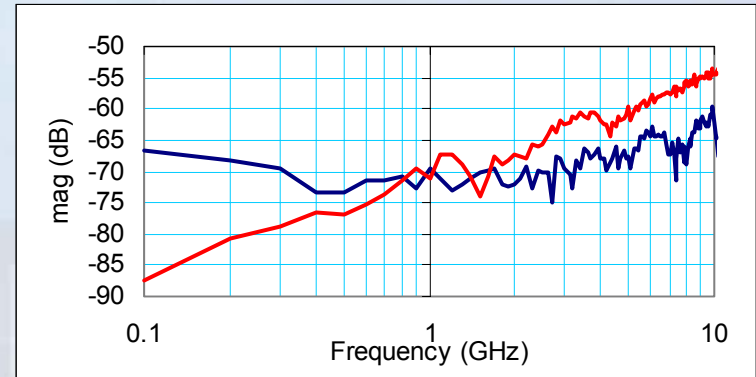
Response

Load

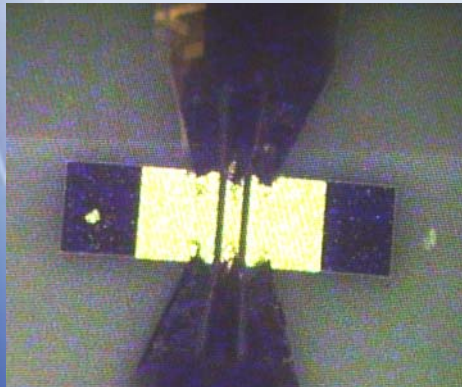


S_{xy}

Ideal: 0 Reflection, 0 Transmission port 1 to port 2

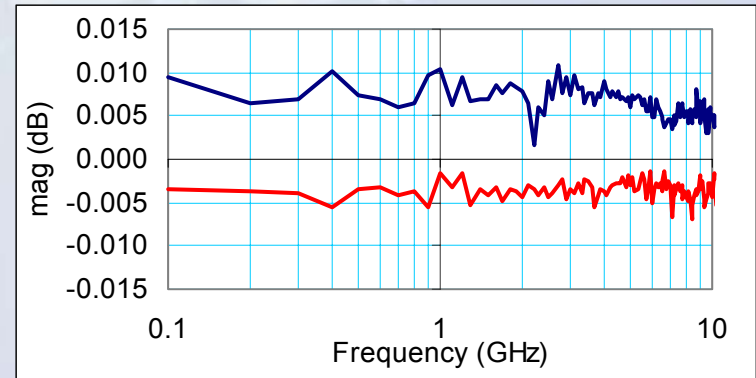


Thru



S_{xy}

Ideal: Unity Transmission port 1 to port 2



Calibration Considerations



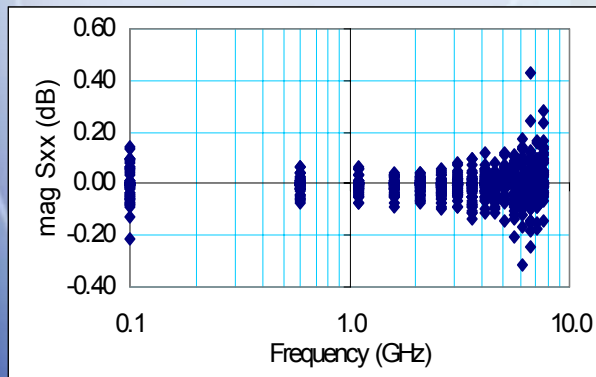
Calibration Frequency

- With each probe card change (when test head docks)
- Periodic by time, DUT type or number of sites probed
- As part of needle cleaning and contact verification

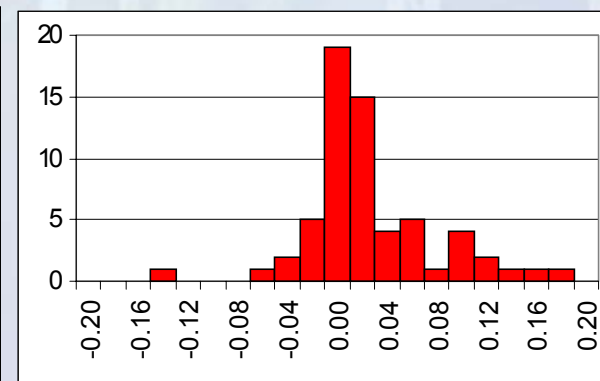
Calibration Pass/Fail Criteria

- Dependent on user requirements (device size, frequency etc)
- Calibration Repeatability Expectations
- Critical factors are probe card docking and probe cleanliness

Frequency Response



Statistics at 7.6 GHz



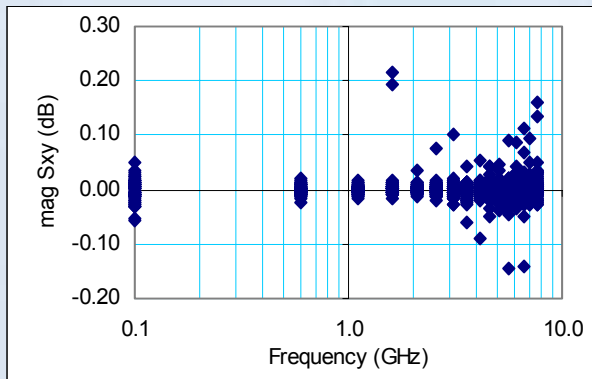
**S11 and S22
Open**



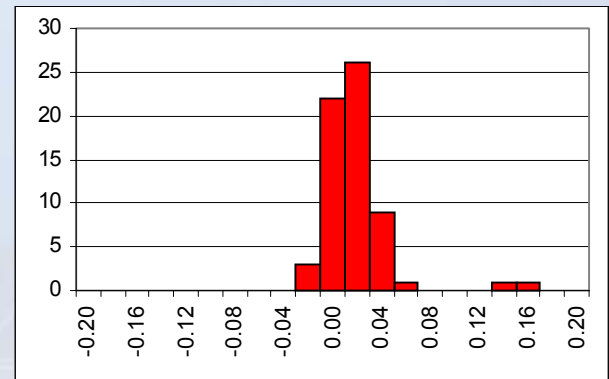
Calibration Pass/Fail Criteria

S12 and S21 Thru

Frequency Response



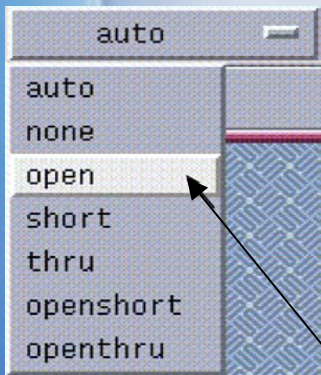
Statistics at 7.6 GHz



Typical Pass/Fail Criteria for MOSFET S Parameter Testing

	OPEN	THRU
S11	0 ± 0.15 dB	< -50 dB
S12	< -50 dB	0 ± 0.10 dB
S21	< -50 dB	0 ± 0.10 dB
S22	0 ± 0.15 dB	< -50 dB

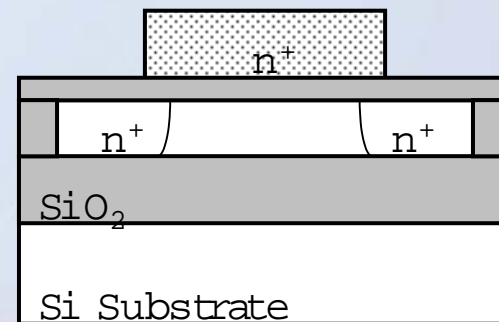
Requirements – Test Structures and De-Embedding



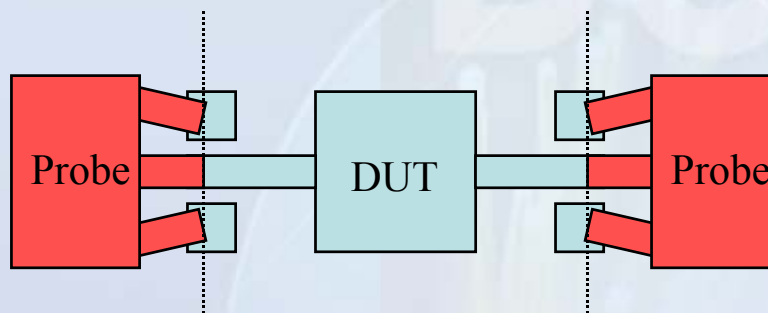
What Type of De-Embedding?



How Frequently?



Technology Considerations?



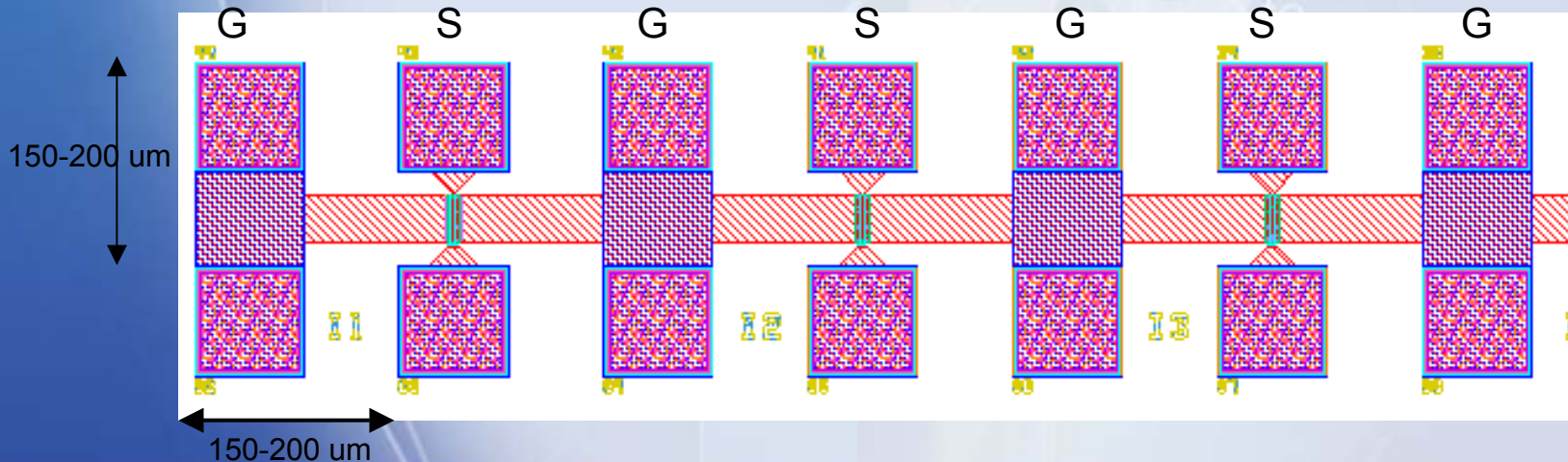
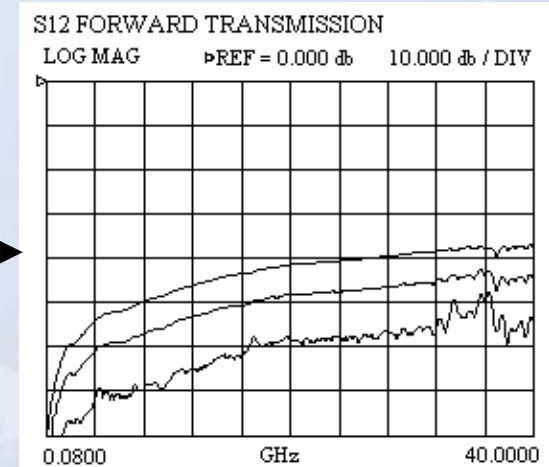
DUT Considerations?

Device Layout Considerations - DUT

Device Under Test (DUT)

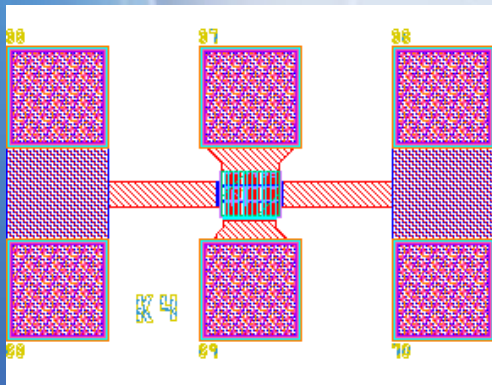
GSG Configuration

- **Fixed Pitch**
typically 100-200um S to G
100-300um S to S
- **Shared Ground for Improved Area Utilization**
- **Pad size - typically 55x55 to 100x100 um**
- **Top layer metal only is best**

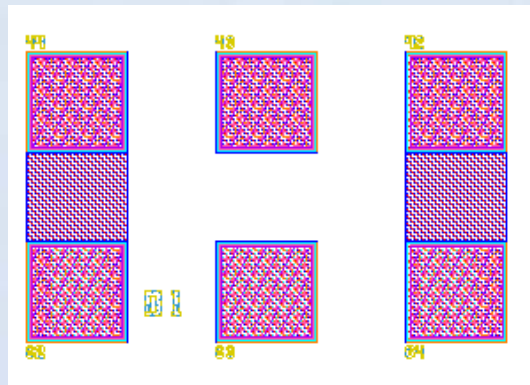


Layout for De-Embedding

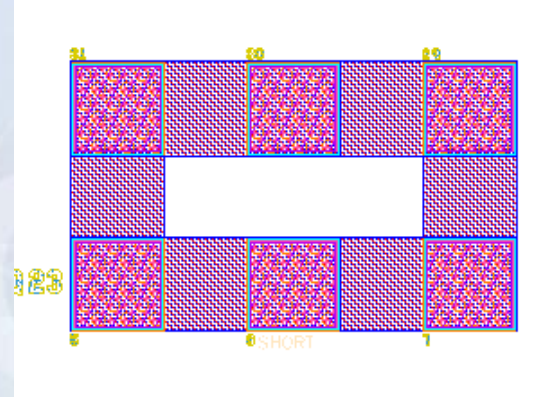
DUT



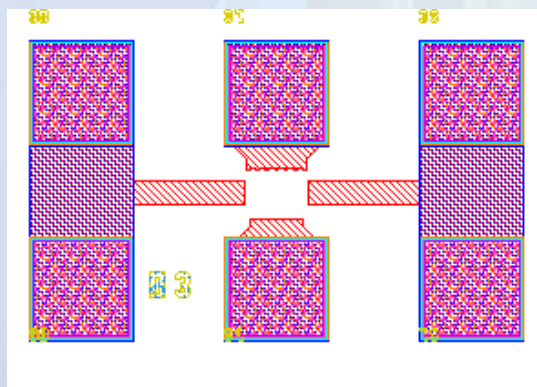
Generic OPEN



SHORT



Ideal OPEN



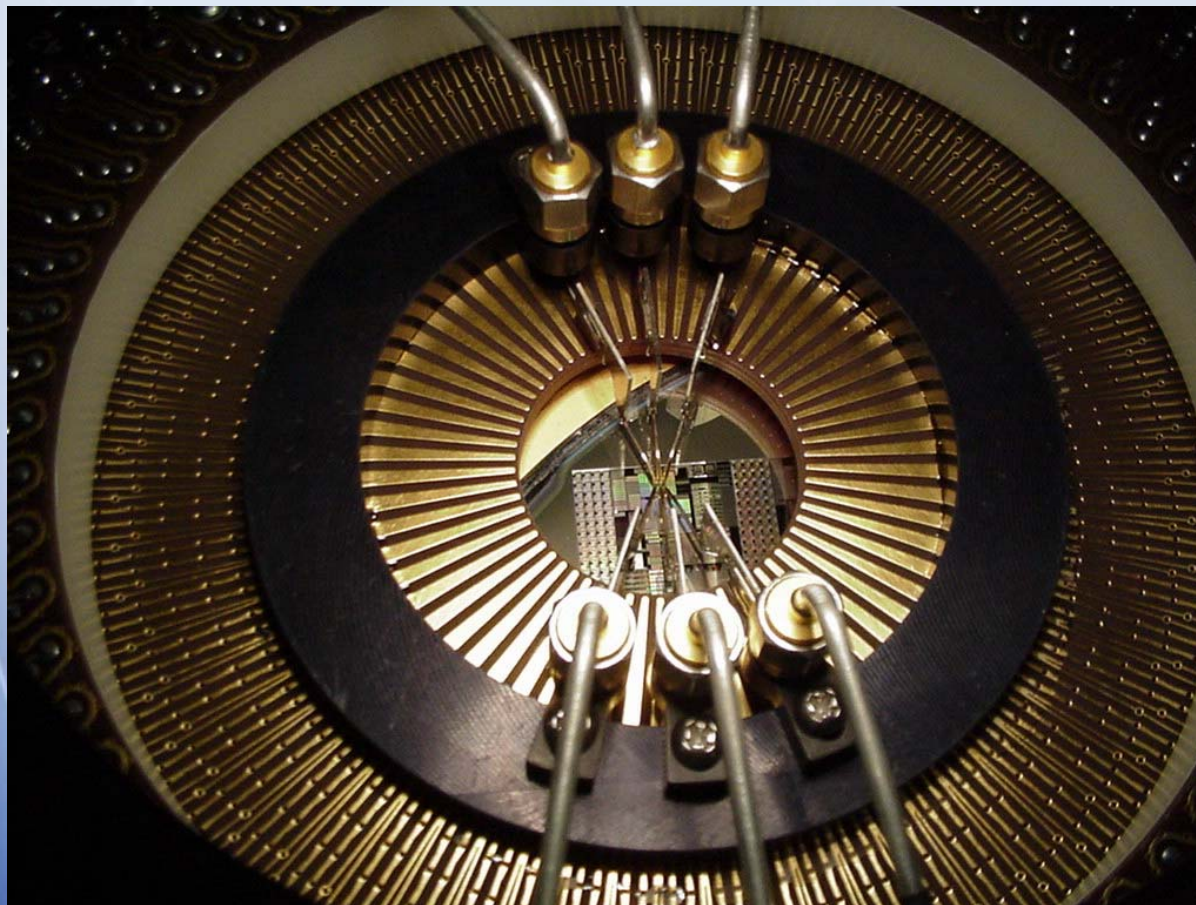
innovate • create • accelerate

RF Probe Card



SOUTHWEST TEST WORKSHOP

2002



ht

KEITHLEY

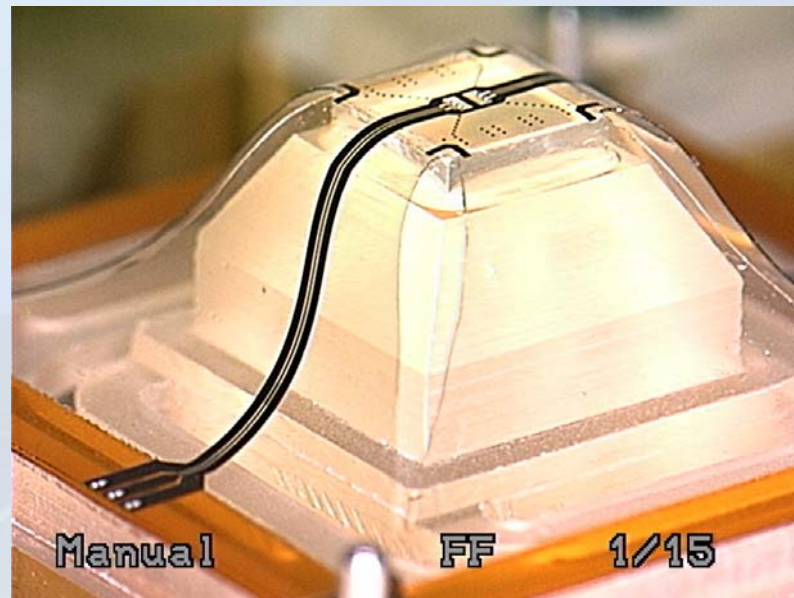
A GREATER MEASURE OF CONFIDENCE

Considerations for Probe Selection

- **50 Ohm impedance match G-S-G construction**
- **Mechanical Design for Fine Pitch Probing (fine point and steep pitch)**
- **Metallurgical match to probe pad requirements**
- **Balance Contact Force and Co-Planarity match to DC probes for mixed DC/RF probe card**
- **Durability and low cost**

DC to light

Available Probe Technologies

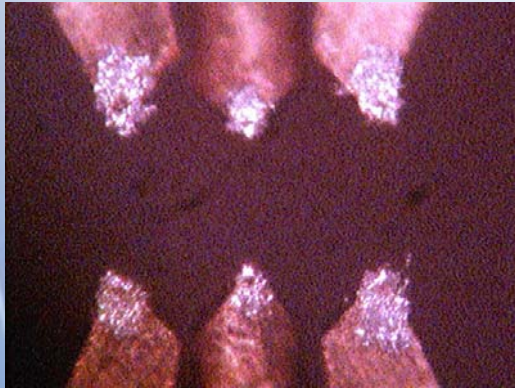


Requirements – Probe Card Stability

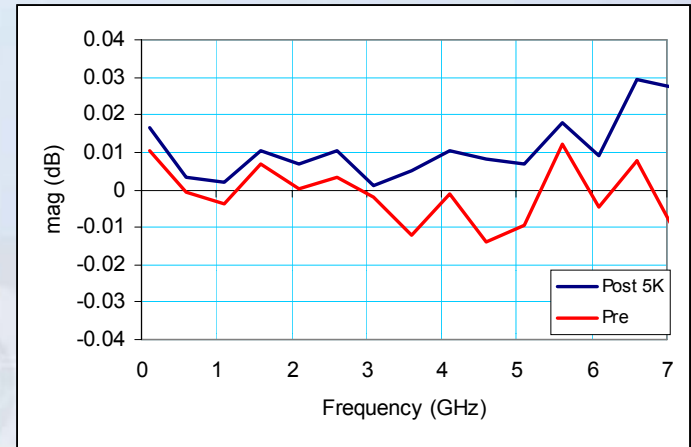


Two types of contamination are most often observed

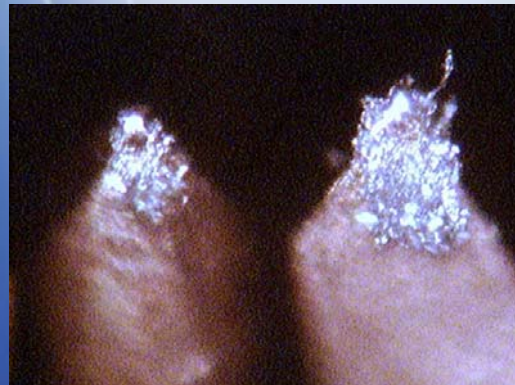
Small particulates which systematically build up over many hundreds or thousands touchdowns.



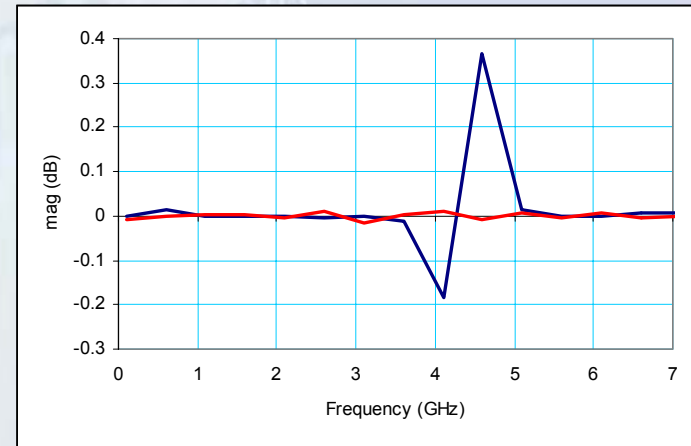
S11 OPEN cal
before and after
5000 touchdowns



Large particulates which are generated on a random basis



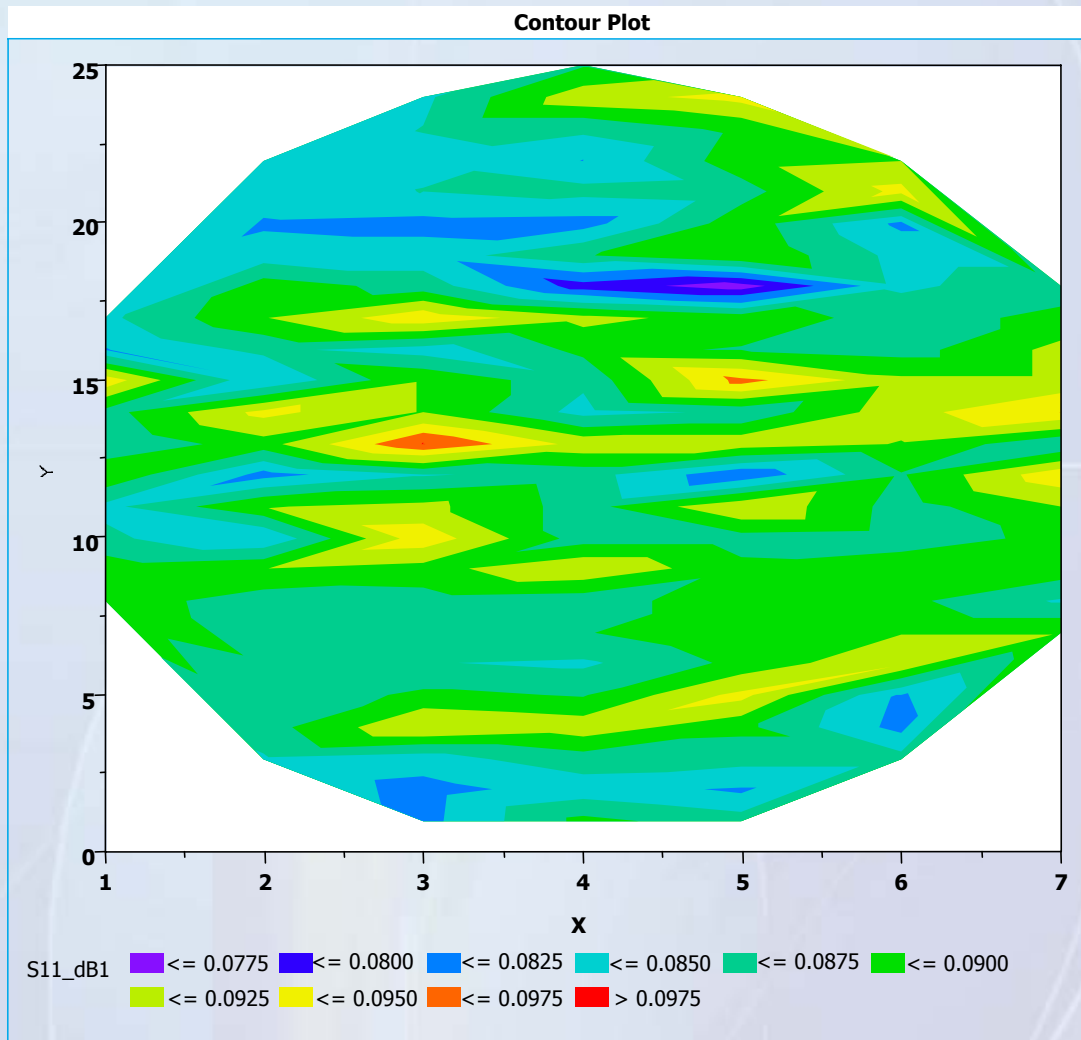
S11 OPEN cal
before and after
particle
contamination



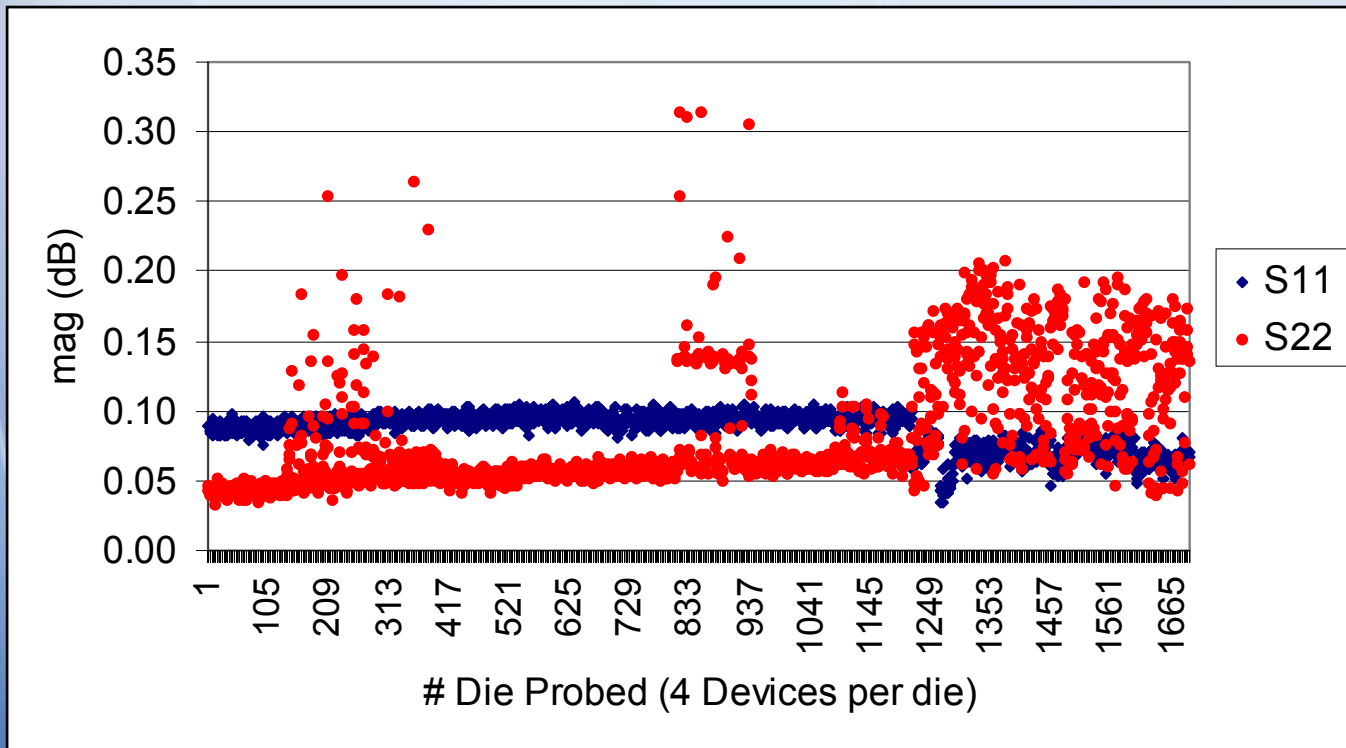


Probe Contamination Monitor

- S11 measured during prober indexing
- Deviation from 0dB plotted
- Probe pattern:



Contamination Monitor Results

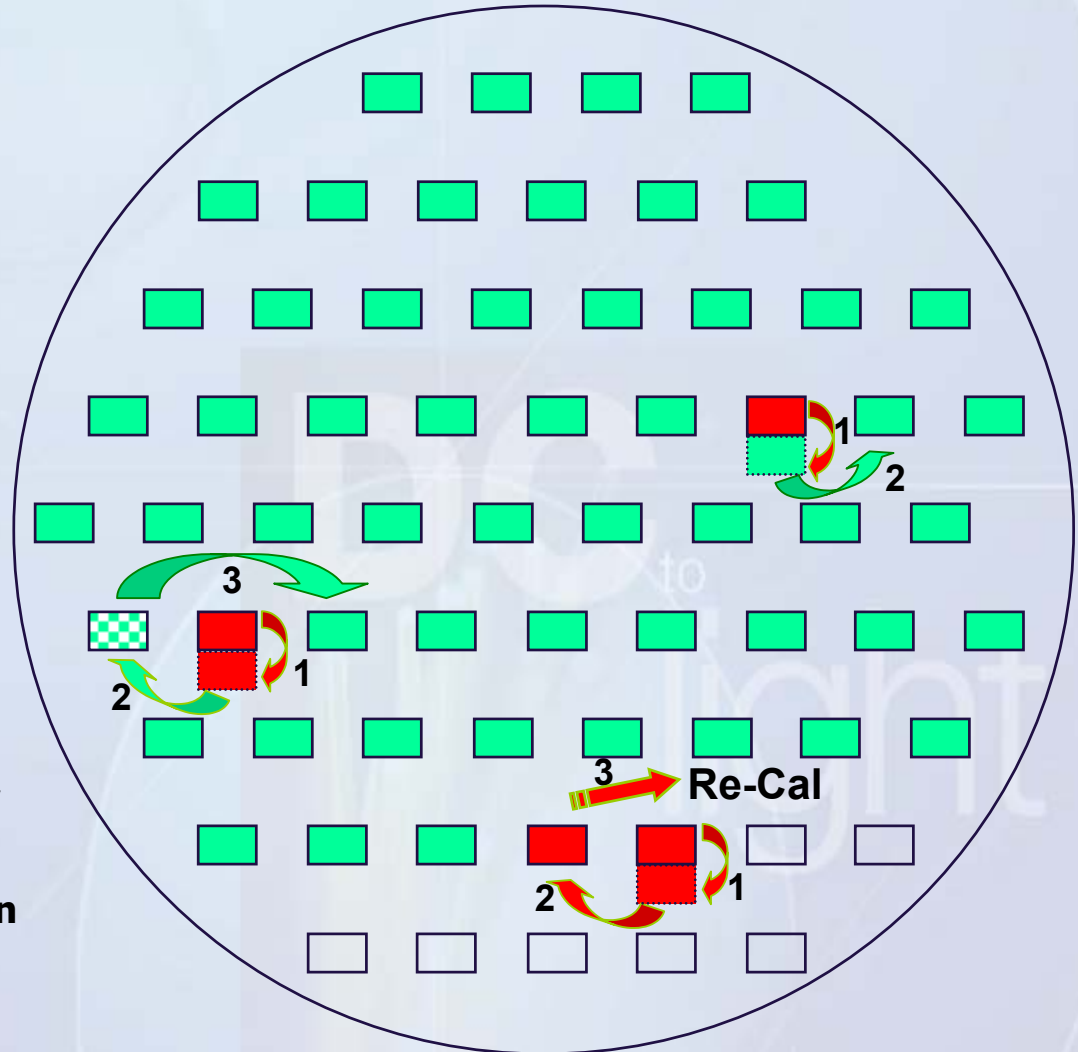


SPC of Probes Up S11 and S22 During a Test with 5000 Devices Measured On Two Sequential Wafer Lots

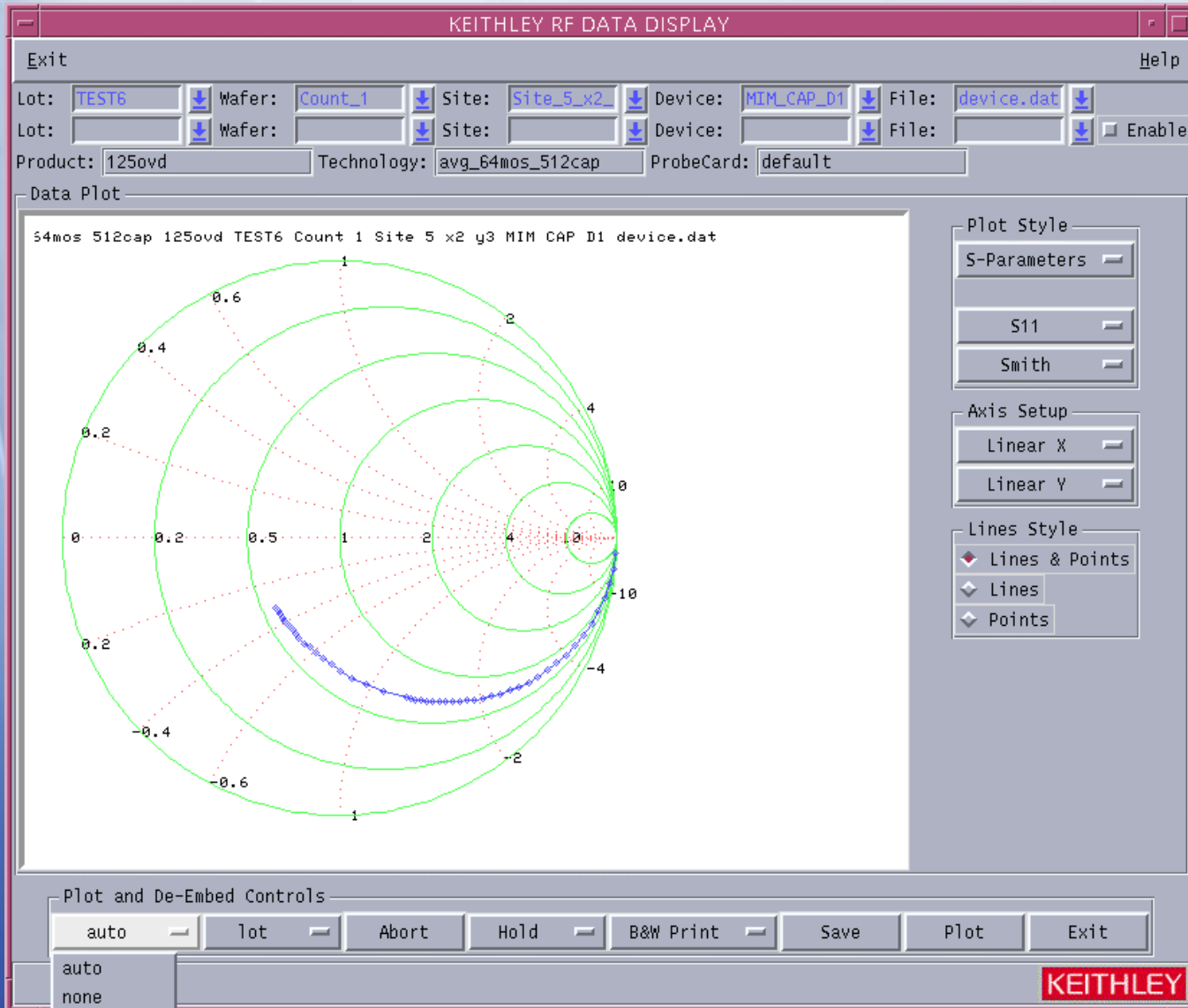


Real-Time Probe Cleaning, Re-Cal

- Measured Data or Probes Up Sxx Fails Limits.
- Probe Clean and Re-Test at Current or Adjacent Site.
- Probe Clean and Re-Test at Current or Adjacent Site Fails.
- Re-Clean and Re-Test Previously Good Site.
- Re-Clean and Re-Test Previously Good Site Fails.
- Stop Testing, Re-Load Calibration Wafer and Re-Cal.

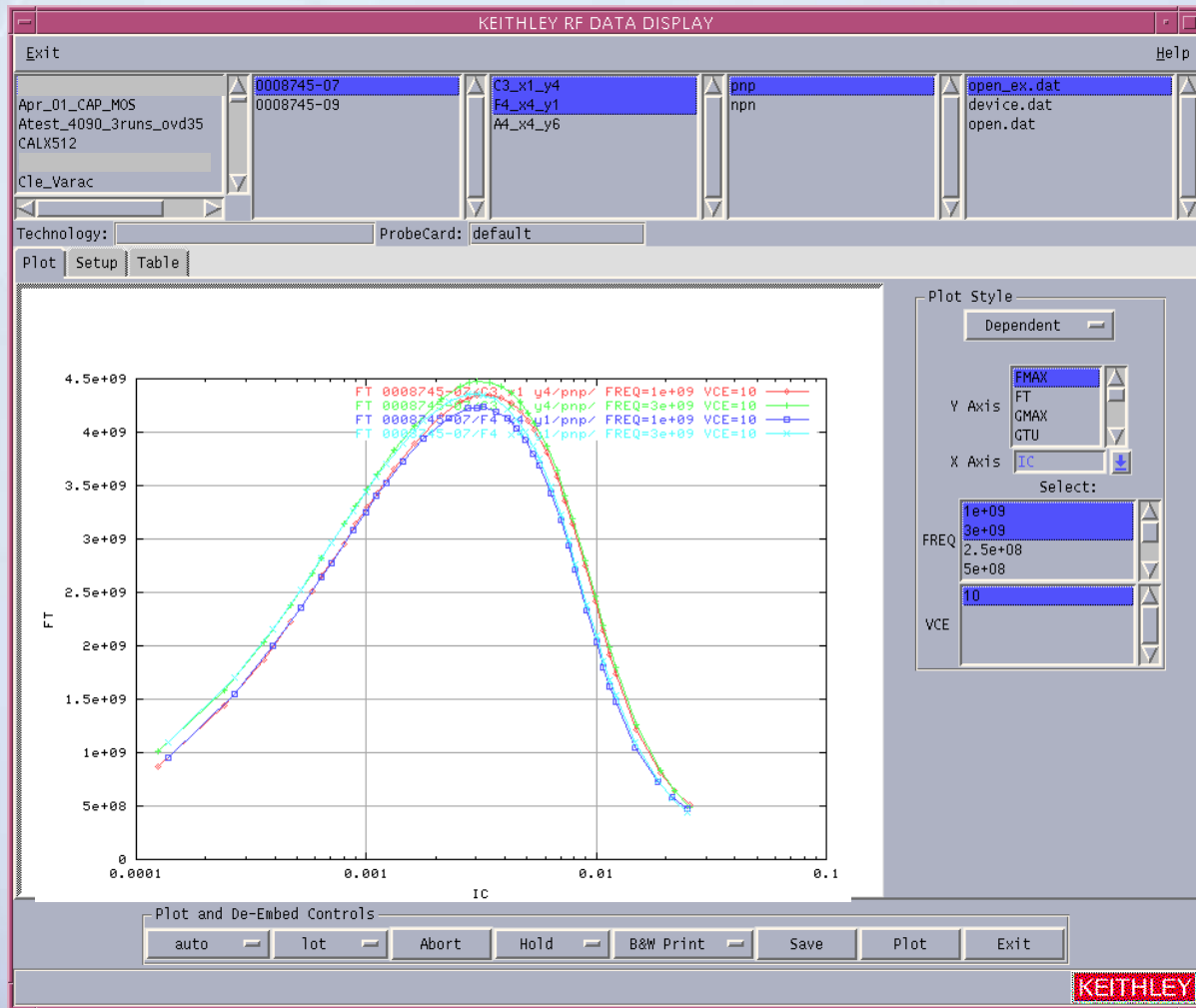


RF Data Display

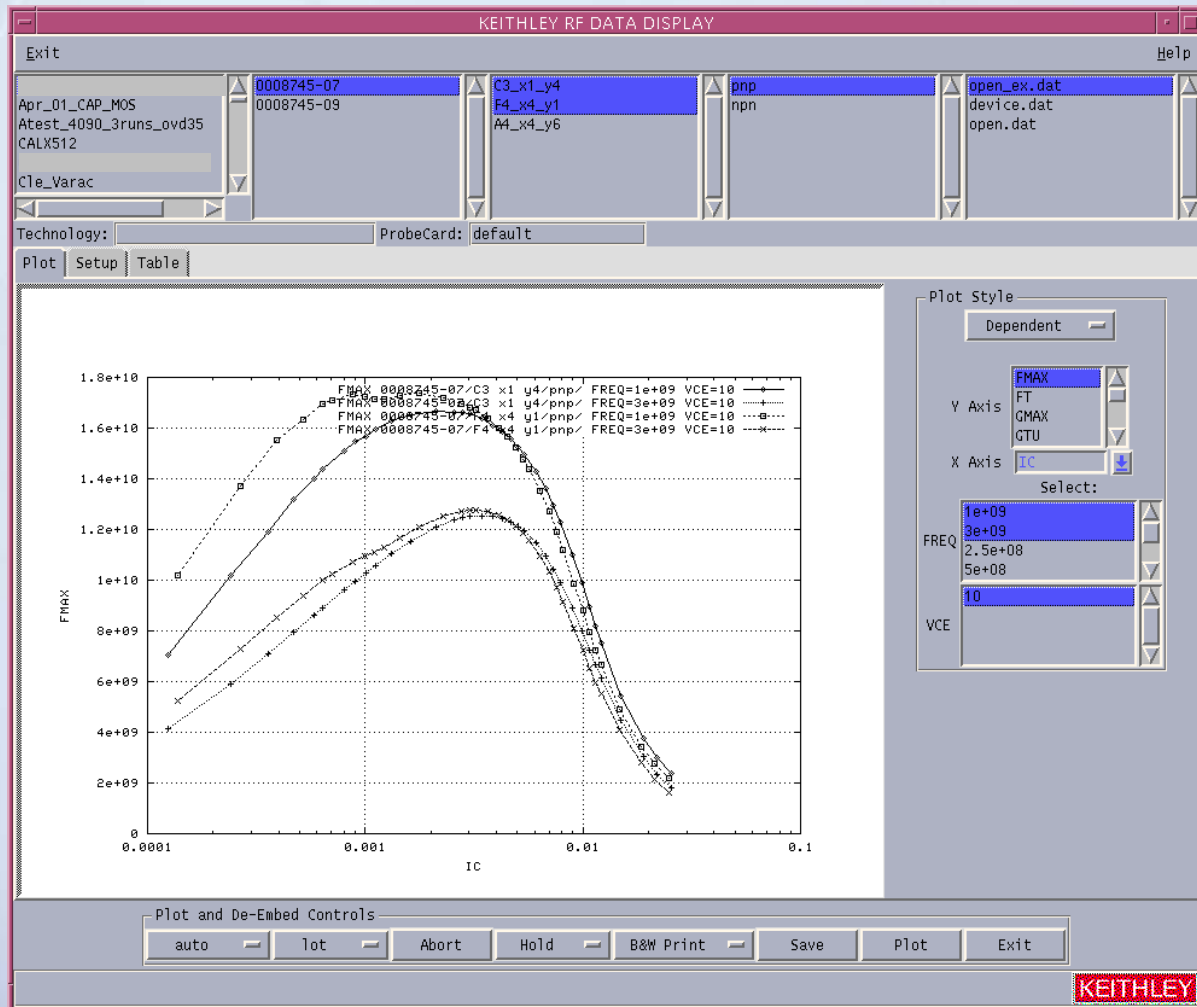


A GREATER MEASURE OF CONFIDENCE

Data Browser - Ft



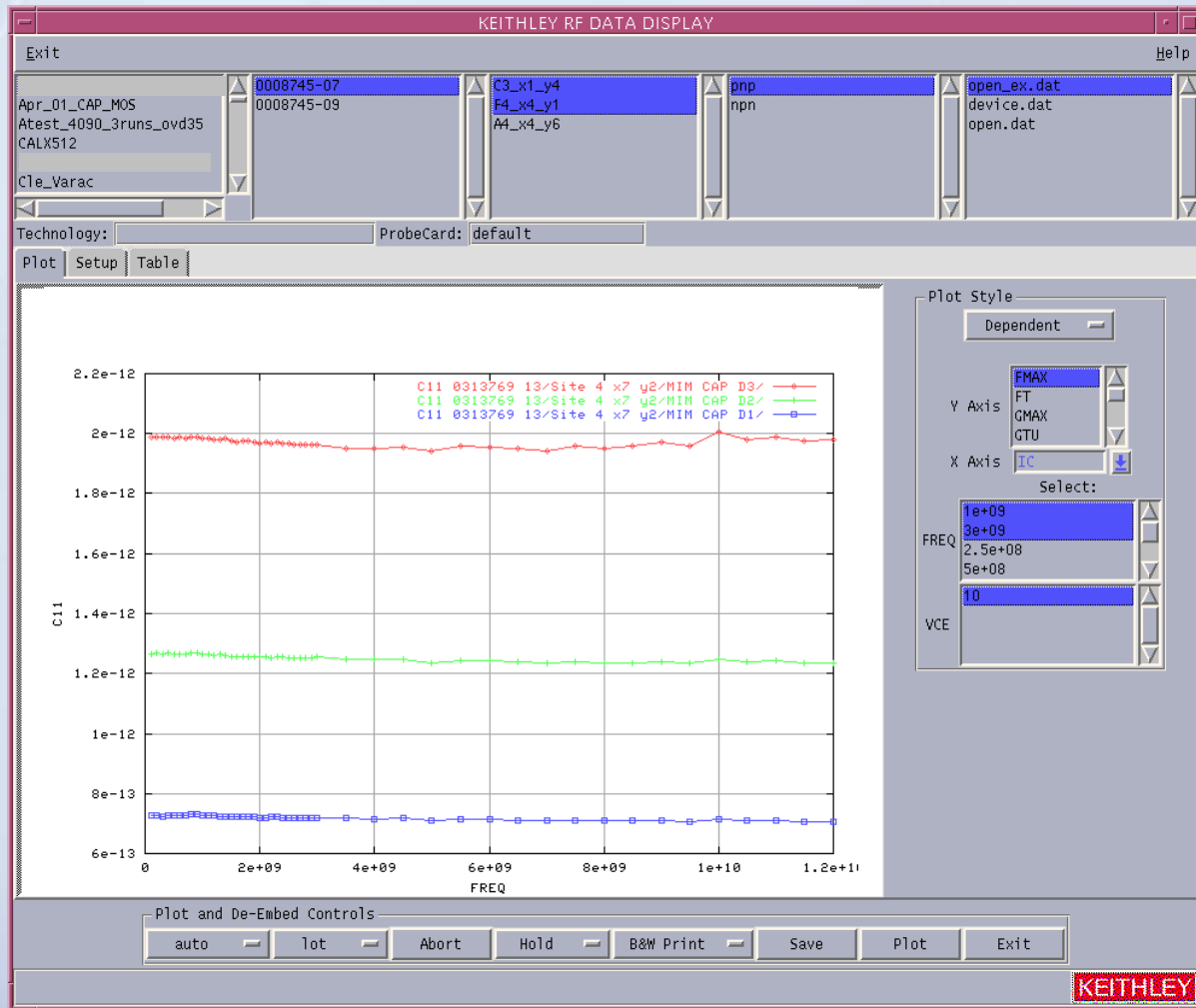
Data Browser - FMAX



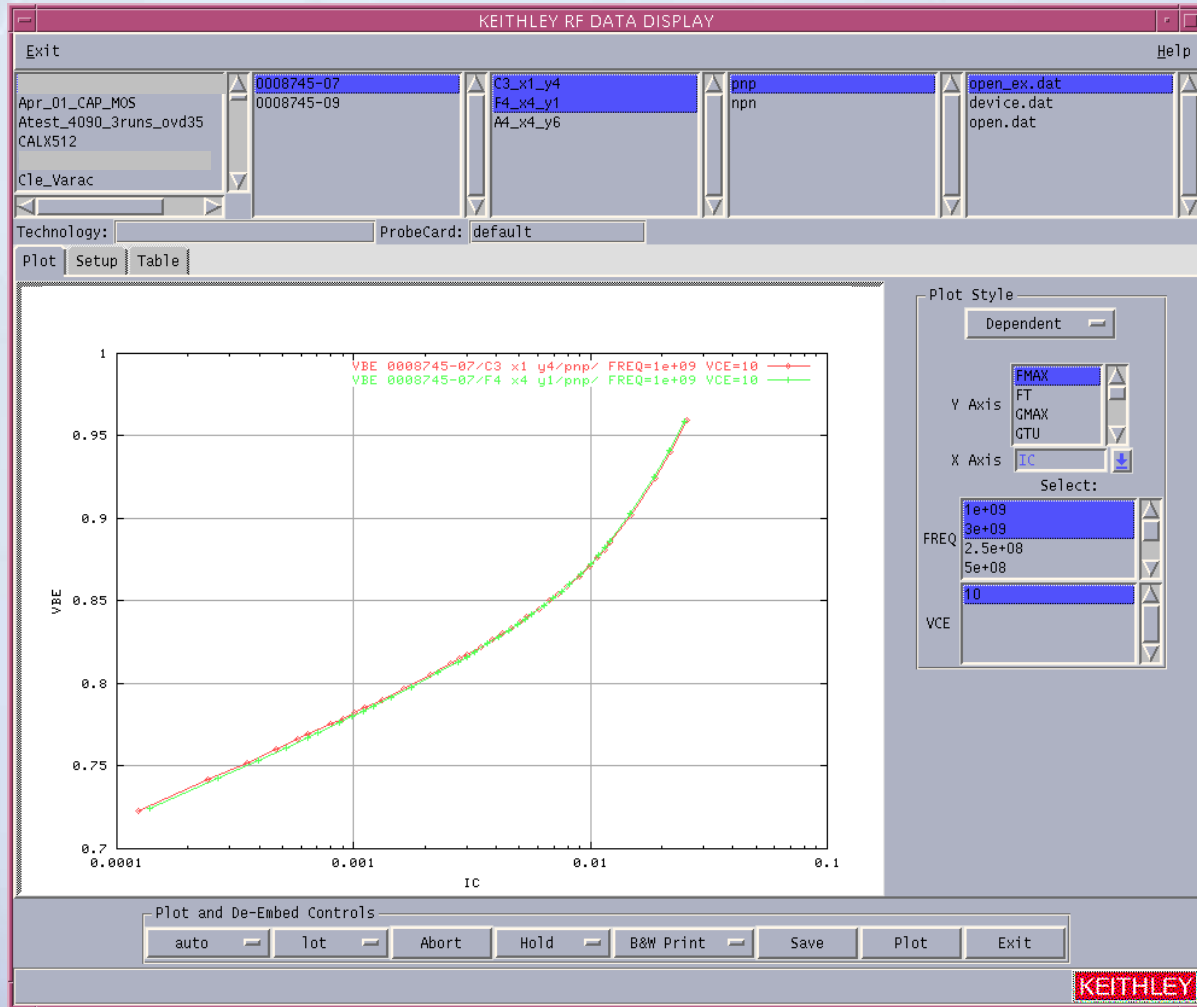


Data Browser - Capacitance

Data showing
3 measured
capacitors



Data Browser – DC; IC vs. VBE



Conclusions

- **The need for large amounts of s-parameter data for statistical modeling and process control is becoming increasingly significant.**
- **The considerations for a solution and the effectiveness of that solution have been demonstrated.**
- **Using this approach enables automated yield optimization tools to support products with DC to Broadband performance parameters.**



Acknowledgements

- Praful Madhani – Texas Instruments
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- David Rose – Keithley Instruments