Speed bumps in Fast probing

> Lalit Kumar

> Janaki Vegiraju

> Bob Fenton

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Introduction

- Bumped wafers are becoming more and more common
- Fast probing – probing of very small die with relatively short test times – is a requirement today.
  - Faster testers (also BIST, DFT) – test time $\leq$ step time in some applications
  - Cost of test pressure
  - Die shrinks
- Both trends combining to generate a new set of prober features

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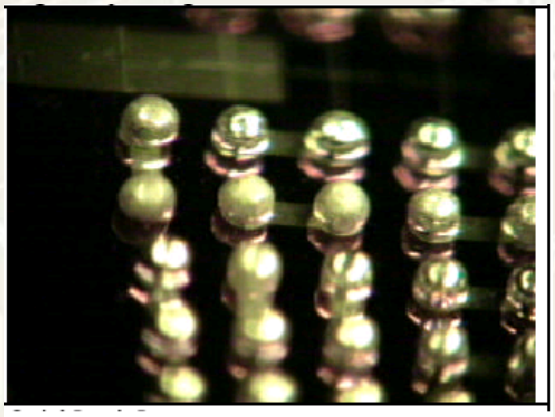
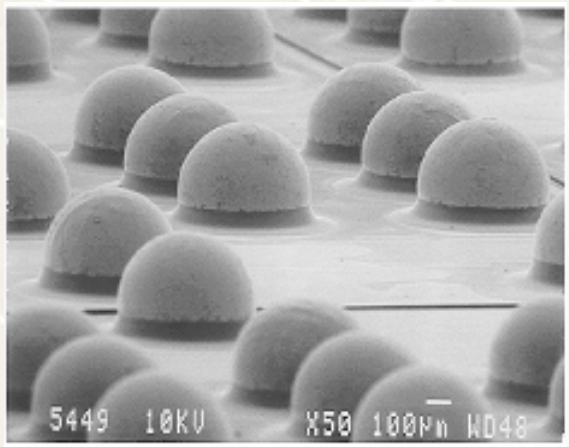
Bumping Processes - Overview





- Evaporated Vs. Electroplated
  - Evaporated bump technology has extendibility issues when bump pitch is decreased below 9 mil.
  - Electroplated bump pitch is limited more by assembly and reliability considerations than by the formation of the bump.
  - We have to probe all of them!

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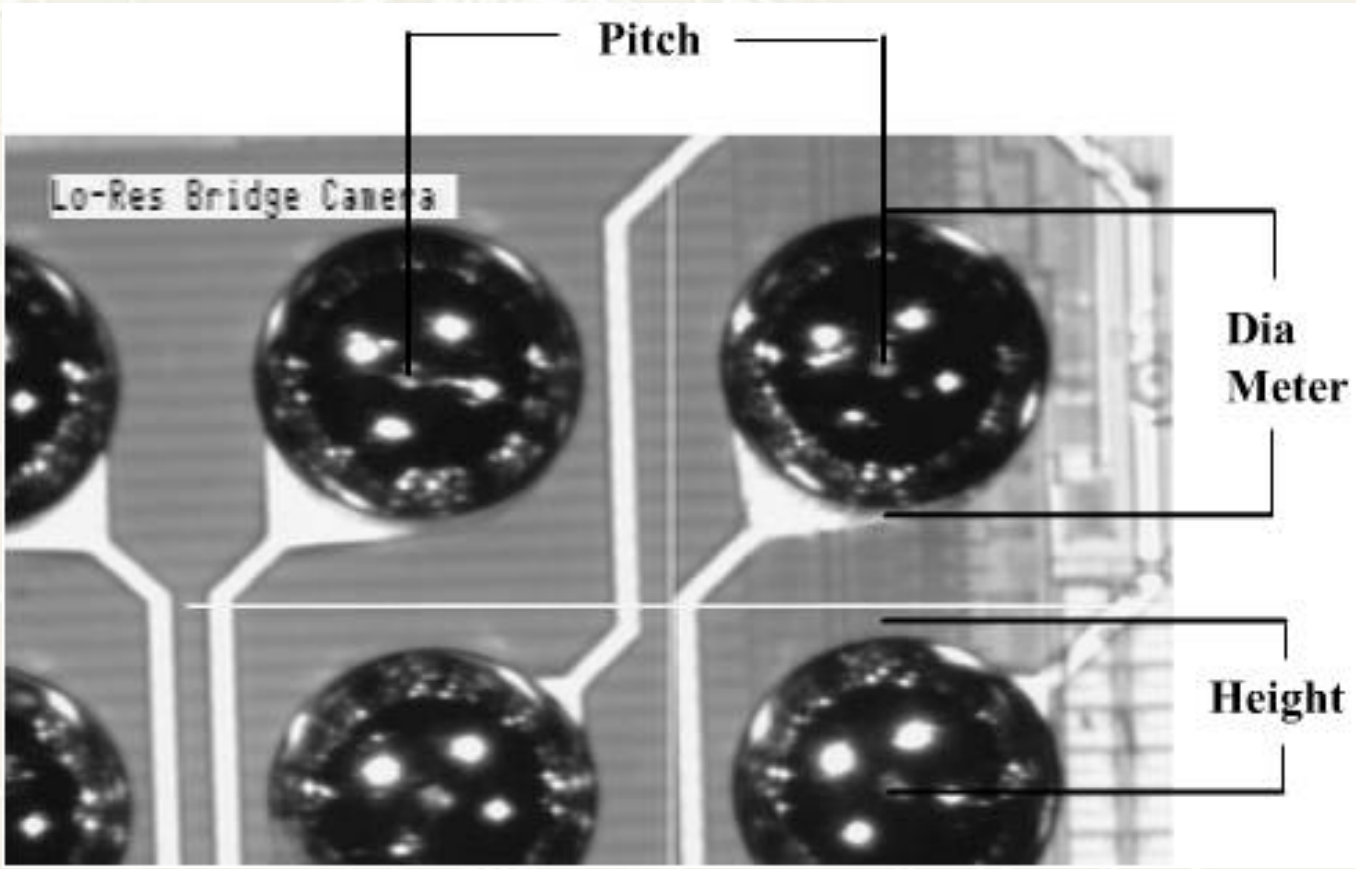
Bumps – a prober's view



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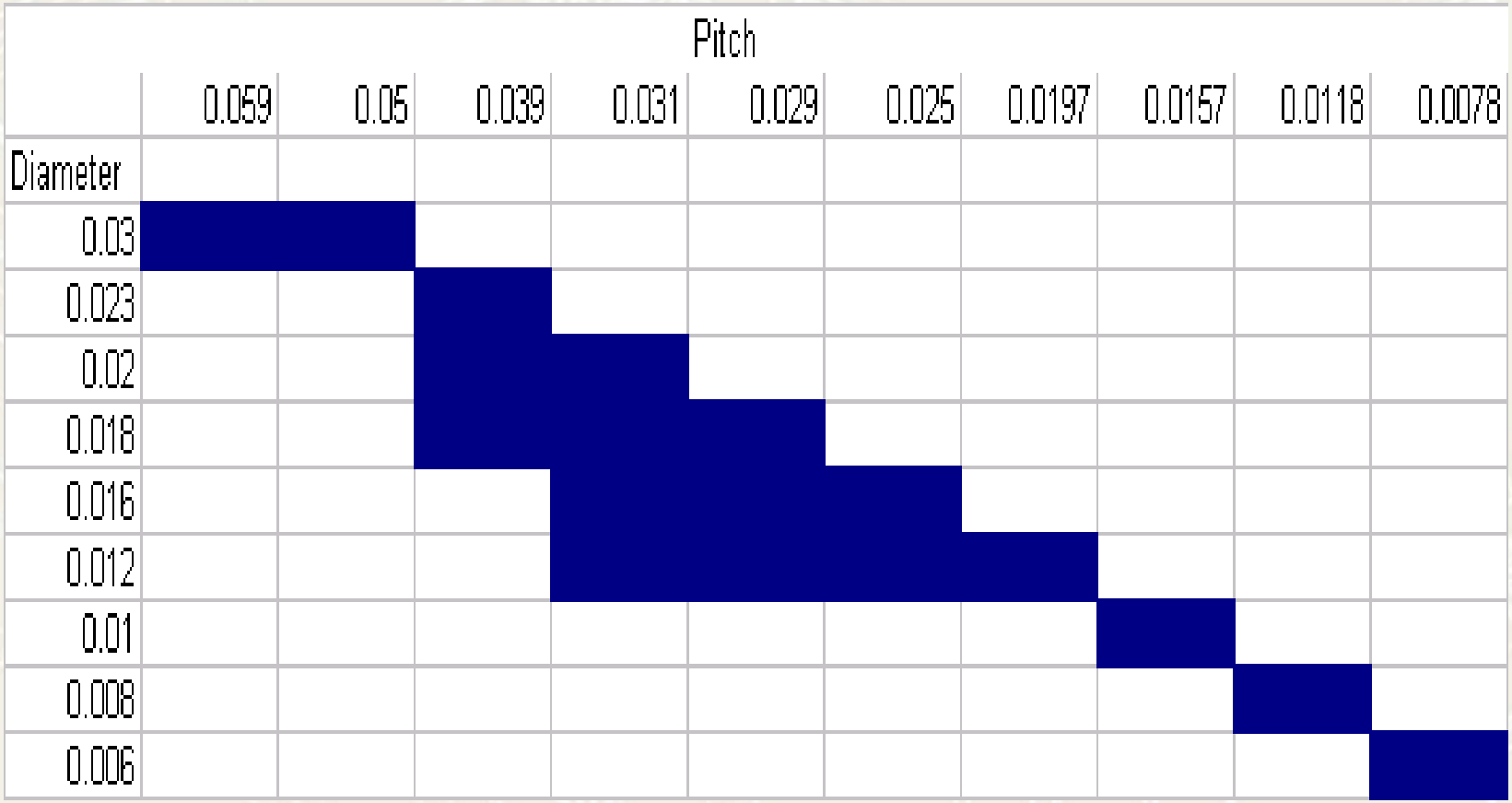
Ball diameter and pitch design rules (WLP)



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FCT Bump design guidelines

Table 1. Peripheral Solder Bump Design Guidelines.

Peripheral Pitch	254 (10mil)	204 (8mil)	152 (6mil)	127 (5mil)
UBM Mask Name	Cap6	Cap4	Cap3.5	Cap3
UBM Diameter	152	102	90	75
Max Passivation Opening Diameter	132	82	70	55
Minimum Final Metal Size	164	114	102	87
Approved for Sn63/Pb37	YES	YES	YES	YES
Approved for Pb90/Sn10	YES	YES	NO	NO
Bump Height Mean	130	100	87	75

All dimensions are microns unless noted.

Table 2. Solder Bump Array Design Guidelines.

Array Pitch	254 (10mil)	227 (9mil)	204 (8mil)	177 (7mil)	160 (6.3mil)
UBM Mask Name	Cap4	Cap3.5	Cap3.2	Cap3.2	Cap3
UBM Diameter	102	90	80	80	77
Max Passivation Opening Diameter	82	70	60	60	57
Minimum Final Metal Size	114	102	92	92	89
Approved for Sn63/Pb37	YES	YES	YES	YES	YES
Approved for Pb90/Sn10	YES	YES	NO	NO	NO
Bump Height Mean	105	100	90	78	75

All dimensions are microns unless noted.

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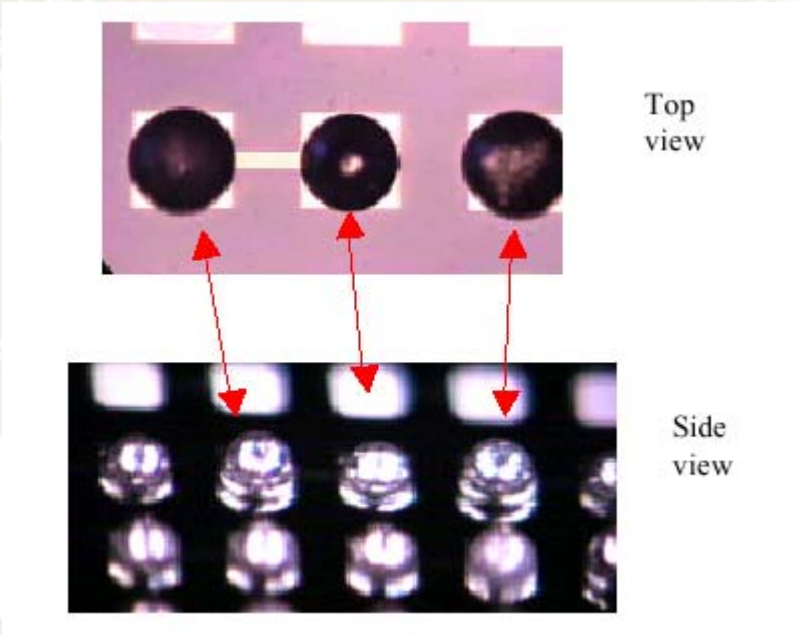
Bump characteristics summary

- Bumps in wide use are .004” to .025” tall
  - Ball tolerance can be as much as ±20%
  - Balls have a wider location tolerance than bond pads
- Bumped wafers typically have areas that do not contain bumps
- Some wafers have no bump free areas



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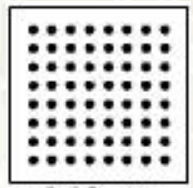
Useful characterizations for probing

> Flip chips can be from 30% to 50% smaller than perimeter attach counterparts



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Challenges in Bump Wafer Probing

- Profile
- Alignment
- Z height detection/probe height measurement
- Automated probe to pad alignment (APTPA)
- High throughput – test cell could be idle during profile and alignment
- Needle cleaning – different needs than bond pads (not covered in this paper)
- “Follow map” probing from inspection equipment (not covered in this paper)

Probe requirements

- Prealignment
  - Must determine center of the wafer relative to chuck center, with bumps as large as .034”.
  - Must find wafer edges for bumped wafers with bump arrays all the way to the edges.
  - Must not “lose” die in the case of very small die and inaccurate edge detection.

Probe requirements

- Profiling/ Z alignment
  - The profiler must be able to detect the wafer surface between bumps, or bump arrays as high as .034”.
  - Determine the nominal height of the tops of the bumps, which is probing height.

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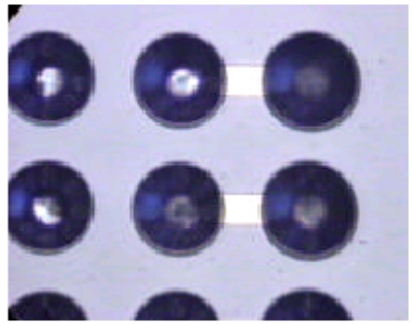
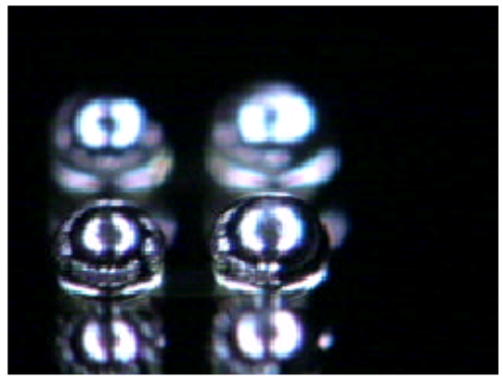
Prober requirements

- APTPA
  - Based on the size and tolerance of the balls, the ball targets could vary. For example, a .020” nominal ball diameter could have balls from .014” to .026”. This range is based on various ball manufacturers specifications and tolerances. In practice, a given wafer would likely exhibit more uniformity.



Top View



Side view

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Prober requirements – high throughput

> Alignment (and potentially profiling) time detracts from overall test cell throughput.

> Tester is “down” during alignment – reducing tester utilization

> Must be accurate, but fast!

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Proposed Solutions

- Finding the Wafer Edge – critical!
  - Scan from outside of the wafer edge at a safe height (nominal wafer thickness + bump height + tolerance) towards the wafer center until the edge is detected.

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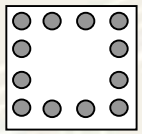
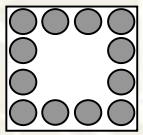
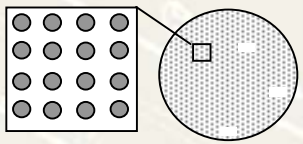
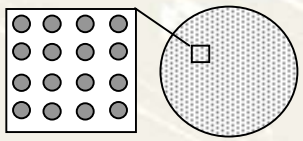
Useful characterizations for probing

Category 1 	**Peripheral bumps with clear area, bumps are .005" or smaller**	**Profile surface between bumps**
Category 2 	**Peripheral bumps with clear area, bumps are up to .035"**	**Profile surface between bumps**
Category 3 	**Die are area array and fully populated. Clear areas exist on wafer edge and OCR**	**Profile clear areas on the wafer edge or OCR**
Category 4 	**Wafer is fully populated with bumps. No clear areas exist**	**Profile bumped area, fit bump by application or offset**

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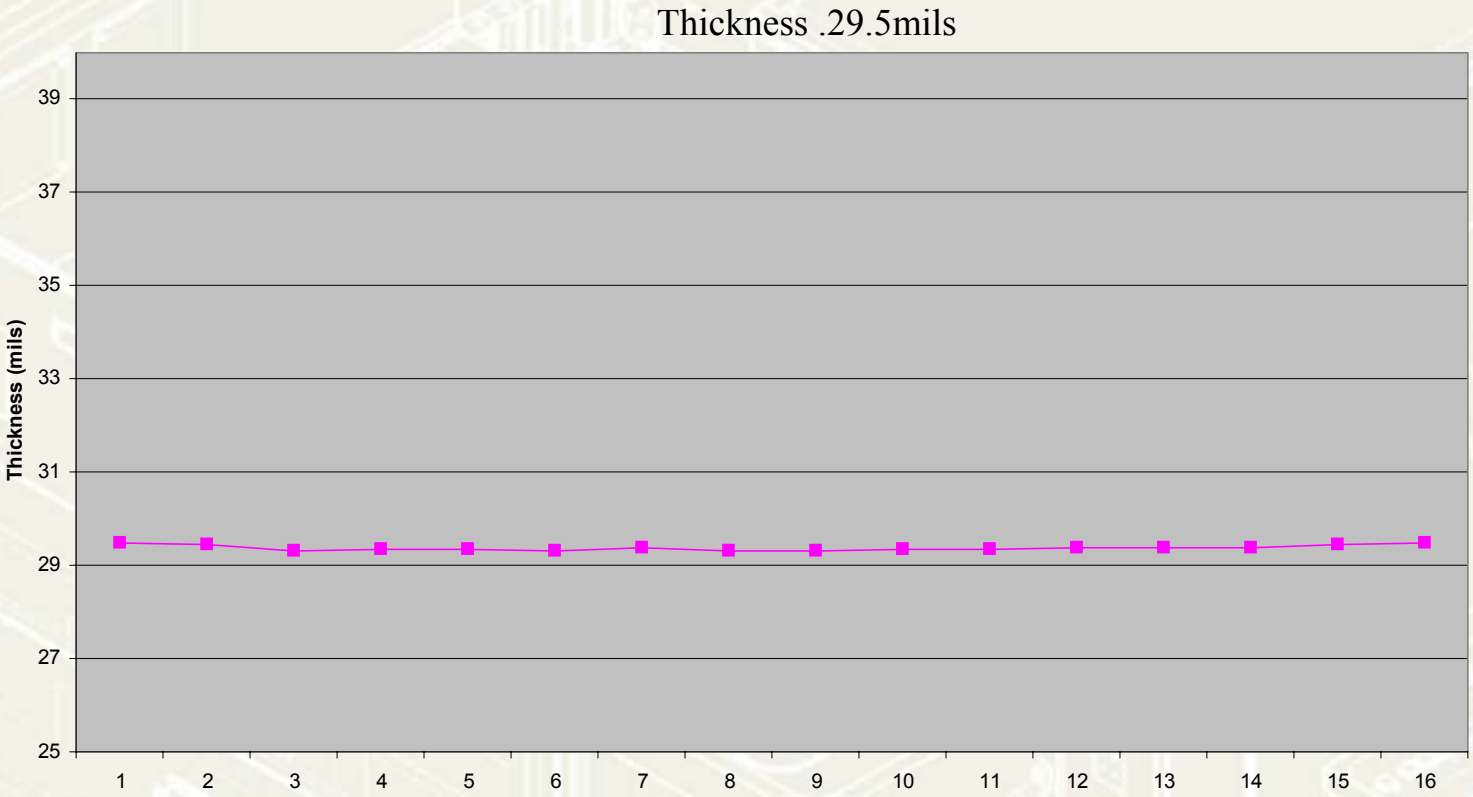
Solutions

- Categories 1 through 3
  - Find the wafer surface and add the bump height
  - Finding the wafer surface height
    - Train several bump free sites.
    - Find the wafer surface height at those sites.
    - Add bump height to the wafer surface height, which becomes probing height.
    - Is this a valid approach?

Finding the wafer surface



Solutions

- Category 4
  - Profile the aggregate surface
    - Determine profiler spot size versus ball area
    - Profiler measurement will be an average of these areas
  - Add in offset to product file to obtain probing "Z" height

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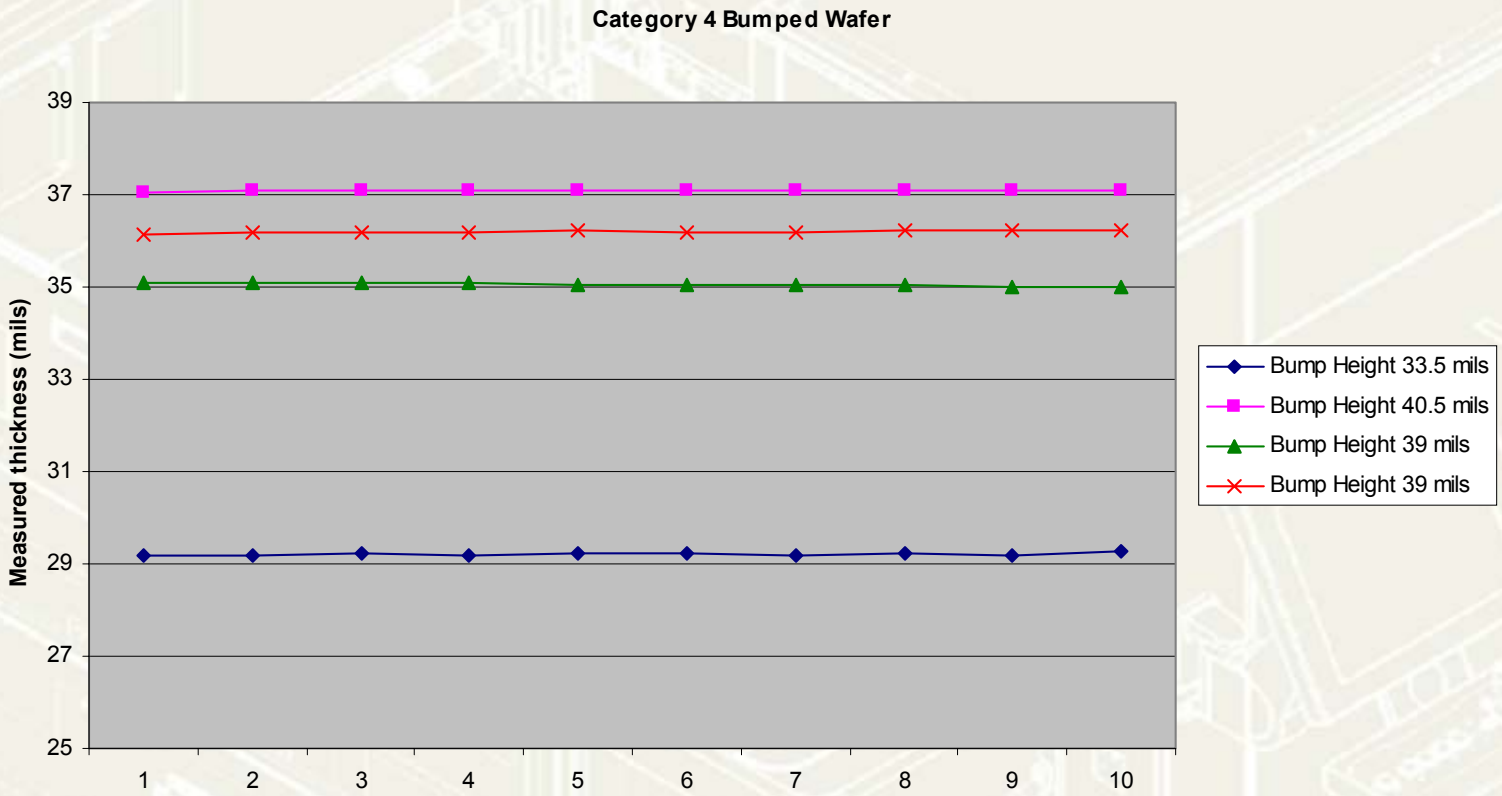
Category 4 data



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Summary and conclusions

> Bump probing is becoming more of a requirement

> New prober features are needed to process bumped wafer

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References

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