High Productivity/Cost Effective Wafer Probing

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Outline

- Overview
- Throughput definitions
- Throughput models
- Throughput Bottlenecks
- Tradeoffs – cost and throughput
- The cost of increased productivity

Overview

- Today's systems and technologies are the stepping stone to the future.
- Will we need enhancements or new designs in the future?
- How much are we willing to pay for more speed?
- What enhancements provide the biggest cost benefit?
- How do we recognize design overkill?

Where are we going?

- Scaling the technology
  - Smaller pads – requiring more accurate probers
  - Larger wafers – more die per wafer
  - Multidie arrays – fewer touchdowns
- More of the existing technology
  - Ramp up in production while getting more done using the existing equipment

Prober requirements

- More accurate
- Higher throughput
- Less expensive

What is a prober?

- A prober is an x, y, z positioning robot
- A prober is a peripheral tool of the tester
  - Maximize tester utilization
  - Minimize time doing everything else

Throughput definitions

- Throughput – the number of wafers probed per unit time
- Process time – the amount of time spent performing a specific task
- Overhead time – the amount of time the system spends preparing for the performance of a task
- Handoff time – the time spent transitioning between tasks
- Throughput limit – the maximum throughput achievable by the slowest component of the process
- Bottleneck – the slowest step of the process

Example – Fast Food

- Throughput
  - The number of customers served per minute
- Process time
  - The time spent preparing the food
- Overhead time
  - The time spent taking the order
- Handoff time
  - Time spent getting the order to the cook
  - Time spent getting the food to the customer
- Time per customer = overhead + handoff + process
- Reduce time per customer – increase throughput

Fast Food – continued

- Assume an infinitely long line of customers
- Process time cannot be reduced
  - Capacity can be increased
- Overhead and Handoff time can be reduced
- Reduce time per customer, increase total customers, increase revenue

Fast Food – continued

- Assume a finite number of customers
- Total revenues are fixed
- Is there a benefit to increasing throughput?

Prober Throughput Model

- We create a throughput model defined by the prober processes and the wafer handling sequences
- Define process time, overhead time, and handoff time
- Simulate the work flow
- Assign the percent utilization of the component

Electroglas Probing Model

- Components
  - Cassette and elevator
  - Material Handler
  - Prealigner
  - Quickloader
  - Chuck
- Processes
  - Prealign
  - Profile
  - Align
  - Probe

Process Flow

MH Flow

- Pickup wafer from cassette
- Prealign
- Transfer to quickloader

Probe Process Flow

- Pickup from quickloader
- Profile
- Align
- Probe
- Move to unload

MH Flow

- Pickup from chuck
- Unload to cassette

Prober throughput will be determined by the slower of the two subsystems. When Probe Process limits throughput, there is no sense in improving MH throughput

Percent Utilization

- Shows the ratio of component activity time to total system time
- High utilization usually indicates a bottleneck
- High utilization of the tester is ideal

Throughput Model Results

Test Scenarios

- Small die, short test times
  - 680 touchdowns, 150 msec test
- Multidie arrays – long test times
  - 25 touchdowns, 1000 msec test
- Solder bump simulation
  - 75 touchdowns, 1000 msec test

Throughput Simulation Data

baseline results

	Tds	Test Time	Throughput wph
Case 1	680	0	10.8
Case 2	680	15 msec	8.2
Case 3	25	1000 msec	22.3
Case 4	75	1000 msec	15.9

- Case 1, 2 – simulates small device, short test time
- Case 3 – simulate DRAM – multidie array, long test time
- Case 4 – simulates solder bump application

Motion improvement

- The benefit of increasing acceleration and slew rate of the drives is a function of the number of touchdowns
- The smaller the die size, the greater the number of steps, the greater the benefit of faster motion
- On small die wafers, increasing all accelerations by 50% will decrease total stepping time by 20% per 1000 die
  - This is mostly because of relatively slow settling times
- On the same wafer, going to 1x8 multi die probing will decrease total stepping time by 80%

Calculated throughput as a function of number of touchdowns, test time, and step time

Tds – test time	300 msec/step	240 msec/step
1000 – 0.15 sec	6.2 wafers/hr	6.9 wafers/hr
125 – 1.20 sec	10.1 wafers/hr	10.3 wafers/hr
125 – 0.15 sec	18.3 wafers/hr	19.1 wafers/hr

Profile and Align Time Improvement

- The smaller the total prober time, the greater the relative impact of profile and align time
- The cost benefit of reduced profile and align time is great because no new equipment is needed
  - Do what you are already doing faster

Effect of Profile Time Reduction on Throughput

	1 x profile	0.5 x profile	0.25 x profile
Case 1	6.2 w/hr	6.6 w/hr	6.8 w/hr
Case 2	10.1 w/hr	11.3 w/hr	12.1 w/hr
Case 3	18.3 w/hr	22.8 w/hr	26.0 w/hr

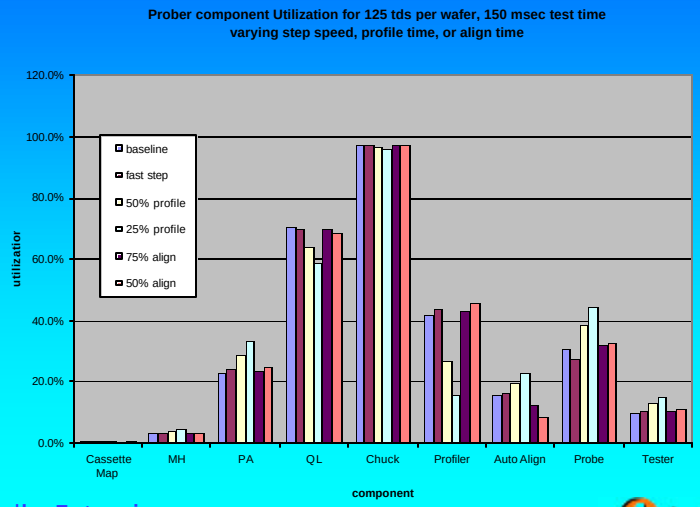
- Case 1 = 1000 tds, 0.15 sec test time
- Case 2 = 125 tds, 1.2 sec test time
- Case 3 = 125 tds, 0.15 sec test time

Effect of Align Time Reduction on Throughput

	1 x align	0.75 x align	0.5 x align
Case 1	6.2 w/hr	6.2 w/hr	6.2 w/hr
Case 2	10.1 w/hr	10.3 w/hr	10.5 w/hr
Case 3	18.3 w/hr	19.0 w/hr	19.7 w/hr

- Case 1 = 1000 tds, 0.15 sec test time
- Case 2 = 125 tds, 1.2 sec test time
- Case 3 = 125 tds, 0.15 sec test time

Component Utilization



Throughput Improvement Economics

- What to improve
  - Prober
    - Profile – small investment quick ROI
    - Align – small investment quick ROI
    - Stepping – large investment slow ROI
  - Test
    - Multi die
    - Parallel test
      - if you have the capability then big benefits, otherwise, big investments

ROI – Increased Stepping Speed

- Annual increased revenues resulting from faster stepping speed

Variable	Baseline Throughput Results	Enhanced Throughput Results
Hrs per week	158	158
Hrs per year (50 weeks)	7,900	7,900
Test time sec.	0.15	0.15
Wafer per hr	6,200	6,900
Wafers per year	48,980	54,510
Delta wafers per year	0	5,530
Die per wafer	1,000	1,000
Die per year (90% yield)	44,082,000	49,059,000
Delta die per year	0	4,977,000
ASP per die	$0.10	$0.10
Rev. per wafer	$100	$100
Rev. per year	$4,408,200	$4,905,900
Rev. Gain		**$497,700**

ROI – Parallel Testing

- Annual increased revenues resulting from 8x1 parallel testing

Variable	Baseline Throughput Results	Enhanced Throughput Results
Hrs per week	158	158
Hrs per year (50 weeks)	7,900	7,900
Test time sec.	0.15	0.15
Wafer per hr	6,200	18,300
Wafers per year	48,980	144,570
Delta wafers per year	0	95,590
Die per wafer	1,000	1,000
Die per year (90% yield)	44,082,000	130,113,000
Delta die per year	0	86,031,000
ASP per die	$0.10	$0.10
Rev. per wafer	$100	$100
Rev. per year	$4,408,200	$13,011,300
Rev. Gain		**$8,603,100**

ROI – Reduced Profile Time

- Annual increased revenues resulting from 50% reduction in wafer profile time

Variable	Baseline Throughput Results	Enhanced Throughput Results
Hrs per week	158	158
Hrs per year (50 weeks)	7,900	7,900
Test time sec.	0.15	0.15
Wafer per hr	18,300	22,800
Wafers per year	144,570	180,120
Delta wafers per year	0	35,550
Die per wafer	1,000	1,000
Die per year (90% yield)	130,113,000	162,108,000
Delta die per year	0	31,995,000
ASP per die	$0.10	$0.10
Rev. per wafer	$100	$100
Rev. per year	$13,011,300	$16,210,800
Rev. Gain		**$3,199,500**

Summary

- There is room for significant improvement in prober throughput with relatively simple changes
  - Great potential increase in throughput by going to parallel test
  - Good potential increase in throughput by decreasing profile time
  - Little throughput benefit in improving the MH side of the prober