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# A Computer-based Probing C.O.O. Model

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# A Computer-based Probing C.O.O. Model
## Outline

- Total Cost of Ownership
- COO as part of IFX Probe Card Selection Tool
- Cost Elements
- Computer-based Probing COO Tool
- Vendor Cost Model Parameters
- Calculation Parameters
- Probe & Test time related costs
- Volume trend analysis
- Examples
- Multi-DUT trend analysis
- Contributing factors

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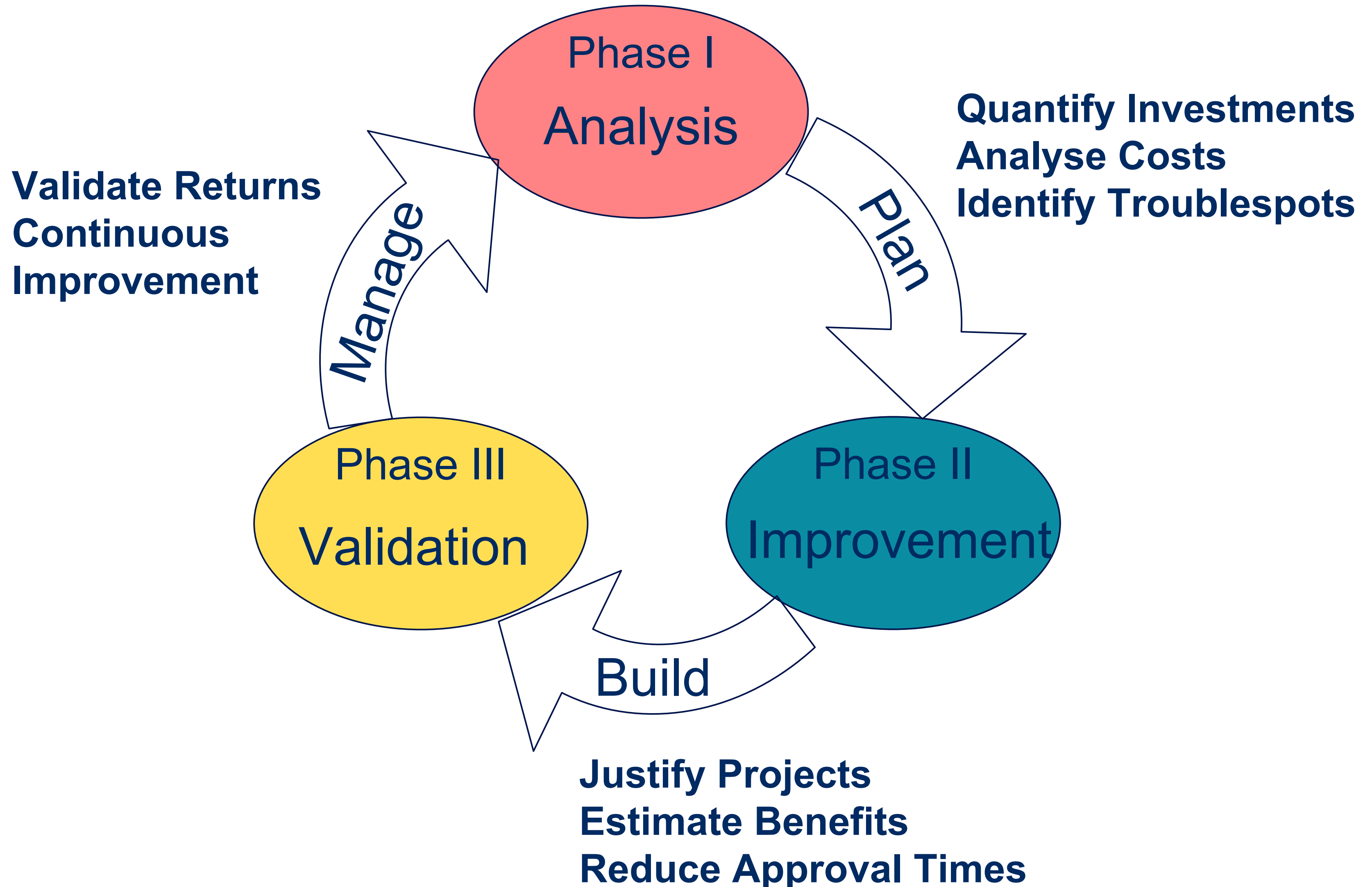
# A Computer-based Probing C.O.O. Model
## What Is Cost of Ownership (COO)?

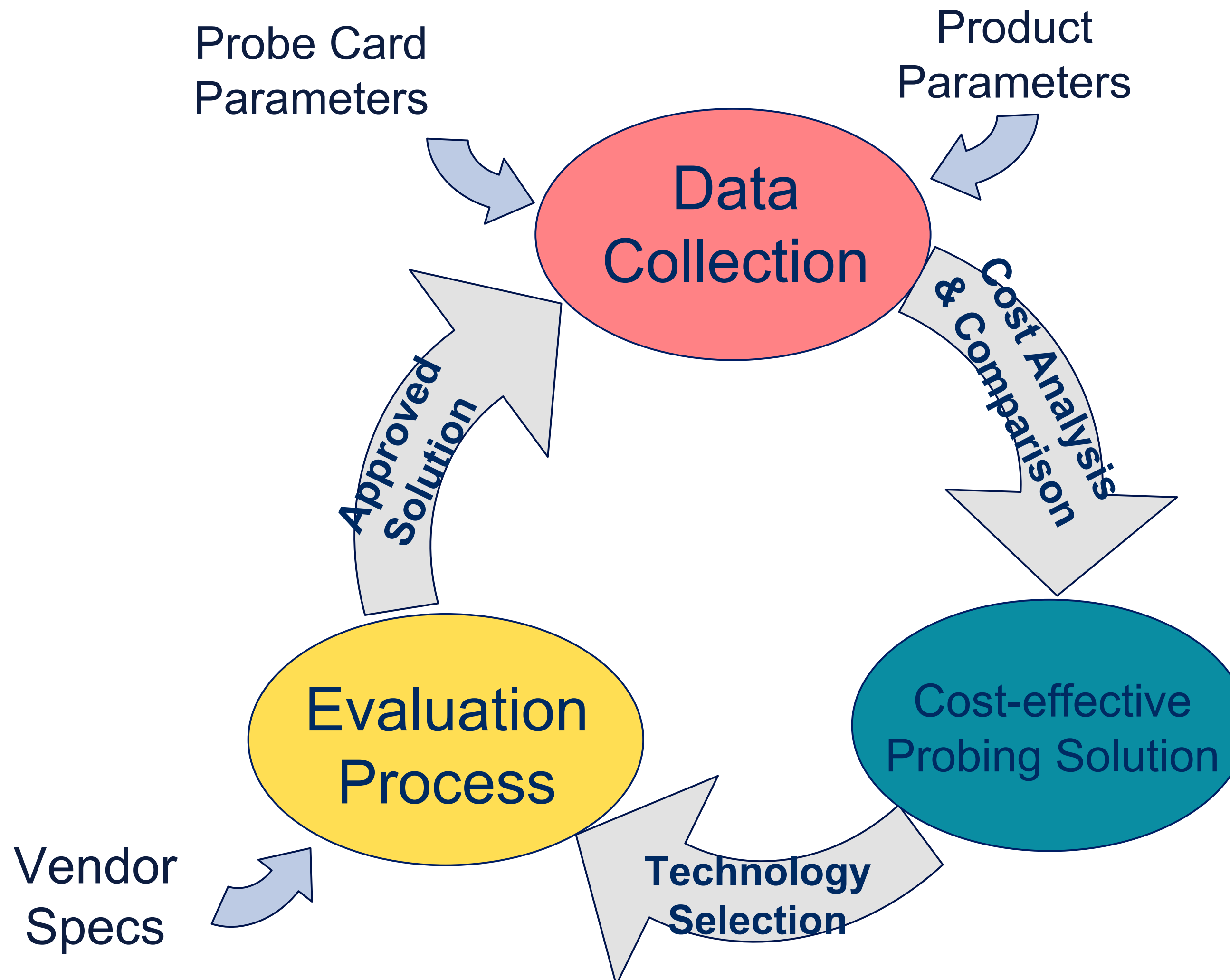
- COO is used to support decisions involving computing systems, laboratory, testers and manufacturing equipment, for instance.
- Calculates total costs over a specific time period
- Includes the 'hidden' costs, e.g. maintenance, cleaning, yield, and installation
- Provides the tool to assess and manage the cost impact of changes in technology, sourcing and support strategies

# A Computer-based Probing C.O.O. Model
## TCO Lifecycle



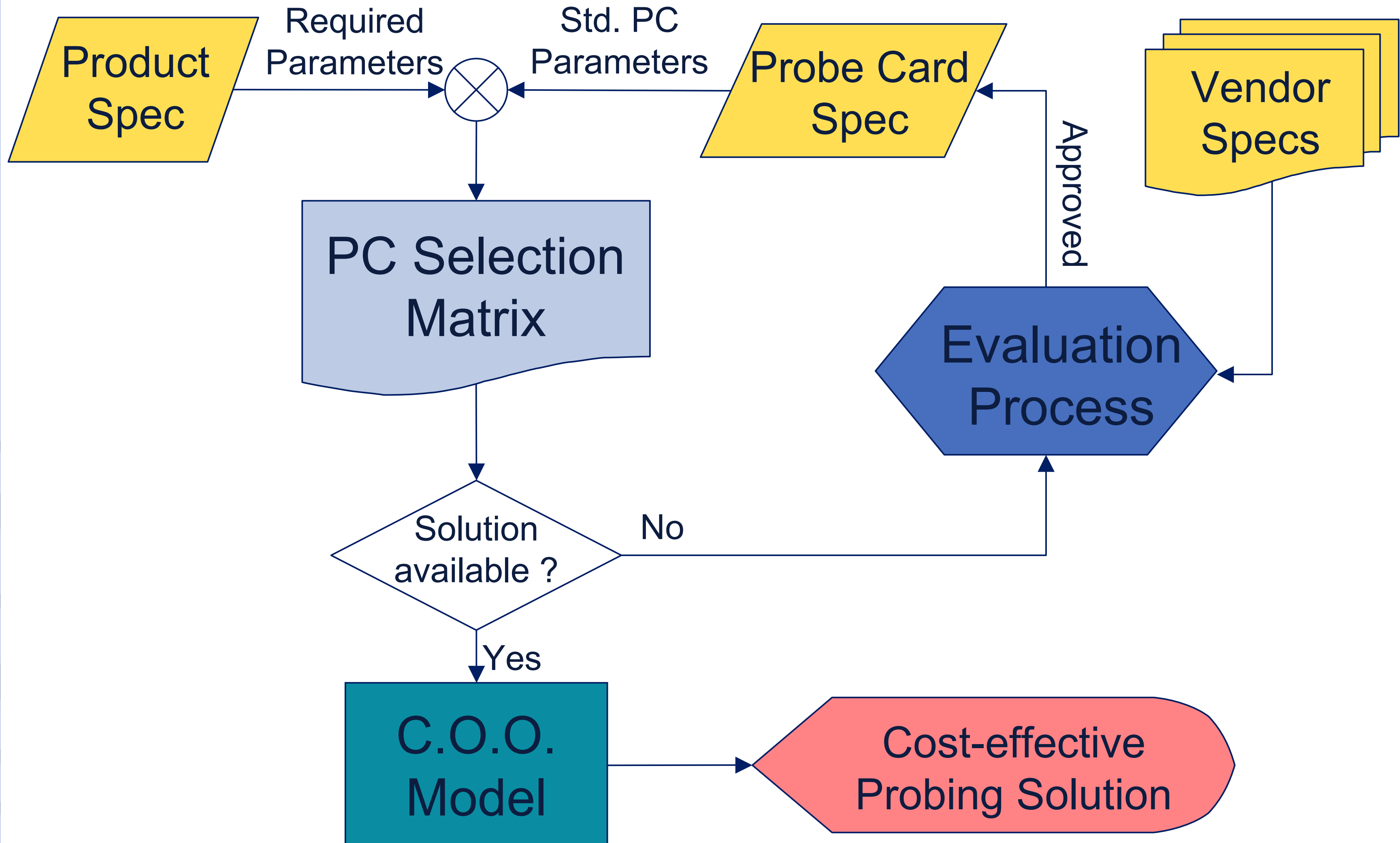
# A Computer-based Probing C.O.O. Model
# Probing COO Lifecycle



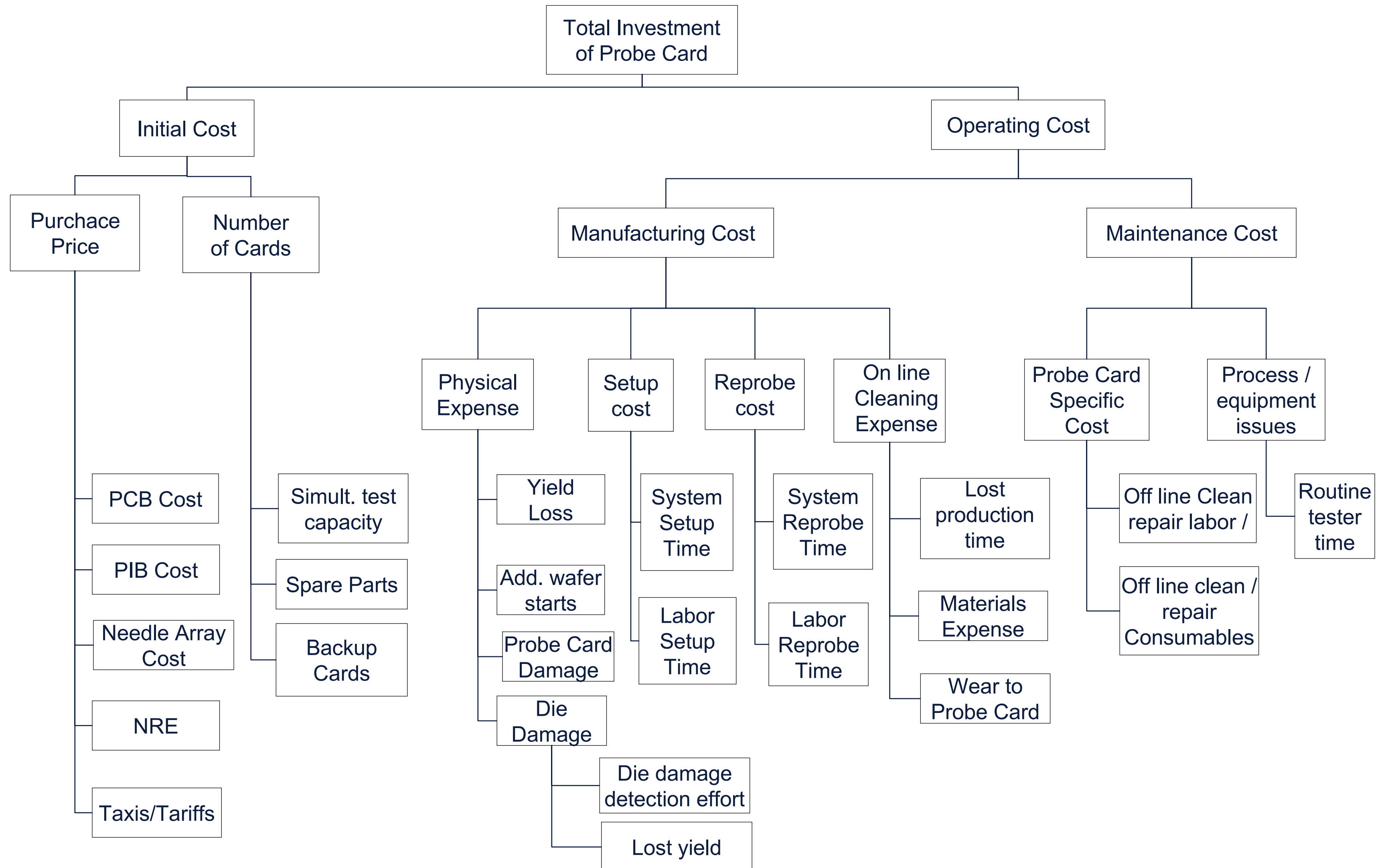


# A Computer-based Probing C.O.O. Model
# Probe Card Selection Tool (PCST)



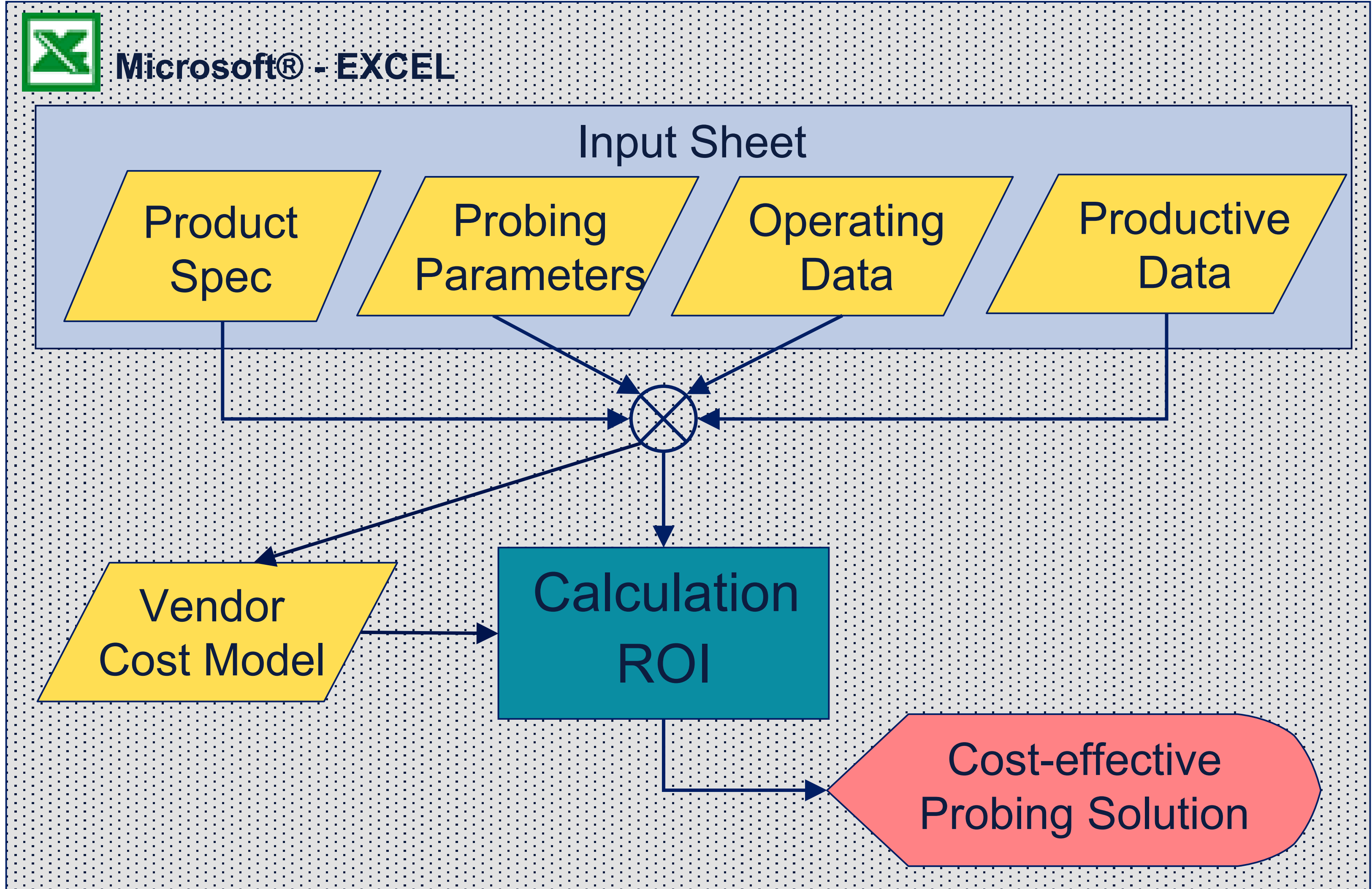


# A Computer-based Probing C.O.O. Model
# Cost Elements



# A Computer-based Probing C.O.O. Model Process Flow





# A Computer-based Probing C.O.O. Model
## COO as MS-EXCEL Tool



Version 15

Notes:

| Mandatory Input Field |
|---|
| Optional input field |

| Parameter | Unit | Value |
|---|---|---|
| **Product Specification** | | |
| Internal Product Name | - | 2222 |
| Dies per wafer | - | 600 |
| Die length | mm | 5.00 |
| Die width | mm | 5.00 |
| Min. Pad pitch | µm | 80 |
| Die contact | - | WB |
| Pad thickness / Bump height | µm | 1000 |
| Bump Diameter | µm | - |
| Pad / Bump material | - | Al |
| Pad layout | - | peripheral |
| Pad length | µm | 70 |
| Pad width | µm | 70 |
| **Probing Parameters** | | |
| # of pads contacted | - | 200 |
| Test temperature (Max) | °C | 25 |
| No. of low speed RF lines (<3Ghz) | - | 0 |
| No. of high speed RF lines (3 - 10 GHz) | - | 0 |
| Maximum current (continuous) | mA | 100 |
| Maximum current (peak) | mA | 200 |
| Bandwidth | MHz | 100 |
| No. of components req'd on the PC | - | |
| **Operating Data** | | |
| Tester model | - | |
| Prober model | - | |
| Test Category | - | |
| # of DUT's | - | |
| Test time per die | s | |
| # of wafers per lot | - | |
| **Productive Data** | | |
| Product life cycle | weeks | |
| Total # of good die | - | |
| Expected yield | % | |
| Cost of wafer (processing) | $ | |
| Ave. # of probers per operator | - | |
| Prober operator cost per hour | $ | |
| Pcard technician cost per hour | $ | |
| Ave. cost of tester time per second | $ | |
| Wafer inspection,points per wafer | - | |
| Wafer inspection,time per point (seconds) | s | |
| Tester working time per week (hours) | h | |

| Probing Technology | Unit | Reference |
|---|---|---|
| Preferred Vendor | - | Supplier A |
| Typical probe card life | # of TD's | 1,000,000 |
| Cleaning frequency | # of TD's | 200 |
| Cleaning cycle duration | s | 20 |
| Maint. cycle | # of TD's | 10,000 |
| Maint. exp. (mat'ls, equip., ...) | $ | $200.00 |
| Maint. time | min. | 90 |
| Pcard rebuild frequence | # of TD's | 500,000 |
| Probe card mishandling loss | % | 2.00% |
| Retest Rate | % | 3.00% |
| Yield loss - pad damage | % | 0.20% |
| Yield loss - Cres | % | 0.0% |
| Ave. pcard setup time | min. | 30.0 |
| Wfr inspect. freq | n wafers | 10 |

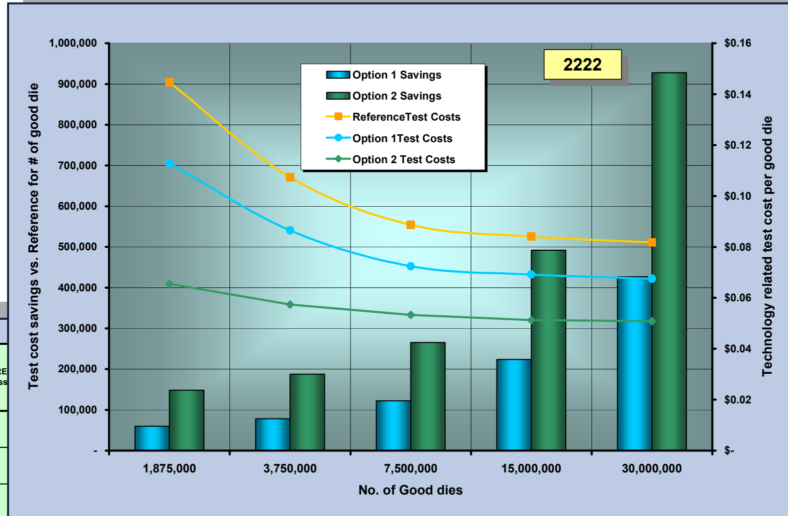
Input Sheet

| Probe card technology | Supplier | Probe head version | Pitch | Test temp. | # of DUT's | Price per Probe Head | Quantity Discount | Discounted Price per Probe head | NRE Probe Head | PCB | NRE Ass |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Cantilever | Supplier A | n/a | ≥60 | RT - 125 | 1<br>2<br>4 | $ 29,759.01 | 0.0% | $ 29,759.01 | $ - | $ 5,000.00 | $ |
| | Supplier B | | ≥60 | RT - 110 | 1<br>2<br>4 | $ 15,870.30 | 0.0% | $ 15,870.30 | $ - | $ 5,000.00 | $ |
| Vertical | Supplier C | Version A | <115 | RT - 124<br>125 - 150 | ≥1 | FALSCH | 4.0% | $ - | $ - | $ 5,000.00 | $ |
| | | Version B | 100 - 114 | ≤150 | ≥1 | $ 24,193.55 | | $ 23,225.81 | $ 2,419.35 | | |
| | Supplier D | n/a | ≥ 80 | ≤ 125 | | $ 23,000.00 | 0.0% | $ 23,000.00 | $ - | $ - | $ - |
| Membrane | Supplier E | Version A<br>Version B | ≥60 | RT - 125 | | | | | | | |
| | Supplier F | n/a | ≥ 70 | | | | | | | | |

| Pitch | 80 |
|---|---|
| No. of Pads | 200 |
| No. of low speed | 0 |
| No. of high speed | 0 |
| No. of DUT's | 4 |
| Test Temp. | 25 |
| Die Size | 25.00 |
| Order Volume | 9 |

| Currency conver | |
|---|---|
| 1US$ = | 0.93 |
| | 119 |

Vendor Cost Model




Graphical Output

| Cost Element | Reference | Option 1 | Option 2 | Comments |
|---|---|---|---|---|
| # of DUTS (ie x 1,2,4 etc) | 4 | 4 | 4 | |
| Number of lots per setup | 3 | 13 | 53 | |
| Average cost per die | | 3.52 | | |
| Ave # of testers per week | | 2 | | |
| Ave. Weekly run rate (die xk) | | 333.34 | | |
| Total die probed | 31,642,232 | 31,610,558 | 31,585,264 | total good die required / elect yield per card technology / mech yield per card technology |
| Run rate per week | 351,580 | 351,228 | 350,947 | total die probed / product life cycle |
| Ave # of probe cards utilized per week | 2.00 | 2.00 | 2.00 | (weekly run rate * test time per die) / # of DUTS per card per week |
| Add. # of probe cards required over life time | 6.00 | 6.00 | 2.00 | = total die probed / typical probe card life rounded up /# of DUTS per card per week |
| Percentage of cards **underutilized** | 1.49% | 1.62% | -194.82% | = % of probe cards (or probe heads) used for less than full life |
| **% usage** of underutilized card | 291% | 290% | 295% | = for card underutilized, %age (0f life in touchdowns) it is used |
| | | | | |
| Probe card purchase price | $29,759 | $23,226 | $0 | Pcard Initial purchase price;for vertical this is replaceable "core" cost |
| Probe card board price | $5,000 | $5,000 | $9,000 | For Pyramid the PCB board is reuseable; cores are replaceable |
| NRE Charge, one time | $0 | $2,419 | $12,545 | Any NRE for the current or alternative probe technology should be input above |
| Cost of pcard mishandling | $ 595 | $ 232 | $ - | Design/robustness of "Alternatives" prevents damage by most simple handling errors. |
| **Total initial probe card costs** | $ 282,834 | $ 230,084 | $ 48,545 | (Cant.pcard(assembled) or vert.core+pcb cost * Qty req'd) + one time NRE |
| | | | | |
| # of backup cards or replacable heads | 1 | 1 | 1 | |
| Cost of backup capability | $ 34,759 | $ 23,226 | $ - | Complete card for cantilever,probe head only for other |
| **Initial purchase cost** | $ 317,593 | $ 253,310 | $ 48,545 | |
| | | | | |
| Probe card rebuilds required | 1 | 1 | 1 | "Current" requires total rebuild - "alts 1&2" eg vertical require core replacement only |
| **Probe card rebuild cost** | $ 34,759 | $ 23,226 | $ - | |
| | | | | |
| Maintenance cycles | 790 | 157 | 38 | = probe life (touchdowns) / maintenance cycle (touchdowns) - 1 |
| Probe card maint. - material cost | $ 158,011 | $ 15,705 | $ 385 | = ext charge or exp. for internal supplies, space, equip. depreciation, etc. per maint. cycle |
| Probe card maint. - labor cost | $ 47,403 | $ 9,423 | $ 257 | = Internal labor cost: maintenance time * probe card technician cost per hour |
| **Offline maint. cost** | $ 240,174 | $ 48,354 | $ 641 | |
| | | | | |
| Number of wafers | 52,737 | 52,684 | 52,642 | |
| Required total setups | 791 | 158 | 39 | total # of lots / setup per # lots (per pcard type) |
| Probe set-up - labor cost | $ 7,911 | $ 1,581 | $ 395 | = no. of required setups * Setup time in hours * labor cost per hour |
| Probe set-up - tester time cost | $ 42,717 | $ 8,535 | $ 2,132 | = Average cost of tester time * Setup time (sec) * no. of setups |
| **Tester set-up cost** | $ 50,628 | $ 10,115 | $ 2,527 | |
| | | | | |
| Online Probe cleaning cycles | 39,553 | 15,805 | 1,579 | = probe life (touchdowns) / touchdowns between cleanings / # of DUTS per card |
| Probe tip cleaning - labor cost | $ 879 | $ 351 | $ 35 | = # of cleaning cycles * cleaning cycle time * operator cost / # of probers per operator |
| Probe tip cleaning - tester time cost | $ 23,732 | $ 9,483 | $ 948 | = # of cleaning cycles*cleaning cycle time* avg. cost of tester time per sec |
| **Online cleaning cost** | $ 24,611 | $ 9,834 | $ 983 | |
| | | | | |
| # of reprobed die | 949,267 | 632,211 | 157,926 | = reprobe % * total number of die probed with single-DUT probe card |
| Reprobe - labor cost | $ 6,328 | $ 4,215 | $ 1,053 | = no. of die reprobed * test time per die * prober operator cost / # of probers per operator |
| Reprobe - tester cost | $ 170,868 | $ 113,798 | $ 28,427 | = no. of die reprobed * test time per die * tester cost |
| **Reprobe(selective retest)** | $ 177,196 | $ 118,013 | $ 29,480 | |
| | | | | |
| Wafer inspection - labor | $ 2,637 | $ 1,054 | $ 263 | = no. of wafers inspected * time per inspection * labor cost |
| Wafer inspection - tester time | $ 4,746 | $ 1,897 | $ 474 | = no. of wafers inspected * time per inspection * cost of tester time |
| | | | | |
| **Mech. yield loss** (pad damage) | $ 211,371 | $ 105,580 | $ 21,099 | good die rejected with Cantilever versus with alternatives |
| | | | | |
| **Cost of test time** | $ 1,423,900 | $ 1,422,475 | $ 1,421,337 | = no. of die * test time per die * tester cost / # of DUTS per card |
| **Relative elect. yield loss** | $ 2,564 | $ 1,138 | $ - | relative to most cost effective option |
| Total tester hours used | 15426 | 14409 | 13457 | |
| | | | | |
| **Probe Card Related Costs** | $ 1,028,955 | $ 548,156 | $ 104,011 | |
| | | | | |
| **Total Probe Cost of GOOD die required** | $ 2,452,855 | $ 1,970,632 | $ 1,525,348 | |
| **Cost savings** | $ - | $ 482,224 | $ 927,507 | |
| | | | | |
| **Total Probe Cost Per Million Good Die** | $ 81,762 | $ 65,688 | $ 50,845 | |
| **Cost savings per Million Good Die** | $ - | $ 16,074 | $ 30,917 | |
| | | | | |
| **Total TEST Cost Per Good Die** | $0.08 | $0.07 | $0.05 | |

Calculation

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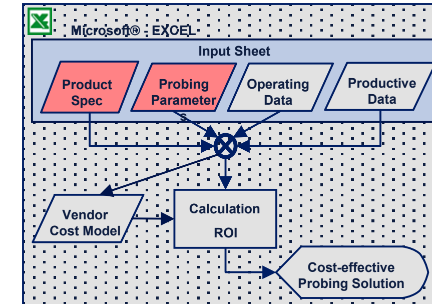
# A Computer-based Probing C.O.O. Model
# Product & Probing Parameters

| Parameter | Unit | Value |
|---|---|---|
| **Product Specification** | | |
| Internal Product Name | - | M1234 |
| Die contact | - | WB |
| Pad thickness / Bump height | µm | 1000 |
| Bump Diameter | µm | - |
| Pad / Bump material | - | Al |
| Pad layout | - | peripheral |
| Dies per wafer | - | 800 |
| Die length | mm | 6.00 |
| Die width | mm | 5.00 |
| Min. Pad pitch | µm | 90 |
| Pad length | µm | 70 |
| Pad width | µm | 70 |
| **Probing Parameters** | | |
| # of pads contacted | - | 200 |
| Test temperature (Max) | °C | 25 |
| Maximum current (continuous) | mA | 100 |
| Maximum current (peak) | mA | 200 |
| Bandwidth | MHz | 100 |
| No. of low speed RF lines (<3GH | - | 0 |
| No. of high speed RF lines (3 - 1 | - | 0 |
| No. of components req'd on the | - | 0 |

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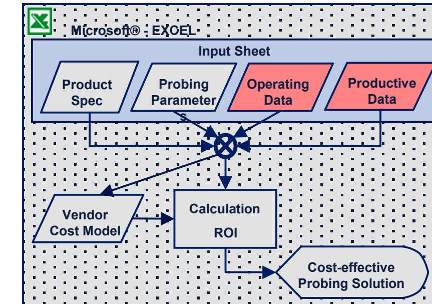
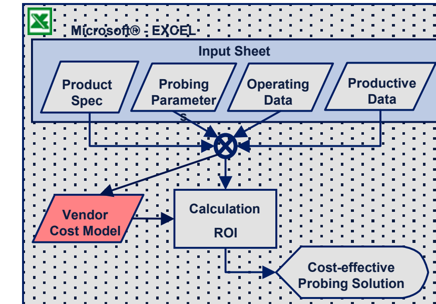
# A Computer-based Probing C.O.O. Model Operating & Productive Data




| Operating Data | | |
|---|---|---|
| Tester model | - | J971 |
| Prober model | - | UF200 |
| Test Category | - | digital |
| # of DUT's | - | 2 |
| Test time per die | s | 2.5 |
| # of wafers per lot | - | 25 |
| **Productive Data** | | |
| Product life cycle | weeks | 60 |
| Total # of good die | - | 7,000,000 |
| Expected yield | % | 90% |
| Cost of wafer (processing) | $ | 2000 |
| Ave. # of probers per operator | - | 5 |
| Prober operator cost per hour | $ | 20.00 |
| Pcard technician cost per hour | $ | 40.00 |
| Ave. cost of tester time per seco | $ | 0.05 |
| Wafer inspection,points per wafe | - | 3 |
| Wafer inspection,time per point ( | s | 30.00 |
| Tester working time per week (h | h | 120 |

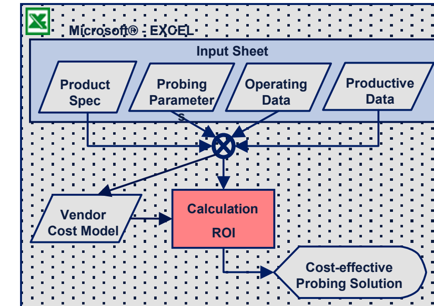
# A Computer-based Probing C.O.O. Model
# Vendor Cost Model

**Technology A / B / C**
**Vendor x / y**




| | Example (in US$) |
|---|---|
| **Probe Head** | |
| Basic Charge (Type, Size, no. of DUT's, Test Temp., Die Size) | 2'000 |
| Price per Pin (Pitch, quantity) | 30 x 150 |
| Price per RF-line (low-/high speed) | 100 x 8 |
| Price per Components (Type) | 100 x 10 |
| **PCB** | |
| Basic Charge (Std./custom design) | 4'000 |
| Sub-total | 4 x 12'300 |
| **Order Volume** | |
| **NRE (one-time)** | |
| Probe Head | 1'500 |
| PCB | 2'500 |
| **Quantity Discount** | 3% 1'596 |
| **Total initial probe card discounted costs** | **51'604** |

# A Computer-based Probing C.O.O. Model Calculation Parameters (I)




- **Initial probe card costs** — from page 12

**+**

- **Total purchase cost** — = Backup Capability

**+**

- **Probe card rebuild cost** — = Depending on Technolgy

**+**

- **Offline maint. cost** — = n cycles x Material + Labor costs

**+**

- **Tester set-up cost** — = n setups x Labor + Tester costs

**+**

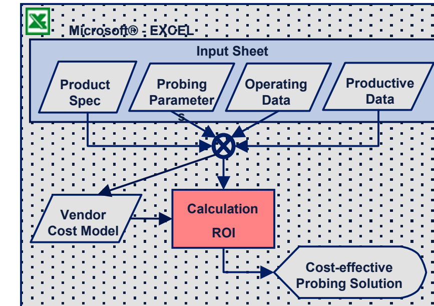
- **Online cleaning cost** — = n cleaning cycles x Labor + Tester costs

**+**

- **Reprobe cost** — = n reprobed dies x Labor + Tester costs

# A Computer-based Probing C.O.O. Model Calculation Parameters (II)






- **Mechanical yield loss** = good dies rejected due to pad damage

**+**

- **Relative electrical yield loss**

**=**

- **Probe related Costs** = Summation of all Pcard related costs

**+**

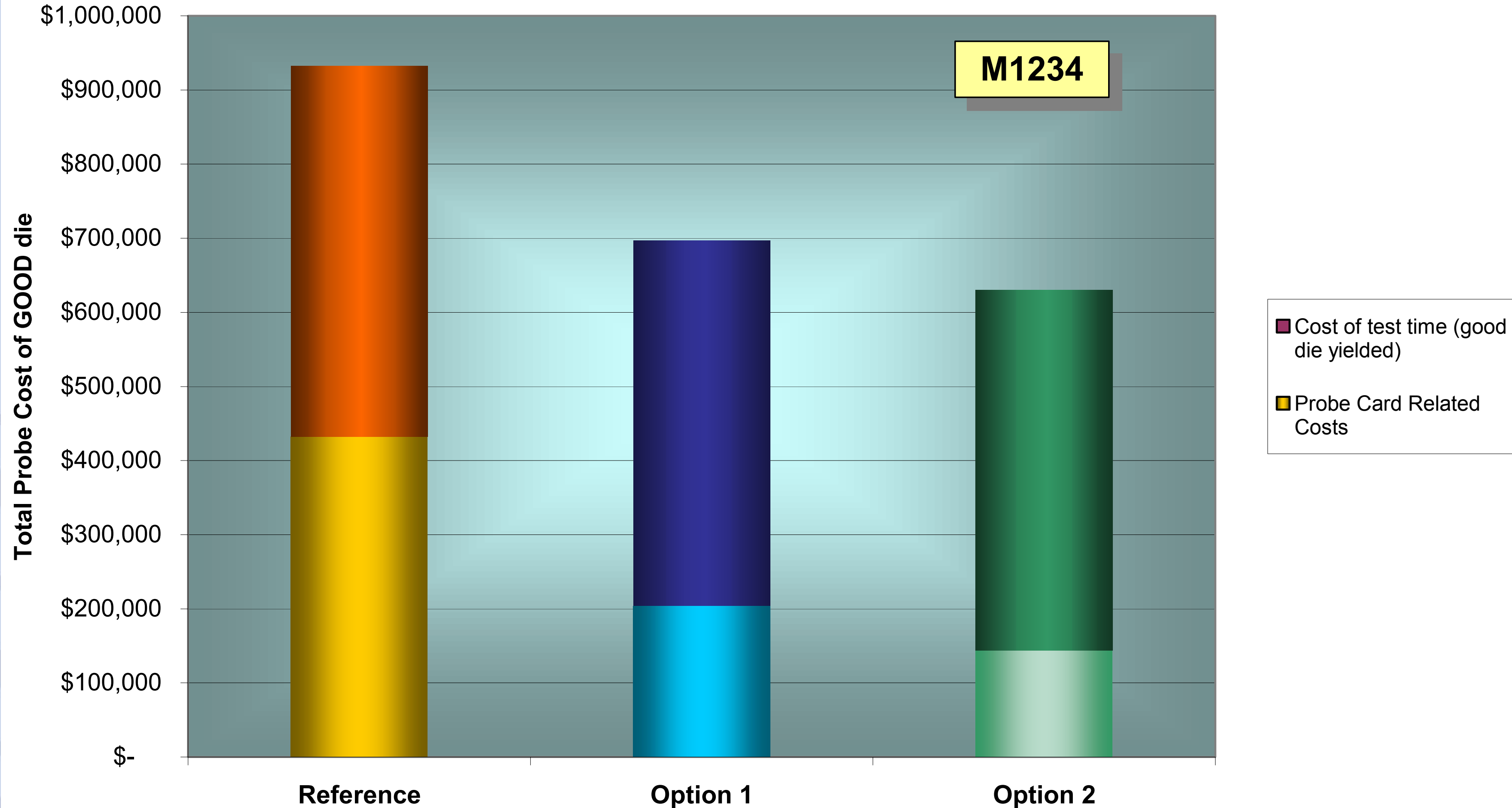
- **Cost of test time** = n die x Tester costs / # of DUTS

**=**

- **Total Probe Costs** = Summation of Tester and Probe Cost

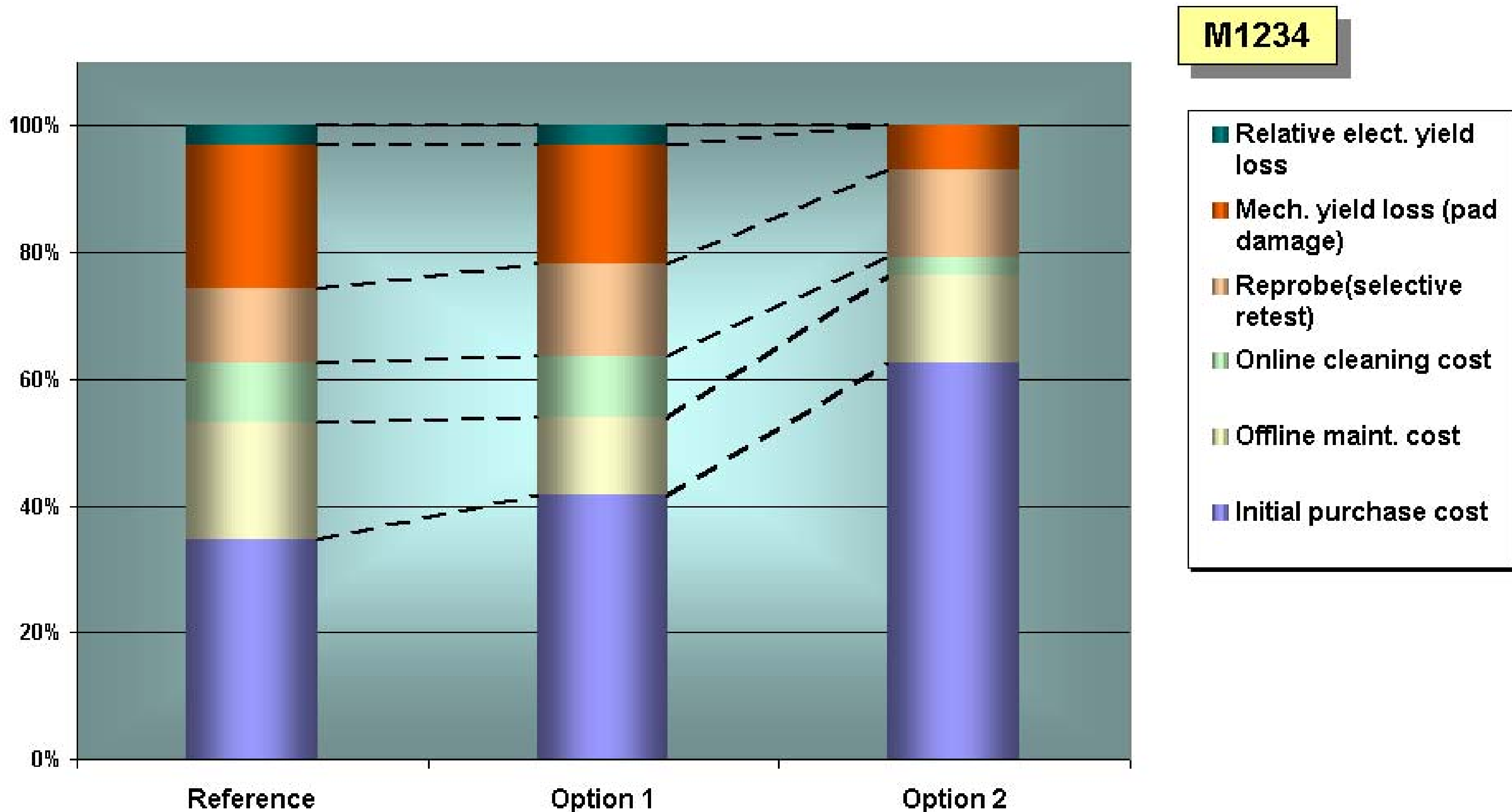
# A Computer-based Probing C.O.O. Model
# Total Probe Cost



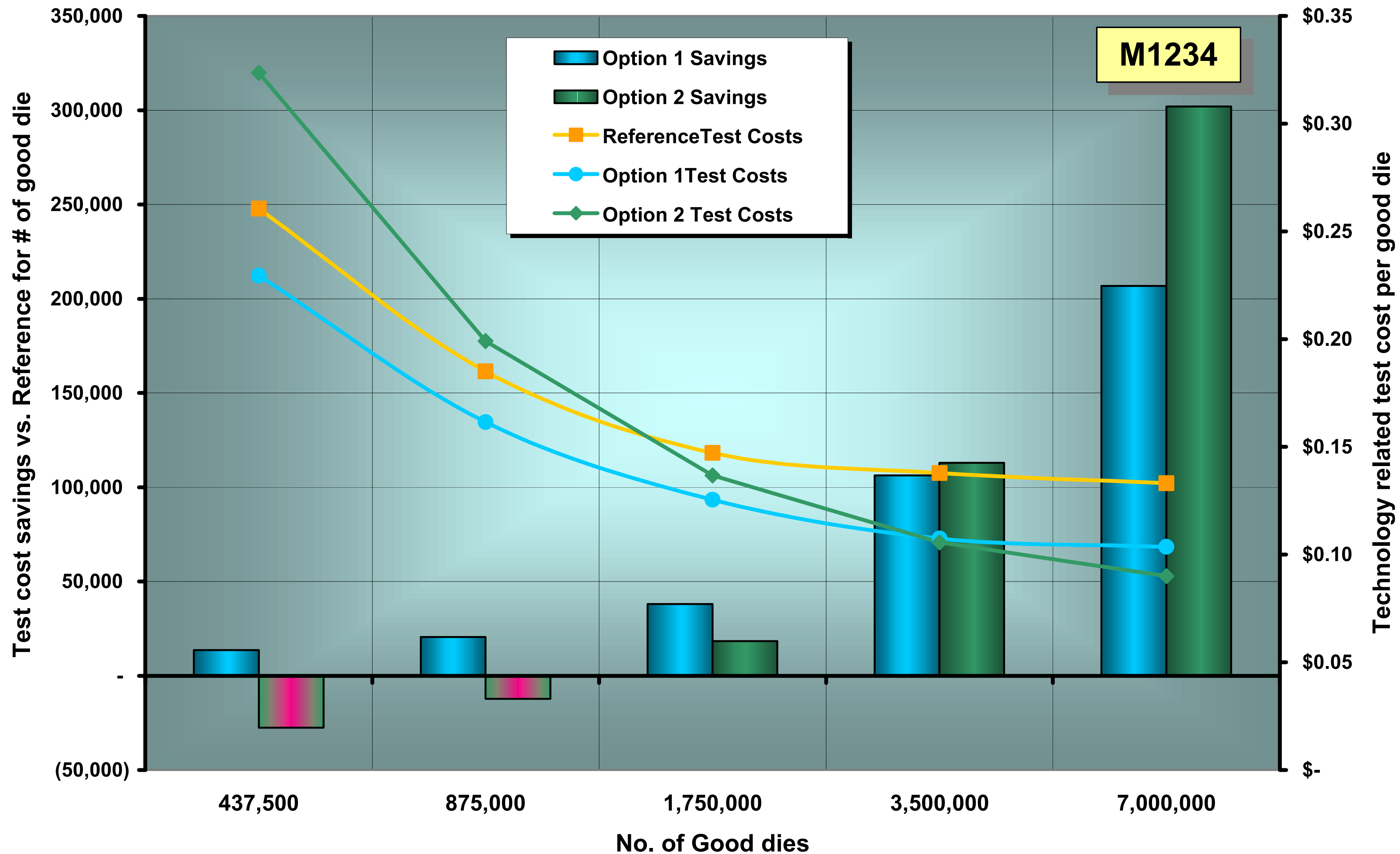


# A Computer-based Probing C.O.O. Model Probe Related Cost





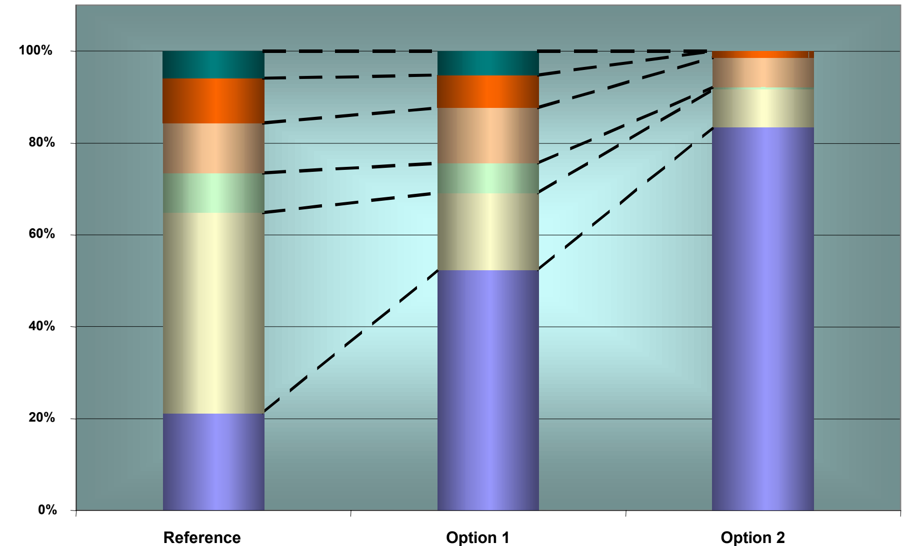
# A Computer-based Probing C.O.O. Model Volume Trend Analysis

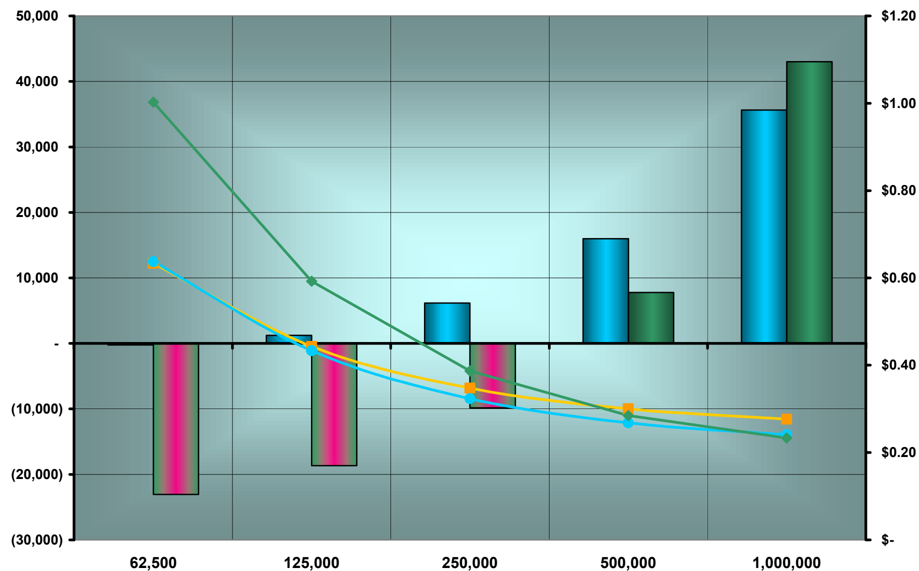


# A Computer-based Probing C.O.O. Model Example 1



- Low pin count (50)
- Low volume (2 Mio.)
- 1-DUT
- Target Yield 85%
- RF-pins
- Short test time (2sec.)
- Cres-related Yield loss
- Max. Retest rate 5%

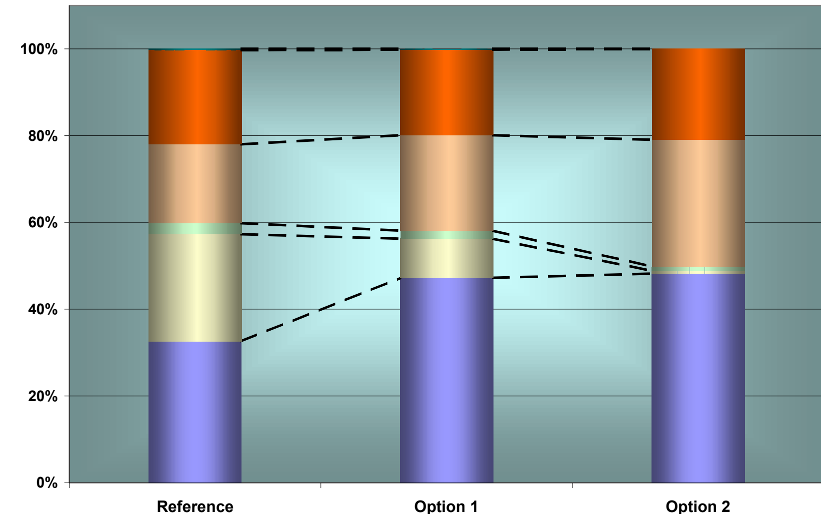


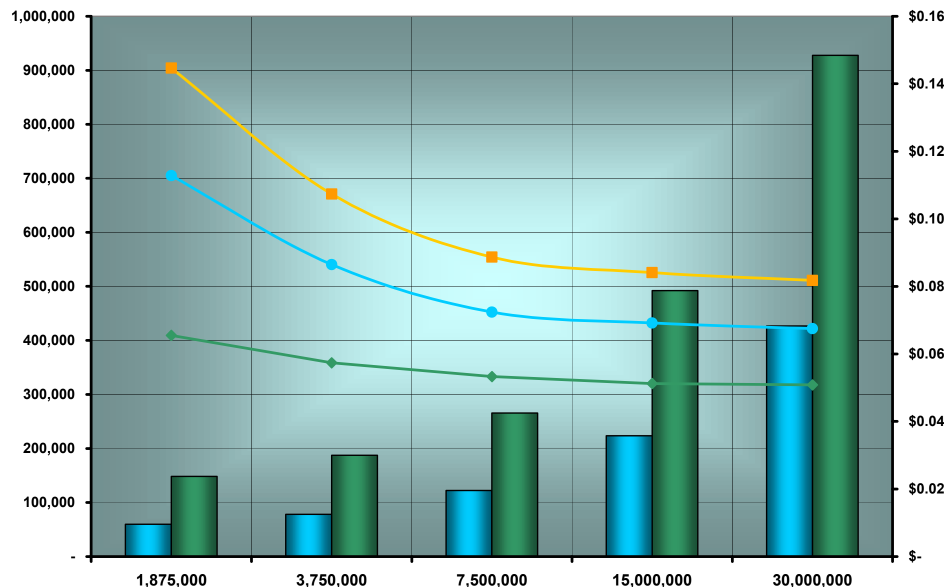



# A Computer-based Probing C.O.O. Model Example 2

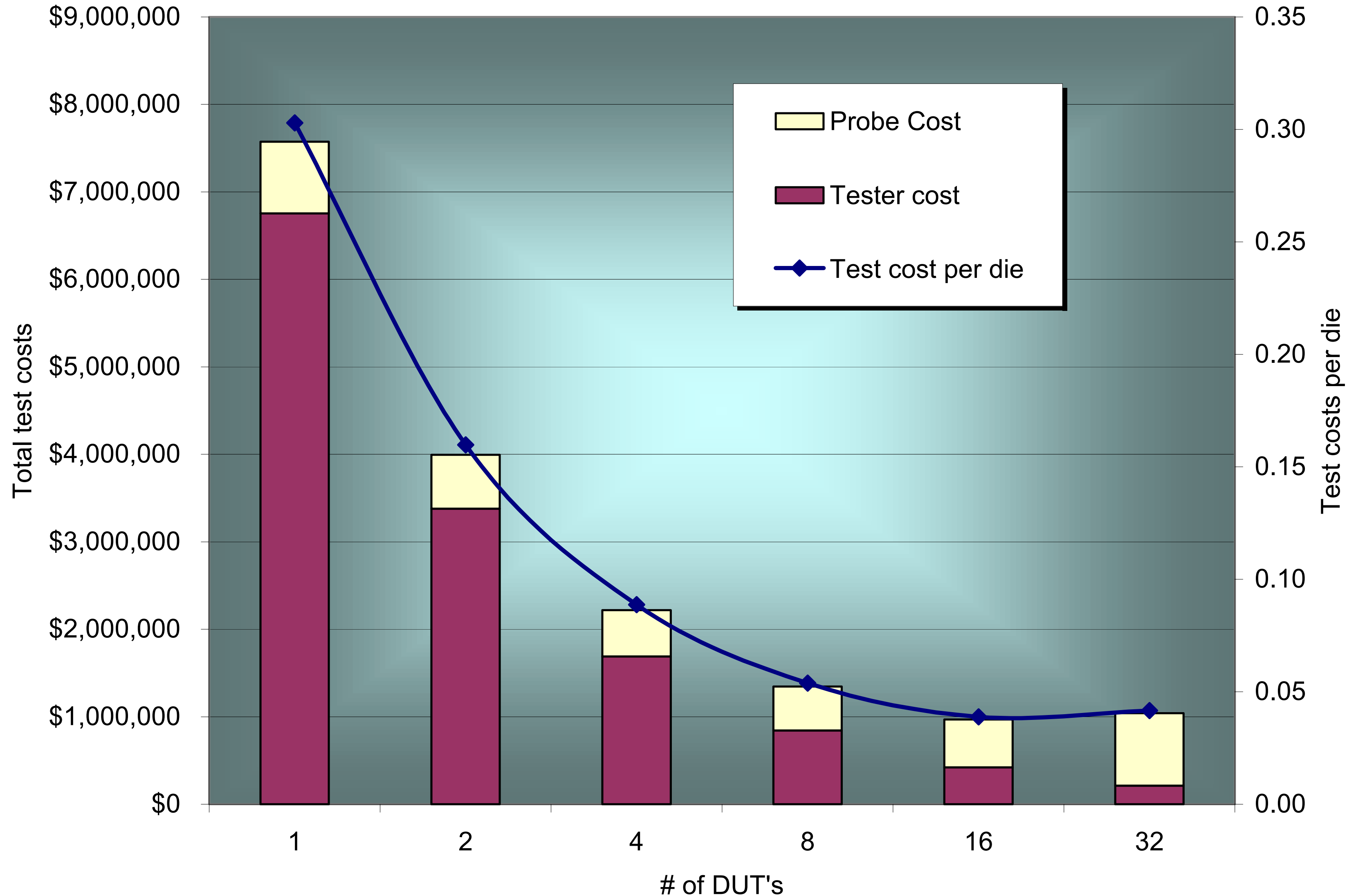


- High pin count (200)
- High volume (>10 Mio.)
- 4-DUT
- Target Yield 95%
- No RF-pins
- Long test time (6sec.)
- No Cres-related Yield loss
- Max. Retest rate 3%



# A Computer-based Probing C.O.O. Model
## Multi-DUT trend analysis



# A Computer-based Probing C.O.O. Model Contributing Factors



- Probe Card Investment
- Probe Card Lifetime
- Cleaning
- Maintenance
- Test time
- Yield/Retest Rate
- Parallelism

} Application Specification

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# A Computer-based Probing C.O.O. Model
## Conclusion

A C.O.O. model applied to probe cards

can determine the most cost effective solution