Intel Test Tooling Operations

Power Delivery Challenges of High Power Logic Device at Sort

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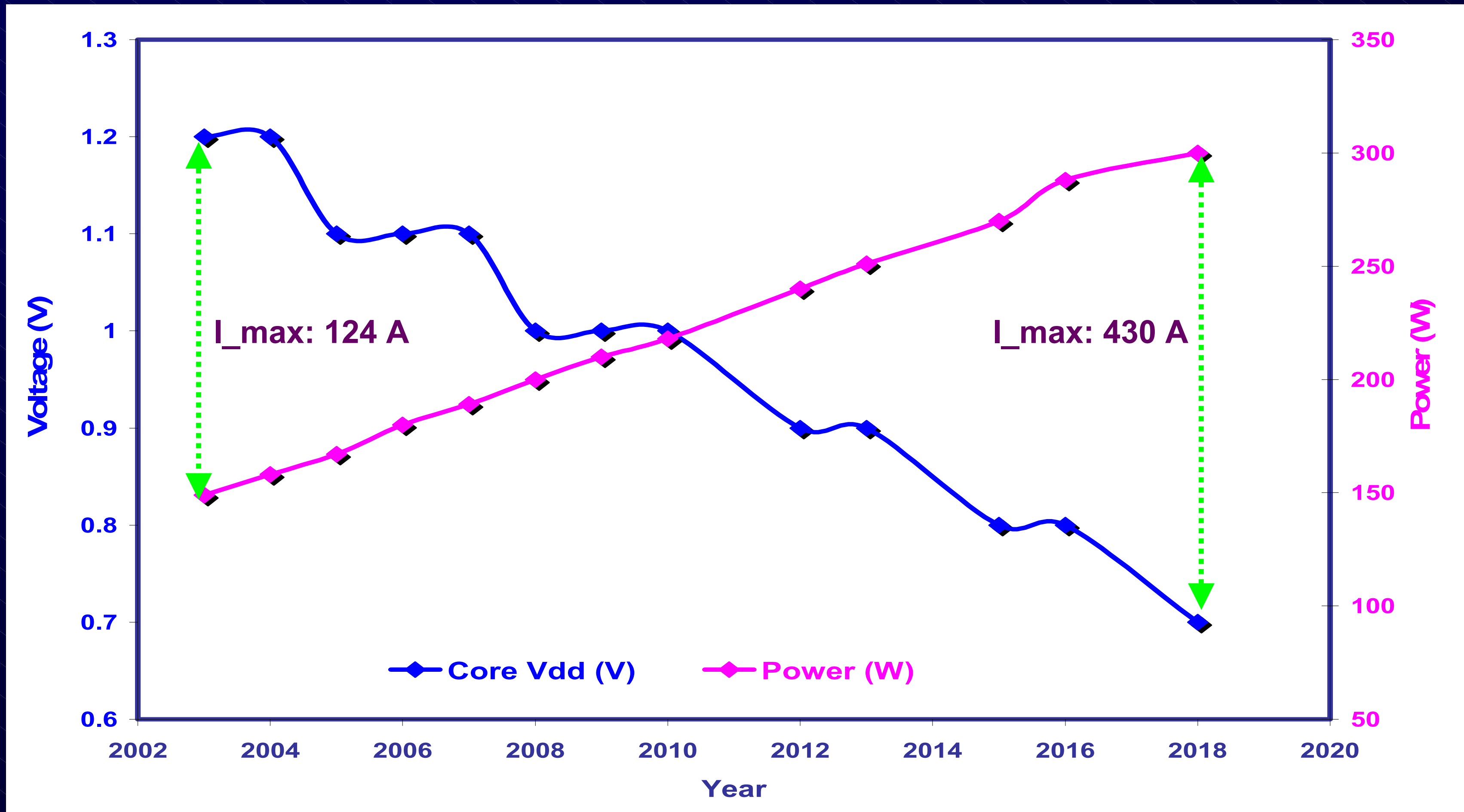
Agenda

- Power Delivery Challenge
  - 2003 ITRS Power Trend
  - Power Trend of Intel® Pentium® 4 Microprocessor
  - Probe Card Power Path
  - Microprocessor Power Distribution
  - Intel® Pentium® 4 Microprocessor Voltage Droop
- Probe Card Power Delivery Improvements
  - Probe Card Power Delivery Design
  - Power Delivery Improvements on Probe Card Components
  - Innovative Improvement Techniques
- Conclusion & Acknowledgement

Probe Card Power Delivery Challenges

Power Trend

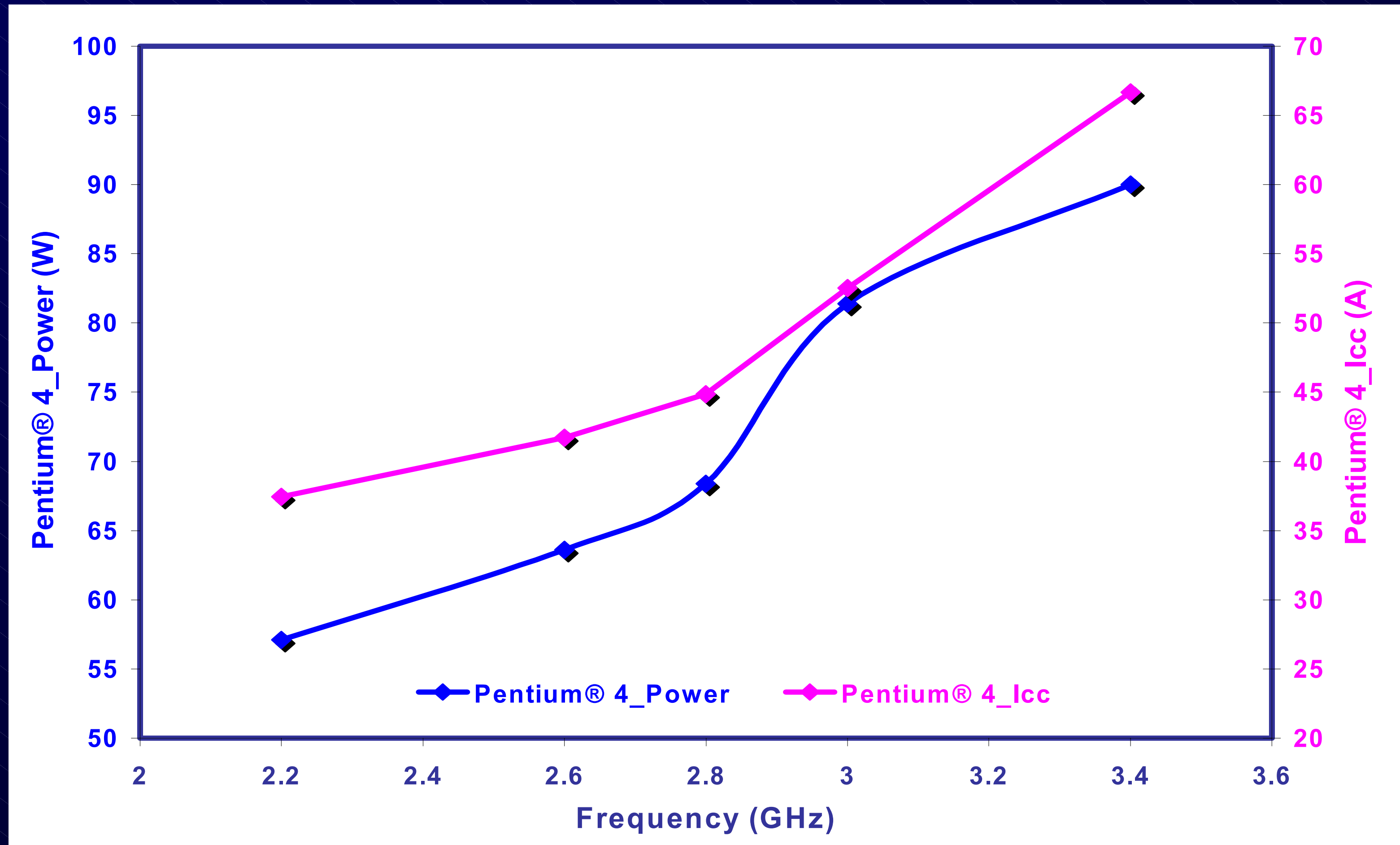
- Voltage is decreasing, Current & Power is increasing



Source: 2003 ITRS Roadmap

Intel® Pentium® 4 Microprocessor Power Trend

- Within Intel® Pentium® 4 generation power increases by 30 Watts and Current increases by 30 Amps



Source: www.tomshardware.com

Probe Card Power Path

ATE Power Supply

Top-side Stiffening Hardware

PCB

Space Transformer

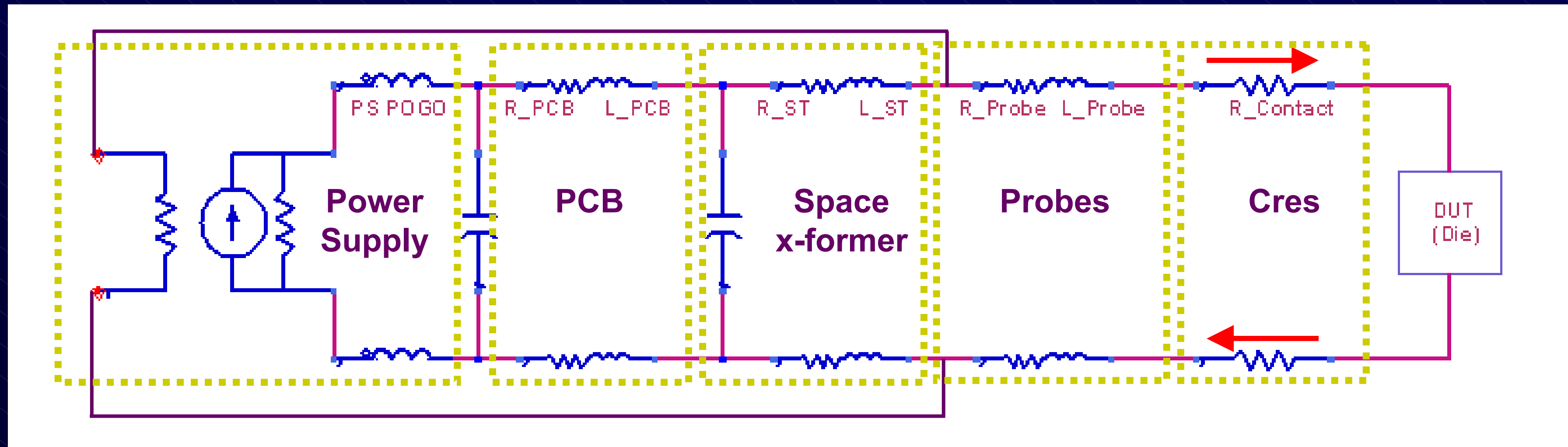
Contact Probes

DIE (DUT)

X

Y

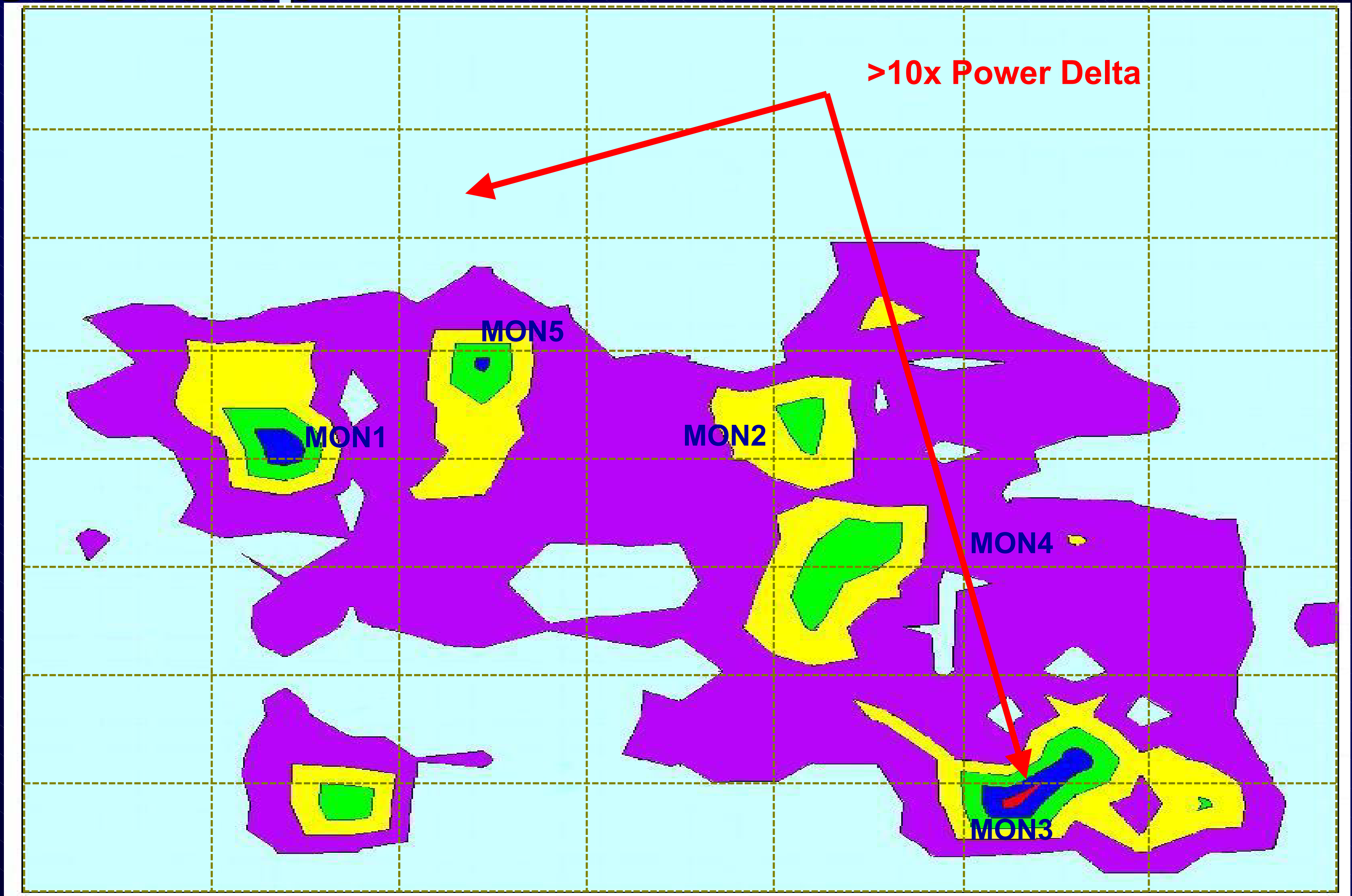
Z



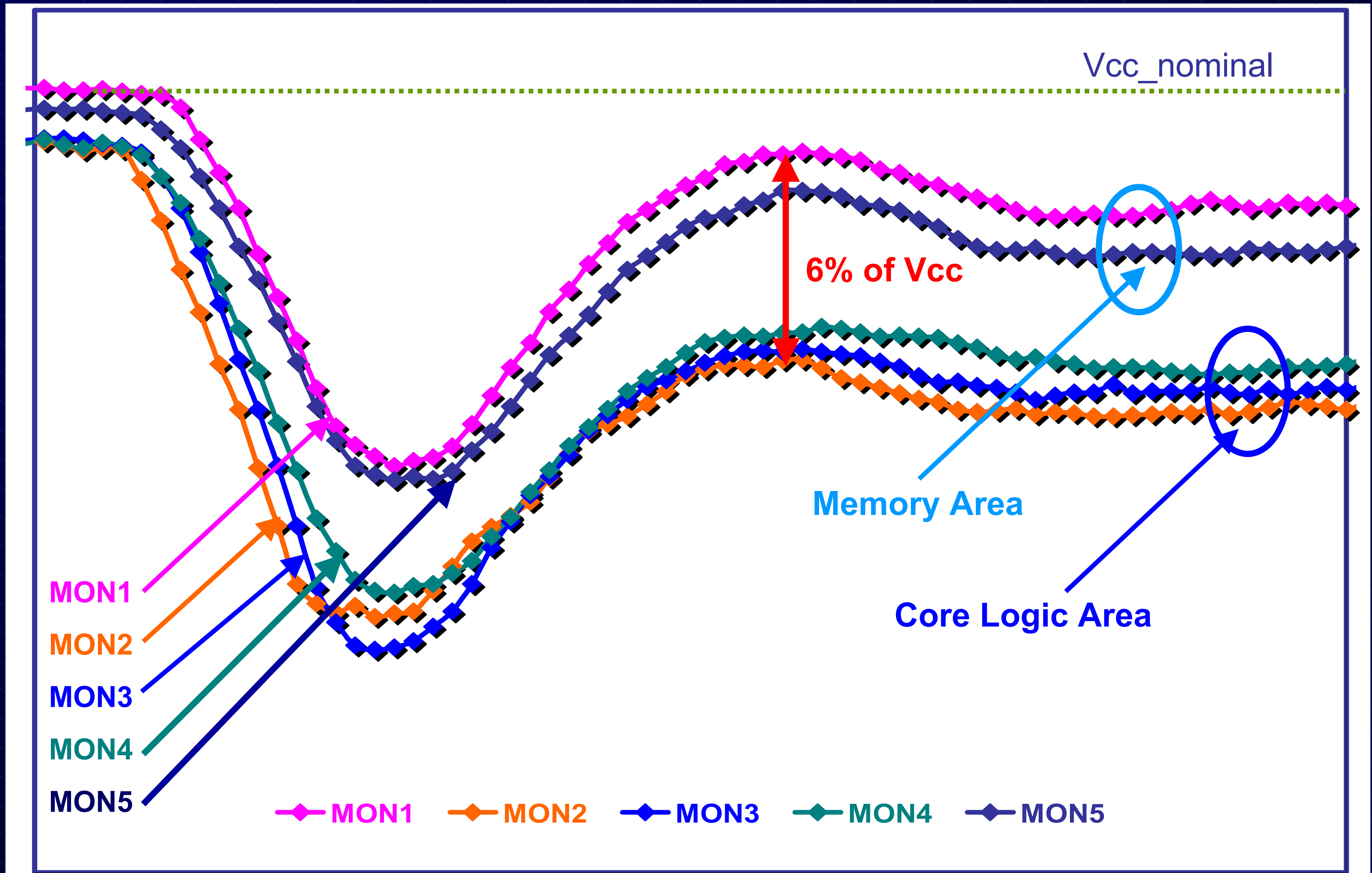
The problem

- Path inductance and resistance are the main contributors to power path voltage droop
  - L*di/dt
  - IR droop
- An Example (Impact of Contact Resistance)
  - Icc: 65 Amps
  - Cres: 0.5 Ohms per probe
  - Vcc probes: 400
  - Total Cres: 1.25 mOhm
  - IR droop=1.25x65=81.25 mV
  - Remaining Resistance will contribute to more IR voltage droop
- Failure to address power delivery challenge at sort is considered a serious risk as it could lead to undesirable or unpredictable sort results

Intel® Pentium® 4 Microprocessor Power Map

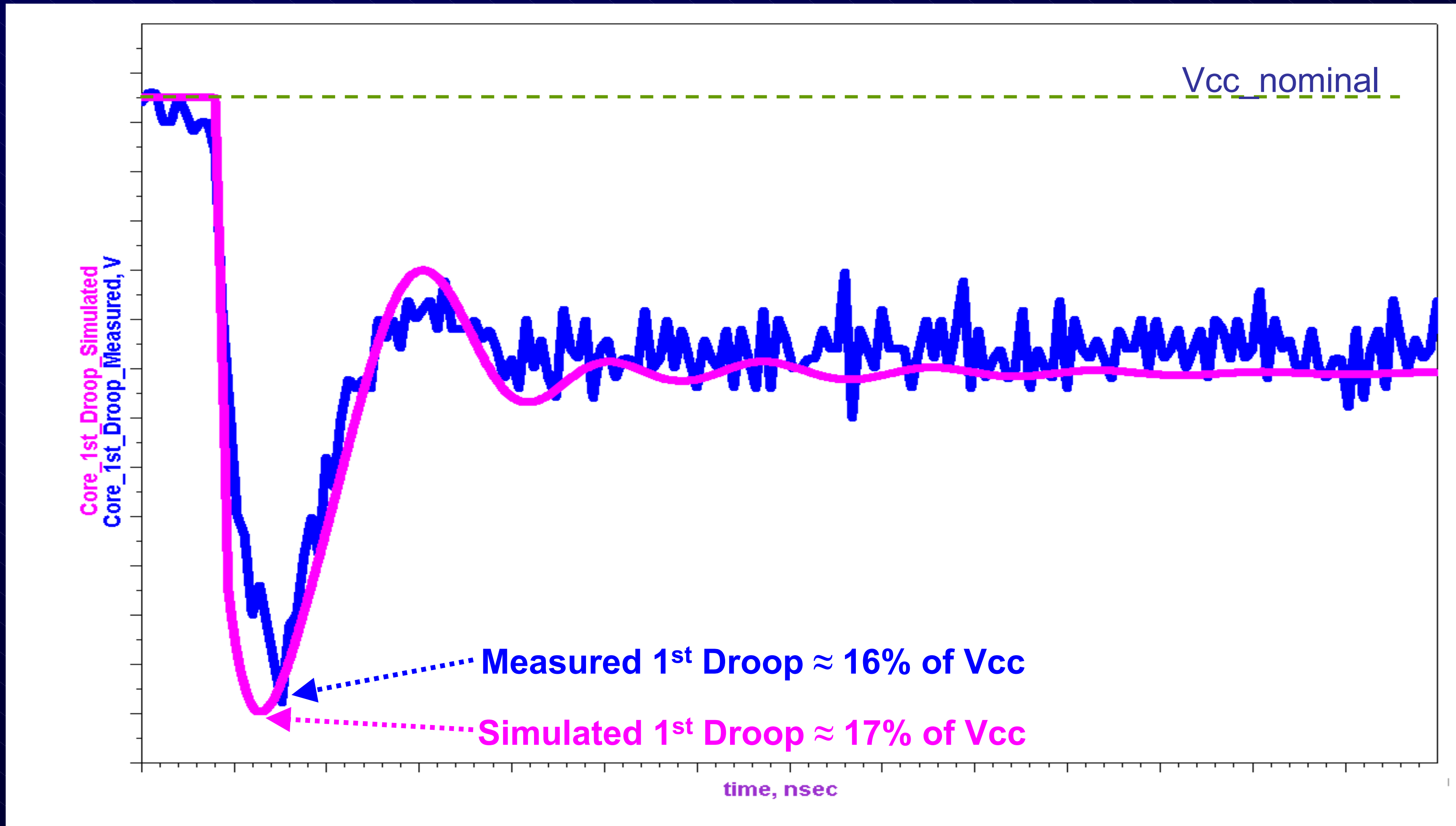


Non-Uniform Power Distribution



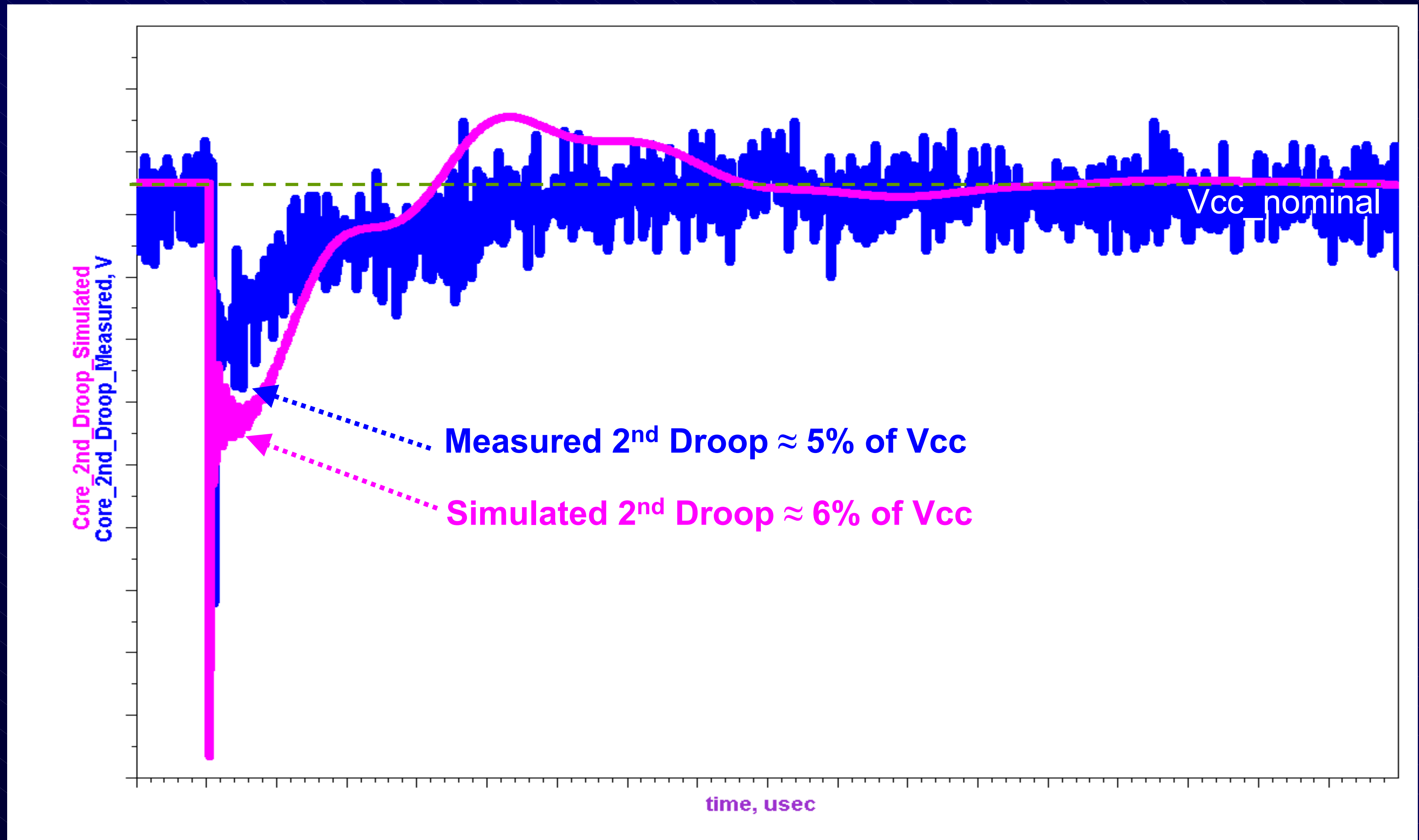
Intel® Pentium® 4 Microprocessor Voltage Droop

- 1st Voltage Droop



Intel® Pentium® 4 Microprocessor Voltage Droop

- 2nd Voltage Droop



Probe Card Power Delivery Improvements

Traditional Probe Card Power Path Design

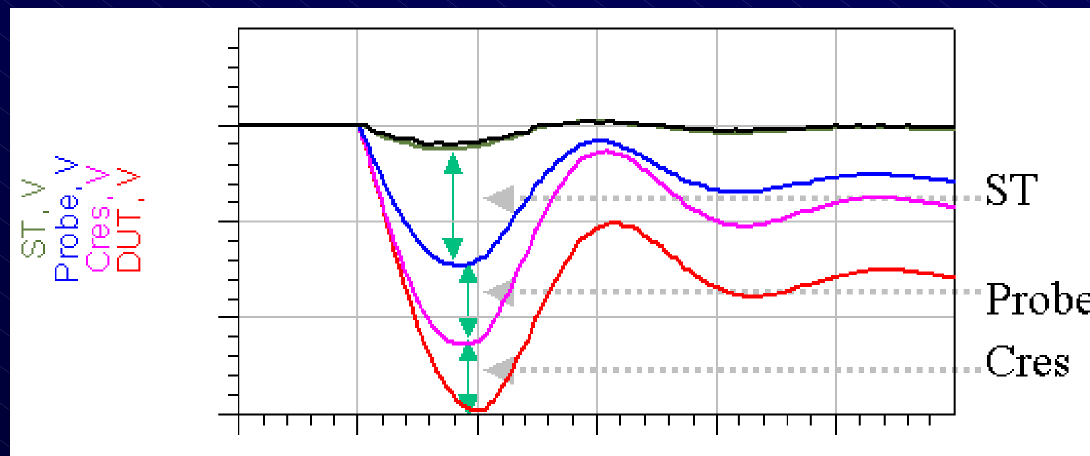
- Minimize power path inductance & resistance
  - Use power planes & Vias only for high current power path design to minimize power path L & R (no routing)
  - Reduce probe L & R
  - Reduce Space Transformer (ST) L & R
  - Reduce contact resistance between probe & wafer bump

- Power path decoupling design
  - For high power device, we usually have two groups of decoupling capacitors for power delivery
    - Local capacitors: on Space Transformer, closer to DUT, usually have relatively small capacitance due to space constraint
    - Bulk capacitors: on PCB with relatively large amount of capacitance
  - Adjusting decoupling capacitance to stable power supply is the traditional way of power delivery design
  - Applying low ESL & ESR capacitors

Probe Card Components Contribution to Power Delivery

- Power delivery quality is measured by "Vcc Droop" or "Load Line"
- Probe card components contribution to Vdroop

Probe Card Component	Contribution % to 1st Vdroop
Contact Resistance	23%
Probes	28%
Space Transformer (ST)	41%
Others	8%
Total	100%



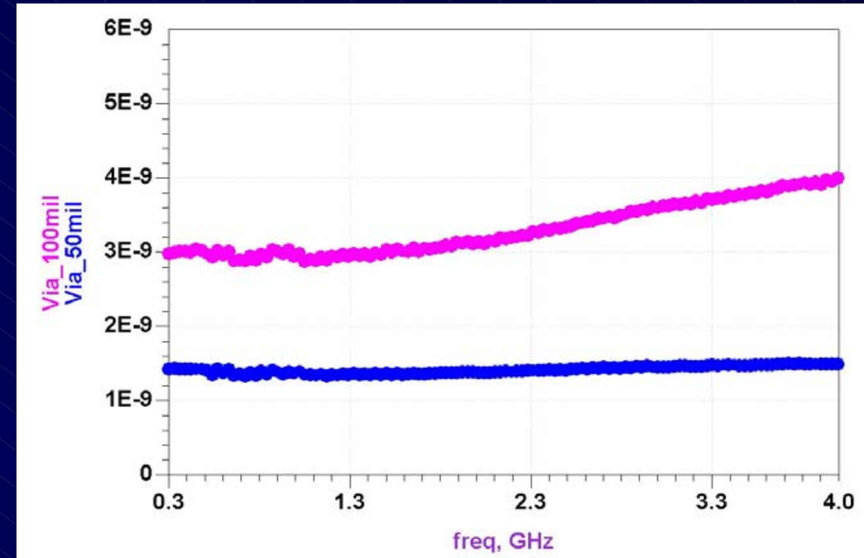
Probe Card Power Delivery Improvements - Probes

- Low inductance & resistance probes
  - In recent years, some new technologies have been introduced to probing industry for making new probes for high power probe card manufacturing
  - Most of these new probe types have smaller size, lower inductance and resistance than conventional probes
  - Current carrying capability per probe is a concern due to smaller size

- Fully populated probe array
  - May not be achievable or affordable with conventional type of probes due to smaller pitch, larger probe count & cost model
    - Intel is doing probe depop at Sort for logic device
  - However with innovative smaller probes, fully populated probe array will be more practical & achievable

Probe Card Power Delivery Improvements – Space Transformer (ST)

- Improvements on ST
  - Increase ST power Via count
    - Checker board Via pattern
  - Reduce ST thickness to reduce power path impedance (L & R)
    - ST thickness reduction: 150mil => 100mil => 50mil
      - ST Via inductance reduction
      - ST Via resistance reduction: proportional to Via length reduction



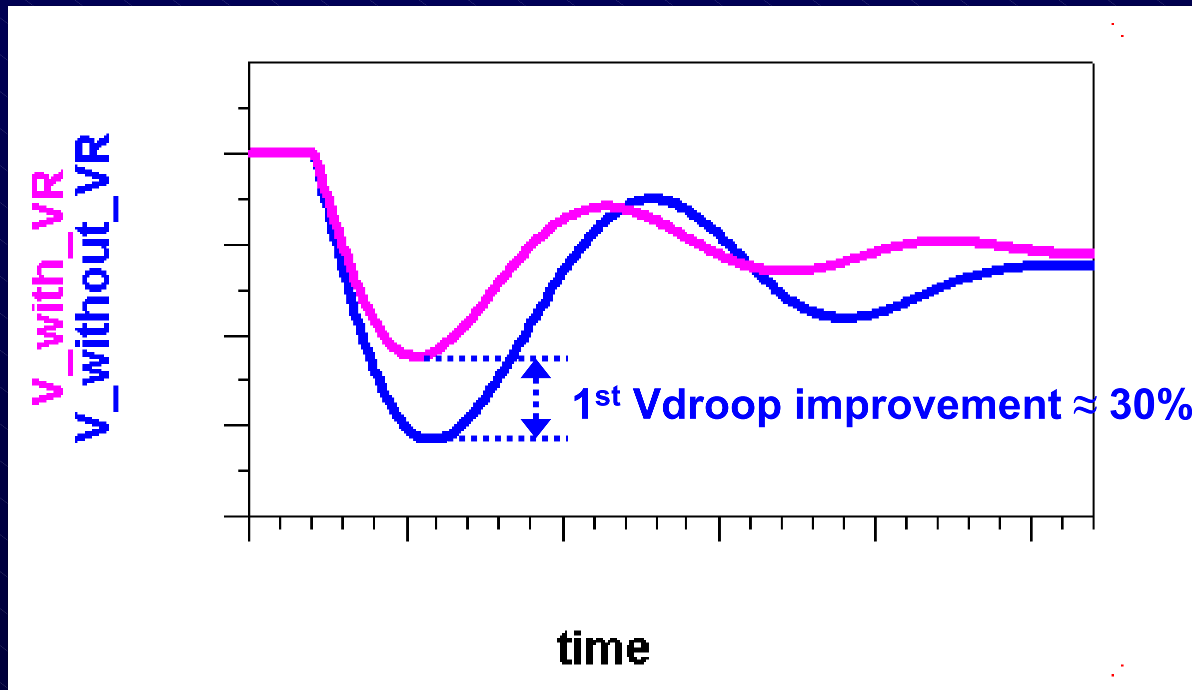
Via Length (50mil pitch)	200mil	150mil	100mil	50mil	25mil
Via Inductance (effective)	3.3nH	2.4nH	1.5nH	0.7nH	0.3nH

Probe Card Power Delivery Improvements - Capacitors & Others

- Use very low ESL & ESR capacitors
  - IDC Capacitors
  - Array Capacitor
- Reduce contact resistance
  - Probe to wafer bump contact resistance is important to probe card power delivery quality, higher contact resistance will result in a bigger Vdroop
- Improve tester power supply
  - Reduce tester power supply response time
  - Reduce power cable impedance

Probe Card Power Delivery Improvements - Innovative Improvement Techniques

- Active power regulation on probe card
  - GHz Voltage Regulation Device on ST
  - VRM Card on PCB
  - Voltage Regulation Circuit on PCB



Simulation of Vdroop improvement with & without Voltage Regulator

Conclusion & Acknowledgement

Conclusion

- In general, Microprocessor power consumption is going up and Voltage is going down, which creates a bigger challenge for power delivery
- Traditional power path design and improvements will be limited by physical & electrical constraints
- Innovative power delivery techniques are in need for future probe card power delivery design
  - Probe card suppliers should work on innovative solutions for next generation high power devices

Acknowledgements

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