Power Delivery Challenges of High Power Logic Device at Sort

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Agenda

- **Power Delivery Challenge**
  - 2003 ITRS Power Trend
  - Power Trend of Intel® Pentium® 4 Microprocessor
  - Probe Card Power Path
  - Microprocessor Power Distribution
  - Intel® Pentium® 4 Microprocessor Voltage Droop

- **Probe Card Power Delivery Improvements**
  - Probe Card Power Delivery Design
  - Power Delivery Improvements on Probe Card Components
  - Innovative Improvement Techniques

- **Conclusion & Acknowledgement**
Probe Card Power Delivery Challenges
Power Trend

- Voltage is decreasing, Current & Power is increasing

![Graph showing decreasing voltage and increasing current and power over time, with max currents at different years. The graph is labeled with 'I_max: 124 A' and 'I_max: 430 A', and includes a source: 2003 ITRS Roadmap.]
Intel® Pentium® 4 Microprocessor Power Trend

- Within Intel® Pentium® 4 generation power increases by 30 Watts and Current increases by 30 Amps

Source: www.tomshardware.com
Probe Card Power Path

The diagram illustrates the power path for a probe card. The ATE Power Supply is connected to the PCB, which then transfers power through the Top-side Stiffening Hardware. Contact Probes are used to connect to the DIE (DUT). The power supply is shown as a circuit diagram with components such as power supply, PCB, space x-former, probes, and Cres. The diagram also includes reference axes X, Y, and Z.
The problem

- Path inductance and resistance are the main contributors to power path voltage droop
  - L*di/dt
  - IR droop

- An Example (Impact of Contact Resistance)
  - Icc: 65 Amps
  - Cres: 0.5 Ohms per probe
  - Vcc probes: 400
  - Total Cres: 1.25 mOhm
  - IR droop=1.25x65=81.25 mV
  - Remaining Resistance will contribute to more IR voltage droop

- Failure to address power delivery challenge at sort is considered a serious risk as it could lead to undesirable or unpredictable sort results
Intel® Pentium® 4 Microprocessor
Power Map

>10x Power Delta
Non-Uniform Power Distribution

- Vcc_nominal
- Memory Area
- Core Logic Area
- 6% of Vcc

Monitor Points:
- MON1
- MON2
- MON3
- MON4
- MON5
Intel® Pentium® 4 Microprocessor Voltage Droop

1st Voltage Droop

Measured 1st Droop ≈ 16% of Vcc

Simulated 1st Droop ≈ 17% of Vcc
Intel® Pentium® 4 Microprocessor Voltage Droop

2nd Voltage Droop

Measured 2nd Droop ≈ 5% of Vcc

Simulated 2nd Droop ≈ 6% of Vcc
Probe Card Power Delivery Improvements
Traditional Probe Card Power Path Design

- **Minimize power path inductance & resistance**
  - Use power planes & Vias only for high current power path design to minimize power path L & R (no routing)
  - Reduce probe L & R
  - Reduce Space Transformer (ST) L & R
  - Reduce contact resistance between probe & wafer bump

- **Power path decoupling design**
  - For high power device, we usually have two groups of decoupling capacitors for power delivery
    - Local capacitors: on Space Transformer, closer to DUT, usually have relatively small capacitance due to space constraint
    - Bulk capacitors: on PCB with relatively large amount of capacitance
  - Adjusting decoupling capacitance to stable power supply is the traditional way of power delivery design
  - Applying low ESL & ESR capacitors
Probe Card Components Contribution to Power Delivery

Power delivery quality is measured by “Vcc Droop” or “Load Line”

Probe card components contribution to Vdroop

<table>
<thead>
<tr>
<th>Probe Card Component</th>
<th>Contribution % to 1st Vdroop</th>
</tr>
</thead>
<tbody>
<tr>
<td>Contact Resistance</td>
<td>23%</td>
</tr>
<tr>
<td>Probes</td>
<td>28%</td>
</tr>
<tr>
<td>Space Transformer (ST)</td>
<td>41%</td>
</tr>
<tr>
<td>Others</td>
<td>8%</td>
</tr>
<tr>
<td>Total</td>
<td>100%</td>
</tr>
</tbody>
</table>
Probe Card Power Delivery Improvements - Probes

- **Low inductance & resistance probes**
  - In recent years, some new technologies have been introduced to probing industry for making new probes for high power probe card manufacturing.
  - Most of these new probe types have smaller size, lower inductance and resistance than conventional probes.
  - Current carrying capability per probe is a concern due to smaller size.

- **Fully populated probe array**
  - May not be achievable or affordable with conventional type of probes due to smaller pitch, larger probe count & cost model.
    - Intel is doing probe depop at Sort for logic device.
  - However with innovative smaller probes, fully populated probe array will be more practical & achievable.
Probe Card Power Delivery
Improvements – Space Transformer (ST)

- **Improvements on ST**
  - Increase ST power Via count
    - Checker board Via pattern
  - Reduce ST thickness to reduce power path impedance (L & R)
    - ST thickness reduction: 150mil => 100mil => 50mil
      - ST Via inductance reduction
      - ST Via resistance reduction: proportional to Via length reduction

<table>
<thead>
<tr>
<th>Via Length (50mil pitch)</th>
<th>200mil</th>
<th>150mil</th>
<th>100mil</th>
<th>50mil</th>
<th>25mil</th>
</tr>
</thead>
<tbody>
<tr>
<td>Via Inductance (effective)</td>
<td>3.3nH</td>
<td>2.4nH</td>
<td>1.5nH</td>
<td>0.7nH</td>
<td>0.3nH</td>
</tr>
</tbody>
</table>
Probe Card Power Delivery

Improvements - Capacitors & Others

- Use very low ESL & ESR capacitors
  - IDC Capacitors
  - Array Capacitor

- Reduce contact resistance
  - Probe to wafer bump contact resistance is important to probe card power delivery quality, higher contact resistance will result in a bigger Vdroop

- Improve tester power supply
  - Reduce tester power supply response time
  - Reduce power cable impedance
Probe Card Power Delivery Improvements - Innovative Improvement Techniques

- Active power regulation on probe card
  - GHz Voltage Regulation Device on ST
  - VRM Card on PCB
  - Voltage Regulation Circuit on PCB

Simulation of Vdroop improvement with & without Voltage Regulator

1st Vdroop improvement ≈ 30%
Conclusion & Acknowledgement
Conclusion

- In general, Microprocessor power consumption is going up and Voltage is going down, which creates a bigger challenge for power delivery.

- Traditional power path design and improvements will be limited by physical & electrical constraints.

- Innovative power delivery techniques are in need for future probe card power delivery design.
  - Probe card suppliers should work on innovative solutions for next generation high power devices.
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