

Application of Larger Probing Area by Cantilevered Probes

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Technology and Science Enabler

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Dave Oh / Chu @ 2005 SWTW

About TSE

As a Technology and Science Enabler in the field of Semiconductor test, TSE has developed the innovative technologies needed by its customer and has engage in continuous research and productivity improvement activities.

Mission:

- **To become a global standard company with leading technology in semiconductor test interface field.**

Technology:

- **To provides the technology getting along customers and the service creating customer's values**

Products:

- **Probe card, Test socket, Handler change kit
High parallel interface board, Logic Load board**

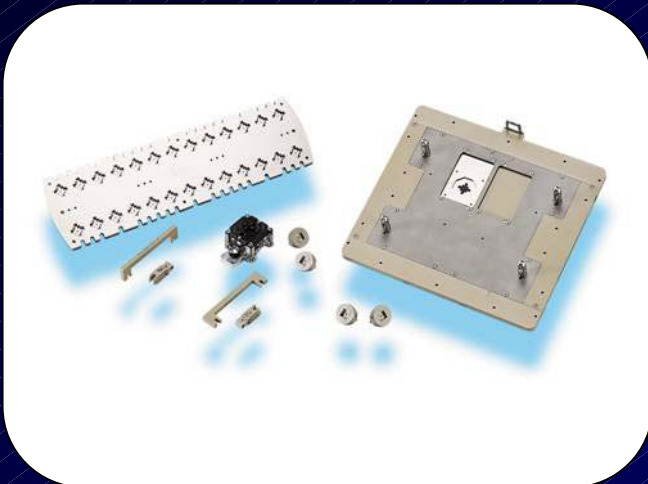
Products



Test interface board



Probe card



Change kit



Test socket

Outline

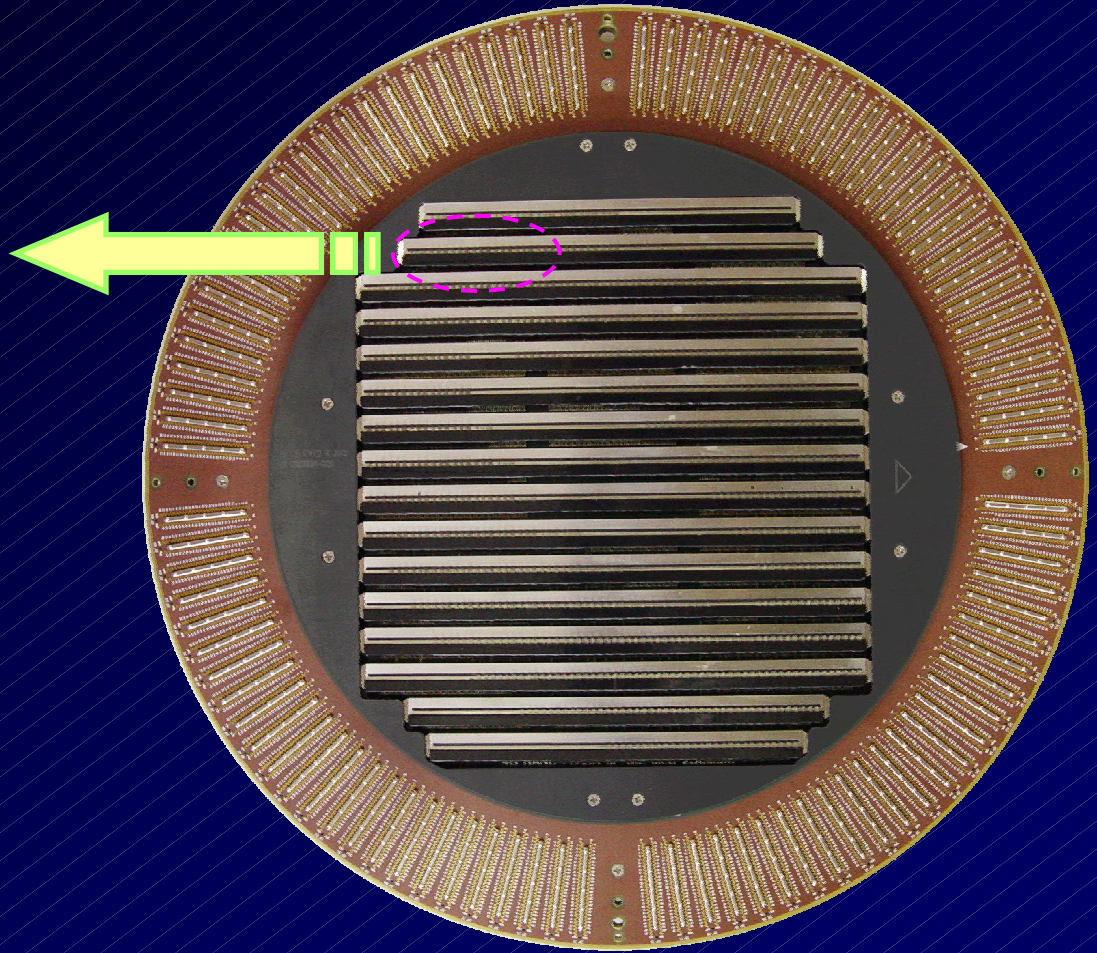
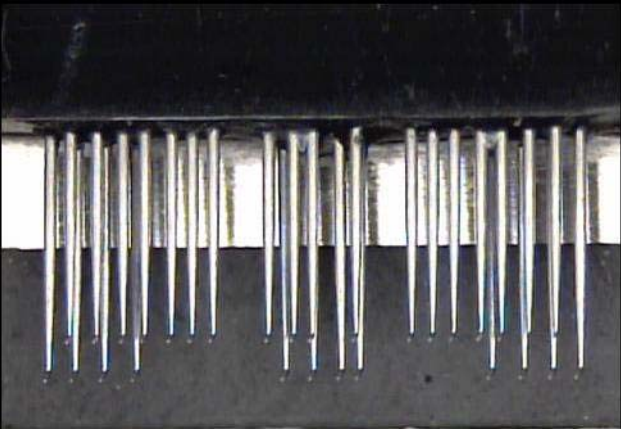
- **CPC-Wafer™ Concept**
- **Roadmap**
- **Advantage**
- **Mechanical Data**
- **Specifications**
- **Summary**

Background

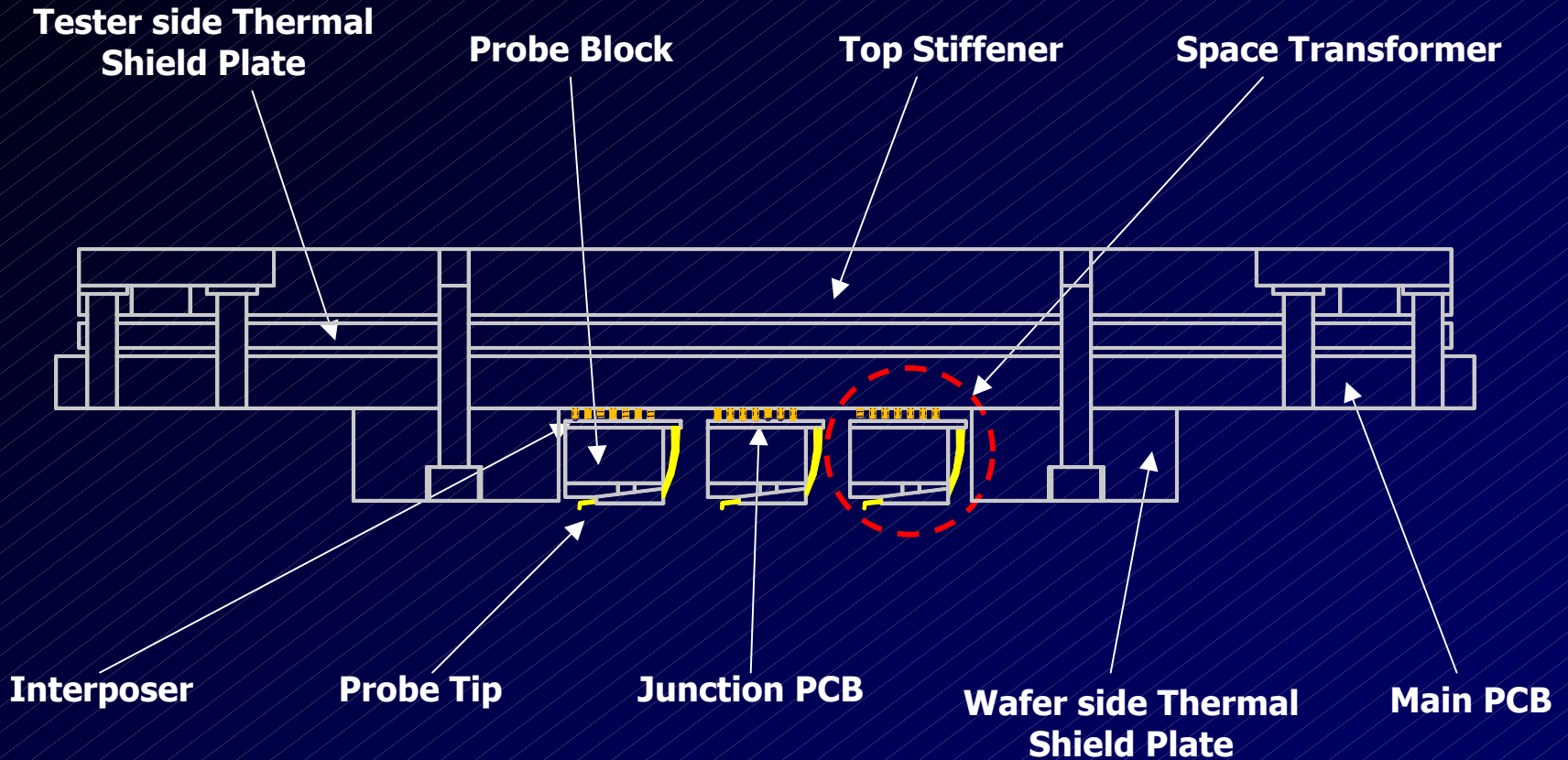
Large Probing Area Probe cards

- **chip size increasing— especially NAND flash**
- **Higher parallel probe card requirement**
- **Drastically test time increasing**
- **DDT Technology available**

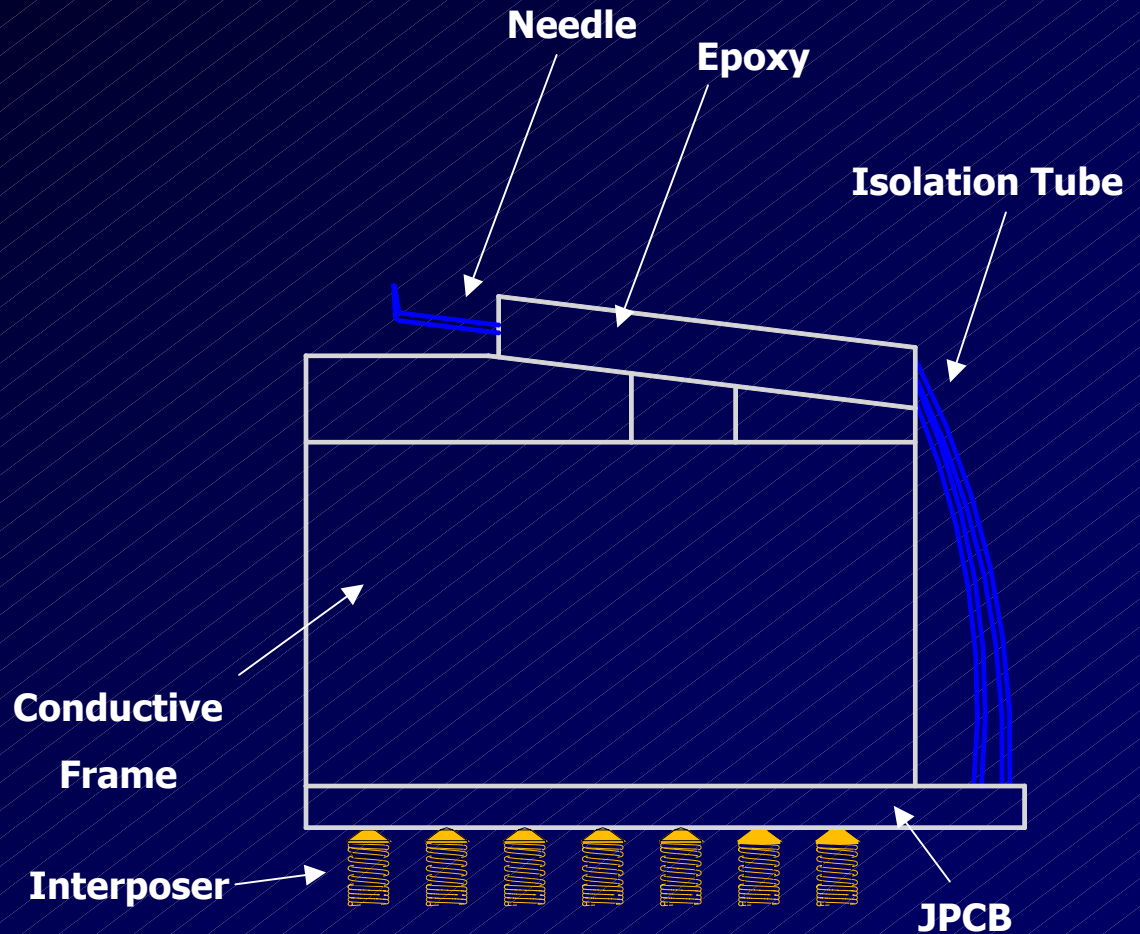
C P C-Wafer™ (Compact Probe Card)



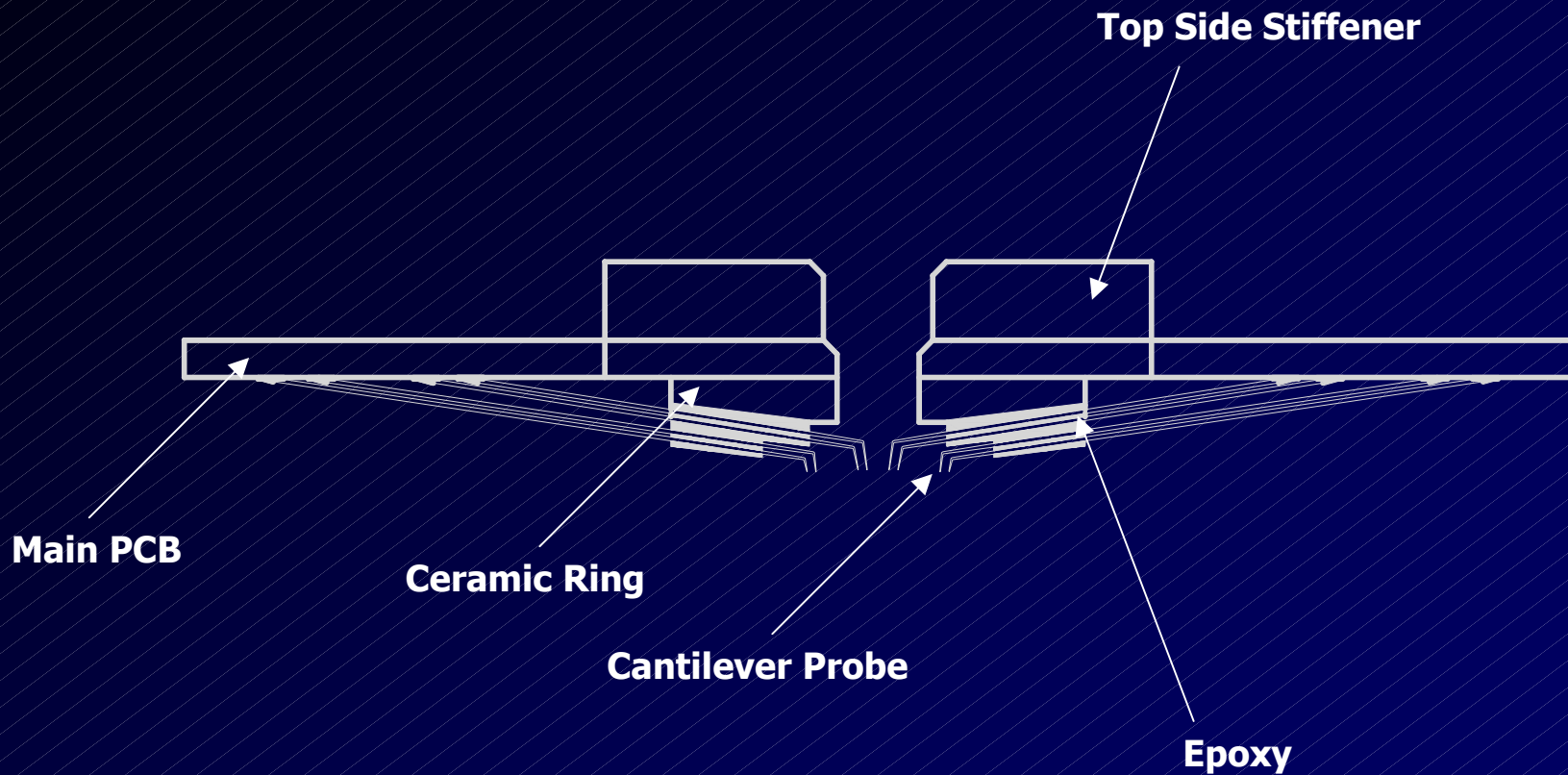
CPC-Wafer™ Structure



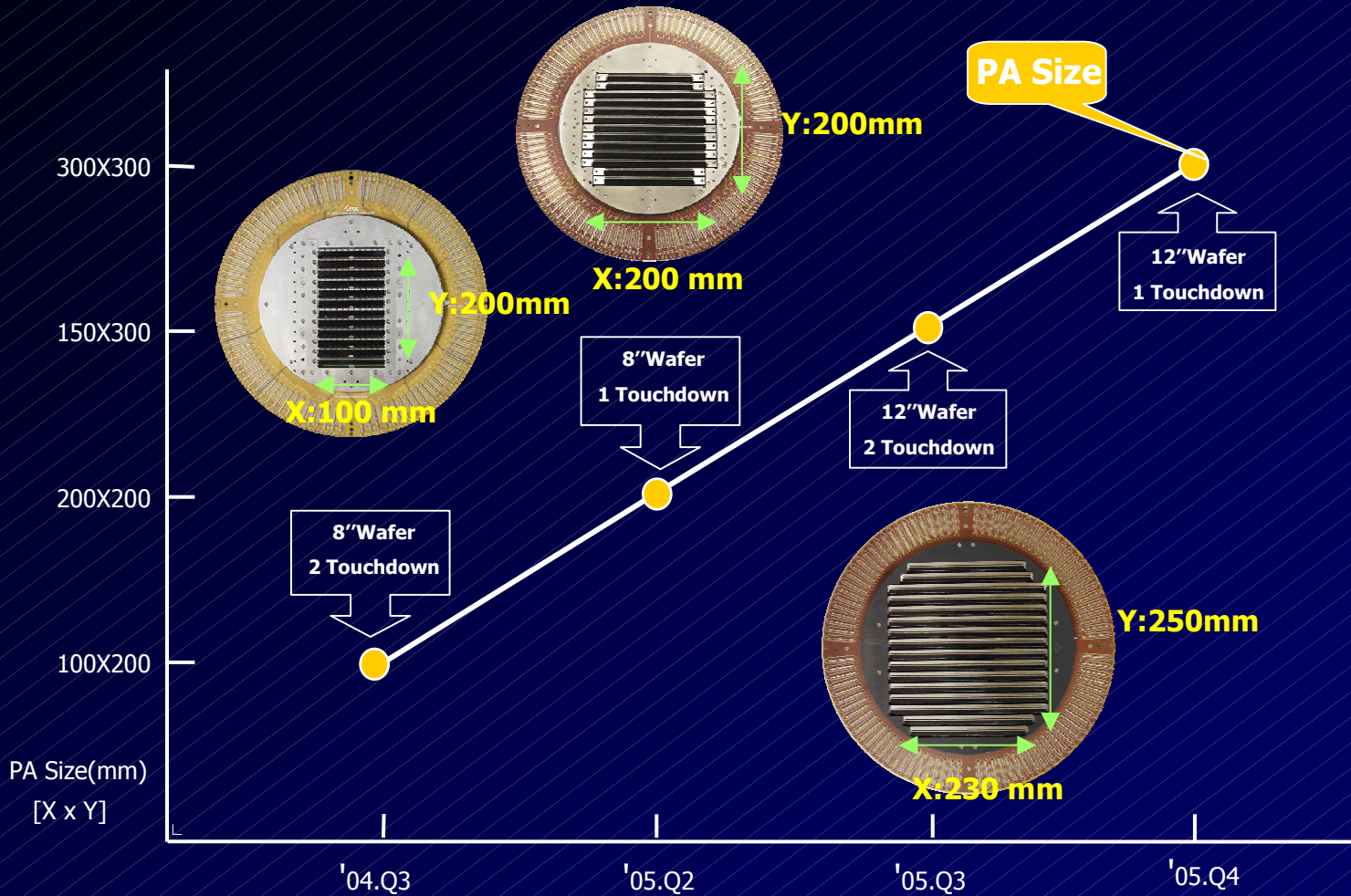
CPC-Space Transformer Structure



Conventional P/C Structure



ROAD MAP (PA SIZE)



Roadmap Overview

No.	Item	Year 2005	Year 2006	Remark
1	PA Size	100mmx200mm	300mmx300mm	Planarity<27um
2	Pin Density	100%	211%	DRAM Application
3	Pad Pitch	90um	70um	
4	Operation Speed	>100MHz	>200MHz	Target is @Speed
5	Delivery	3~4weeks	2~3weeks	Repeat Order Case
6	Min.Chip Y Size	7.9mm	5.9mm	Application Limit Overcome
7	Pad Array	△	○	Rectangle,'H'Array

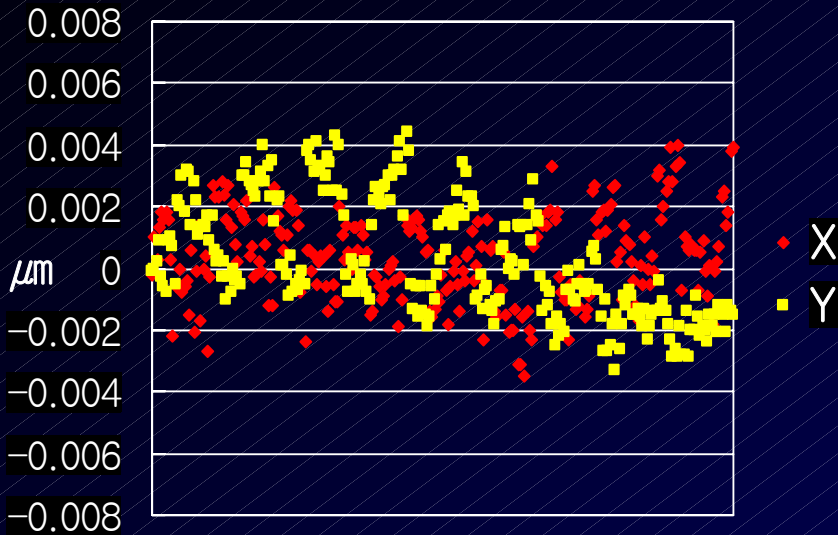
Why CPC-Wafer™ ?

- **Large PA(Probing Area) size**
- **Parallel manufacturing process**
- **All probe have same scrubbing direction**
- **Improved contact force uniformity**
- **Improved electrical signal performance**

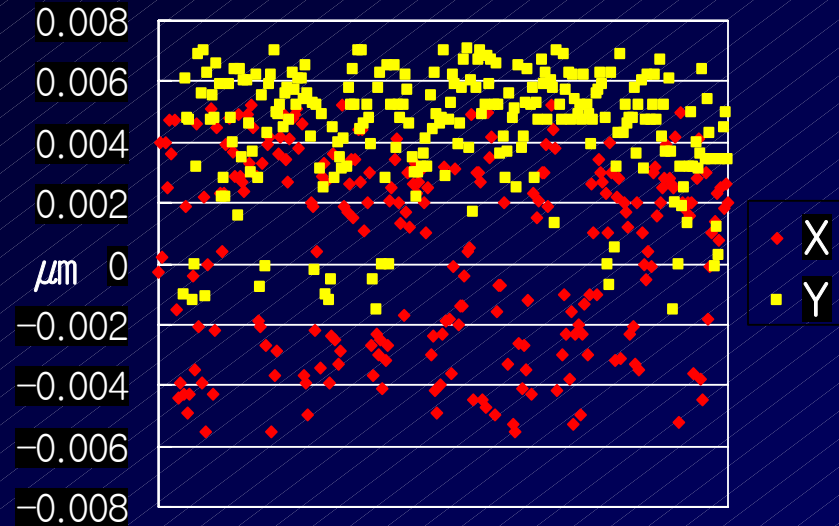
Why CPC-Wafer™ ?(continue)

- **Cantilever probe**
- **Individual/module base replaceable probe**
- **Improved probe planarity**
- **Flexible PH(Probing Head) outline**

X, Y Alignment



BEFORE



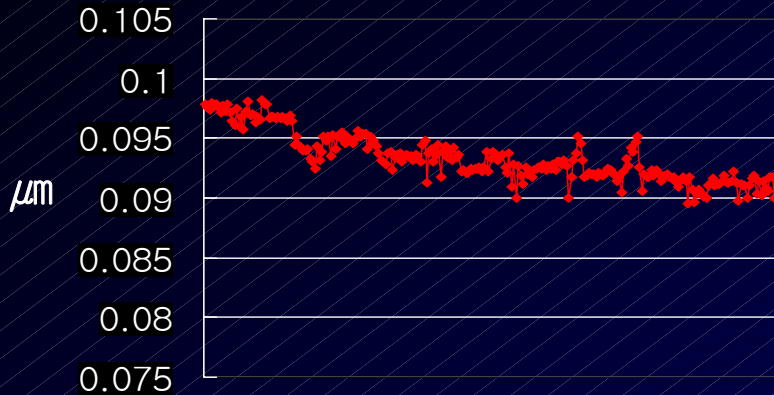
AFTER (10K TD)

RESULT		
	Before	After
X	$\pm 4 \mu\text{m}$	$\pm 5.5 \mu\text{m}$
Y	$+4.4 \mu\text{m}, -3.0 \mu\text{m}$	$+7.0 \mu\text{m}, -1.5 \mu\text{m}$

TEST CONDITION

- **TEMP : 85°C**
- **Pin : 5,448Pins**
- **OD : 85μm**
- **PA SIZE : 200mmx200mm**

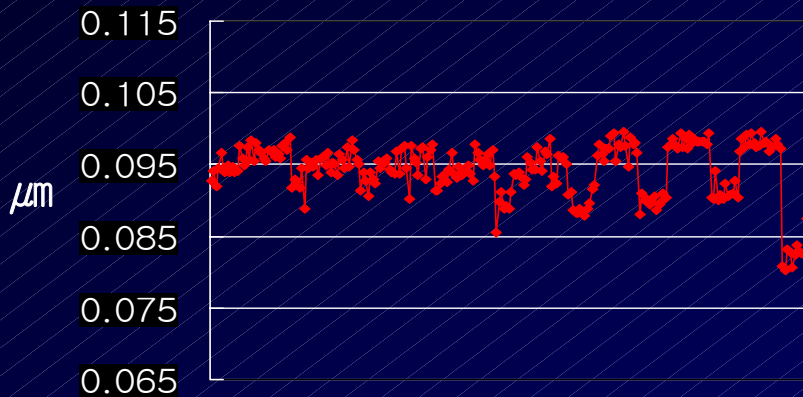
Z - Planarity



BEFORE

TEST CONDITION

- **TEMP : 85°C**
- **Pin : 3636Pins**
- **OD : 85 μm**
- **PA SIZE : 100mmx200mm**

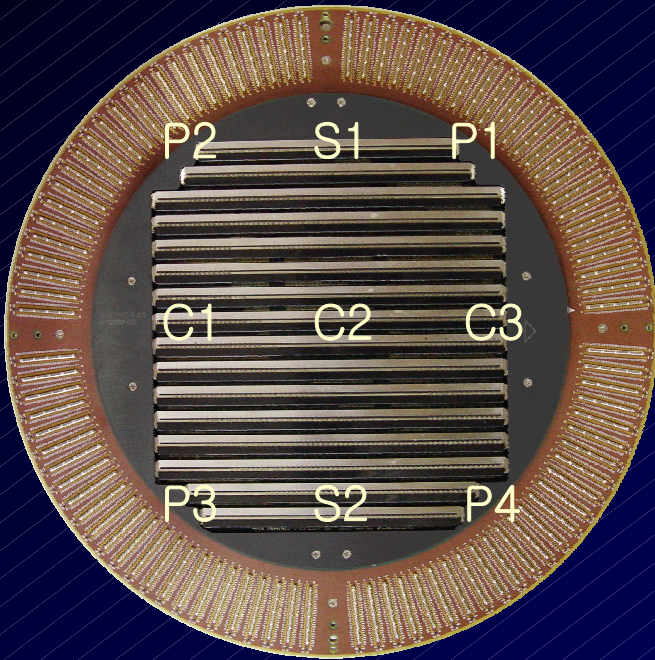


**AFTER
10K TD**

RESULT		
	Before	After
Z	8.2 μm	19.3 μm

Thermal Test Procedure

Measuring Position

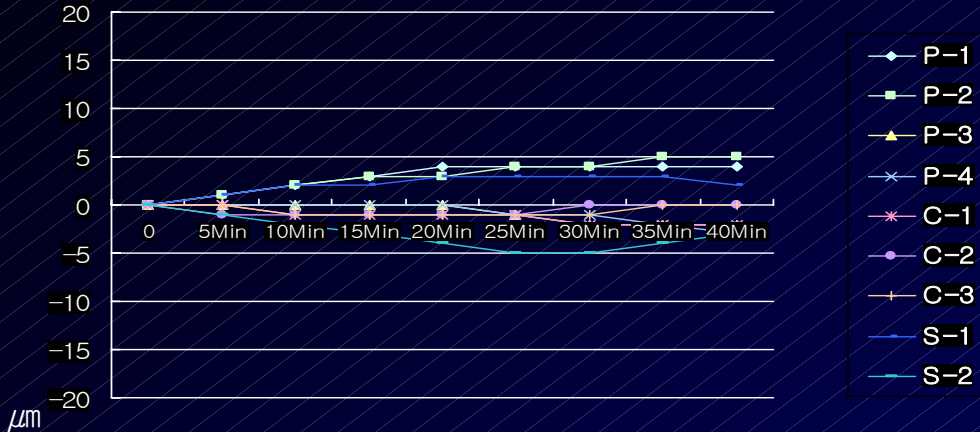


TEST STEP

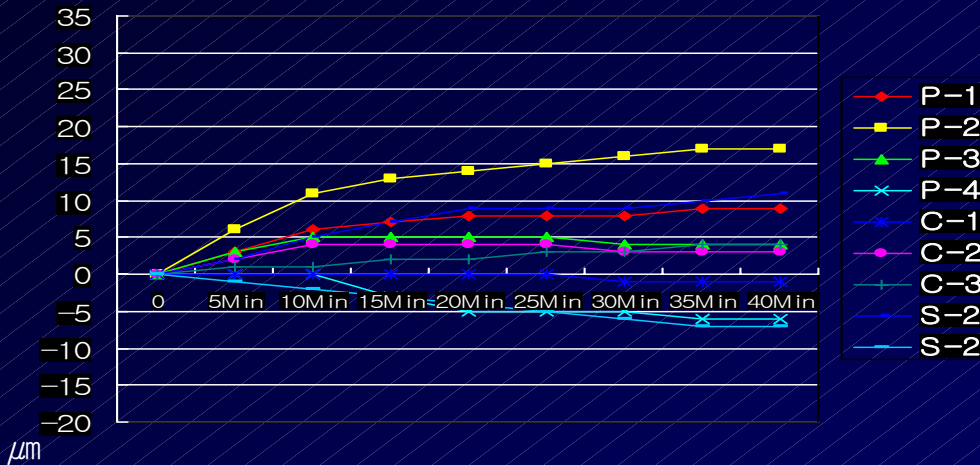
- 1. Measure the each position Before Contact to Wafer**
- 2. Contact for 10min.**
- 3. Recheck each position**
- 4. Repeat above #1. to #4. 4 or 5 times**

Thermal Expansion Test

(X & Y - Axis)



"X" AXIS



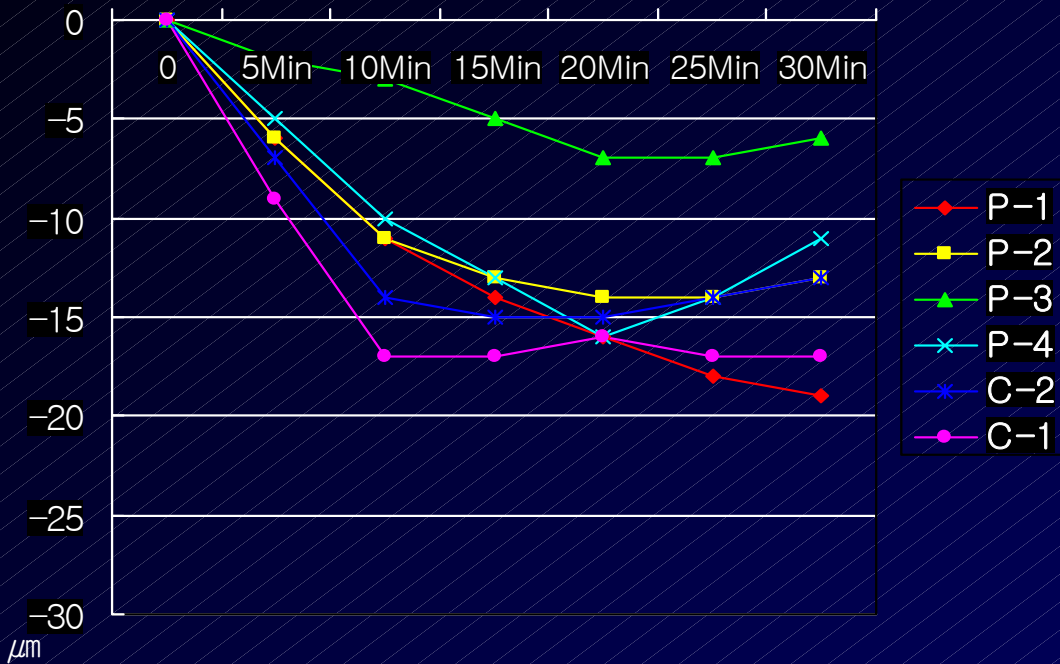
"Y" AXIS

RESULT			
	40min. Later		
		Pos. Movement	Expansion Gap
X	P1	4 μm	1 μm
	P2	5 μm	
	P3	-2 μm	1 μm
	P4	-3 μm	
Y	P1	9 μm	5 μm
	P3	4 μm	
	P2	17 μm	23 μm
	P4	-6 μm	

TEST CONDITION

- TEMP : 85 °C
- Pin : 6120Pins
- OD : 85 μm
- PA SIZE : 230mmx250mm

Thermal Test (Z - Axis)

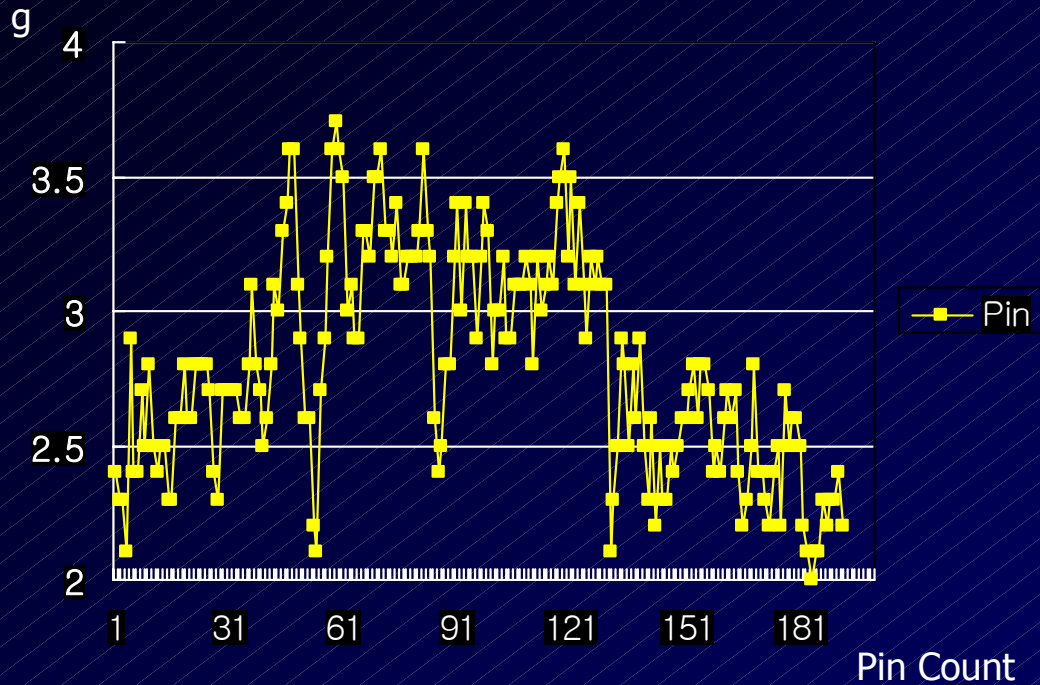


RESULT	
	40min. Later
GAP	13 μm
Z-Down	Min : -6 μm Max : -19 μm

TEST CONDITION

- **TEMP : 85 °C**
- **Pin : 6120Pins**
- **OD : 85 μm**
- **PA SIZE : 230mmx250mm**

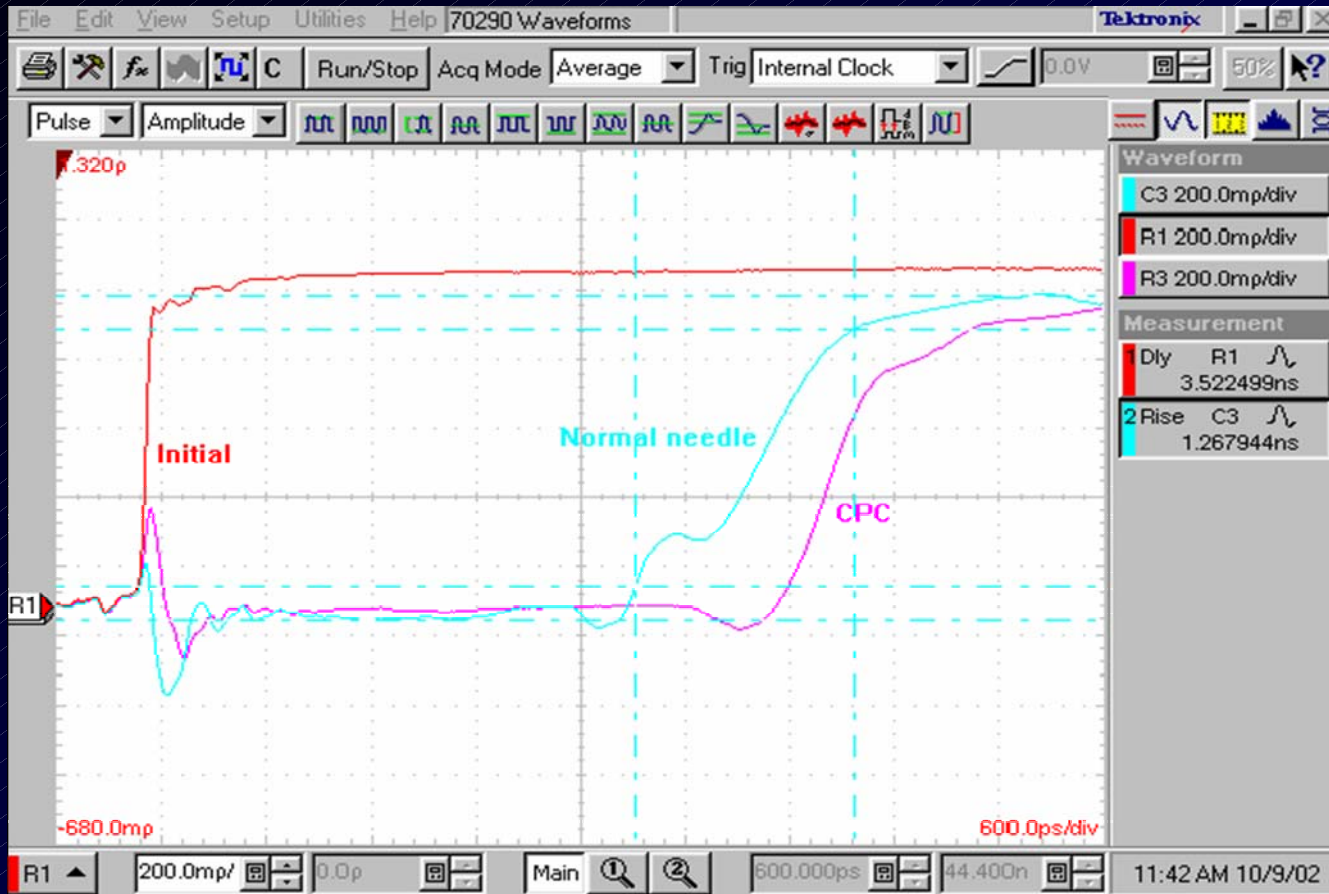
TIP FORCE



TEST CONDITION

- **TEMP : Room**
- **Pin : 340Pins**
- **OD : 50 μ m**

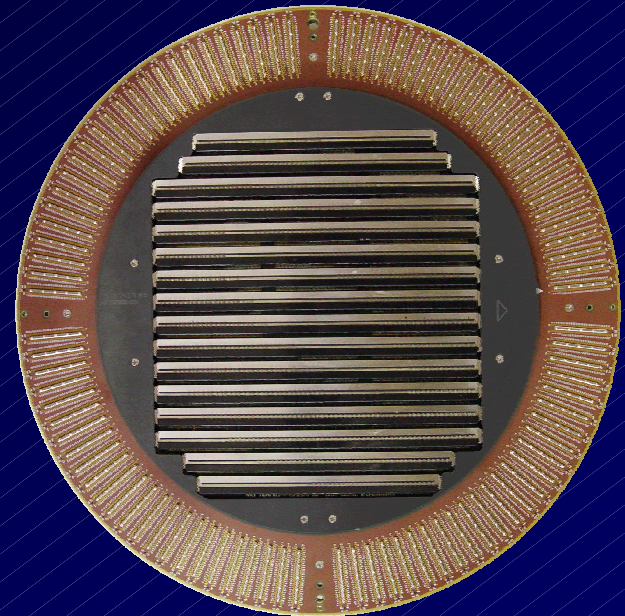
Signal performance



Item	Product	CPC-wafer™	Cantilever
Tr/Tf		839.5 ps	1267.9 ps
PA Size		200mm X 100mm	120mm X 60mm
Needle length		18mm	68mm

CPC – Wafer™ Specifications

- Tester : AL6050/T5375
- PCB Diameter : Ø440mm X 6.2 Thickness
- Device : NAND Flash
- PA Size : 240mm x 250mm
(12" wafer 2 touchdown)
- Probe Depth : 12mm ± 0.2mm
- Minimum Pitch : 90um
- Probe Force : 2.5g/mil
- Max. Scrub Mark : 25um
- Alignment : ±12um
- Planarity : 22um(max-min)
- Tip Shape : Semi-Round
- Tip Size : 23±2um
- Max. Current : 500mA(continuous)



< 2TD/12" NAND Flash >

SUMMARY

- **New solution for full wafer touchdown**
- **Shorter delivery**
- **Short and easy Repair**
- **Application to Any Device**
- **Free Expanded Area (Multiple Probe Block)**

What are next step?

- **Minimize contact force difference**
- **Overcome pad array type**
- **Improve tip position reliability after >100k TD**
- **Round tip shape**
- **Study more stable cleaning period and method**

Thank you very much for your attention!

Question ?