Dynamic Switching Test Technology for IGBT Chip Under High Power Operating Condition

Y. Masuma

A.Yoshida, K.Yamada, S. Sumi

E-mail: masuma-yoshitaka@fujielectric.co.jp

Fuji Electric Device Technology Co., Ltd.

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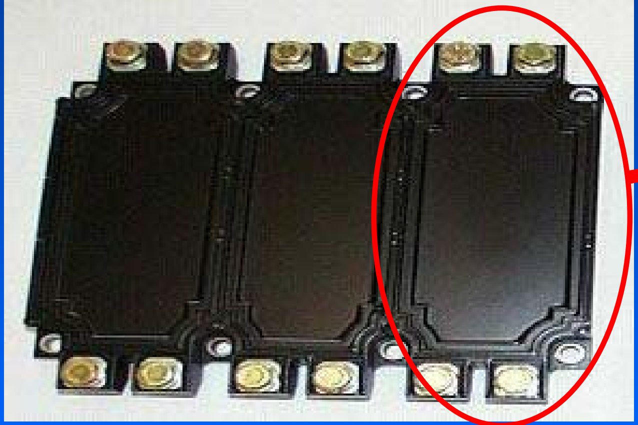
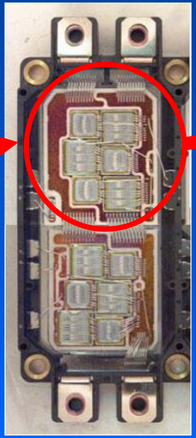
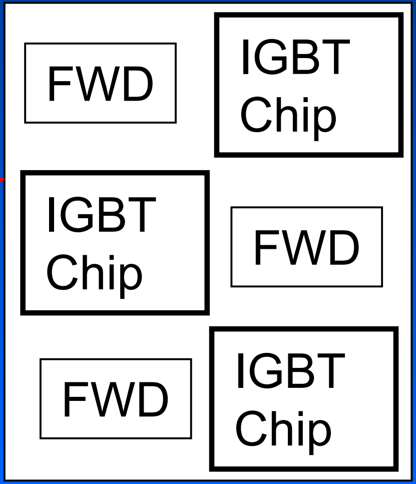
IGBT Module







FWD

IGBT Chip

IGBT Chip

FWD

FWD

IGBT Chip

6 in 1 Package Module

450A
1.7kV

Applications:

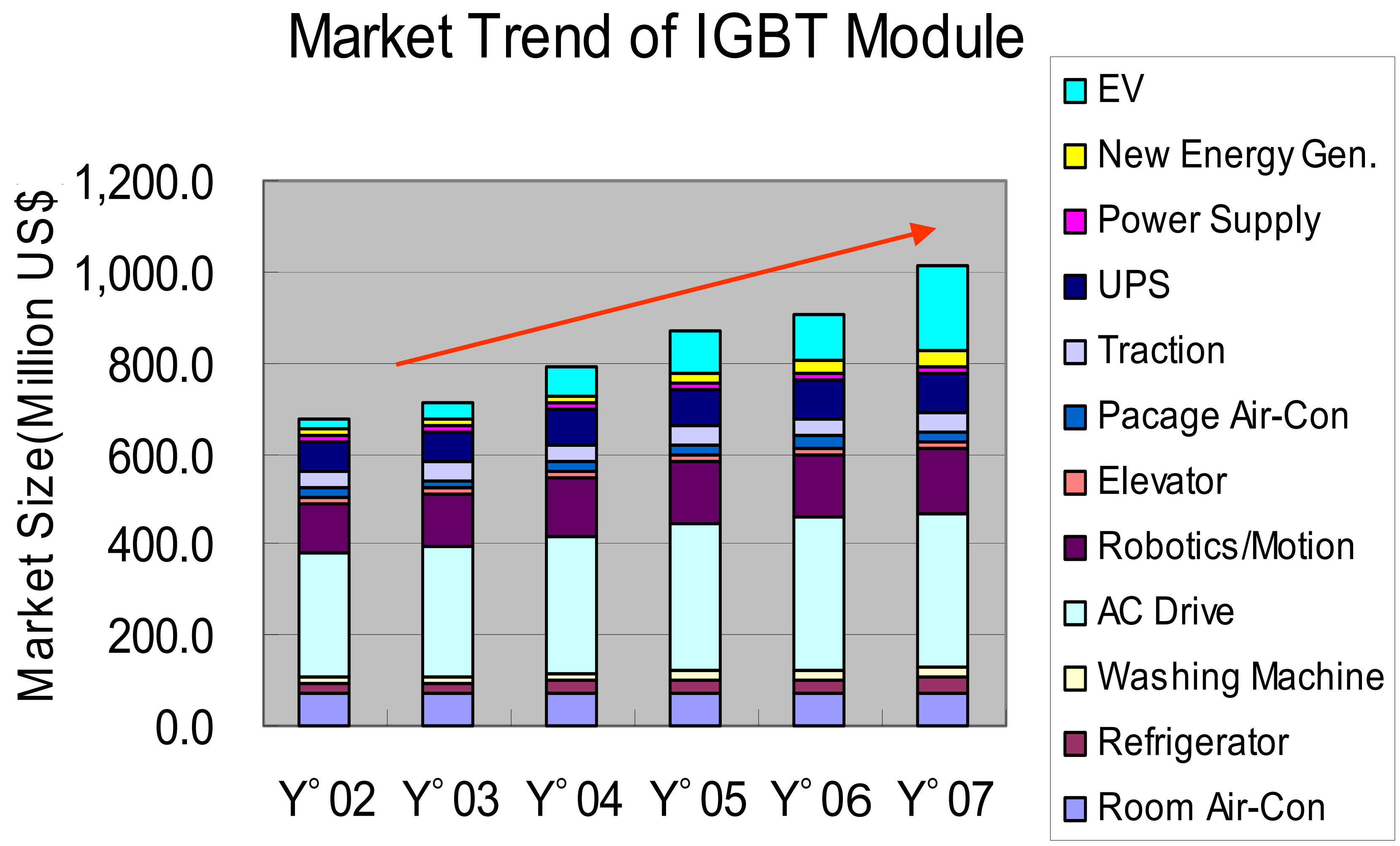
Inverter

Industrial Robots

High Speed Elevator

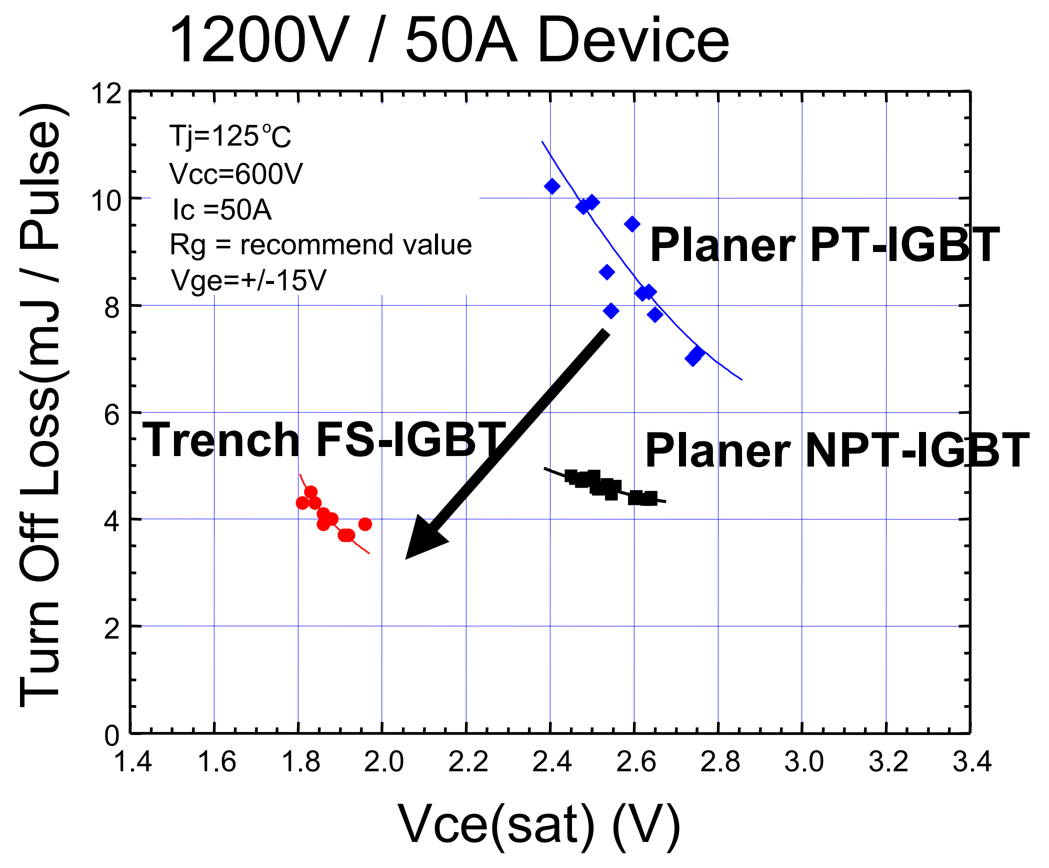
NC Machine Tools

1.Introduction



1.Introduction: IGBT Development Focus

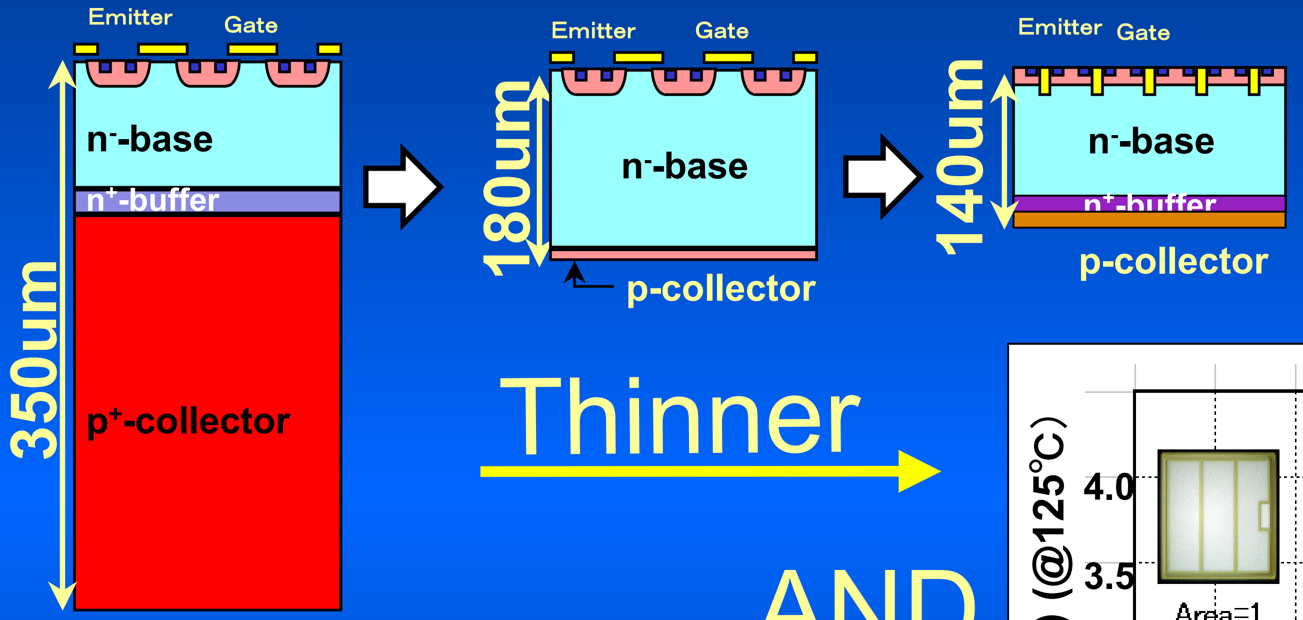
Power Loss Improvement



The focus of IGBT development used to be minimizing of Vce(sat) and Turn Off Loss to reduce power consumption.

1.Introduction: How to improve the power loss

Planer PT-IGBT Planer NPT-IGBT Trench FS-IGBT

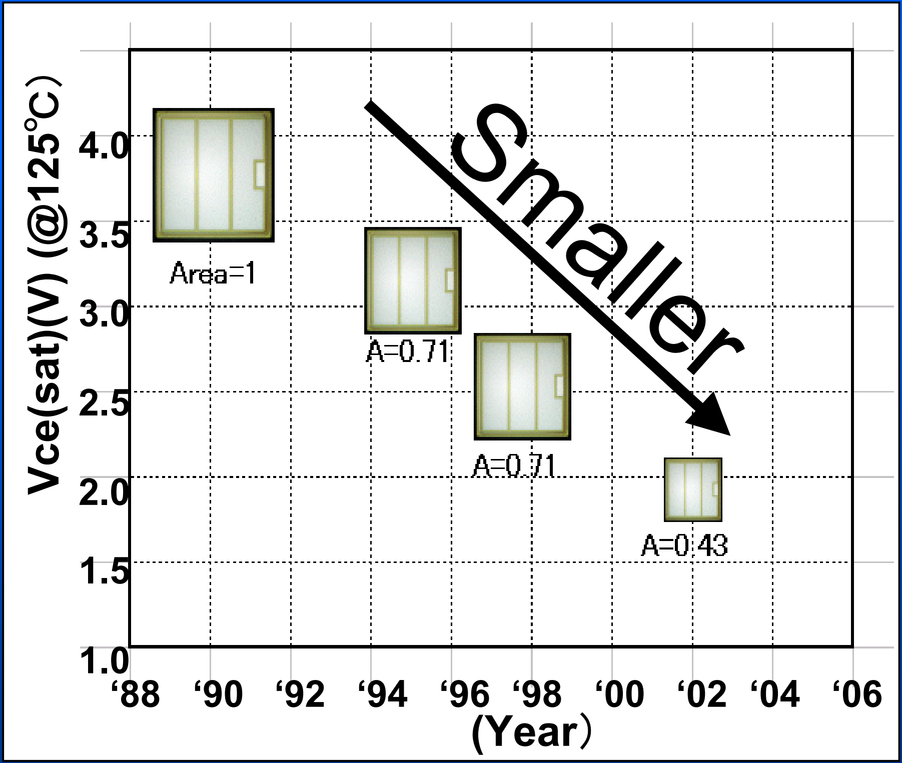


Thinner

AND

Current Density ×2.3

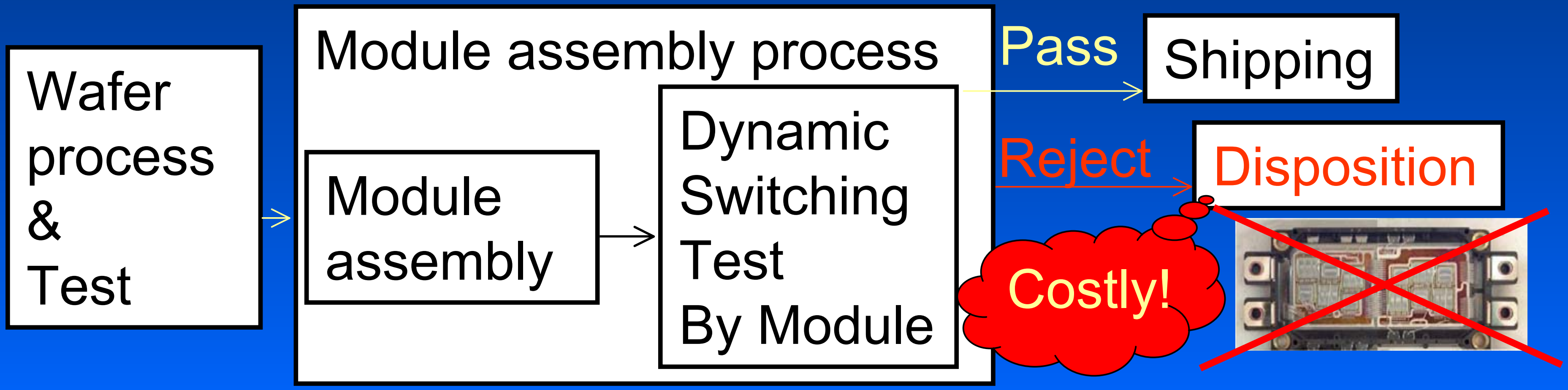
Approx. 100A/cm^2 in rating



2.Dynamic Switching Test

2.Dynamic Switching Test

Process Flow



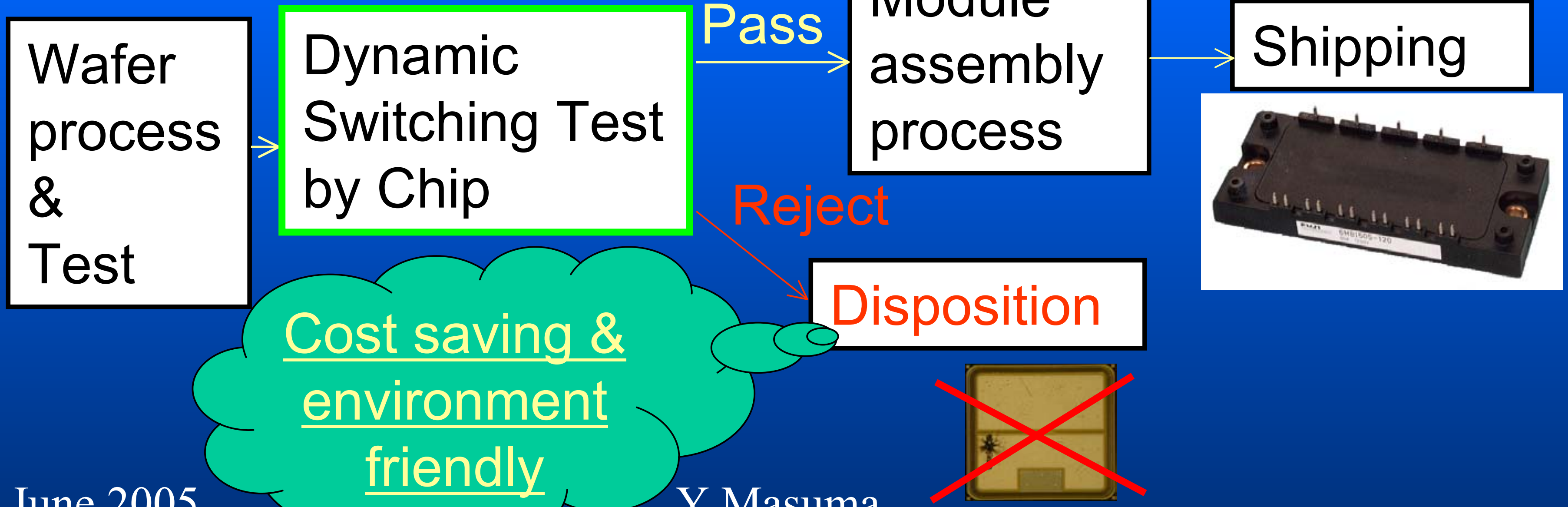
Wafer process & Test → Module assembly process [Module assembly → Dynamic Switching Test By Module]

Pass → Shipping

Reject → Disposition

Costly!

Solution for saving the Earth



Wafer process & Test → Dynamic Switching Test by Chip

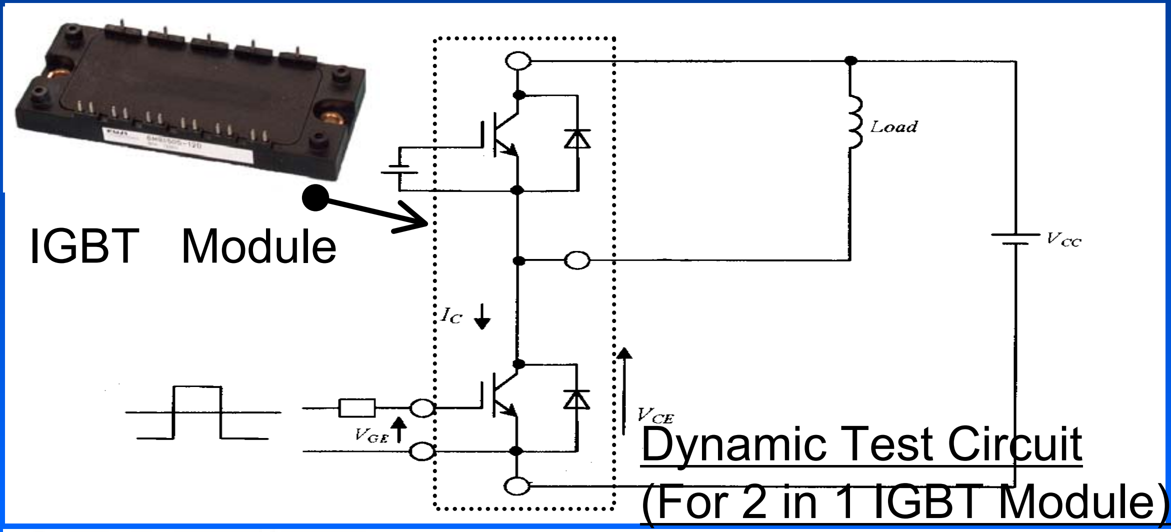
Pass → Module assembly process → Shipping

Reject → Disposition

Cost saving & environment friendly

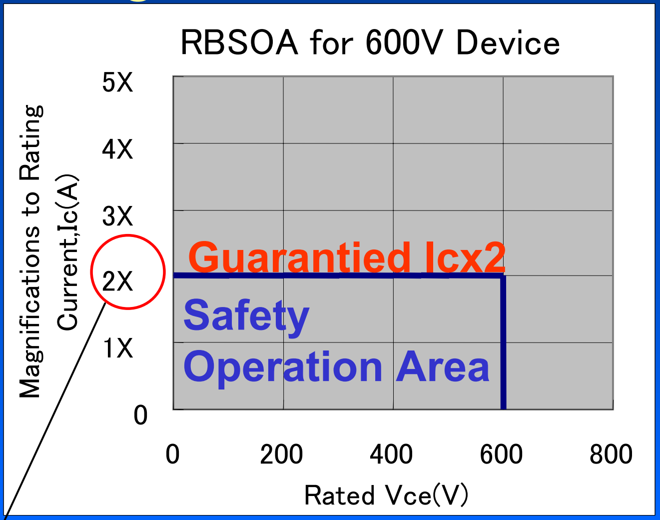
2.Dynamic Switching Test : Current density

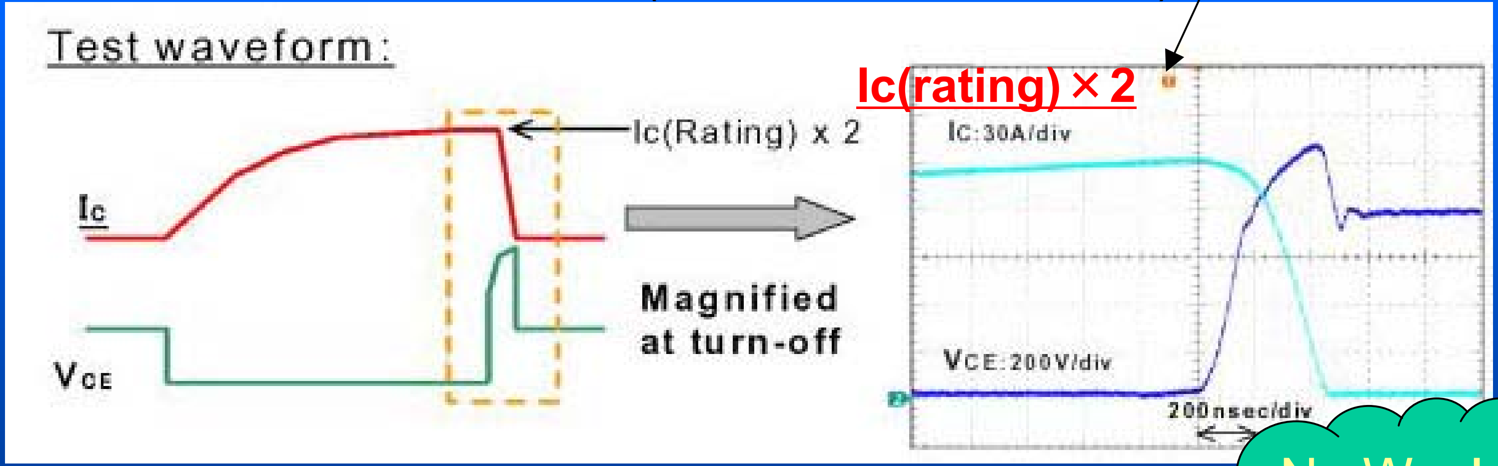
Dynamic Switching Test by Module



Dynamic Test Circuit
(For 2 in 1 IGBT Module)

Regulation of RBSOA





RBSOA
=**R**everse
Bias
Safety
Operation
Area

Dynamic Switching Test by Chip

Ic is rating×2 ⟺ approx. 200A/cm² !

No Way!
Too High!

3.The Key Technology of This Development

1) Development Theme:

The Realization of the Dynamic Switching Test for IGBT Chip

2) Technical Issue：

The Contact Technology under High Current(200A/cm^2)

3) The Key Technology of This Development ：

3.1 Probe mark depth control under WDBD.

3.2 To overcome trade-off between Probe mark depth & CRES

3.3 The design criteria for Probe Assembly:current distribution in Probe Assembly & maximum current per probe

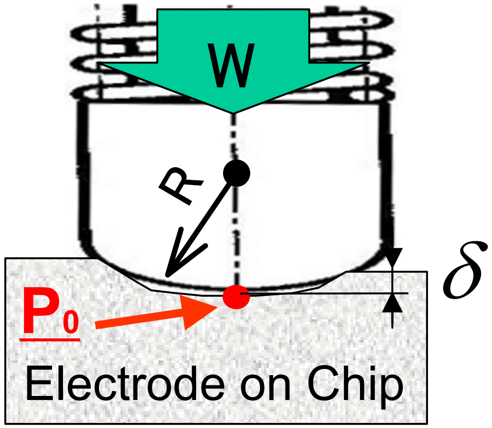
3.1 Probe mark depth control under WDBD

Probe mark depth(δ) is proportional to Hertz pressure(P_0)

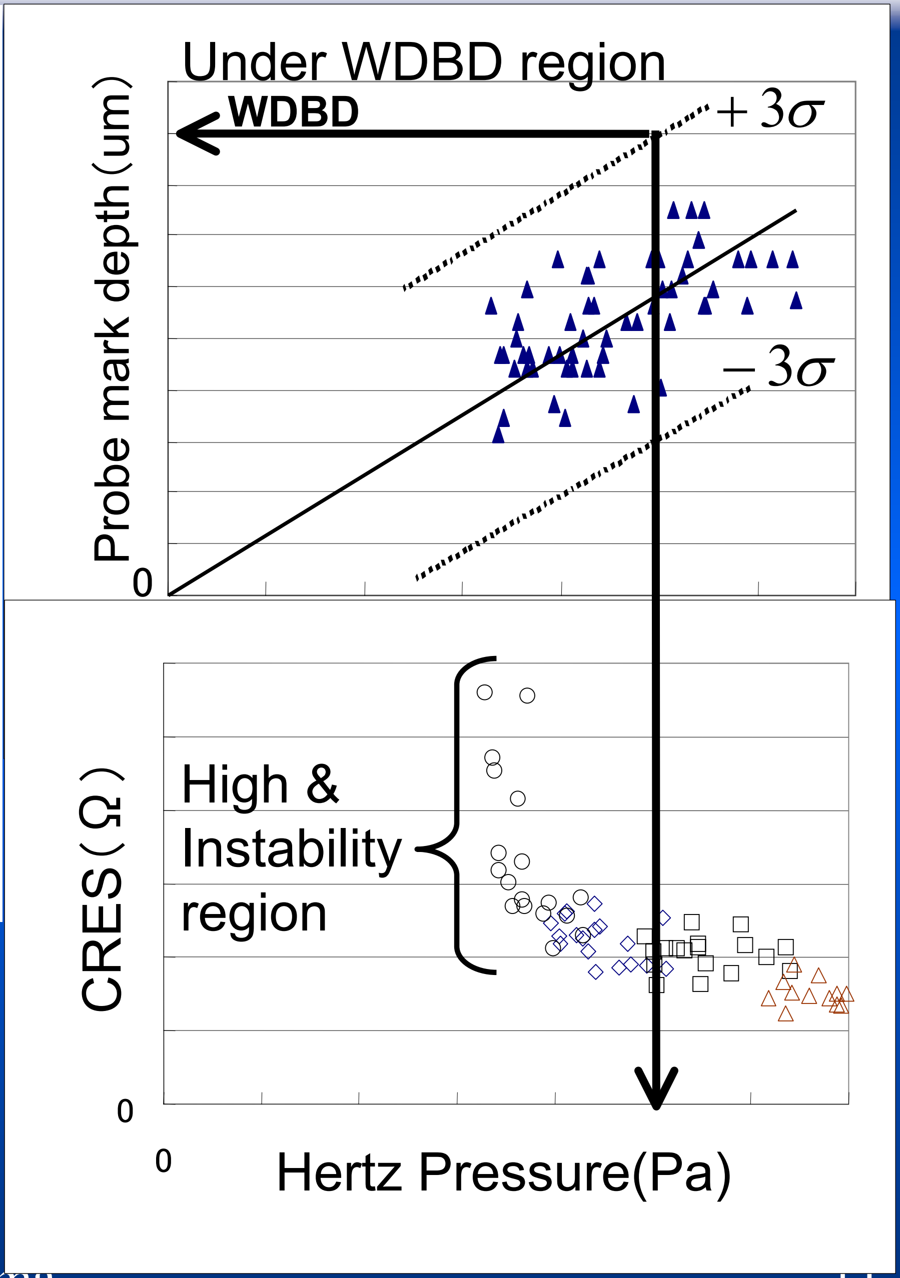
$$\delta \propto P_0 = \left(\frac{6E^{*2}}{\pi^3}\right)\left(\frac{W}{R^2}\right)^{\frac{1}{3}} = const.\left(\frac{W}{R^2}\right)^{\frac{1}{3}}$$

R: Probe Tip Curvature(um)、W: Load(gf)

E∗: Elastic Modulus



Hertz pressure controls Probe mark depth(δ) under WDBD



Shallow Probe Mark Depth

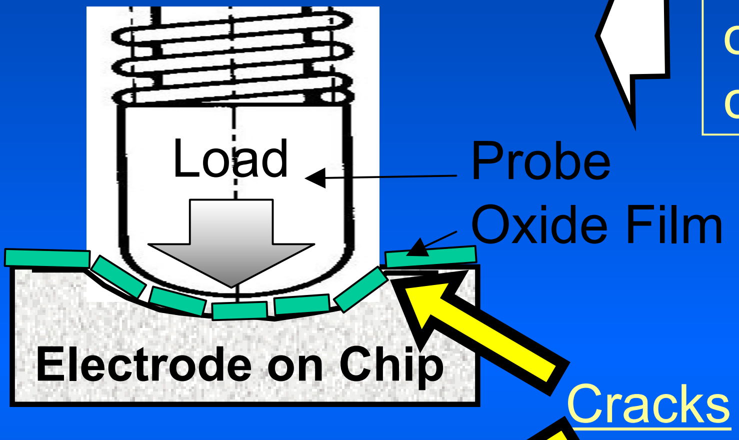
Trade Off

High & Instability CRES Region

3.2 To overcome trade-off between Probe mark depth & CRES

Minimization of CRES:

B-Fritting Phenomena

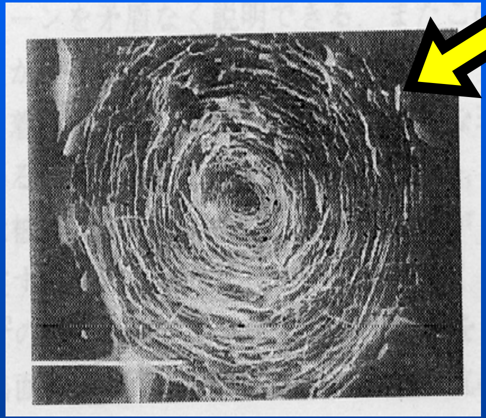


Probe touching down on chip makes nano-cracks

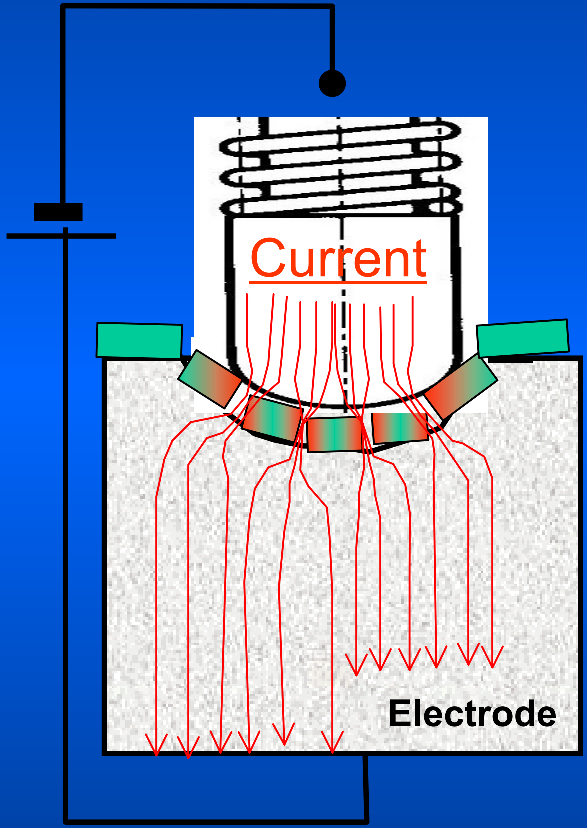
Joule heat enlarges nano-cracks.

nano- Spot welding

CRES decrease



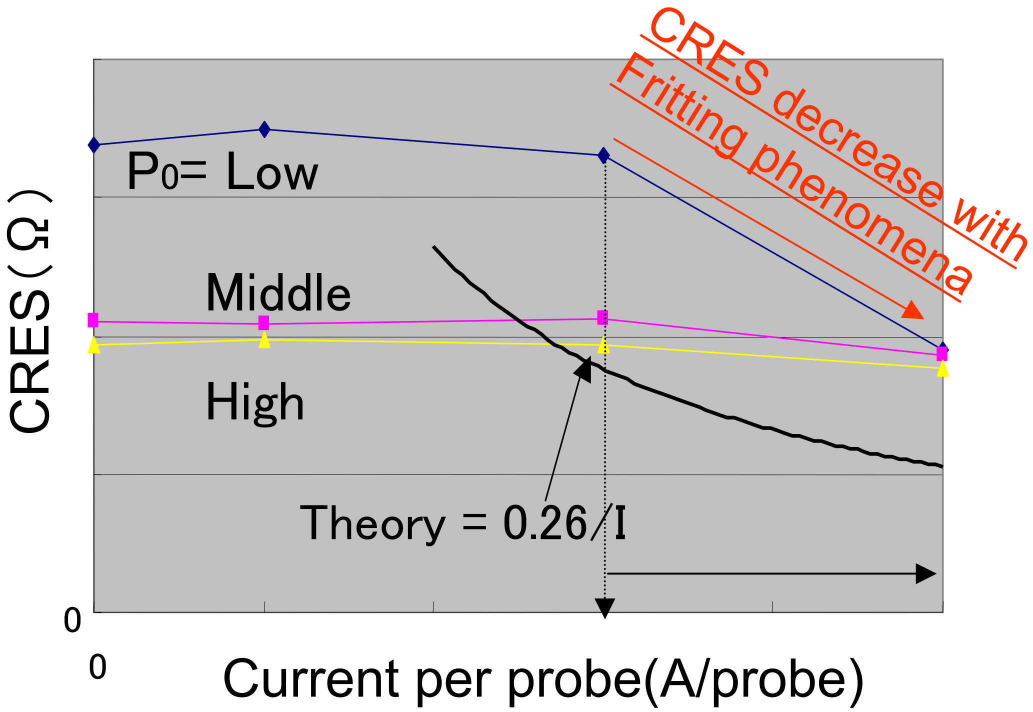
Cracks on 80nm carbon film（SEM–Image）
（Ando et al. IEICE'96）



3.2 To overcome trade-off between Probe mark depth & CRES

Fritting phenomena

Effect of Fritting phenomena



In low Hertz pressure region,
Fritting phenomena realized.

Fritting phenomena（B-Fritting）

Based on the law of Widemann-Franz-Lorenz

$$\frac{\kappa}{\sigma} = L \cdot \theta$$

κ : Thermal Conductivity 、σ =1/ρ : Electrical Conductivity、L : Lorenz-Number（2.45E-8 $\left(\frac{V}{K}\right)^2$）、θ : Temp. at contact point

According to this relationship between thermal and electrical conductivity, the voltage drop(Vc) at actual contact point is expressed (on steady state) ;

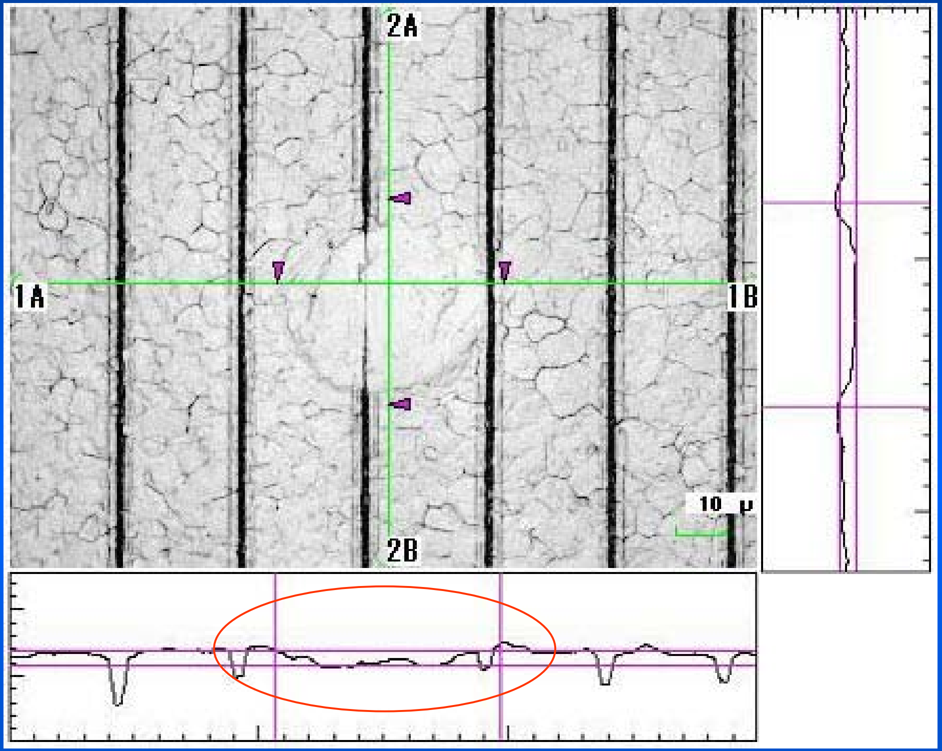
$$Vc = \left[4L(\theta^2 - \theta_0^2)\right]^{\frac{1}{2}}$$

CRES is,

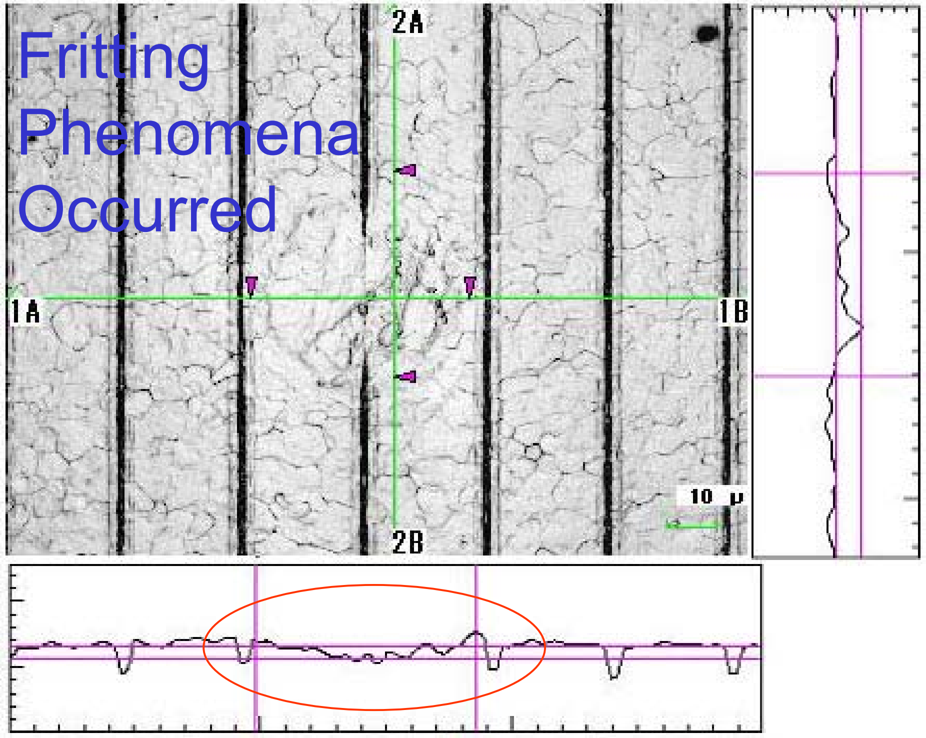
$$CRES = \frac{Vc}{I} = \frac{\left[4L(\theta^2 - \theta_0^2)\right]^{\frac{1}{2}}}{I}$$

3.2 To overcome trade-off between Probe mark depth & CRES

Non Fritting and after Fritting probe mark

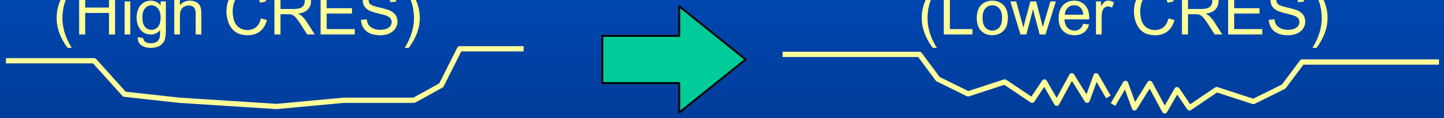


Non Fritting


Fritting Phenomena Occurred

After Fritting

Cross section

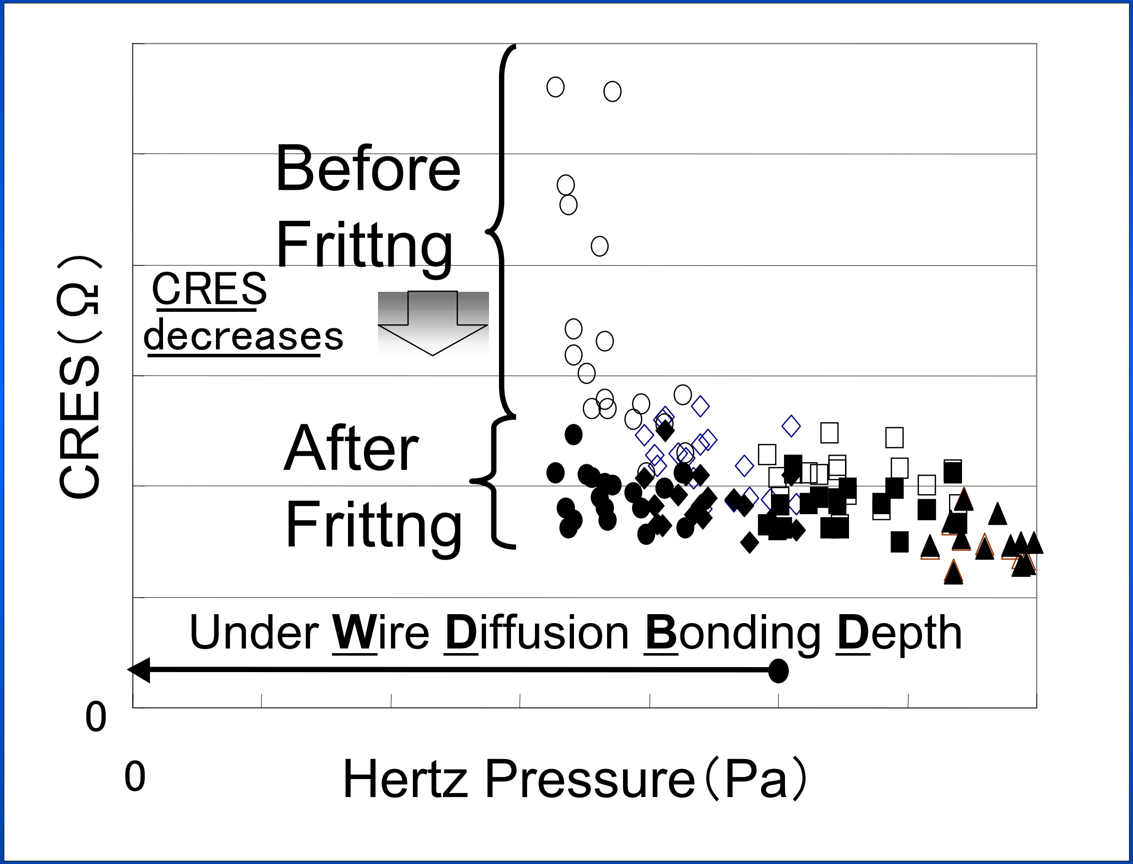

(High CRES)

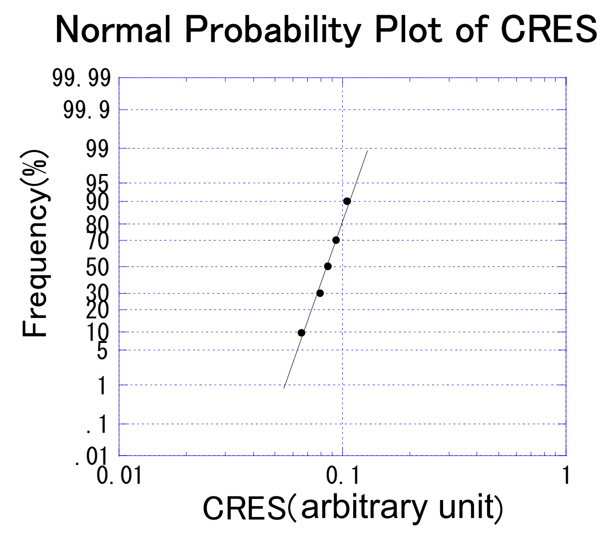
(Lower CRES)

Fritting-Mark

3.2 To overcome trade-off between Probe mark depth & CRES

Low CRES is realized by Fritting phenomena under WDBD region (low Hertz pressure region).





CRES is Normal distribution

CRES after Fritting;

Ave.+3σ=Const.
(Design parameter)

3.3 The design criteria for Probe Assembly

1) Current distribution in Probe Assembly
2) Maximum current per probe

3.3 The design criteria for Probe Assembly

1) Current distribution in Probe Assembly

CRES distribution after Fritting is normal distribution

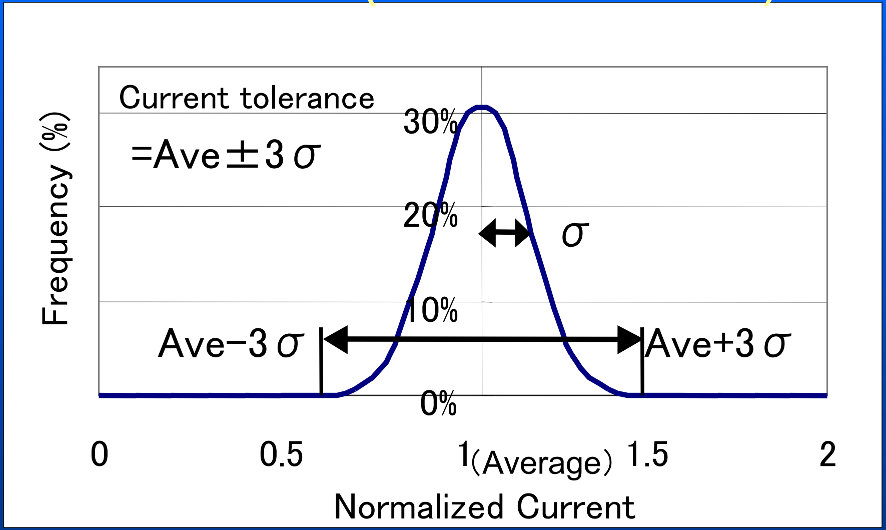
Normalized Ave.=1 & σ

⇩

Current distribution obeys CRES distribution(assumption)

⇩

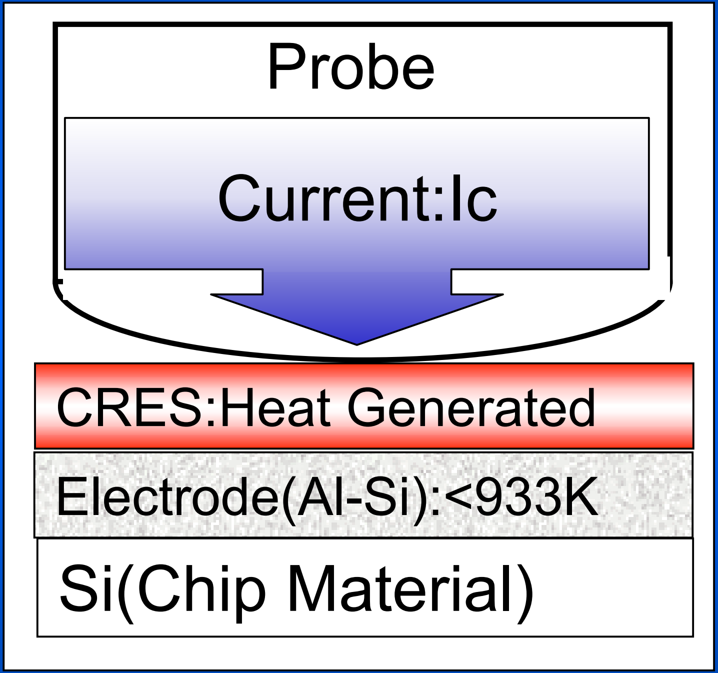
Current tolerance(in normalized)=Ave.±3σ



3.3 The design criteria for Probe Assembly

2) Maximum current per probe is derived by the numerical analysis of un-steady state heat transfer

Model



$$\frac{\partial\theta}{\partial t} = D\frac{\partial^2\theta}{\partial x^2} + Q$$

$$Q = \mathrm{CRES} \cdot I_c(t)^2$$

$$D = \frac{\kappa}{C_p \cdot \rho}$$

θ : Temperature(K)

D:Thermal diffusivity

κ : Thermal Conductivity

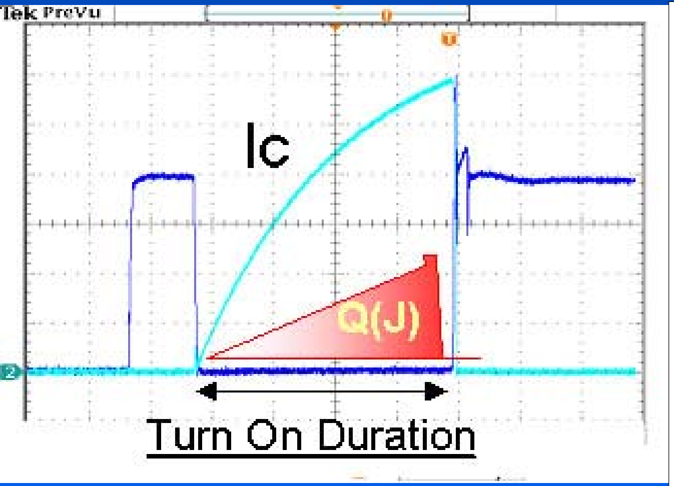
ρ : Mass Density

Cp: Specific Heat at Const. Pressure

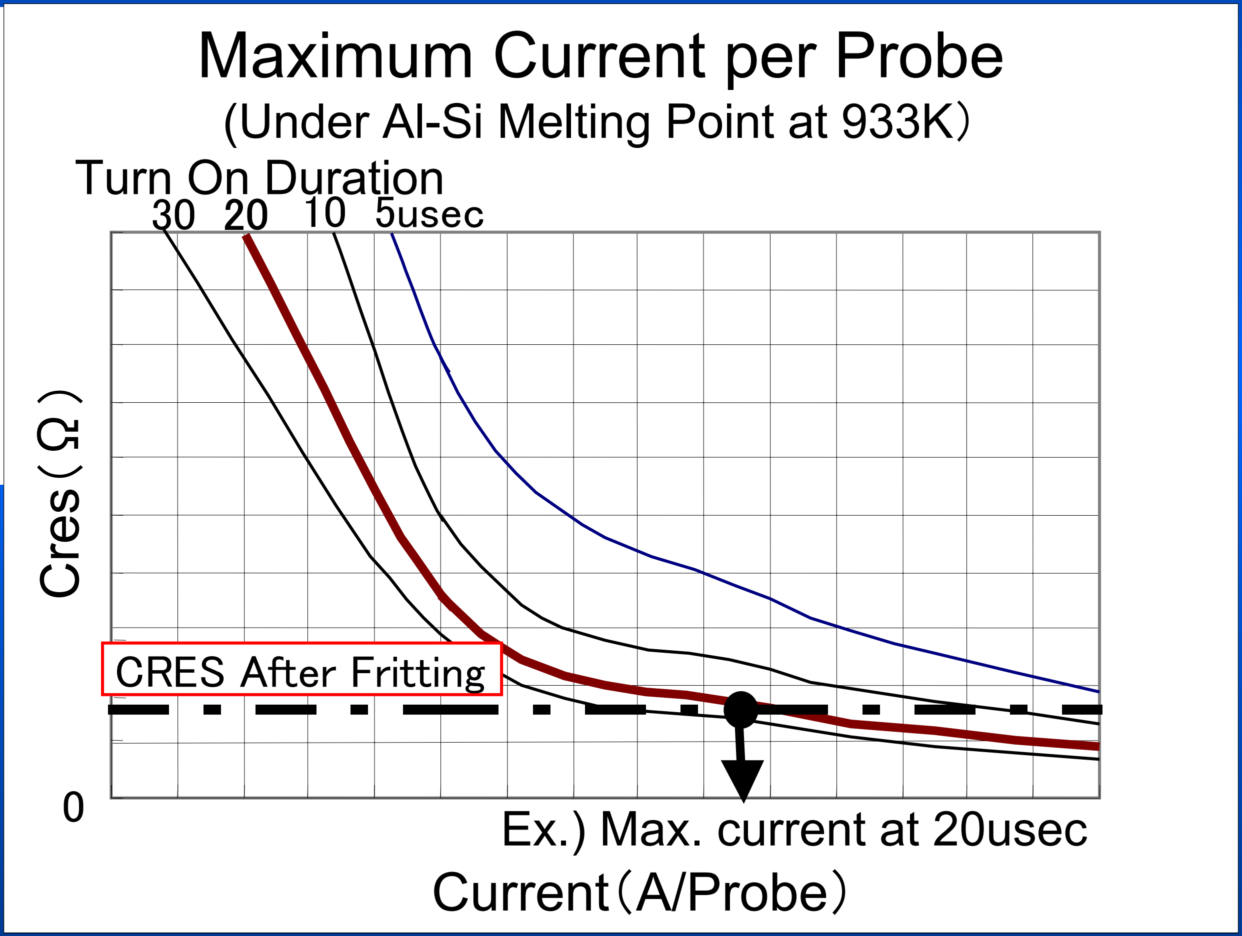
3.3 The design criteria for Probe Assembly

2) Maximum current per probe

Load Condition



Calculated Results


Maximum Current per Probe

(Under Al-Si Melting Point at 933K)

4. The Design Criteria Verification

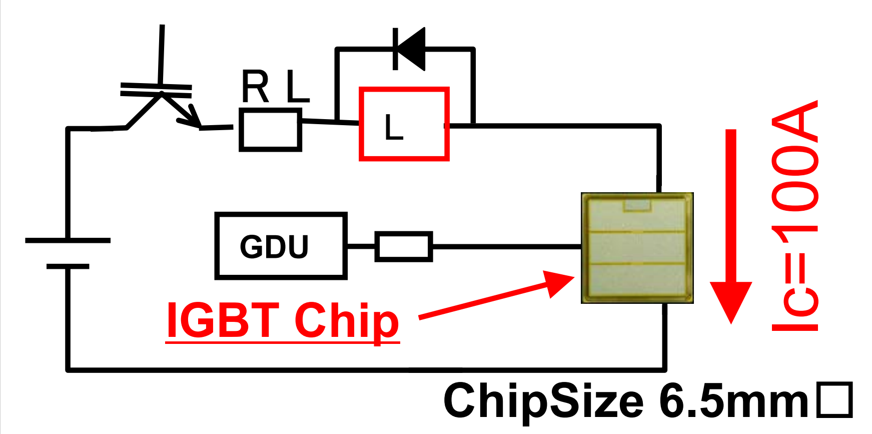
4. The Design Criteria Verification

Ex.) Design for 50A at 600V IGBT chip

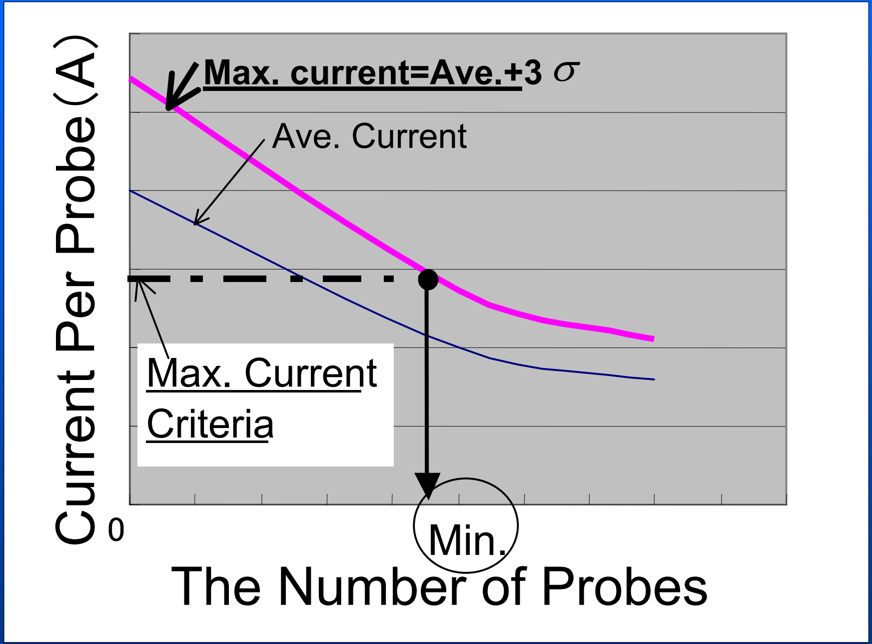
Test condition:

Ic= 100A =50A × 2(rating × 2)

Turn On Duration = 20us



Probe Assembly Design:



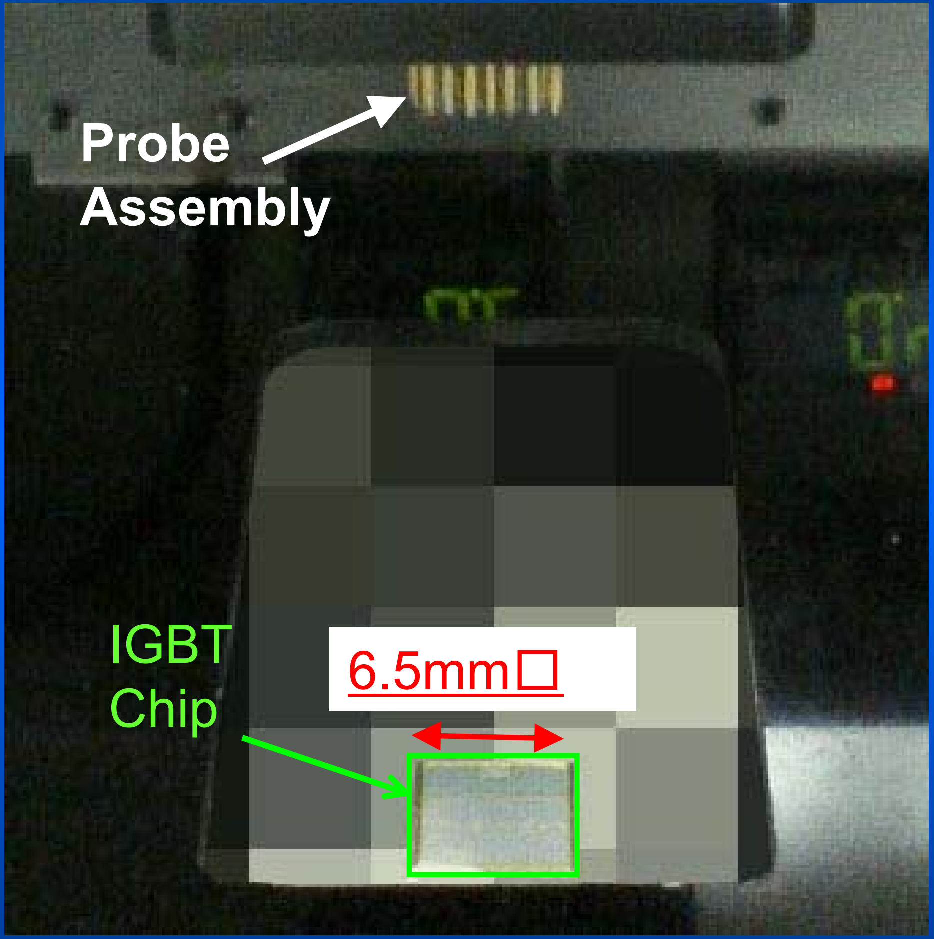
- The number of probe tolerance
  1)Min. ; limited by Max. current
  2)Max. ; limited by chip size

$$\text{MaximumProbeNumber} = \frac{\text{ChipArea}}{\text{ProbePitch}^2}$$

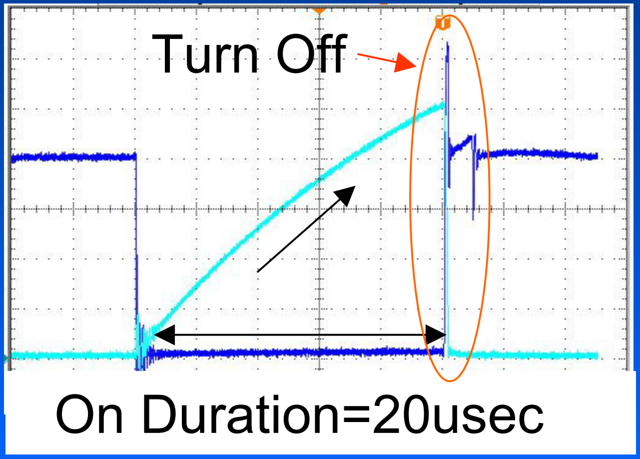
- Design Results :
  The number of probes : Max.
  Ave. current : 100A / Max.
  Current tolerance : Ave.±3σ
  (Ave. – 3σ ～Ave.+3σ)

4. The Design Criteria Verification

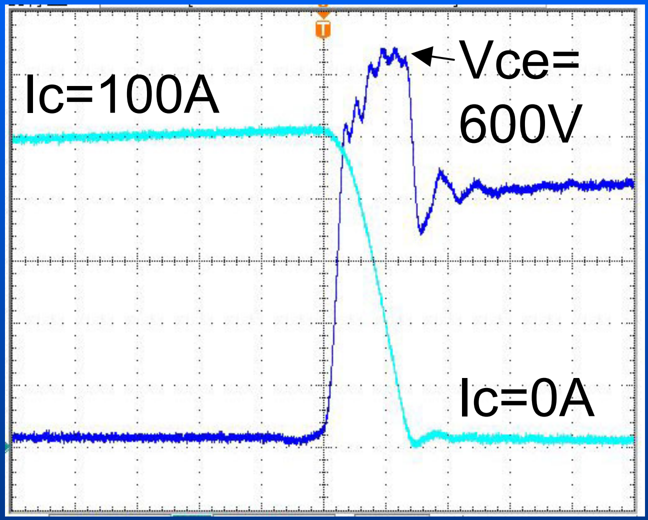
1) Probe Assembly & IGBT Chip



2) Test Waveform



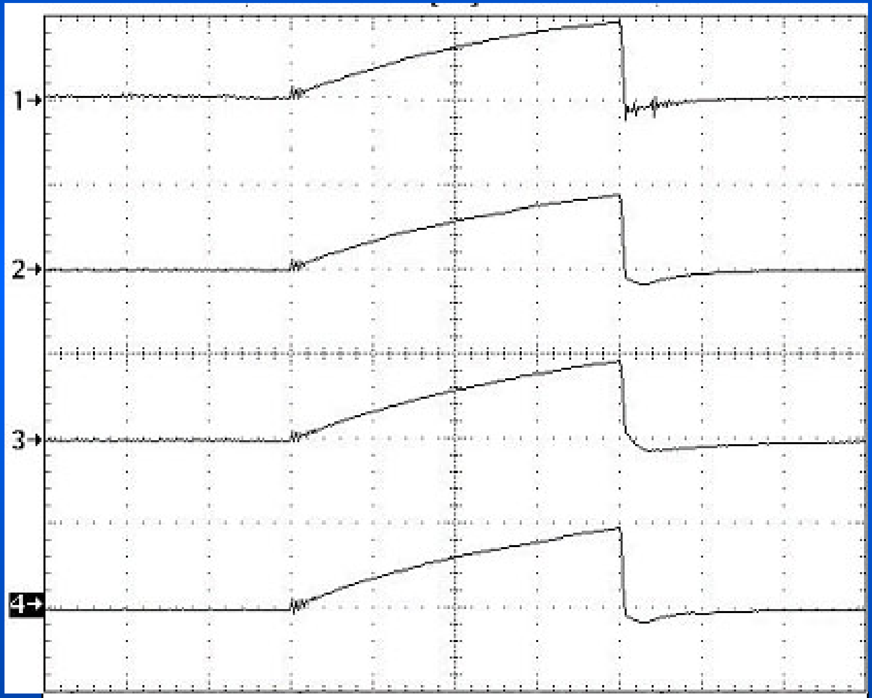
Magnified at Turn Off



4. The Design Criteria Verification

3) Current distribution（30 samples ）

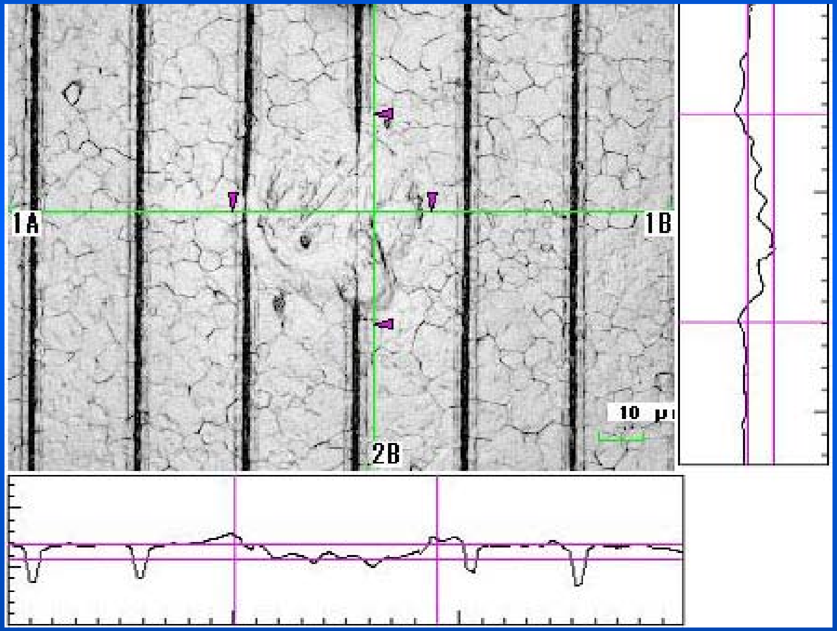
Ave. : 97% of design value
σ : 68% of design value
Ave.$\pm 3\sigma$: In Design Range



Typical 4 Probe Current

4) Probe mark depth

Ave. Depth : 49% of WDBD
Ave. $+3\sigma$: 79% of WDBD
Samples : 84points

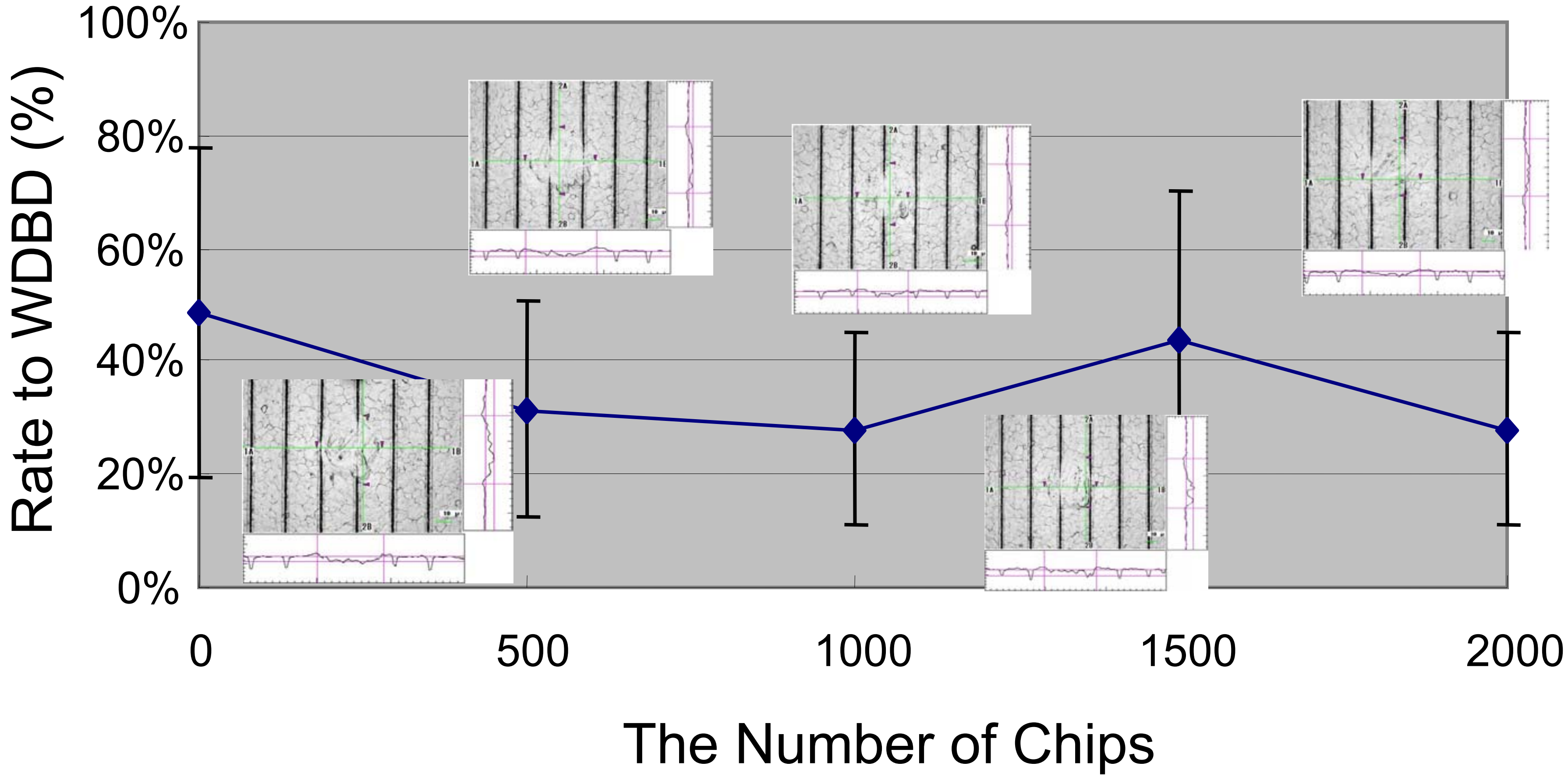


Measured by laser microscope(VK-8500)

4. The Design Criteria Verification

5) Stability of Probe mark depth

Probe mark depth(Ave.+3σ）keeps under WDBD.



5. Conclusion

1) Probe mark depth:

Hertz pressure achieved under WDBD.

2) For trade off for minimization of Probe mark depth and CRES:

Utilization of Fritting phenomena realized simultaneous achievement of CRES and Probe mark depth targets.

3) The design criteria for high current contact probe was established.

The current per probe and distribution are in design range.

4) The Dynamic Switching Test for IGBT Chip applied to our outgoing test in production line.