SIU Probe Burn Control
Southwest Test Workshop

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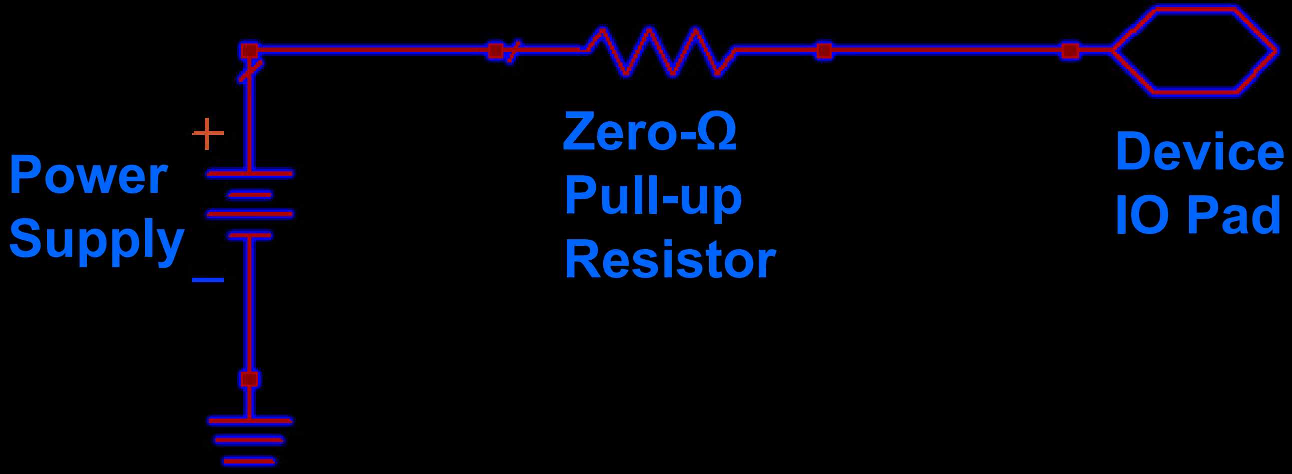
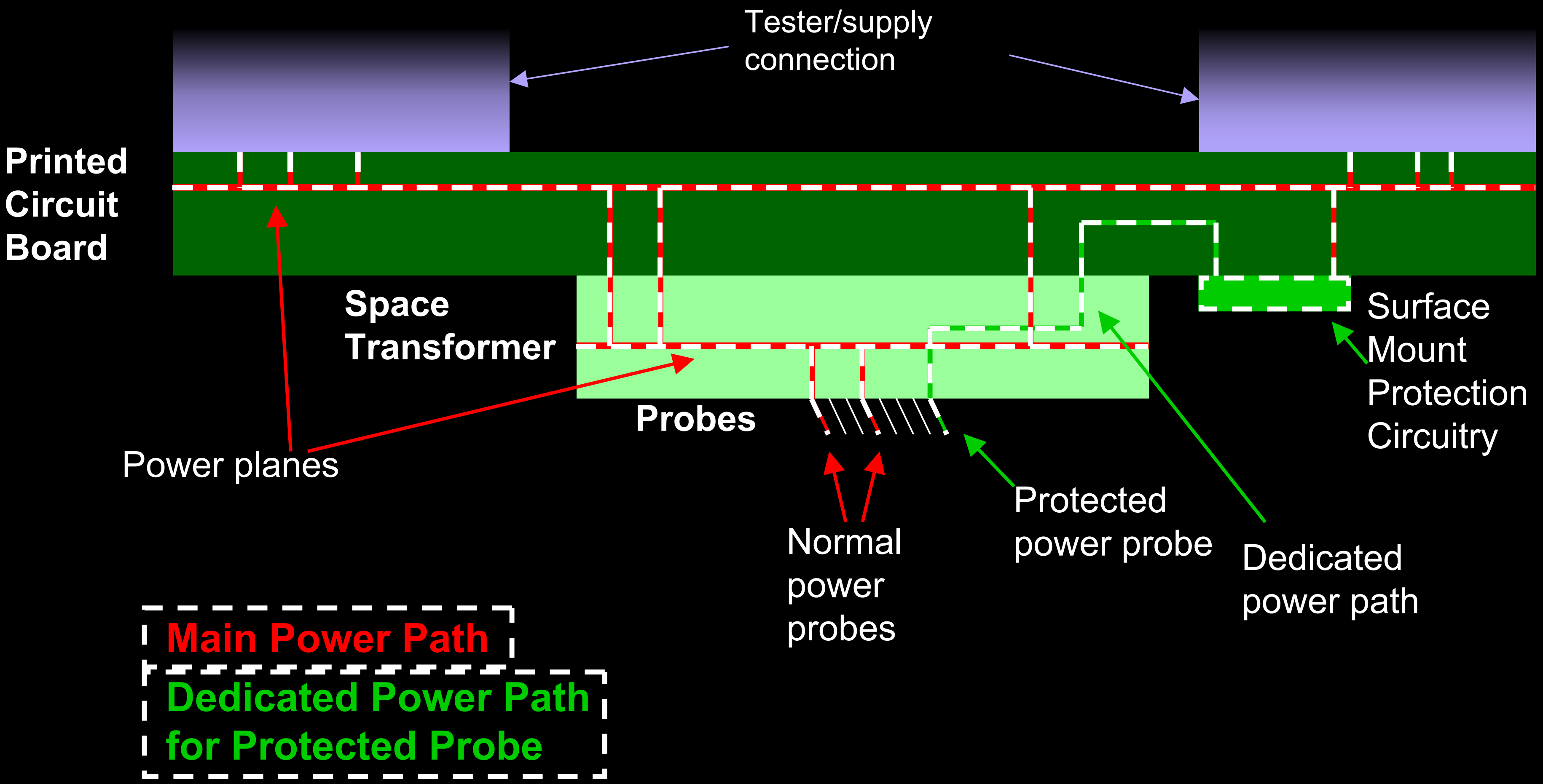
Background and Scope

- Probe types: “critical” and “redundant”
- Redundant probes have plenty of backups
- Critical probes are lonely but crucial
  - ➔**Example: device IO pads tied high or low (see schematic)**
- This presentation just covers criticals



Probe Card Architecture

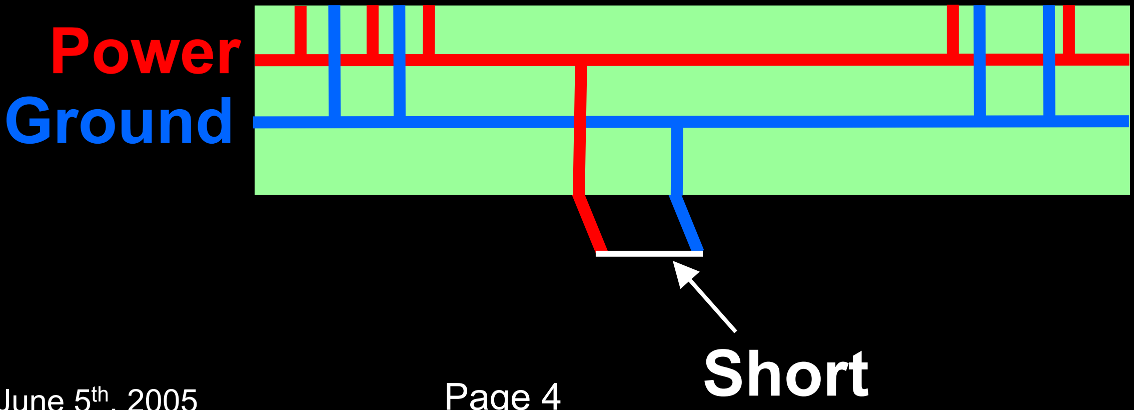
Simplified Sort Interface Unit (SIU)



What Causes Probes to Burn?

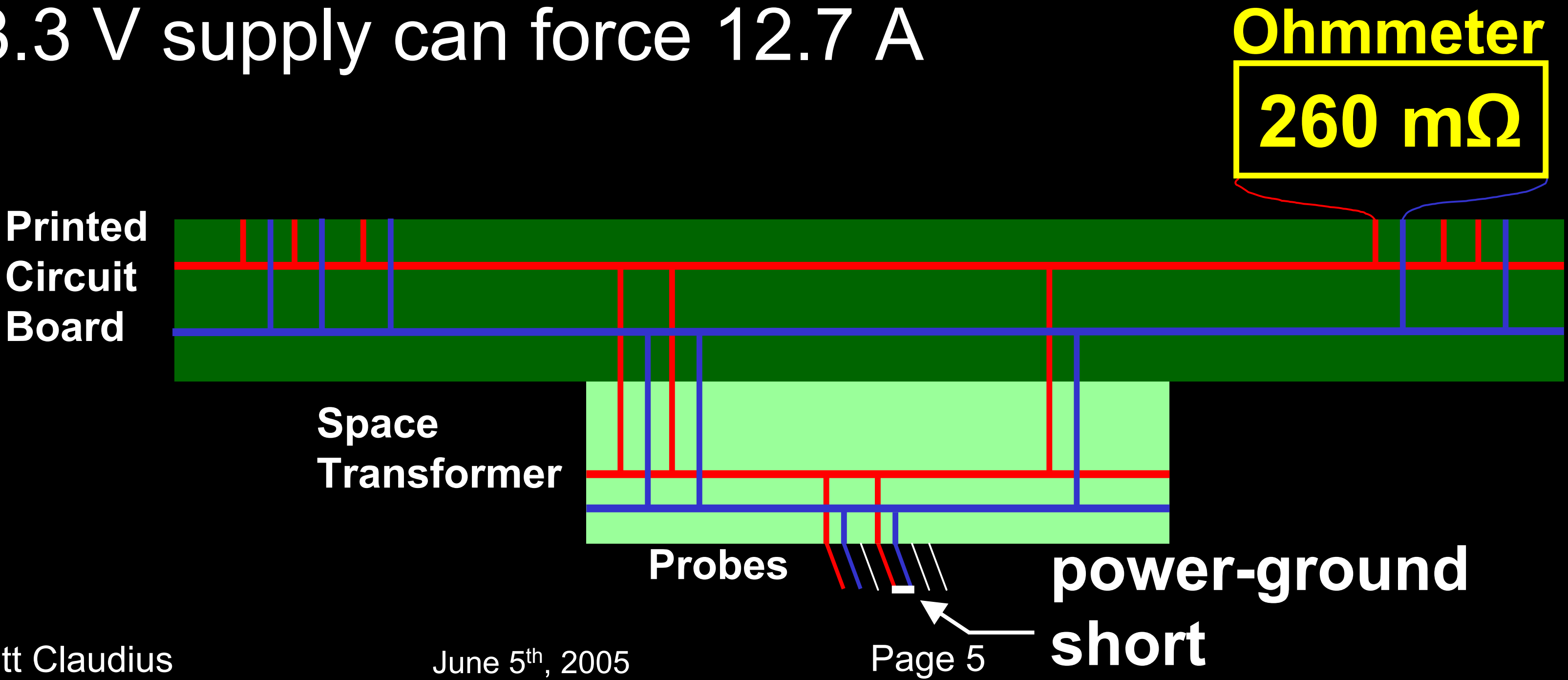
- ☞Some probes are made for low-current
- ☞Low-current probes get themselves into high-current trouble
  - ➔**Short locations**
    - » Probe card surface
    - » Inside the die

Simplified Space Transformer



The Short Event

- Shorted probe current and Ohm's Law: V=IR
  - ➔V = supply voltage
  - ➔I = current flow through probe
  - ➔R = total path resistance (both power and ground paths)
- Power-ground loop resistance as low as 260 mΩ
- A 3.3 V supply can force 12.7 A

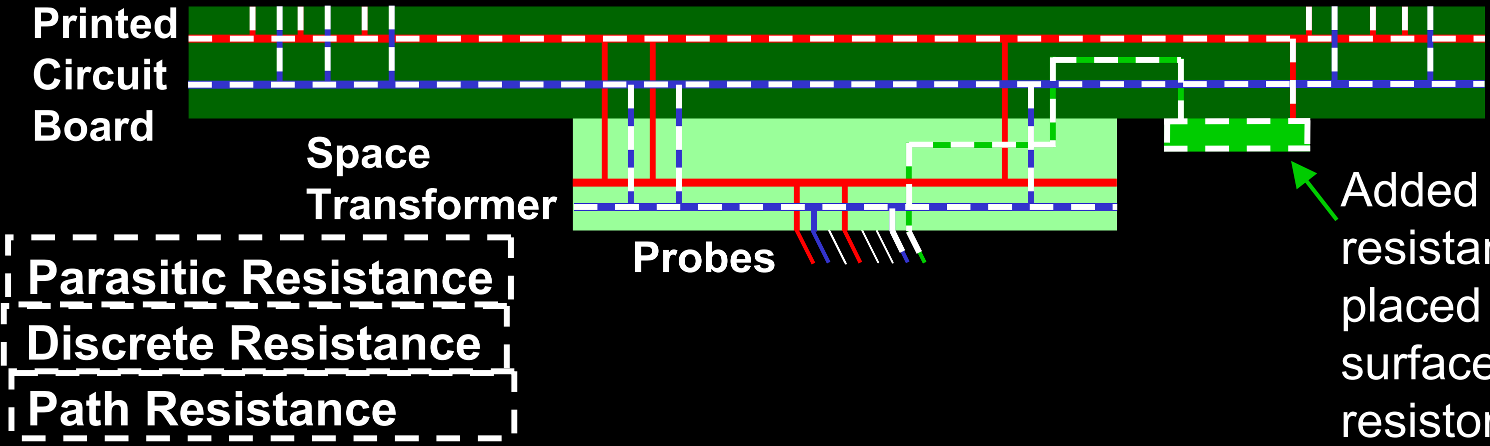


The Solution: Theory

☞ Add resistance to the path.

☞ Add resistance to the path?!? This is power delivery!!!

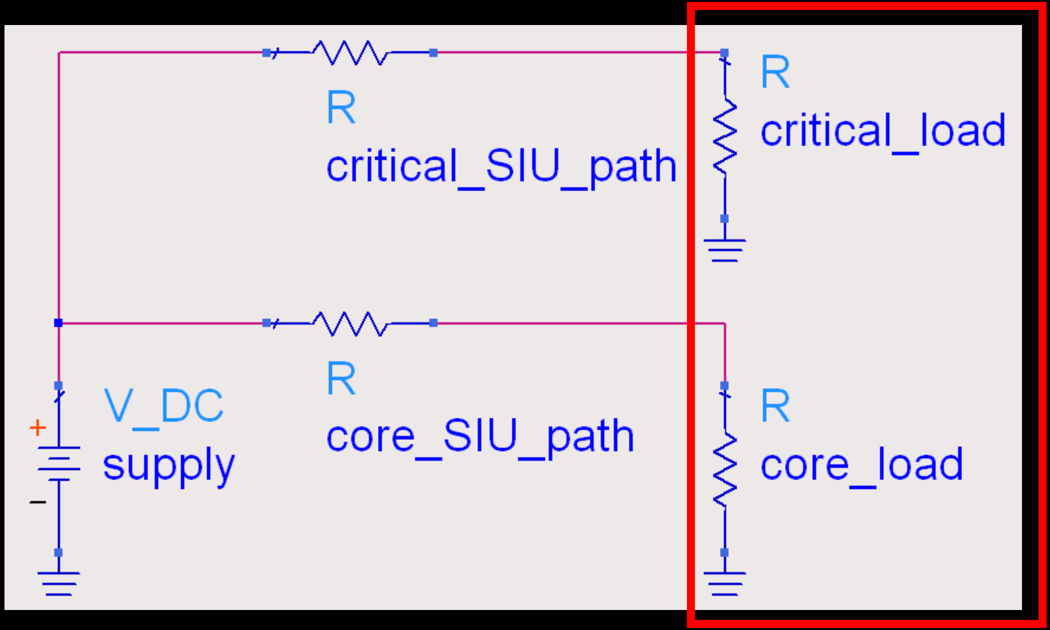
☞ $R_{path} = R_{parasitic} + R_{discrete}$



Added resistance placed here: surface mount resistor

The Solution: Theory

- ☞Core and critical probes—a single supply for conflicting applications
  - ➔Supply compensation at a loss
  - ➔A 100 amp clamp does little for a 1 amp probe

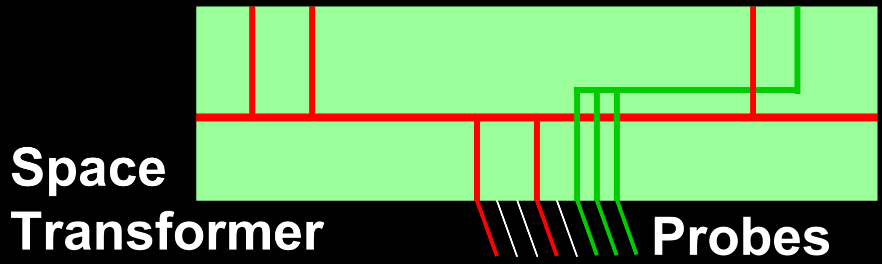


DUT loads

The Solution: Theory

- Normal sort, without a short
  - V = voltage drop
  - I = current through critical path during normal operation
  - R = resistance of critical probe’s dedicated path
- Multiple probes behind the same circuit.
  - Current per probe, R_{path} and V_{drop}
  - Example: 3 probes draw 50 mA each with a 2 Ω path

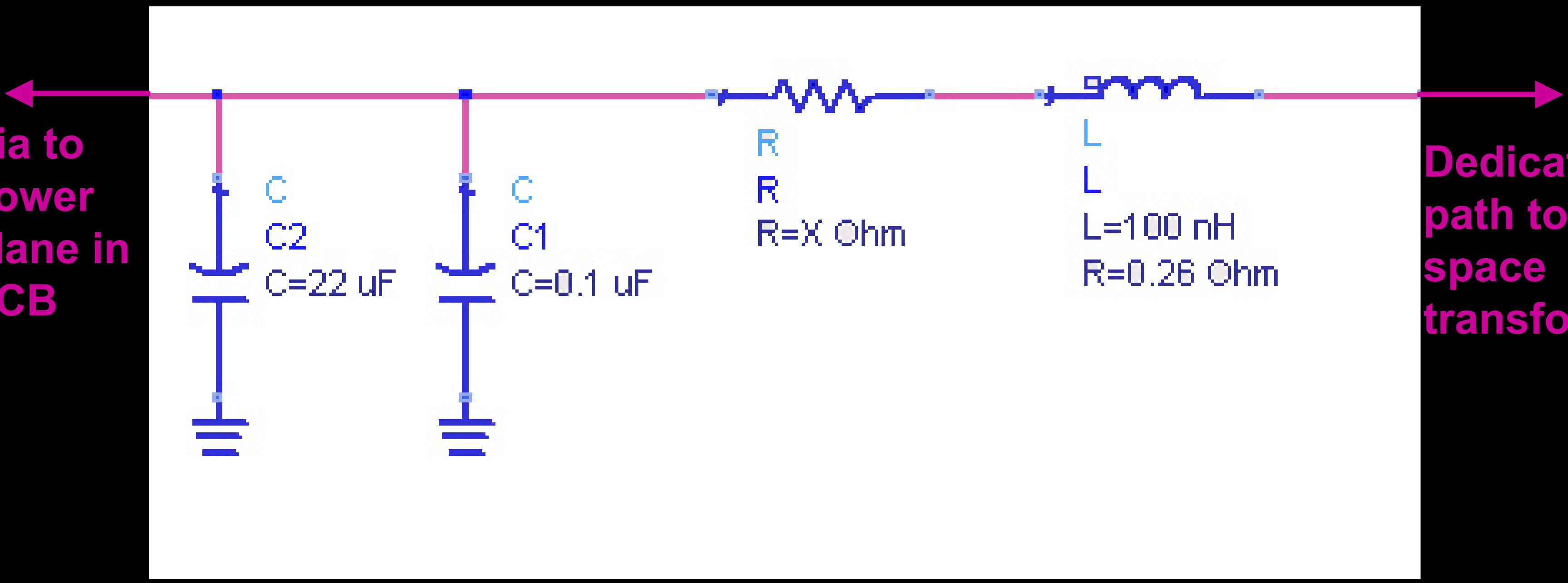
$V_{drop} = (0.050A * 3) * 2\Omega = 0.300\ V$ or $300\ mV$



Critical Path for Multiple Protected Probes

The Solution: Implementation

- Inductance and capacitance slow things down
- Critical probe protection circuit components…



Via to power plane in PCB

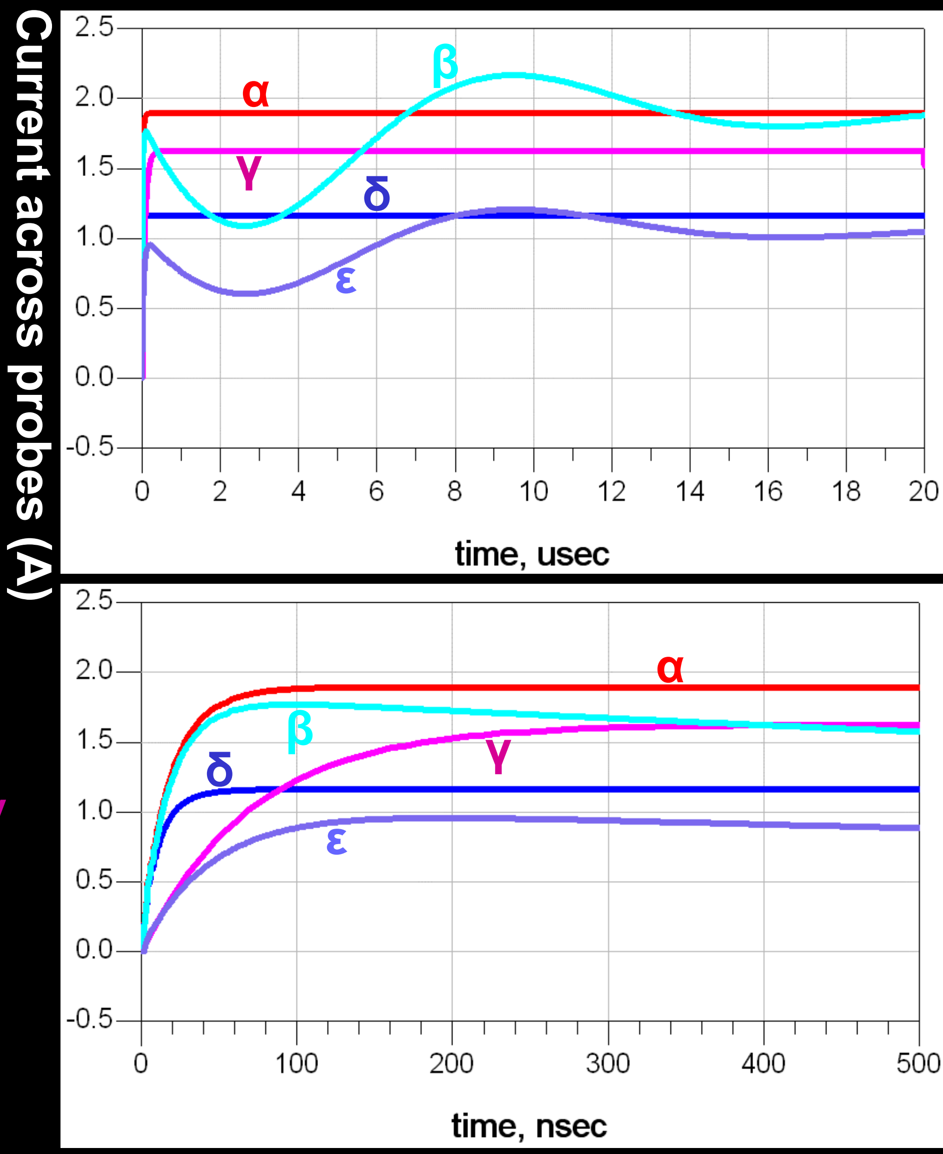
Dedicated path to space transformer

Respective Effects of R, L and C

- Both plots show the same simulations on different time scales.
- Input
  - **3 V**
  - **100 ps rising edge**
- This modeling is useful only to analyze trends.
- α: no protection circuit
- β: cap—22.1 uF only
- γ: ind—100 nH, 0.26 Ω only
- δ: res—1 Ω only
- ε: Full Circuit

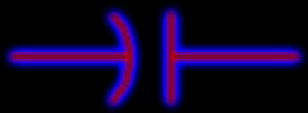
Greek notation here used only for identifying each curve

Probe Current vs. Time in a Short Event



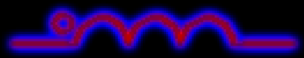
Respective Effects of R, L and C

- ☞ Capacitance



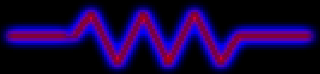
  - ➔ After initial rise, capacitance pushes out the current edge in the µsecond range

- ☞ Inductance



  - ➔ Pushes the initial edge out in the nanosecond range

- ☞ Resistance



  - ➔ Causes steady-state voltage drop

- ☞ LC calculation currently unclear
- ☞ Protection through procrastination

Choosing the Right Resistance

- The right resistance stops burns without getting in the way.
- Lower is better, as long as it works.

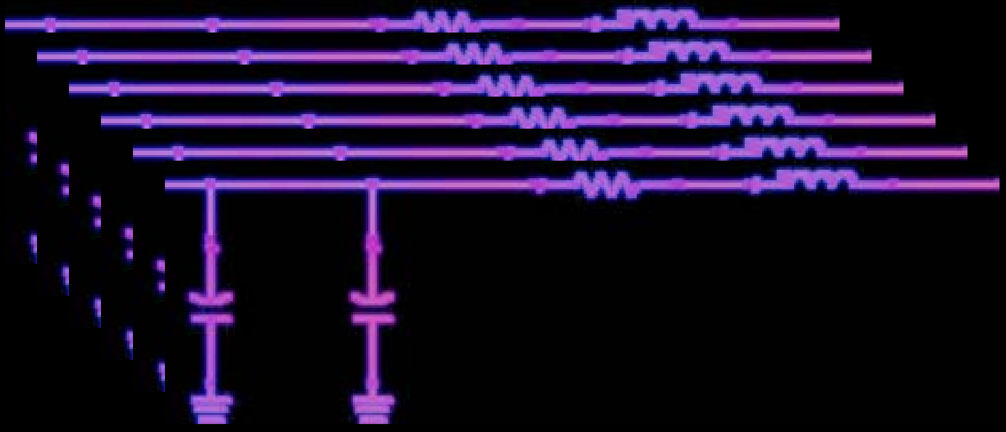
$$R_{discrete} = \frac{V_{supply}}{I_{max}} - R_{parasitic}$$

Probe current carrying capability

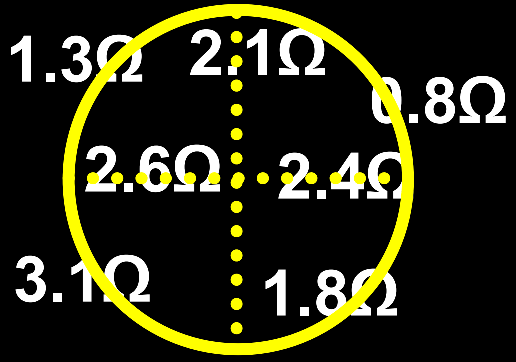
$$R_{discrete} = \frac{V_{supply}}{1.7A} \quad 0.260\Omega$$

Real World Problems

- ☞TOO MANY CIRCUITS



- ☞Hard to find a resistance window
  - ➔**Reckless resistance requires component swap**



NOTE: Above animation is shameless and gratuitous. It implies nothing about the specific resistance of 2.6 Ω.

Current Application

- Initial circuit development required best guesses
- ITO-SIU’s role
  - **Research, standardize and proliferate**
- Strong success with an ambiguous source

Future Work

☞ Research Wanted

- ➔ **Sort floor validation**
  - » Burn, protect, repeat
- ➔ **Accurate path resistance measurements**
  - » Technology-specific precision protection
- ➔ **Supply current clamp response time**
  - » Lock the barn door *while* the horse is escaping
- ➔ **Poly-Fuse technology**
  - » Great technology, useless datasheets

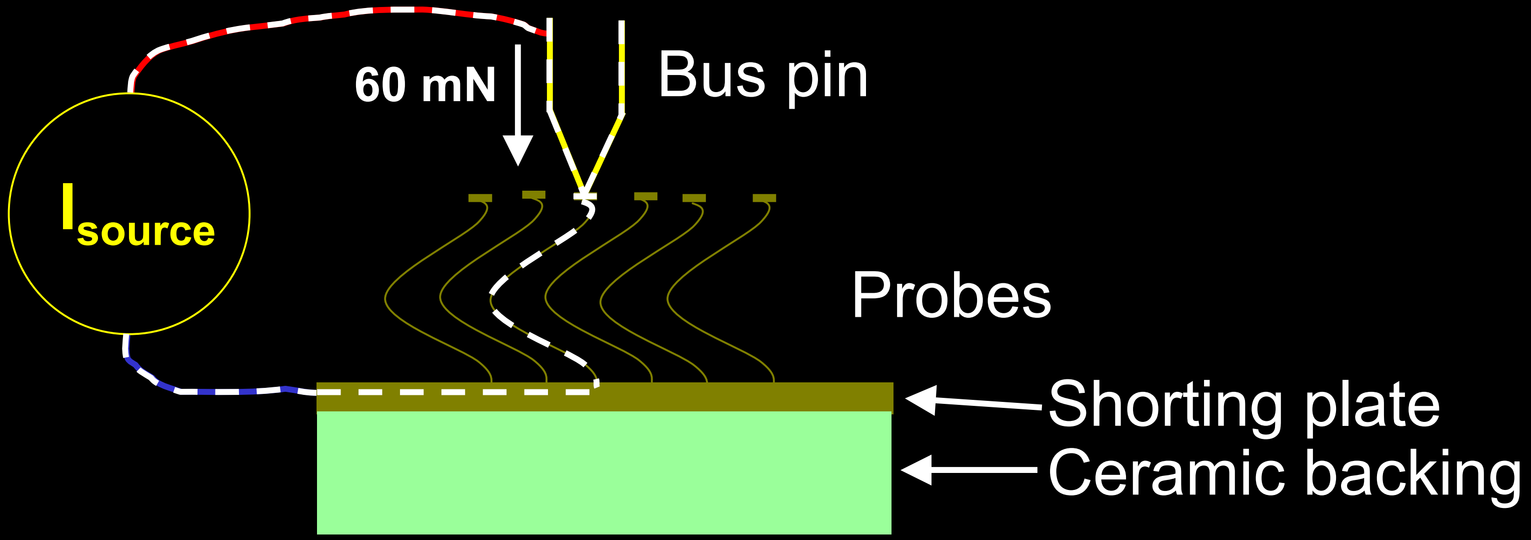
Acknowledgements

- Rod Martens, Form Factor, Inc.
  - **Probe current carrying capability**
- Jason McDaniel, Intel
  - **Sort practices, test methodology, supply current clamping**
- Intel desktop chipset test division
  - **Original protection circuit design**

Backup

Probe Current Carrying Capability

- ☞ The probes' ability to withstand high current was measured for two different scenarios:
  - ➔ **Realistic sort times**
  - ➔ **Fast pulses**
- ☞ All the measurements were completed in the lab environment with the setup shown below.



Probe Current Carrying Capability

- Realistic Sort Timing
  - **Pulses were 5 seconds long**
  - **750 ms between pulses**
  - **3, 10 and 30 pulse runs**
  - **Current increased 0.1 A between runs, then reproducibility was performed at anticipated max current for 15 more runs**
  - **New probe used every run**
  - **After reproducibility runs were completed, 1.7 A was determined to be max current**

Experiment completed on Form Factor, Inc. 6.3.5 springs

- Fast Pulse
  - **Pulses were 17 ms long**
  - **Only one pulse per run (i.e. no pulse train)**
  - **Current increased 0.1 A between runs, then reproducibility was performed at anticipated max current until failure was obvious**
  - **New probe used every run**
  - **Initial runs implied capability up to 3.1 A (max current of lab supply), but reproducibility runs proved this untrue**
  - **No special case was made for fast pulses compared to normal sort**