Searching For Correlations in HVM Wafer Testing

Zhineng Fan, Ph.D
Youssef Fassi
Rey Rincon

Tuan Duong

Agenda

1. Introduction
2. Direct Correlation Model
3. Proposed Correlation Model
   - Modeling
   - Validation
4. Application Example
5. Limitations/Next step
6. Summary

Introduction

Current Status

- Cost benefit relationship between suppliers and down stream customer is not clear
- Probe card manufacturers speaks a different language than their customers
- Probe card suppliers critical parameters do not directly correlate to test floor performance

Probe Card Supplier Critical Parameters

- Force
- Planarity
- PCA Cres
- Scrub
- Alignment

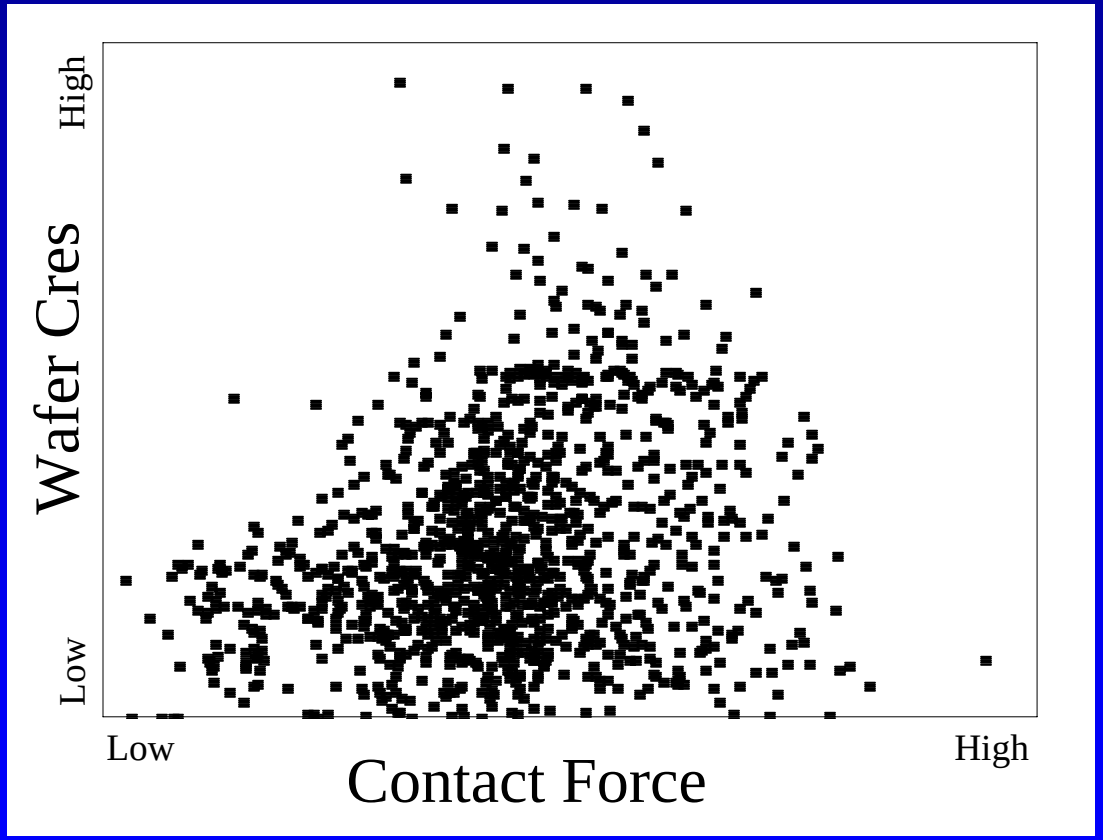
Test Floor Performance Indicators

- Binning
- Wafers Per Setup
- Resort Rate
- Wafer Cres

Direct Correlation Model

Correlation map of contact force vs. wafer Cres. Data collected from multiple samples.

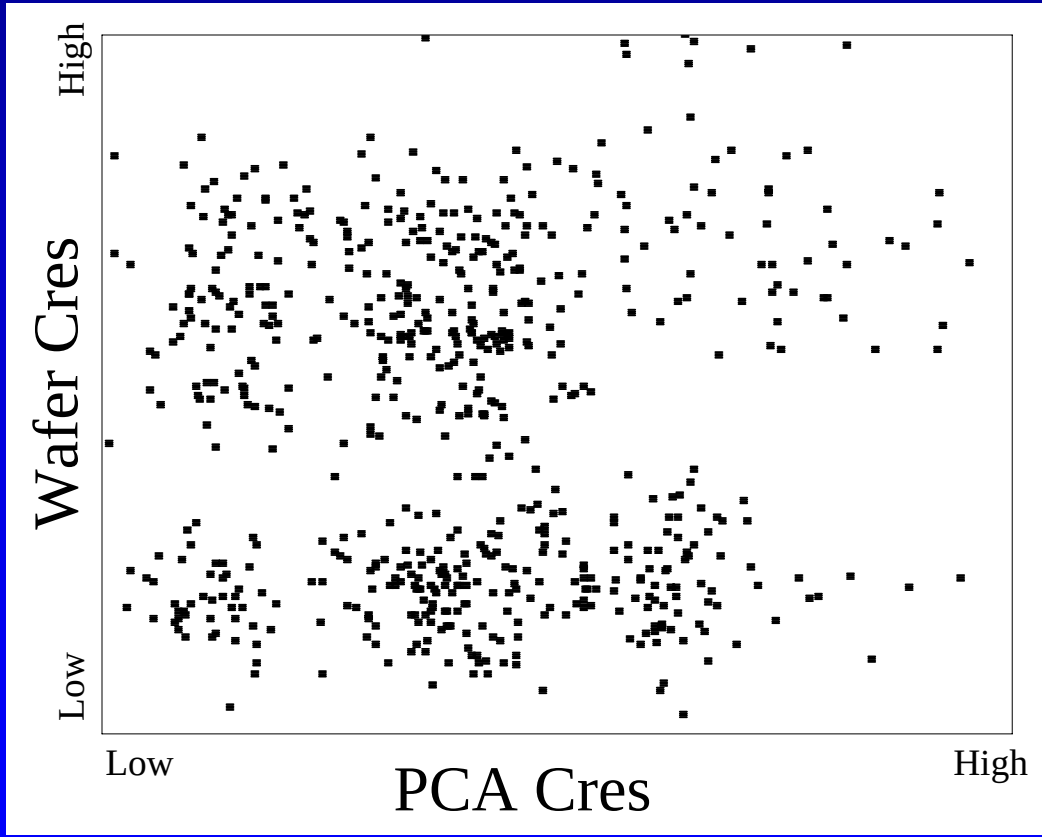
No direct correlation identified



Direct Correlation Model

Correlation map of wafer Cres vs. metrology Cres. Data collected from multiple samples.

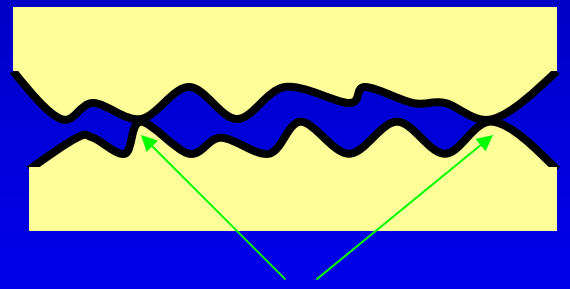
No direct correlation identified.



Why No Direct Correlation?

Contact Model

- Contact resistance is governed by A-spots which are random
- Total area of A-spots depends on force, material properties, contact motion and surface condition
- Testing environment also affects Cres

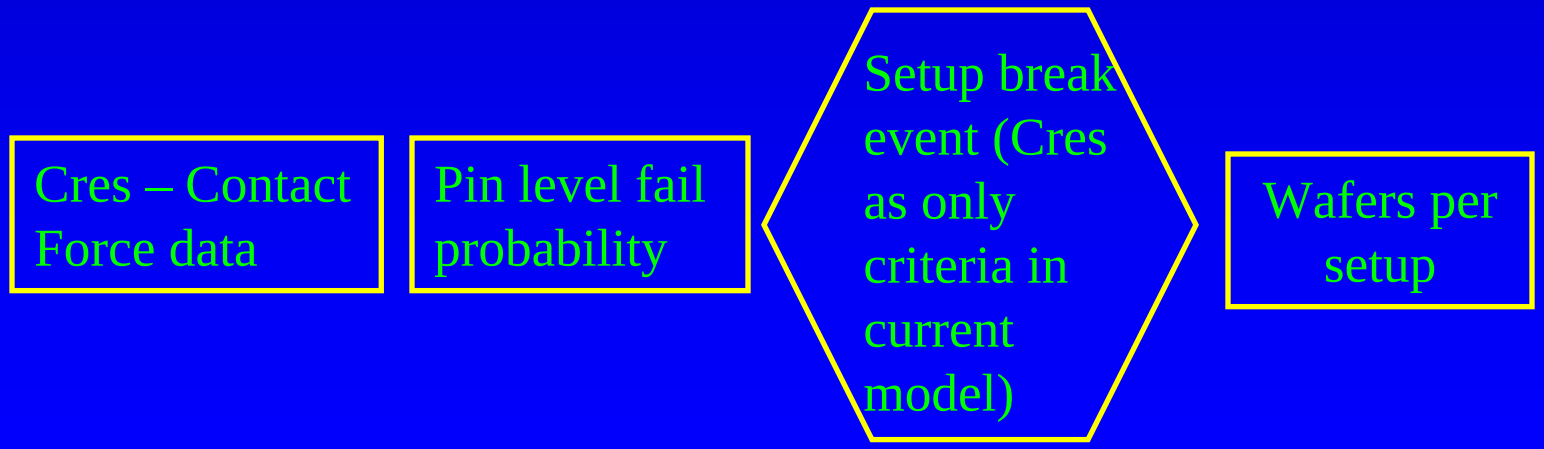


Why No Direct Correlation?

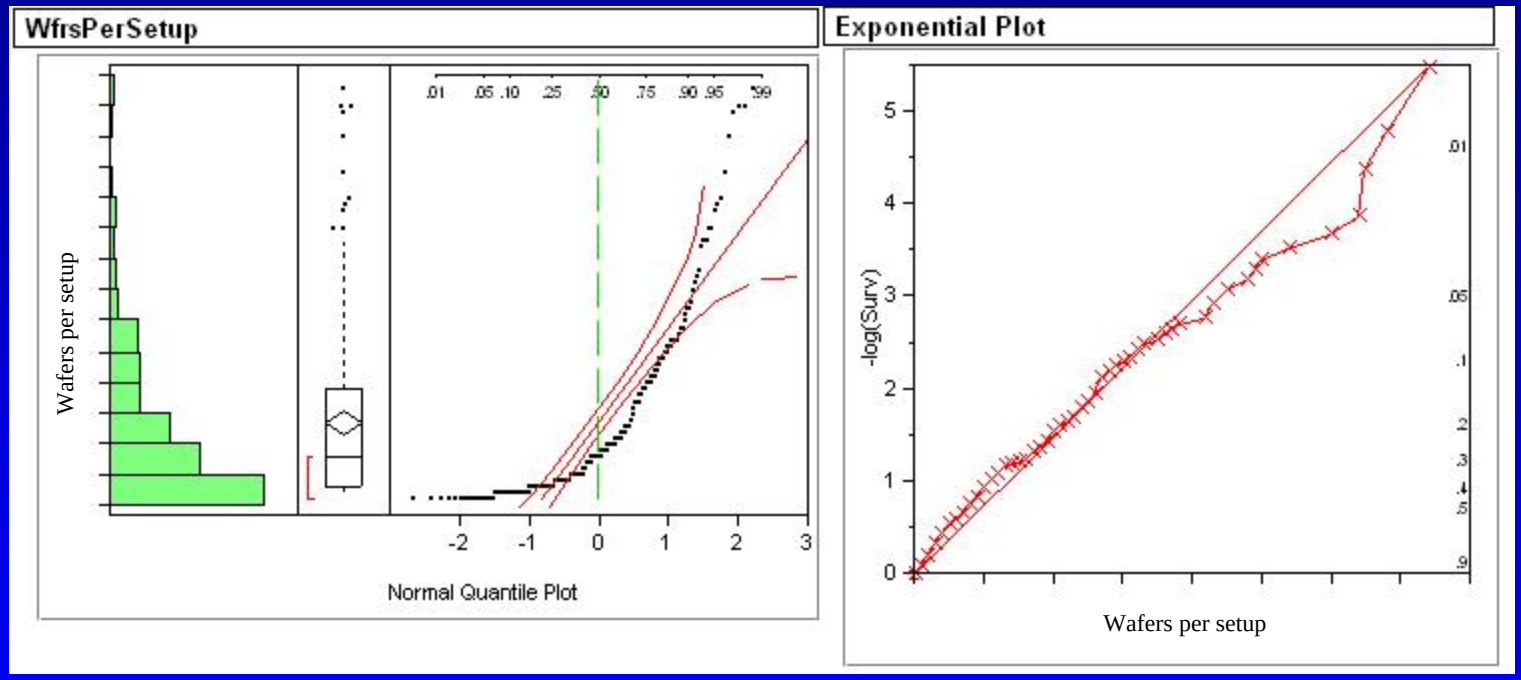
- The contact performance is determined by the interface quality. Probe card manufacturers control half of this. The other half is controlled by the down stream customers
- There are real contact interface differences between the metrology tools used for quality check and the test floor environment
  - Different material properties
  - Different surface cleanliness
  - Different topography
  - Different contact motion

Proposed Correlation Model

- In a run-to-fail model, wafers per setup (WPS) is a performance indicator that counts wafers from fail-to-fail
- If a simple probability model can describe WPS, we are able to correlate the model parameters to pin level fail probability that can be extracted from Cres - contact force data when setup is only broken by high Cres



Wafers Per Setup Distribution



In the above population, WPS follows an exponential distribution

Wafers Per Setup Distribution

- Exponential distribution:

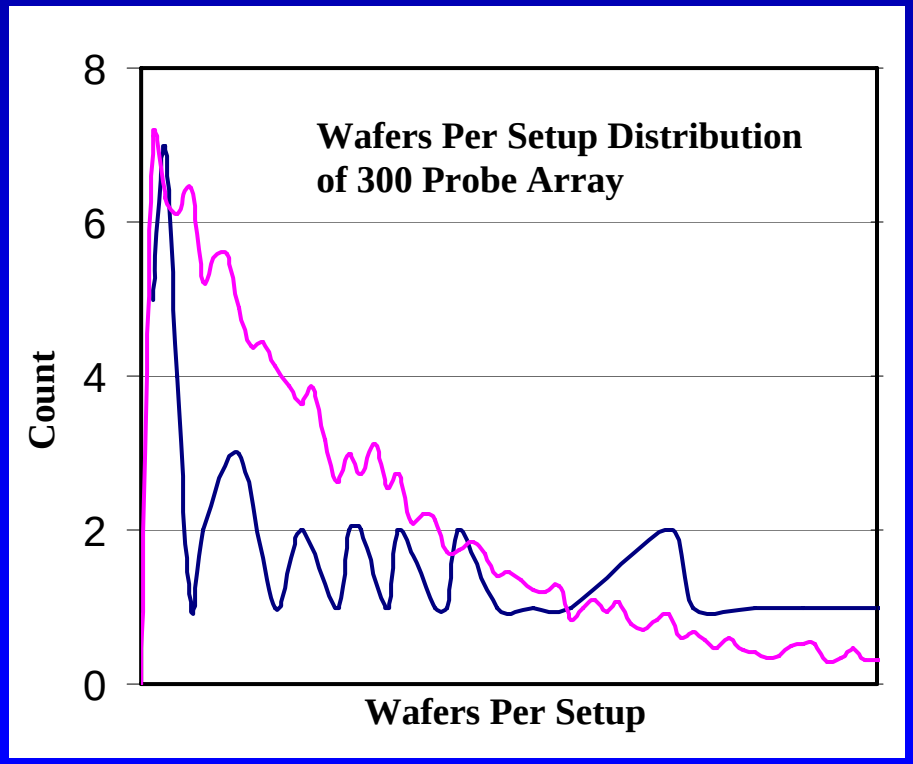
$$P(t) = \lambda e^{-\lambda t}$$

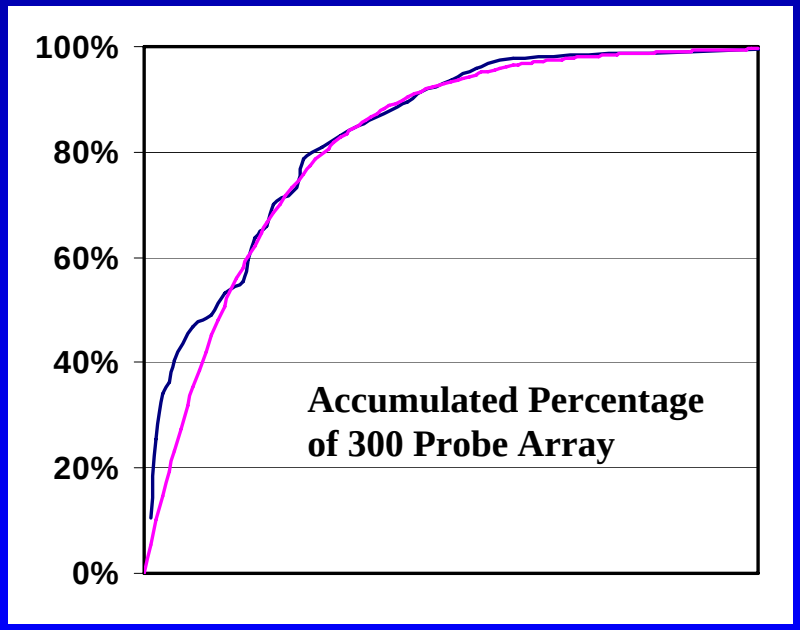
  where, λ is the only characteristic parameter determining the distribution
- The wafer sorting process can be simulated as a Poisson process which can be easily programmed

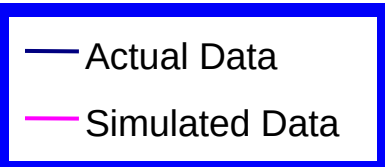
Poisson process		Wafer Testing
Event	⟷	Setup fail
Waiting time	⟷	Wafers per setup

Validation

- To validate the simulation, a probe card is populated with a 300 IO probe array
- The wafers per setup data were simulated and the pin level probability of setup fails was extracted.

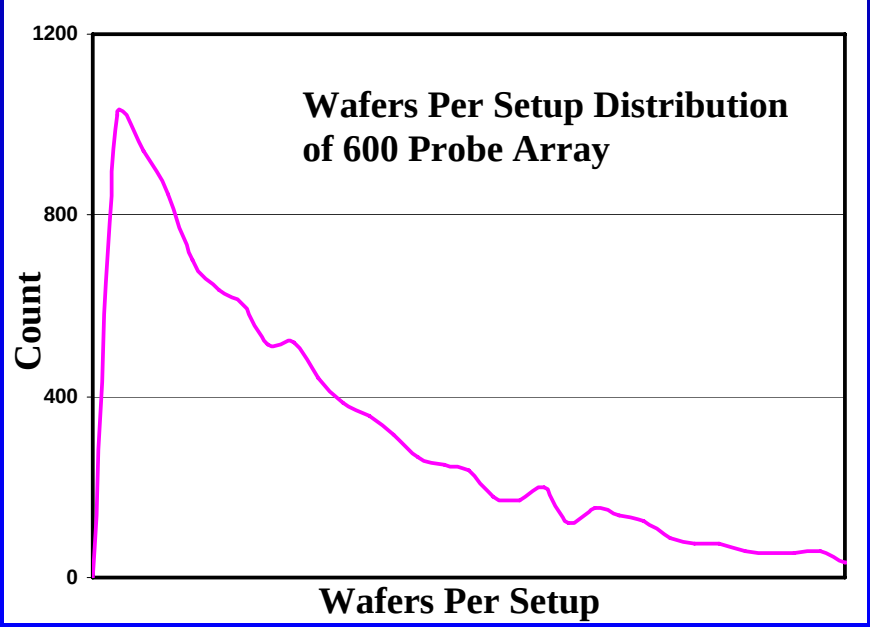


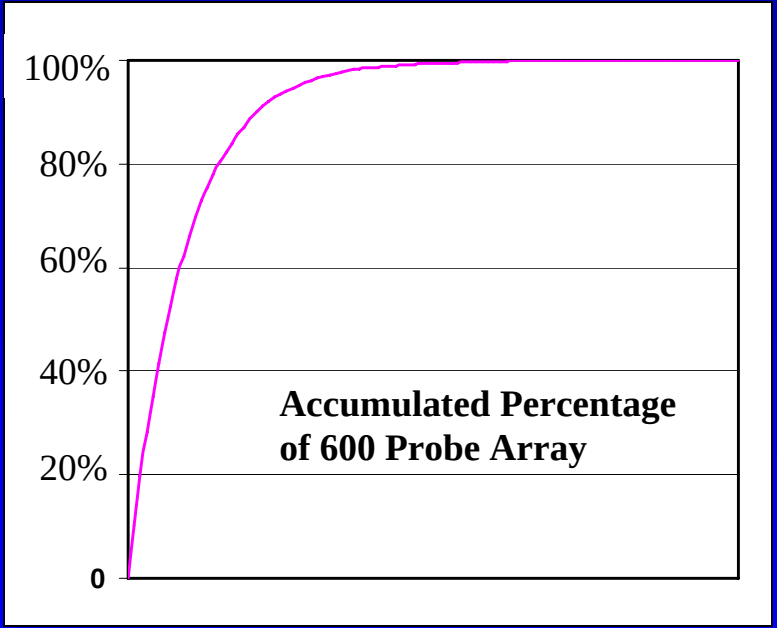




Validation

- The same probe card is then populated with a 600 IO probe array
- Applying the pin level probability extracted from the previous experiment to the model, we simulate the new wafers per setup distribution

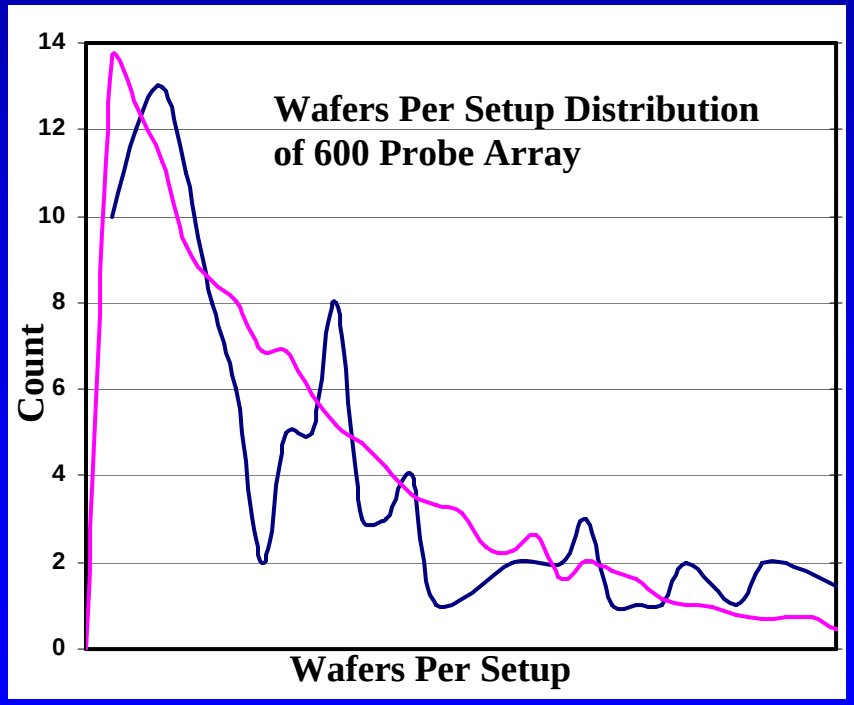


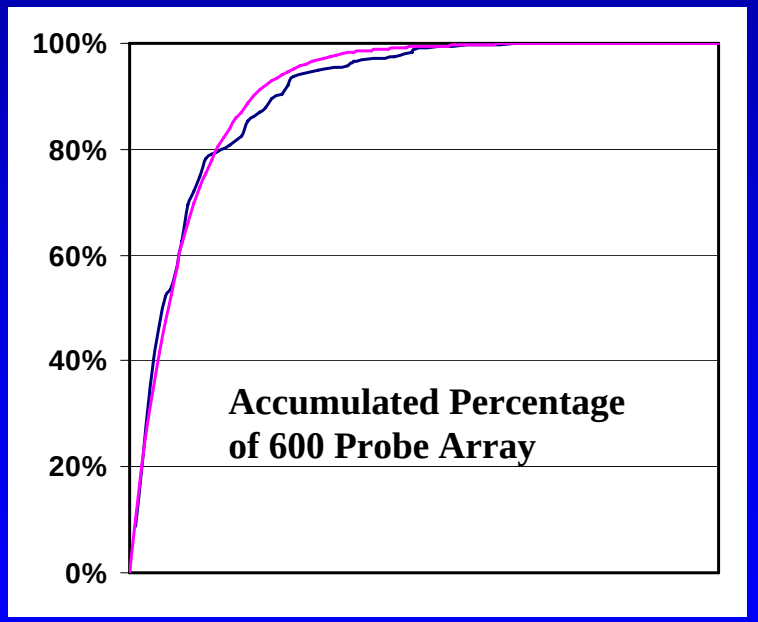


Simulated Data

Validation

- The probe cards are then released to the field.
- Actual wafers per setup data match very well with the simulation results



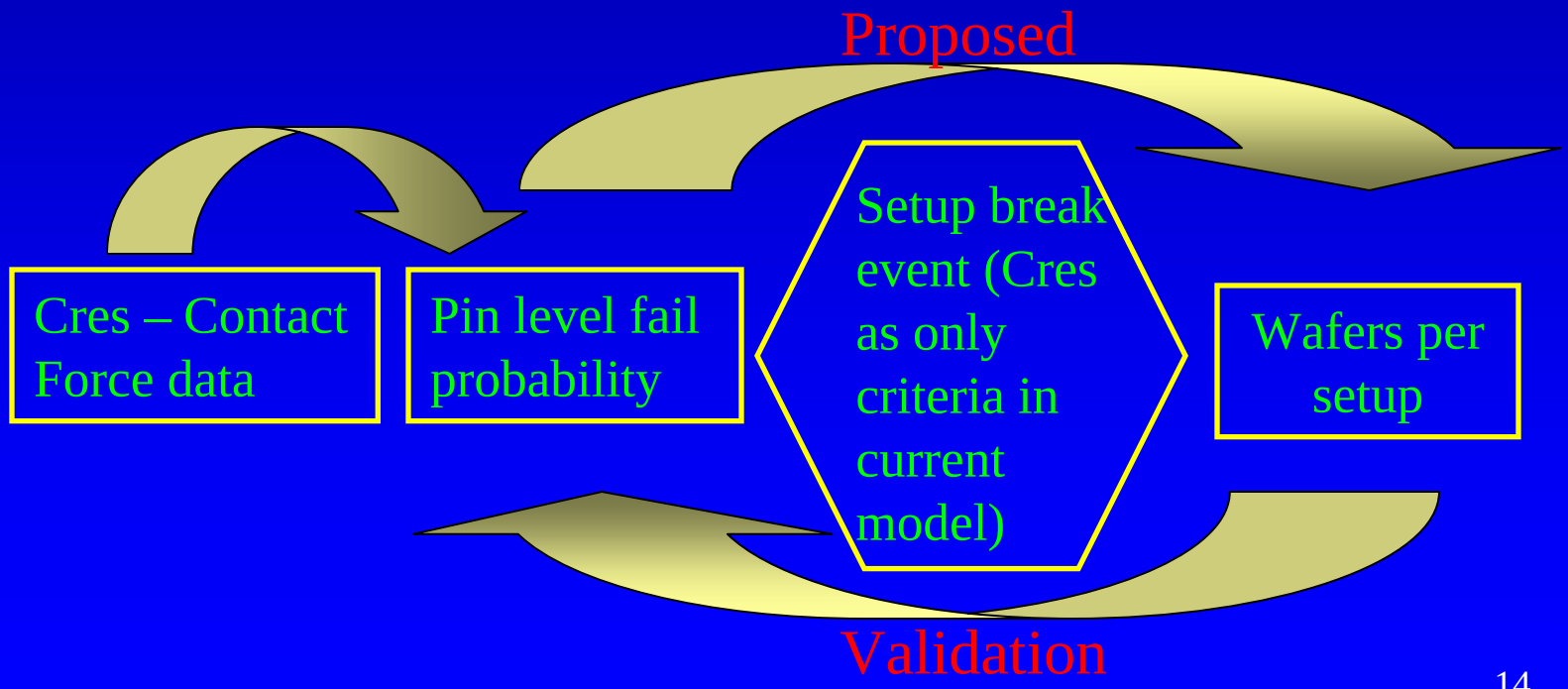


Actual Data

Simulated Data

Proposed Correlation Model

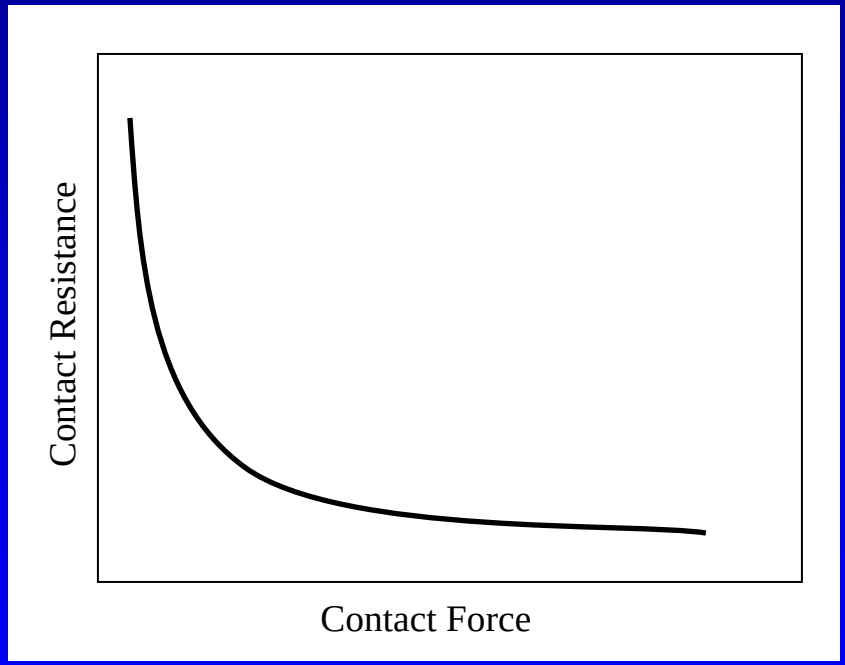
When the floor test data is not available for extracting pin level probability, Cres- contact force data can be collected for estimating the pin level probability.



Pin Level Probability

Calculation Method

- Test probe cards using a medium as close to field conditions as possible
- Collect a statistically significant amount of data
- Extract pin level Cres fail probability



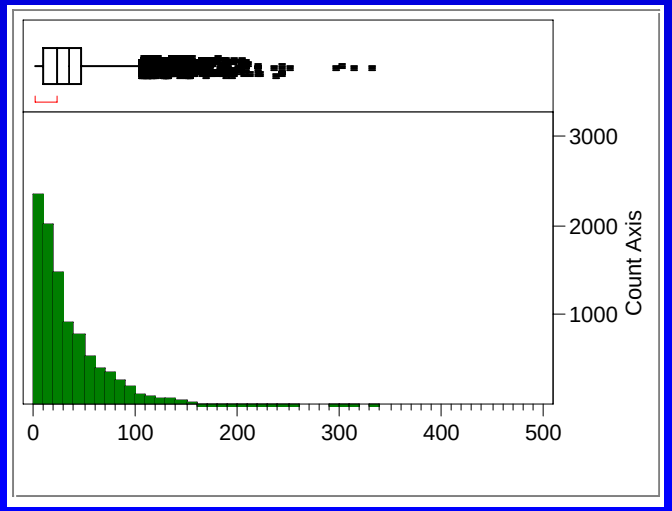
Simulation

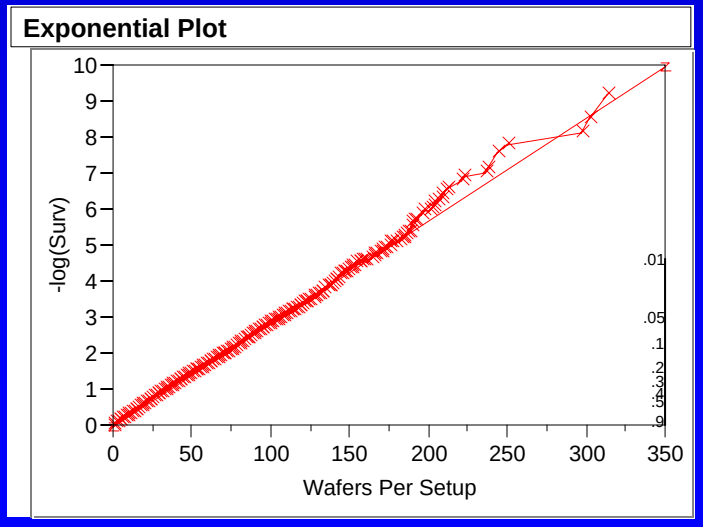
Assumptions:

- 300 IO
- 400 die/wafer
- Cres fail at >10 Ohm
- Setup fails at >5 occurrence high Cres fail

Simulation Results:

- Average wafers per setup: 35





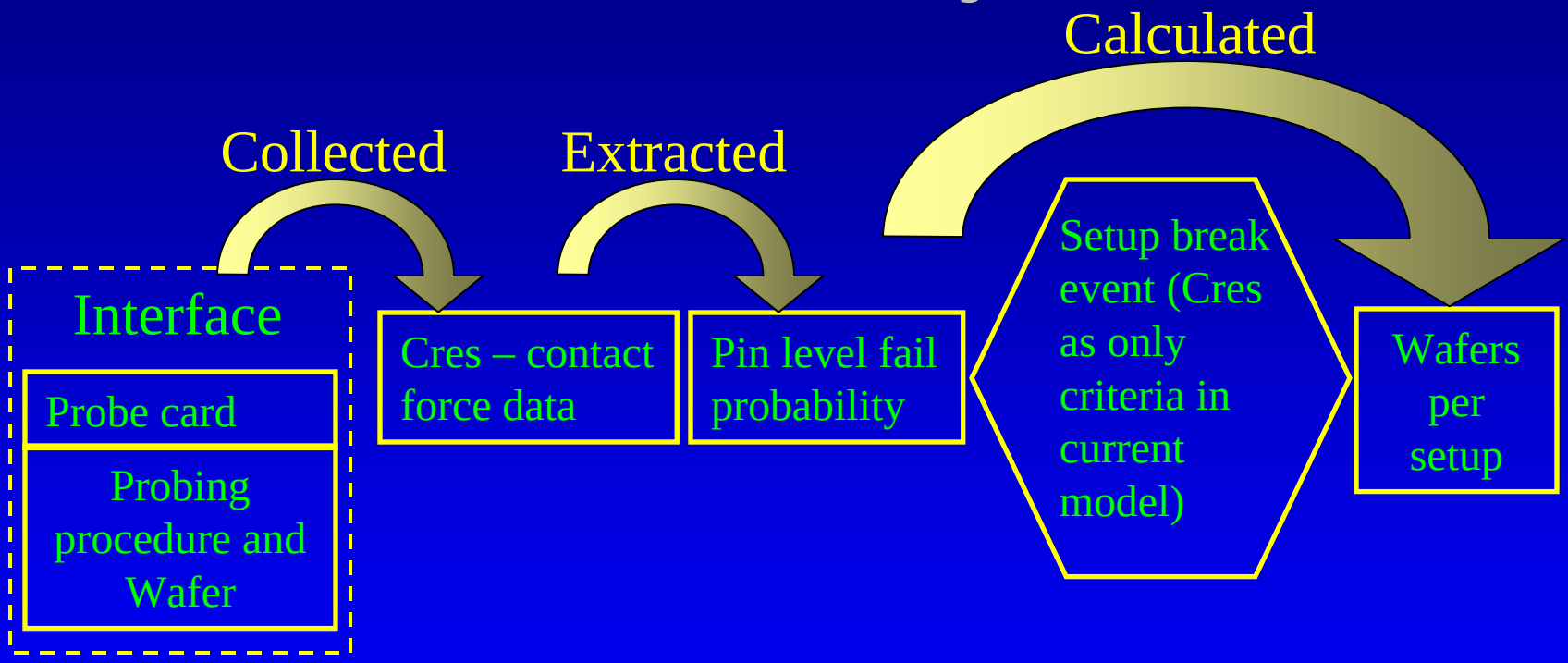
Limitation of the Current Model

- The model assumes each high Cres fail event is independent. In the reality, one fail may impact the probability for next fail
- The model treats every pin statistically equal. In reality, they are different, depending on components, geographical location, etc
- The model assumes a constant probability across a probe card lifetime. In reality, the probability increases as a function of life
- The model does not include intentional interference during the process, such as in process assistance
- This research is based on single product line. We do not have enough data to tell how widely exponential distribution can be applied to other products.

Next Step

- Extend the model to accommodate variable probability
- Study what sample size is needed for WPS estimation
- Add cost model to the simulation to evaluate the cost benefit relationship

Summary



- Demonstrated a simulation method to correlate the pin level probability to wafers per setup
- The pin level probability can be extracted from Cres – contact force data
- There are limitations on the current model. We will add more functionality at next step