

Methodology of Stable Probe Card Power Path Design for Wafer Level Testing

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Agenda

- ▣ Example of Instability
- ▣ Instability in Probe Card Power Path
- ▣ Concept of Stability Analysis
- ▣ Stability Indicator Tool
- ▣ Performance of Closed Loop System
- ▣ Conclusion & Acknowledgement

Instability – An Example

- ▣ Consider an automatic control system such as the stabilizer on a ship
 - ⦿ In the even of a roll the stabilizer change angle to correct it
 - ⦿ Suppose due to the delay in the response system, by the time the stabilizer responded the ship has already corrected the roll
 - ⦿ The stabilizer will now be in the wrong position and roll the ship further in the wrong way
 - ⦿ If this continues, rolling will go out of control and eventually the ship will sink. **Effect of instability.**

Instability – An Example



Stable Operation – Happy Cruise

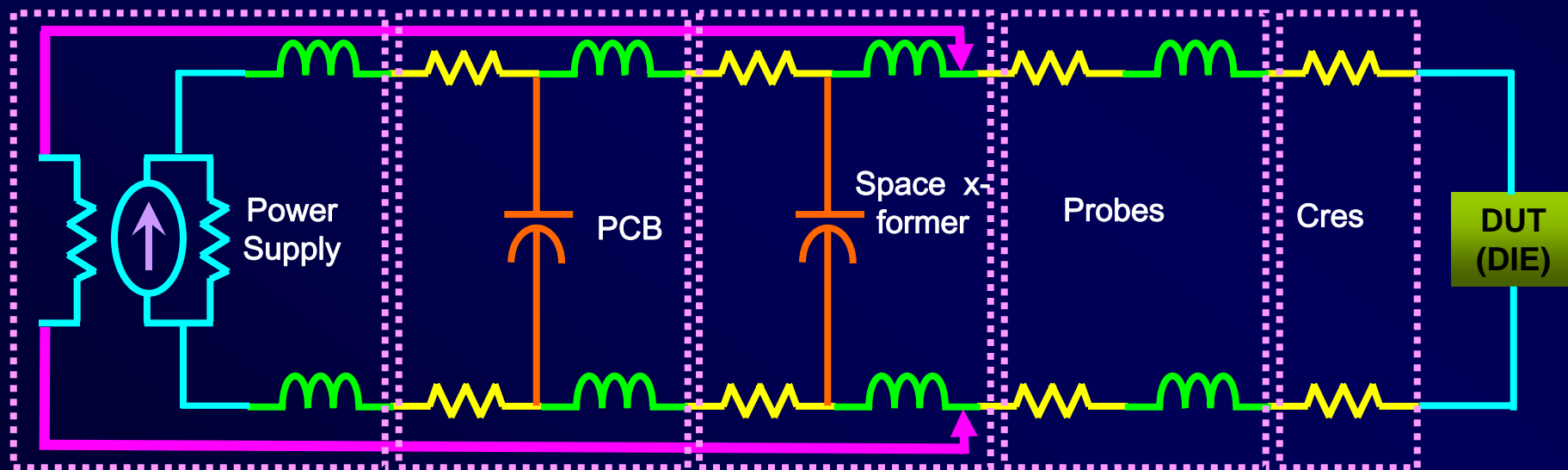
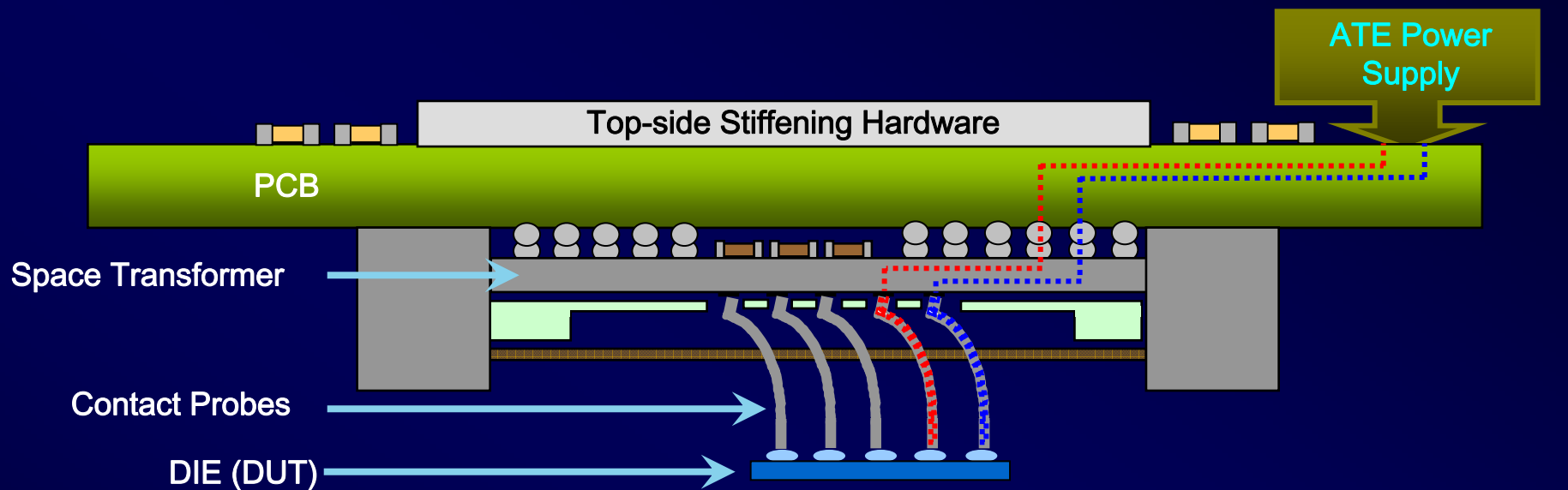
Learning: Design your system as stable as possible. Or pay the consequences.

Instability can make any system go out of control and eventually destroy the system

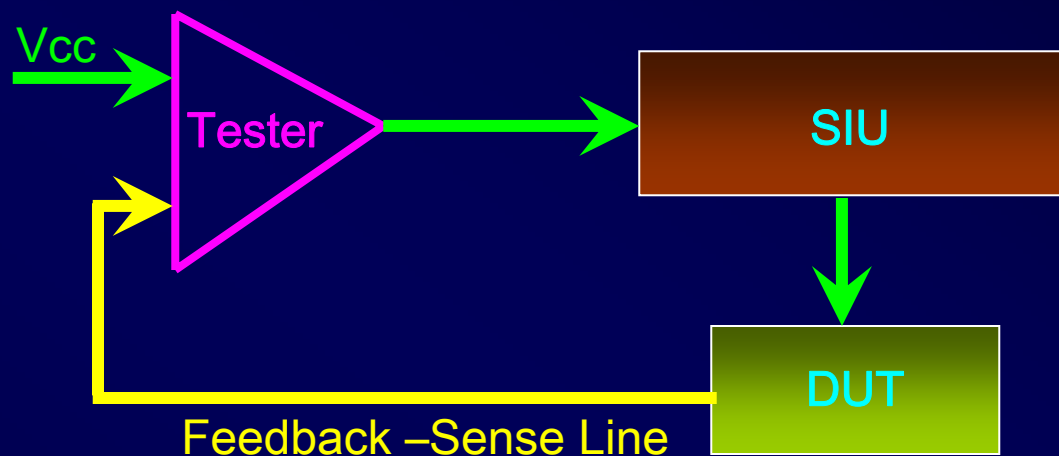


Instable Operation –??

Probe Card Power Path

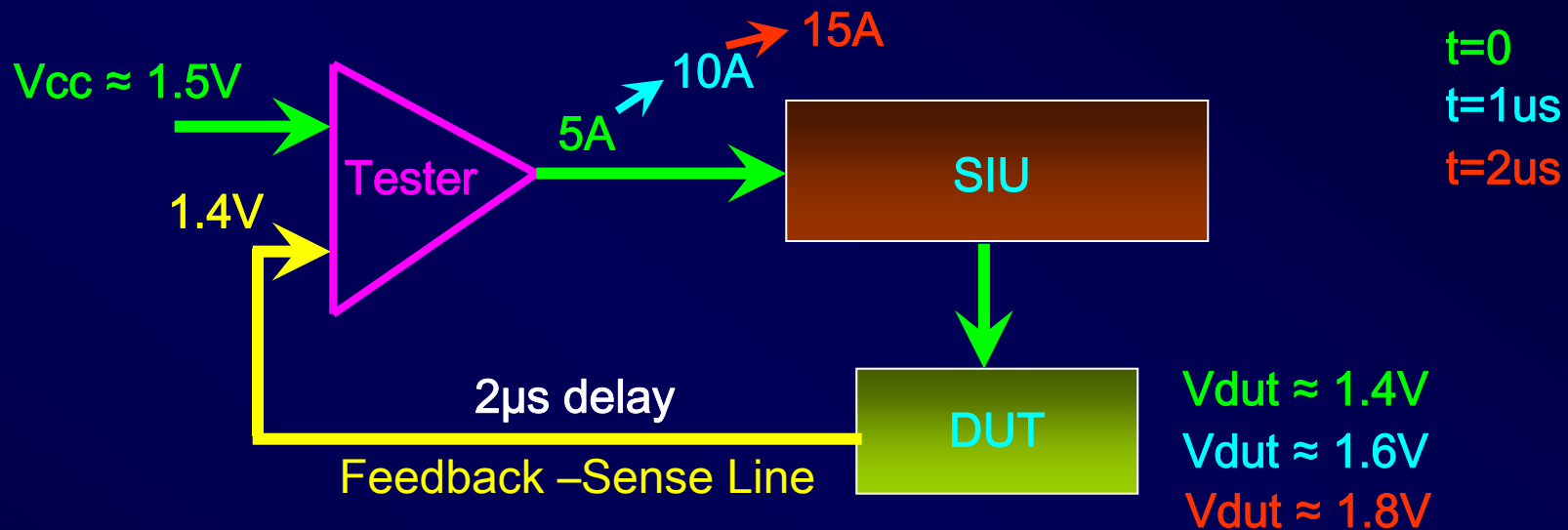


Probe Card Power Path



- ☐ ATE power supply constantly sense the DUT voltage
 - ⦿ If DUT voltage is smaller than V_{cc} , ATE injects more current until the DUT voltage is V_{cc}
- ☐ Probe card power path constitute a Closed Loop System
- ☐ Response time of ATE power supplies are fast ($\approx 1\mu s$)

Probe Card Power Path Stability



☐ At $t=0$

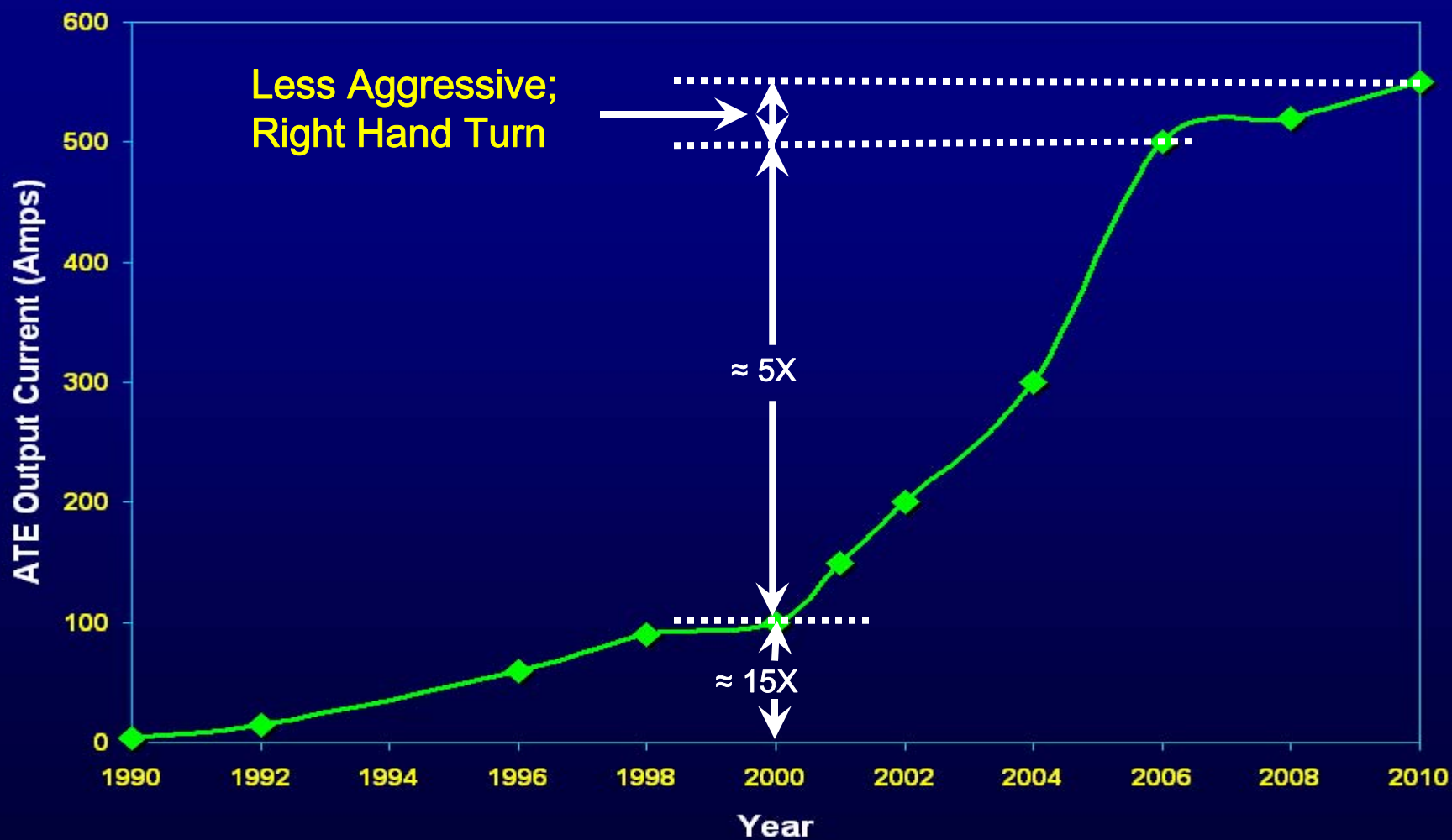
⦿ ATE sense $1.4V$ at

☐ Suppose there is $2\mu s$ delay in sense line

⦿ ATE will inject more and more current for next $2\mu s$

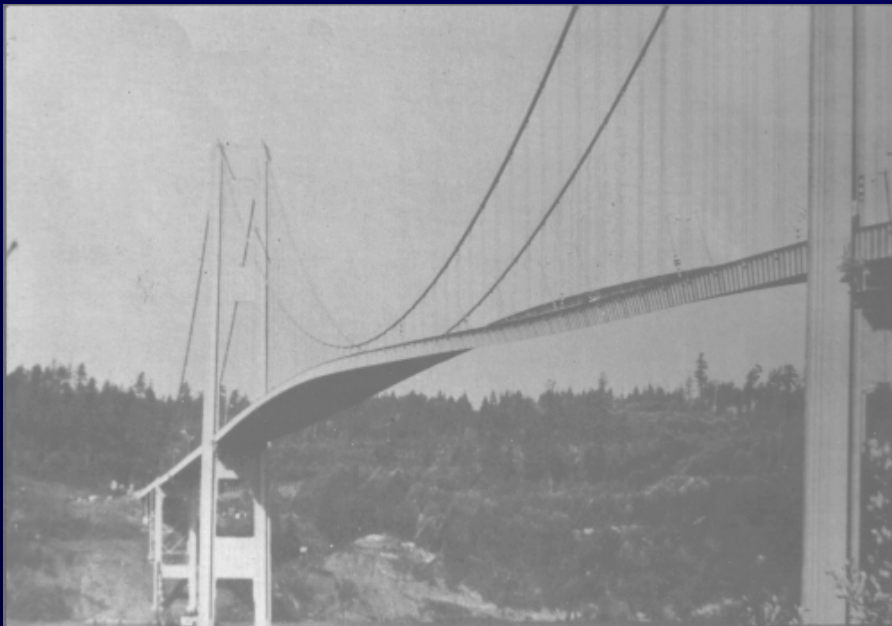
The Problem

▣ Trend of ATE power supply output current with time



The Problem

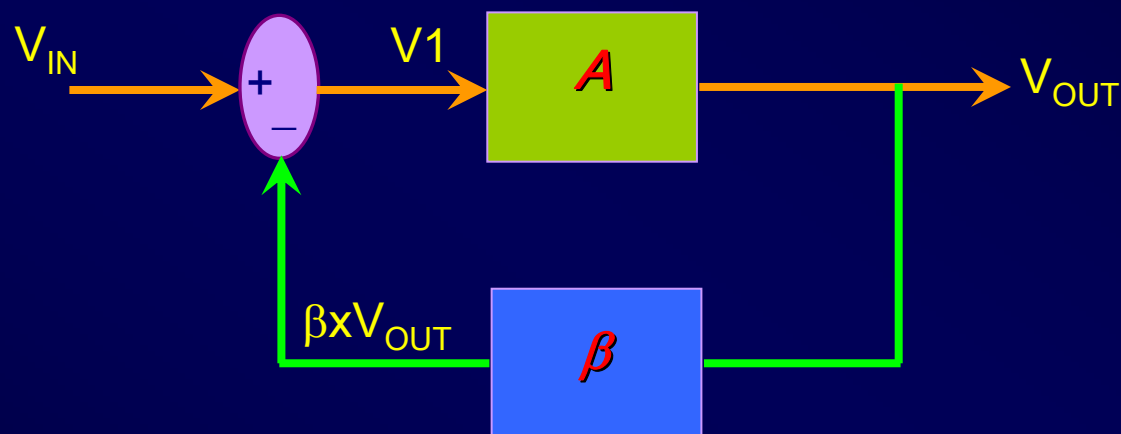
- ▣ Higher power and fast response time causes the power supplies to be inherently less stable
- ▣ Instability can lead to
 - ⦿ Huge current surge and uncontrolled large voltage swings (Oscillation) on the power supply output



Probe Card Design Consideration

- ▣ Design a stable system with out compromising performance
- ▣ Power supply cannot protect against stability by itself
- ▣ It requires an optimum design of the rest of the power path, or more specifically, of the test interface board (Probe Card)

Concept of Closed Loop System

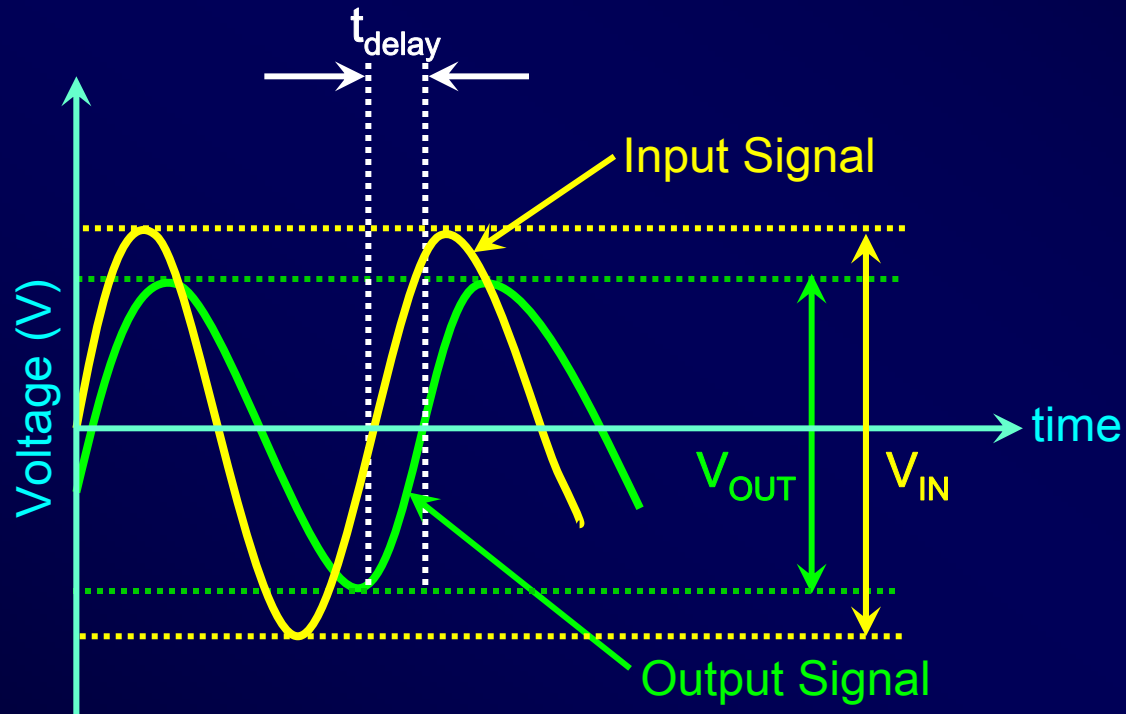


$$V_{OUT} = A \times (V_{IN} - \beta \times V_{OUT})$$

$$\text{Gain} = \frac{V_{OUT}}{V_{IN}} = \frac{A}{1 + A\beta}$$

- ☐ $1 + A\beta > 1$ (Negative Feedback)
 - ⦿ System is stable (gain < A)
- ☐ $1 + A\beta < 1$ (Positive Feedback)
 - ⦿ System is unstable (gain > A)
- ☐ Computing A and β for a complex circuit is very hard
- ☐ Easier to work with voltages (V_{IN} , V_{OUT}) in real life

Stability Indicator Tool

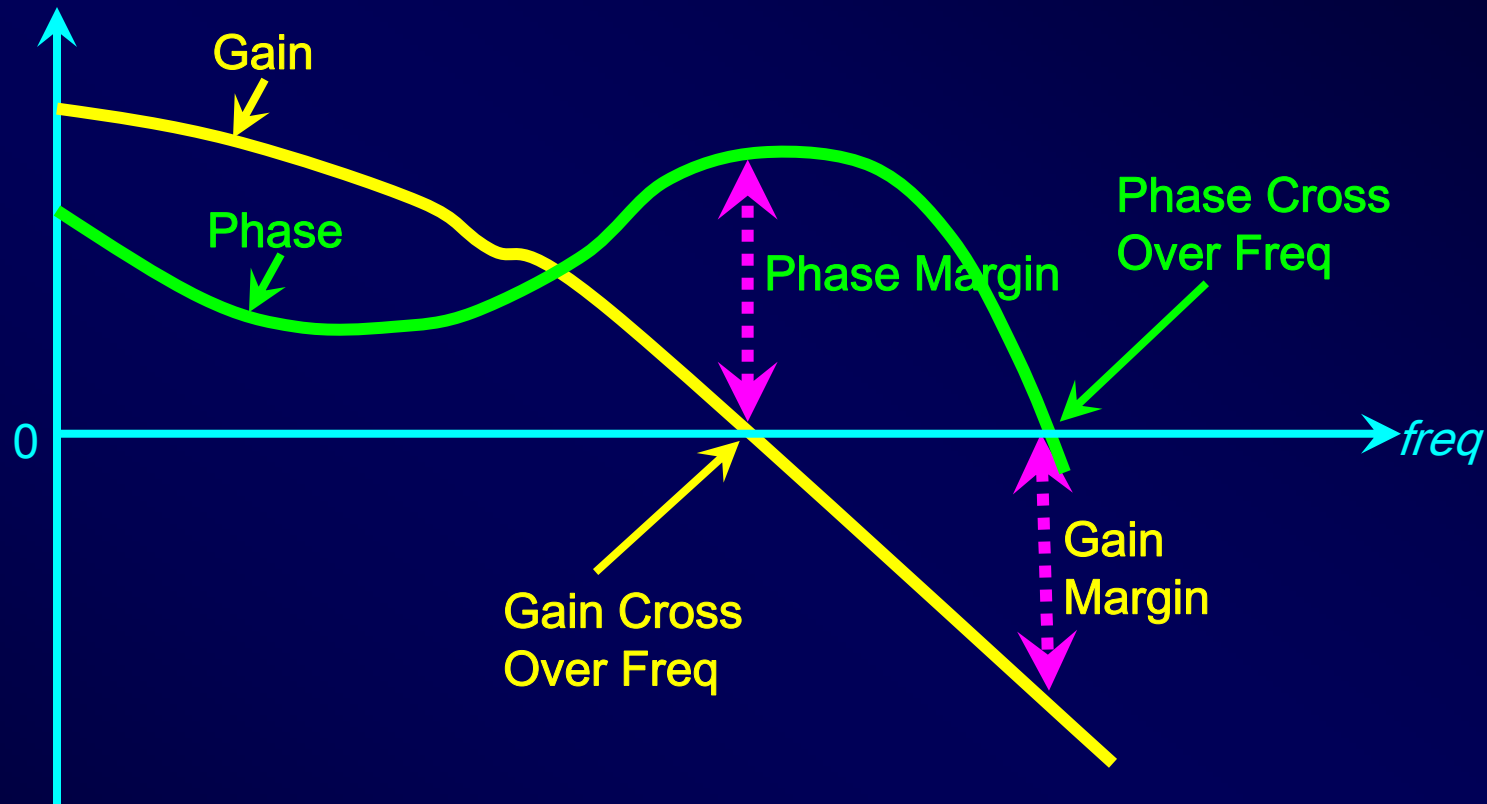


$$\text{Gain} = 20 \times \log_{10} \frac{V_{OUT}}{V_{IN}}, \text{dB}$$

$$\text{Phase} = t_{delay} \times \text{freq} \times 360^\circ$$

- ▣ Bode Plot: Plot of gain and phase of a closed loop system
 - ⦿ Powerful tool for ensuring stability

Bode Stability Criterion



☐ For a closed loop system to be stable

- ☉ The gain should be below zero dB at phase cross over freq
- ☉ The phase should be above zero deg at gain cross over freq

Performance Indicator

- ▣ Two fundamental characteristics of a closed loop system are *Responsiveness* and *Stability*
- ▣ Responsiveness is the transient response of the system
- ▣ Stability measures the quality of that response
- ▣ For optimum design both transient and stability requirements need to be met

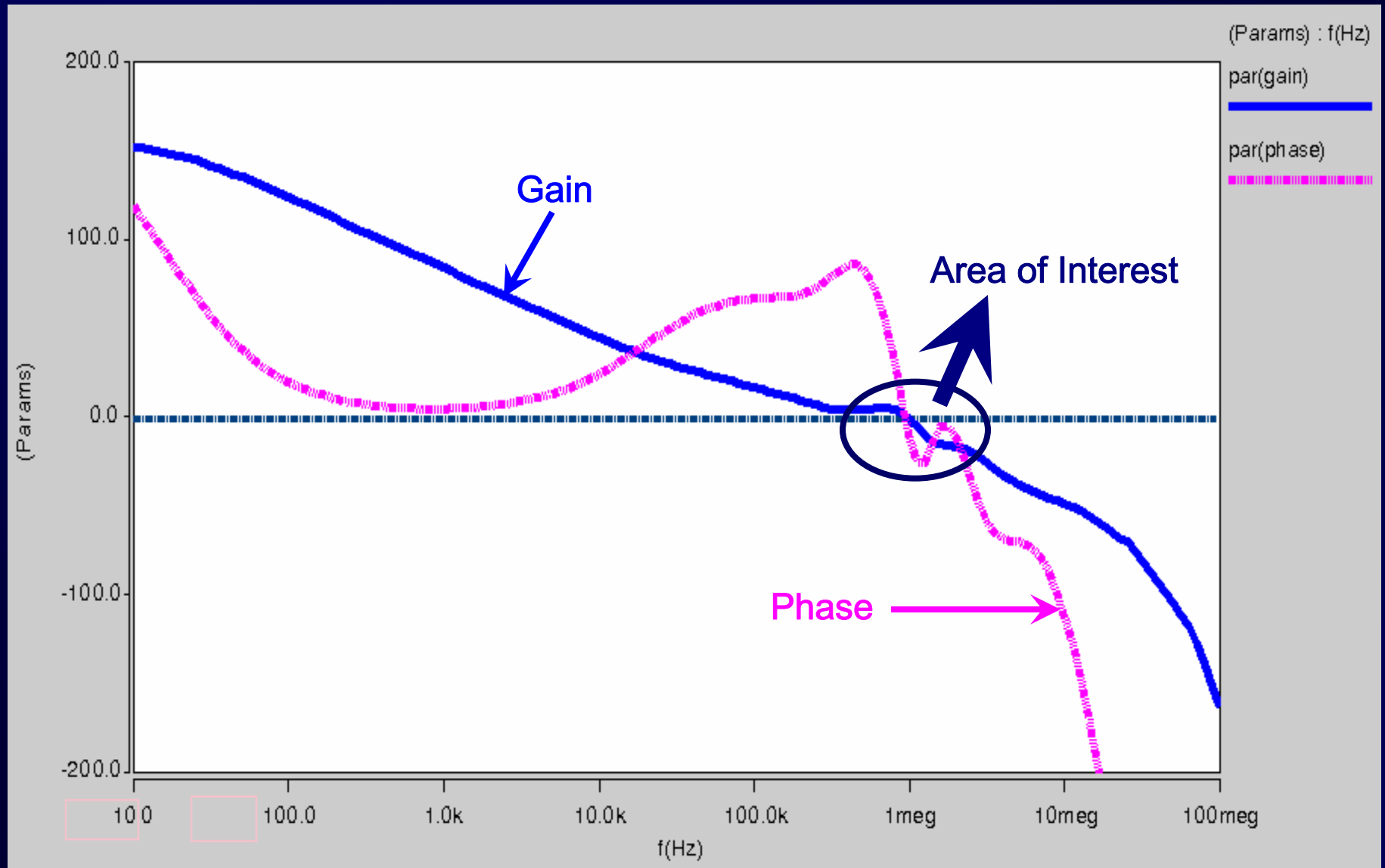
Simulated Results

- ▣ Stability analysis has been performed on a Intel Chipset Product

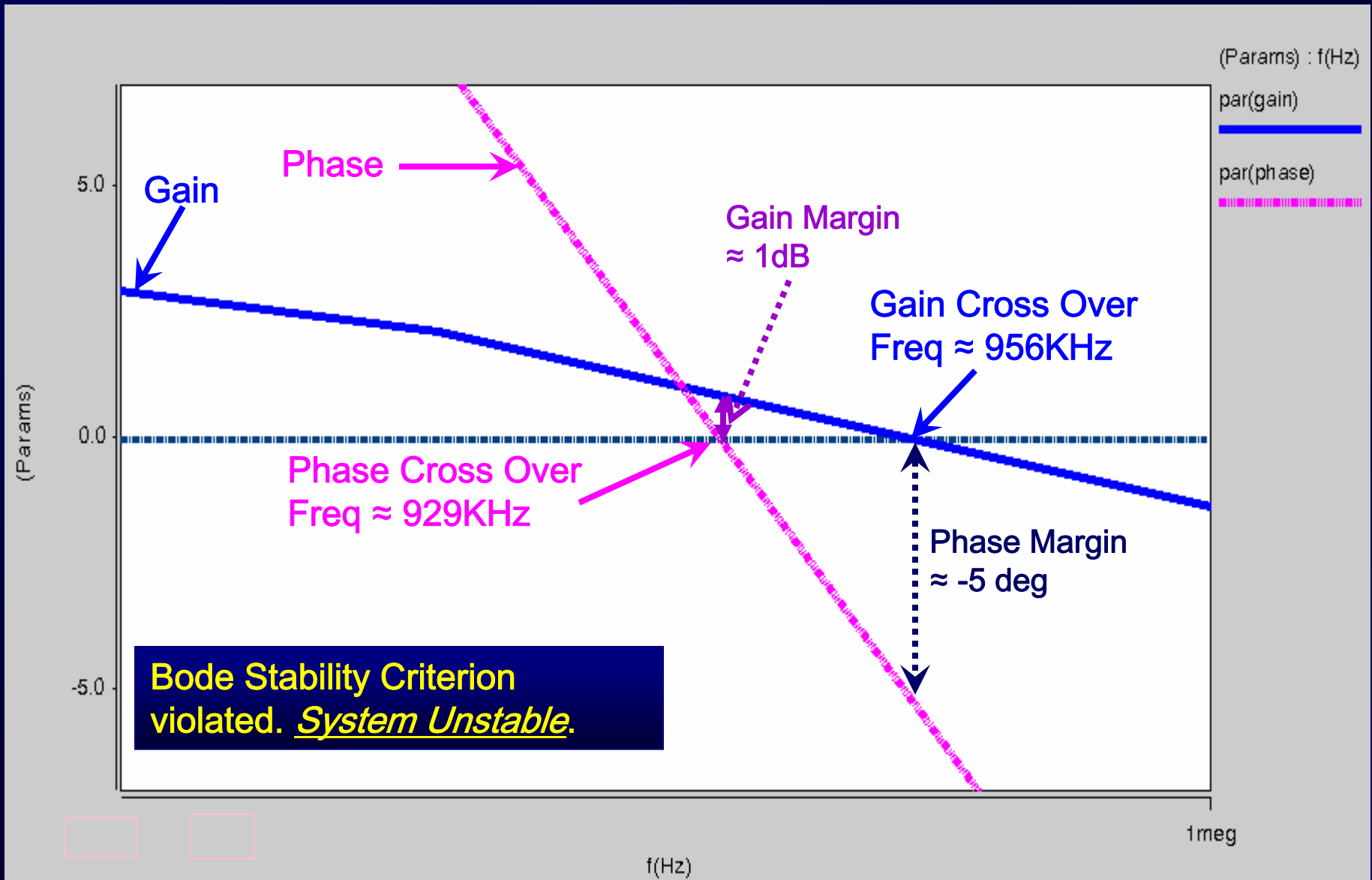
- ▣ Simulations have been performed for the following two decoupling schemes
 - ⦿ Option 1: 2x2.2uF (ST) + 1x10uF (PCB) + 1x100uF (PCB)
 - ⦿ Option 2: 2x2.2uF (ST) + 2x10uF (PCB) + 3x100uF (PCB)

- ▣ Results have been validated with actual measurement

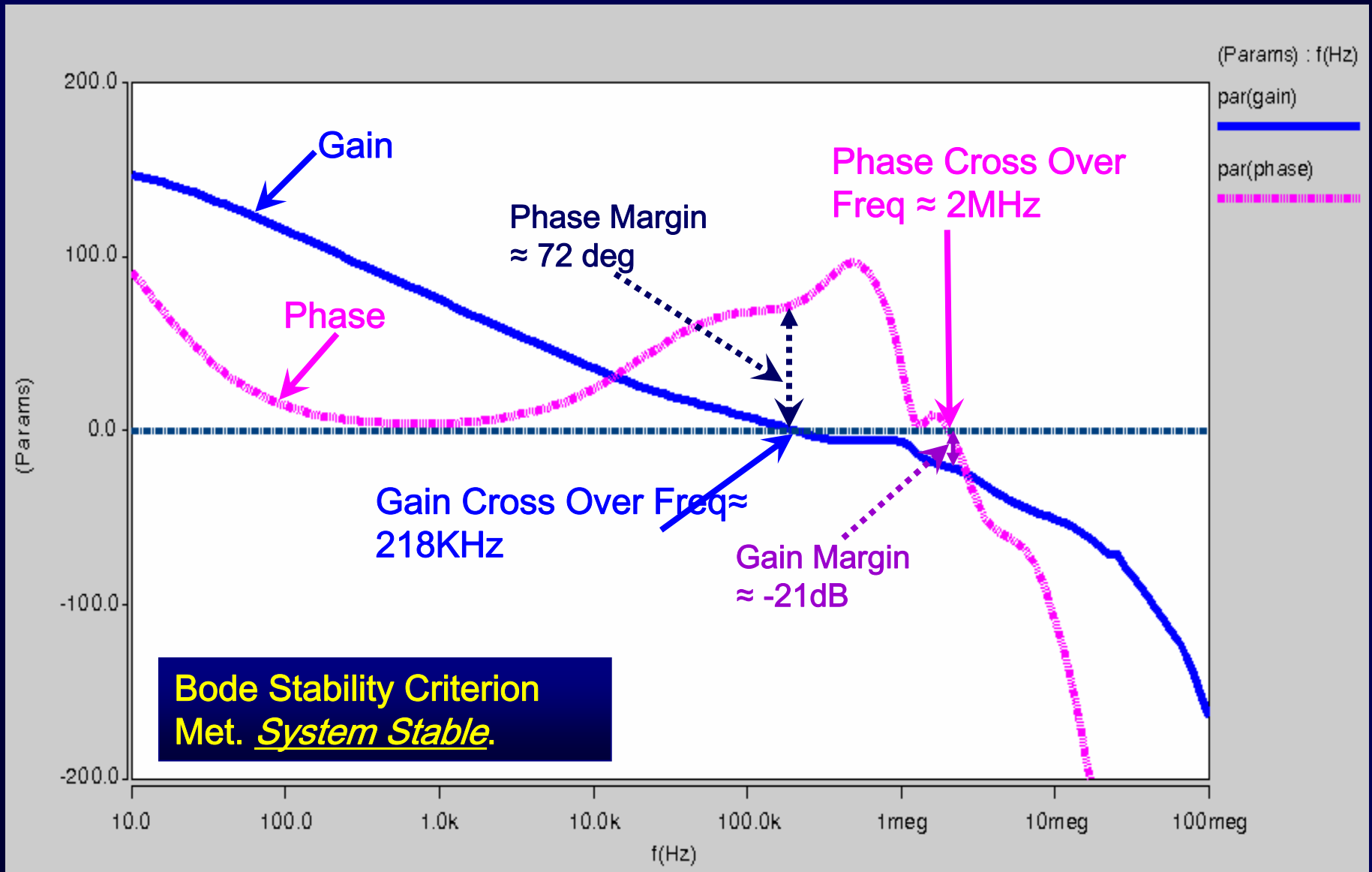
Bode Plot - Option 1



Bode Plot – Option 1



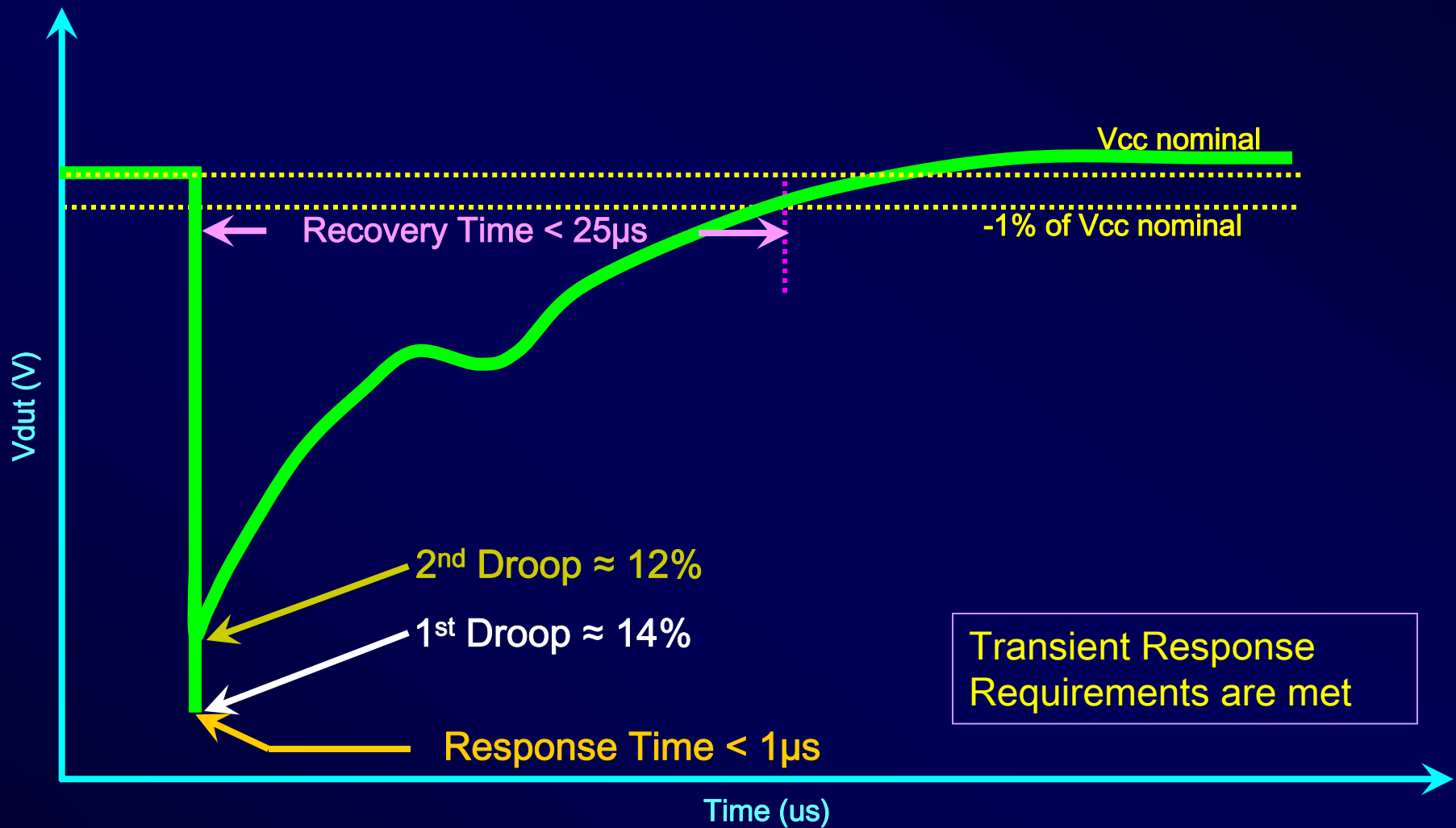
Bode Plot – Option2



Responsiveness

- ▣ Transient analysis is performed to meet the voltage droop, response and recovery time requirements
- ▣ Transient requirements are
 - ⦿ Voltage droop \leq Allowable voltage droop target
 - ⦿ Response time $\leq 1 \text{ us}$
 - ⦿ Recovery time $\leq 25 \text{ us}$
 - ⦿ Overshoot $\leq 50\text{mV}$
- ▣ Response Time
 - ⦿ Time difference between the start of voltage droop to the minimum of voltage droop
- ▣ Recovery Time
 - ⦿ Time difference between the start of voltage droop to the voltage when it reaches to -1% of V_{cc} nominal after the minimum droop

Transient Response – Option2



Conclusion

- ▣ Tester (ATE) power supply instability is a significant problem in tooling power path design

- ▣ Stable power path can be designed following power supply decoupling guide line

- ▣ However for an optimum design it requires to perform both stability and transient analysis
 - ⦿ Particularly true if active components are introduced in probe card

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