High Current Wafer Probing Solution

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The Problem

- Testing moving from packaged parts to wafer level or bare die level
- Drivers for this
  - Known Good Die (KGD)
  - Bumped Die
  - Chip on Board
- Probe technologies have been developed to address test speeds, high pin counts, high parallelism
- No technology available for high current probing

Background Information - 1

- Since late 1980's ITC has been the leading supplier of Dynamic "surge" test systems to the Power MOSFET and IGBT mfr's.
- Volume test is the Unclamped Inductive Switching (UIS) test
- Until recently this has been a ruggedness test at the package level

Background Information - 2

- New market drivers have seen increase in UIS test volume
  - Automotive
  - Power management – Portable electronics, laptops, PC's
- Many of these applications require on wafer or bare die test in some cases up to 200A

Background Information - 3

- Present approach
  - Spread the current through multiple probes, hope the contact is good enough with sufficient probe redundancy
  - Run test at lower current – not very informative
  - As probes lose contact the good probes carry increasing current

Background Information - 4

- As a manufacturer of both the UIS test systems and probe card analyzers ITC has a knowledge base that puts us in a unique position to address the problem

Program Goals

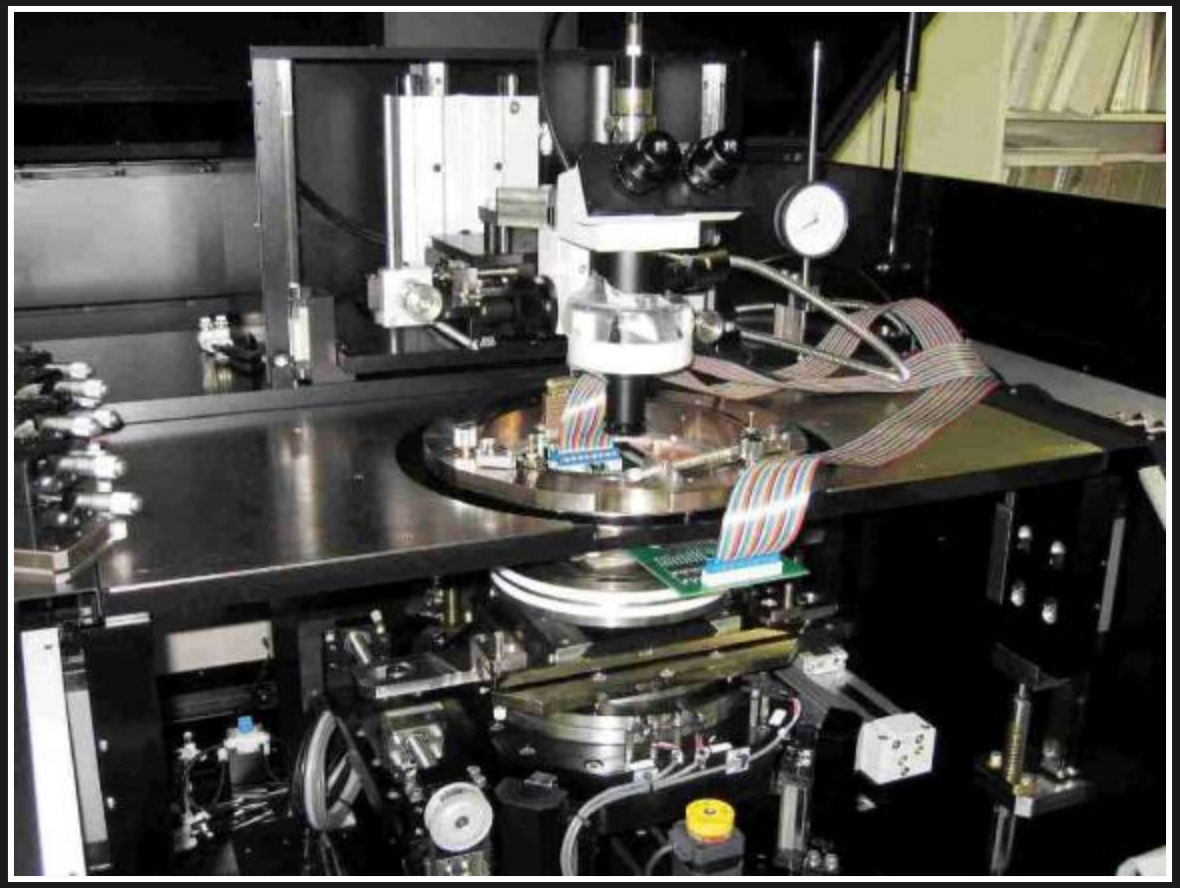
- Develop a method to control the current flowing in each probe
- Stop the probing operation if the current in an individual probe exceeds the pre-defined value
- Develop a method to measure the contact resistance of each probe to inhibit testing if there are insufficient low resistance probes available

Approach to the Solution

- Test device is a power semiconductor device requiring UIS testing at currents up to 200A at 1000V as a bare die
- Test system to be used is the ITC55100 UIS tester (200A/2500V)
- Probe card is a Celadon ceramic tile card with 111 probes
- Manual Probe station and chip holder supplied by Hisol, Japan

Complete System

Chip Probe System



Top-side of Probe Card

Bottom side of Probe Card

Celadon Probe Card Specs

Ceramic Type: 72mm Rectangle

Thickness: 3.3mm

Spacer: No

Single/Multisite Tile Design Orientation of Tile: Custom

Number of Sites: 1

Die Step X (in microns) 0.0

Die Step Y (in microns) 0.0

Probes Type: BeCu

Radius of Tip(mm): Flat 2.5mil

Beam Length(mm): Varies

Probes Per Site: 111

Probe Count: 111

Probe Card Interface Board

Typical power device layout

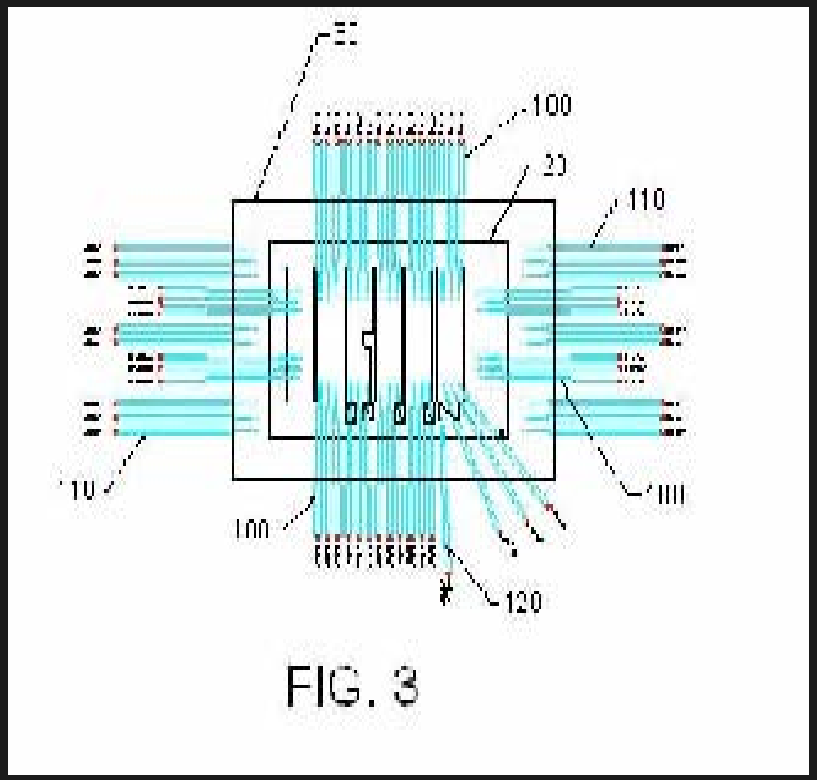


FIG. 3

- Large pads on top side are source or emitter connections
- Drain or collector connection is through back of chip
- Gate can be contacted with single probe

Device connection requirements

- Celadon card can handle a pulsed current of ~6A/probe
- Test to be run at 200A, card has been designed with 56 probes on the emitters and 40 probes touching down on the chip carrier for the collector

ITC55WPS Current Limit System

ITC55WPS Current Limit System

- System has one current limiter (CL) channel per high current probe needle
- 96 channels required, each set for maximum of 6A per probe
- 16 channels per board
- Protection of tester, probe card and DUT is key

Design Aims - Current Limiter (CL)

- Fast Response
- Low Resistance Path
- Good surge characteristics – Rugged
- No overshoot/undershoot
- Simple – potential to need lots of them in any application

System Block Diagram

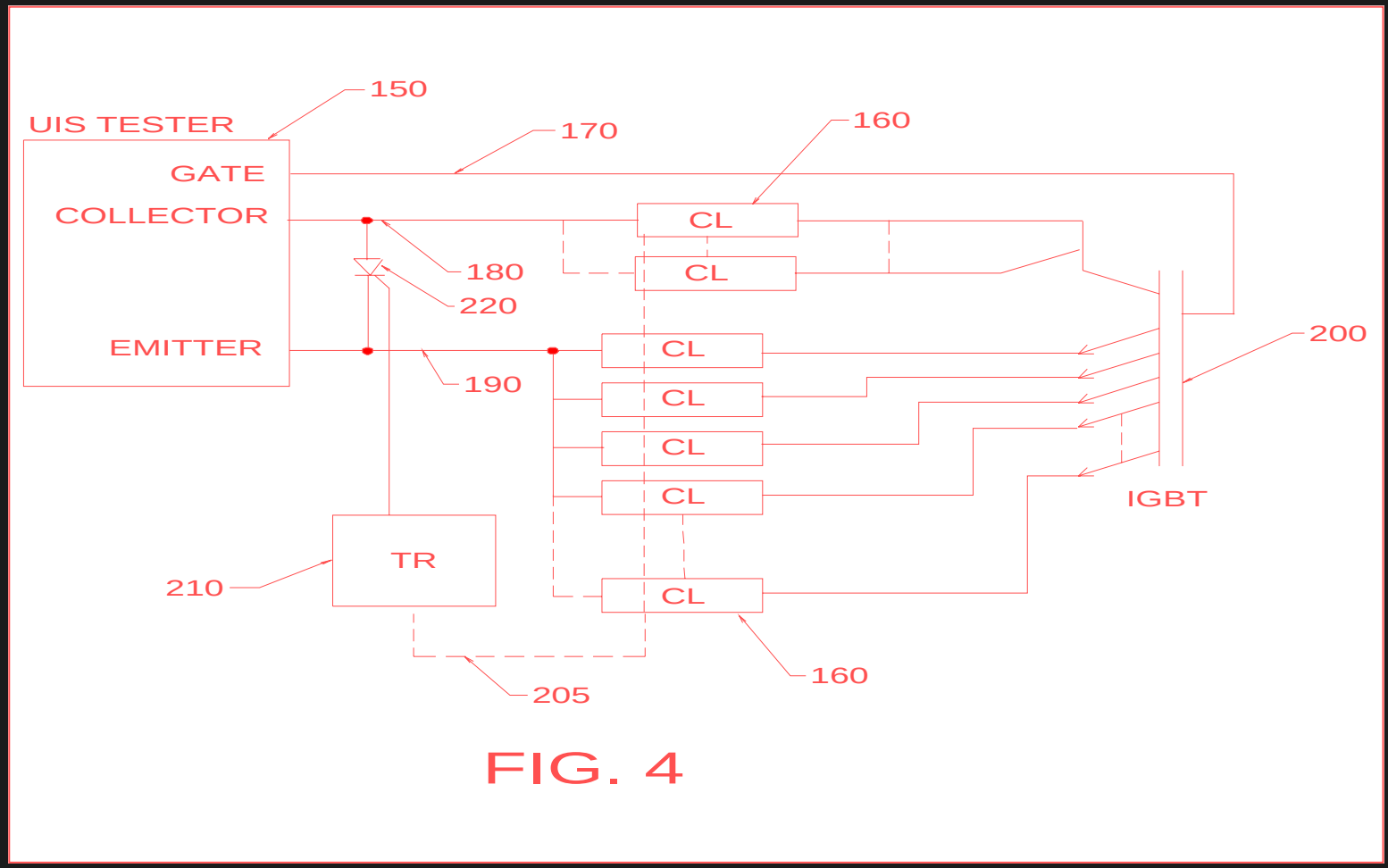


FIG. 4

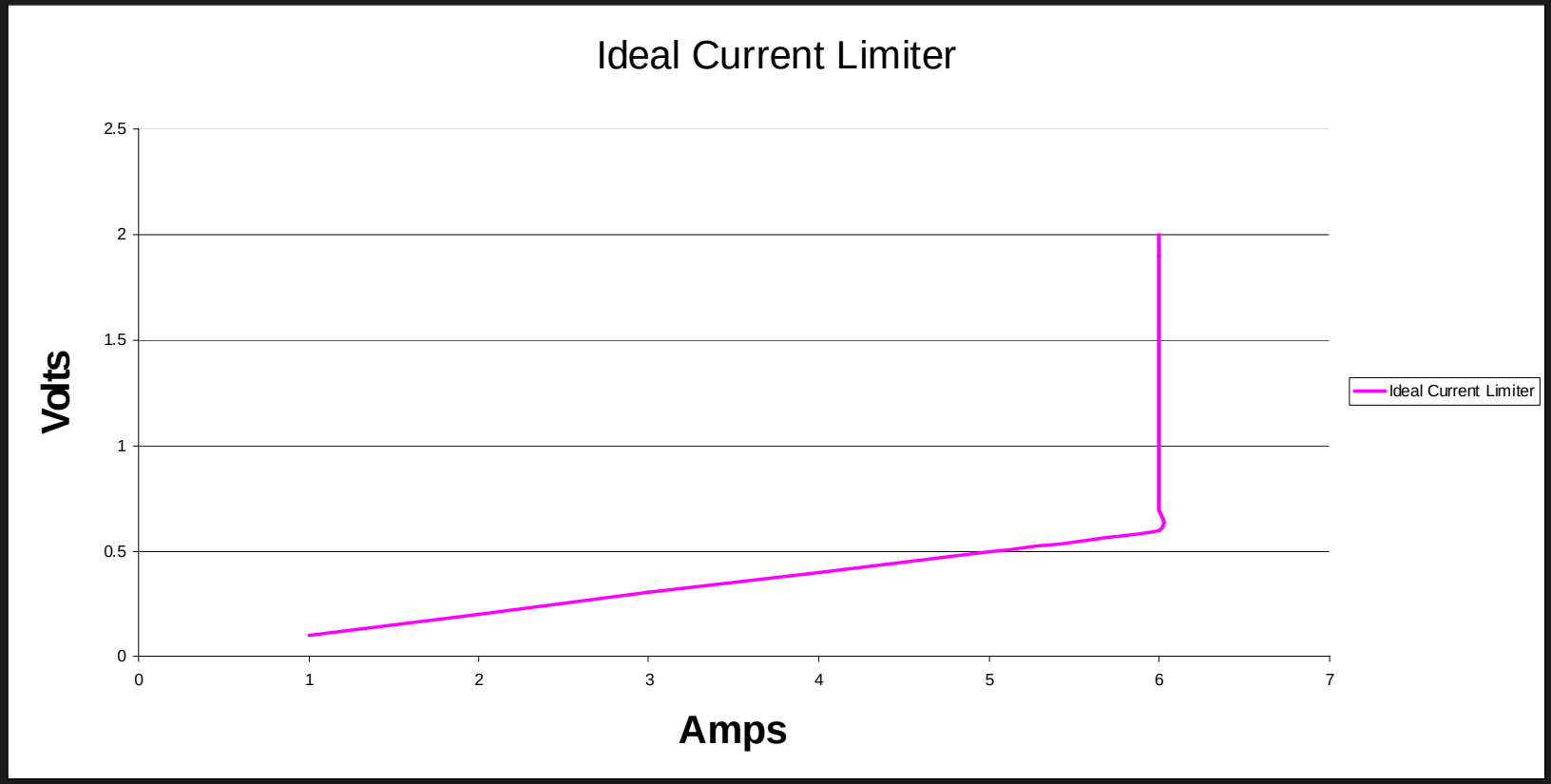
System Overview - 1

- Each probe path will have different resistance
- Higher resistance paths will cause that probe to carry less current
- Redundancy means we could lose the equivalent of 22 probes on the emitter or 6 probes on the collector and still have sufficient probes to carry current

System Overview - 2

- The CL protects each probe by limiting max current per probe to 6A
- We monitor the voltage on each current limiter, if it becomes greater than 5V we have a problem
  - Insufficient good probe contacts available to carry the current
  - Device failed in one area causing all current to flow in that area

Ideal Current Limiter Response



System Overview - 3

- At the set current the limiter becomes a current source
- The voltage across the best current limiter is a reflection of the voltage drop on the highest resistance probe

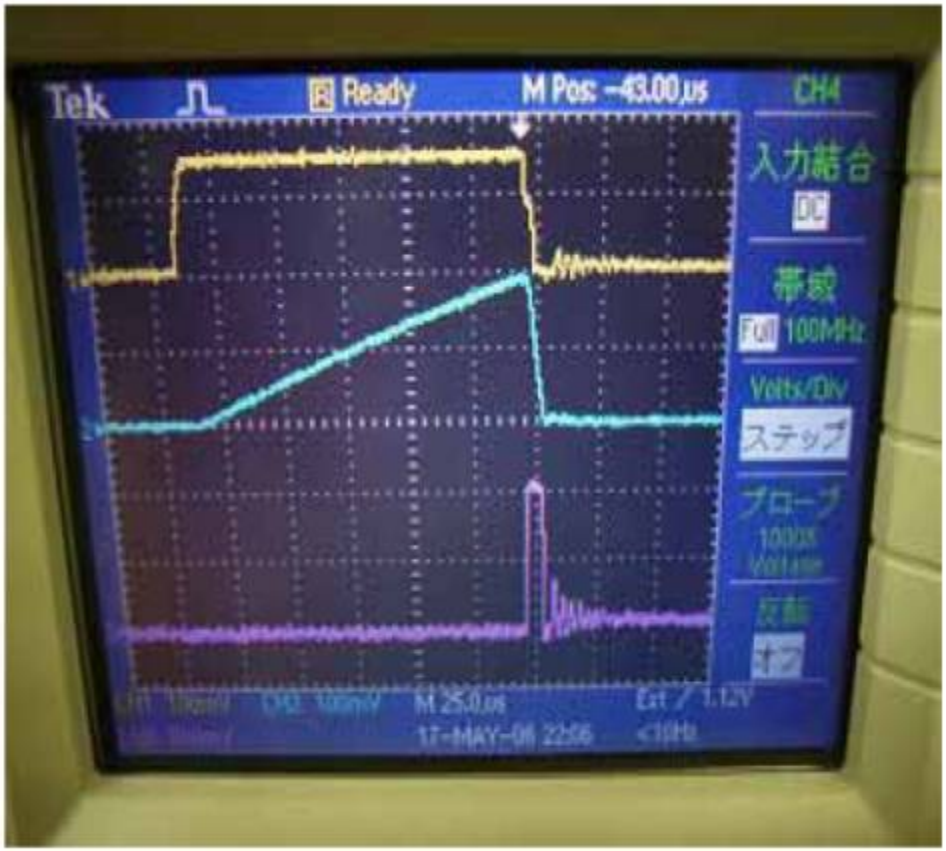
System Overview - 4

- At the point the voltage on any CL rises to 5V the test needs to be terminated in a way that protects the tester, the probes and device from the high current.
- CL sends signal through a trigger circuit to fire an SCR
- This sets up parallel path, high current is removed from DUT and probe needles preventing damage

Observations/Concerns

- Chip carrier must make good contact with back of chip to avoid localized arcing and chip damage
- Ability to read contact resistance on each probe would improve system capability
- Probe cards must be maintained to give good contact on all probes

Waveforms at 70A



===Test Parameters===

Rg=12ohm,Vg=15V,

Id=70A,L=100uH,

Vd=75V,clampSW=OFF

Double pulse= OFF,

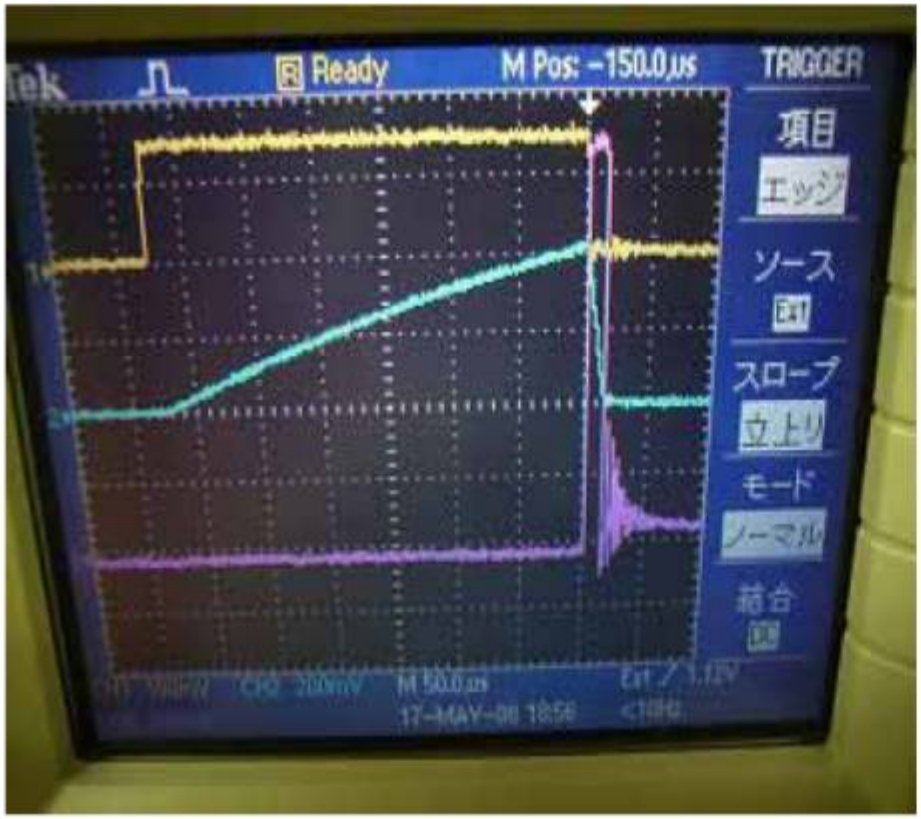
E=245mJ, RatedVds=1000V

Pulse dip switch=No2ON,

No3OFF,clampV=1110V

Zener=RD15F

Waveforms at 150A



===Test Parameters===

Rg=12ohm,Vg=15V,

Id=150A,L=100uH,

Vd=75V,clampSW=OFF

Double pulse=OFF,

E=1125mJ, RatedVds=1000V

Pulse dip switch=No2ON,

No3ON,clampV=OFF

Zener=RD15F

Conclusions at this point

- Basic concept is working
- Contact to chip carrier is critical
- We are terminating the test based on a voltage rise on the CL for a good probe
- An additional capability that would improve the system would be to look at contact resistance of each probe at the start of the test

Future Developments

- Ability to detect/measure the contact resistance path for each probe fast enough not to impact throughput
- Look at wafer probe applications
- Look at other applications requiring high current carrying capabilities

Acknowledgements

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