BANDWIDTH IMPROVEMENT TECHNIQUES ON PROBE CARDS

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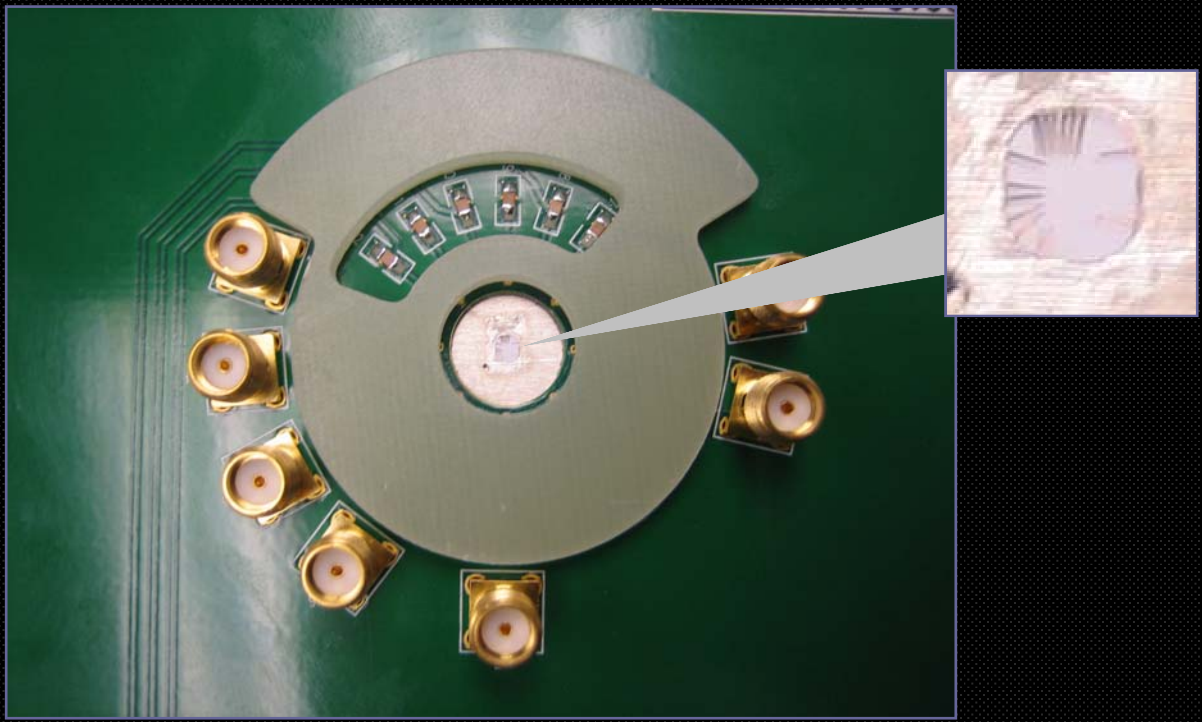
SV Probe

Agenda

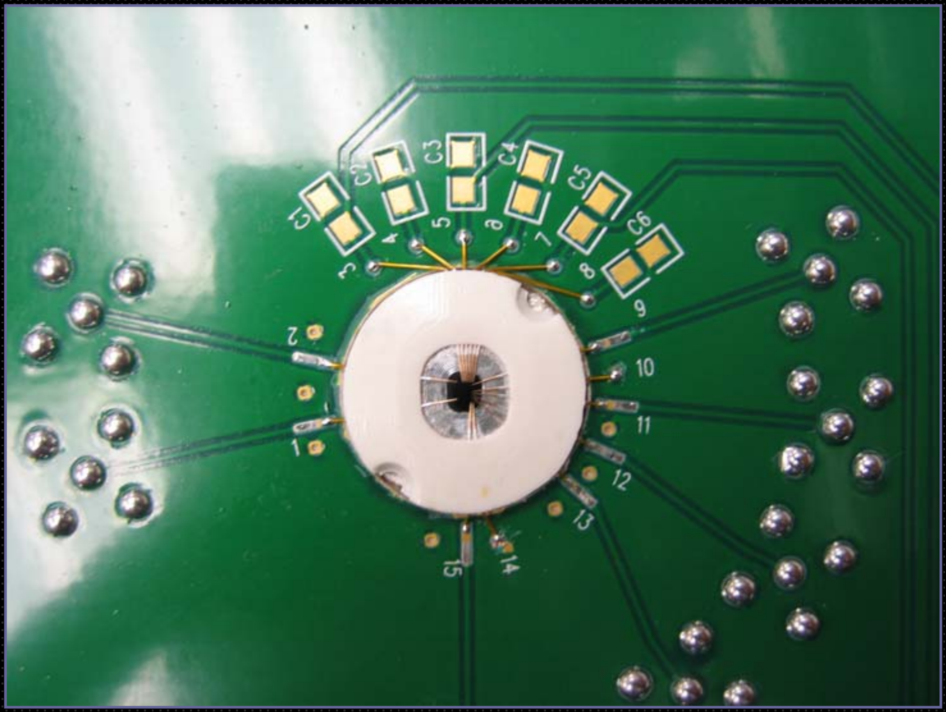
- Factors affecting the bandwidth on probe cards
- Connector issues
- Impedance discontinuities
- PCB design and losses
- Probe design (geometry, materials, termination)
- Crosstalk and data rate

Bandwidth



- Closed loop bandwidth is from connector to probe tips
- Connector to connector characterization is possible
- Maximum data rate of probe cards are determined by bandwidth of probe card and crosstalk.

Factors that affect bandwidth



- Connector
- Connector PCB mount point
- PCB losses (conductor and dielectric)
- PCB line discontinuities (corners, via etc)
- Probe end connection
- Probe design
- Probe materials
- Probe configurations

Tools to characterize?

SOFTWARE

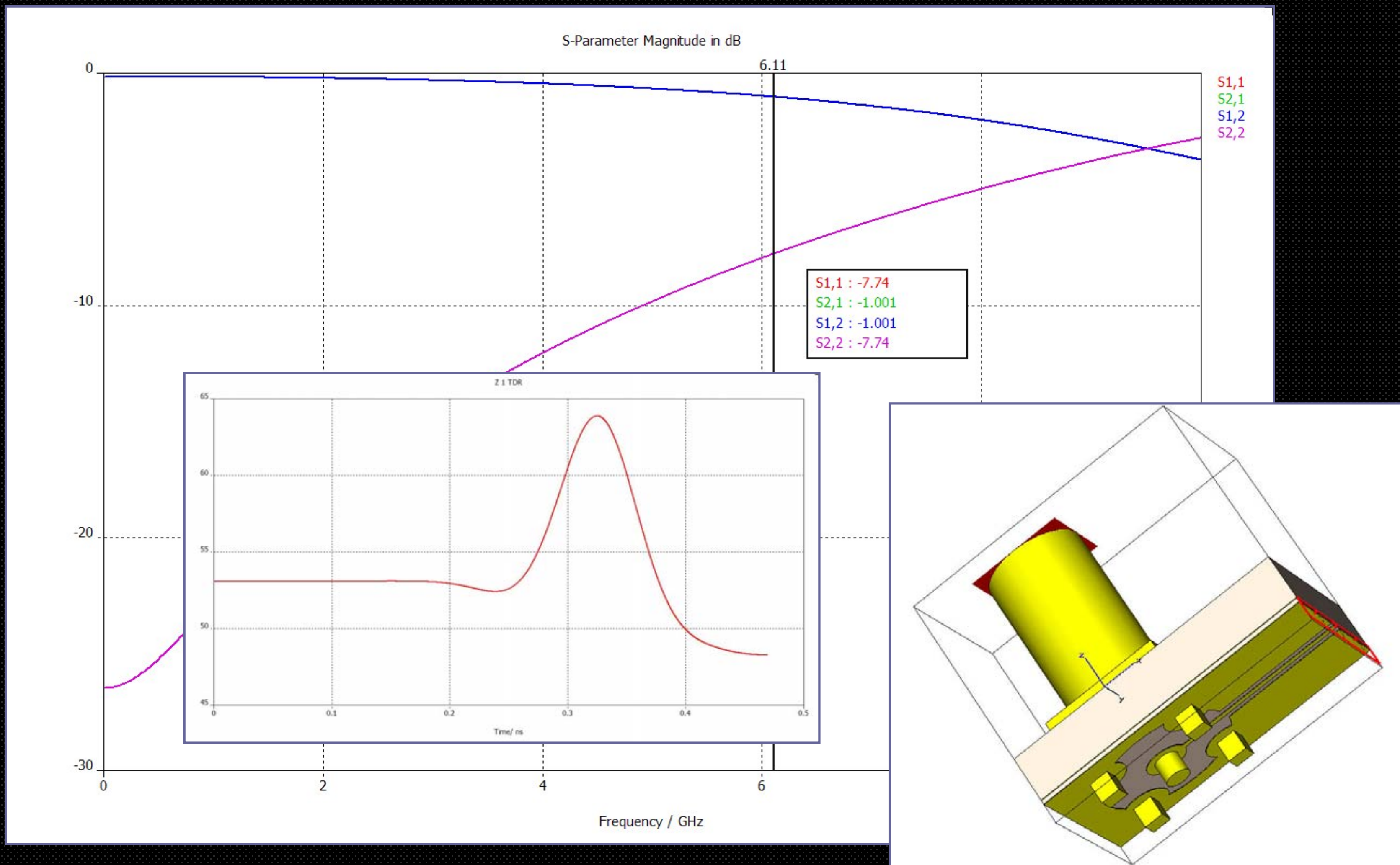
- ADS - Advanced Design System from Agilent Technologies for system level simulation
- CST - Microwave Studio for 3D electromagnetic simulation

HARDWARE

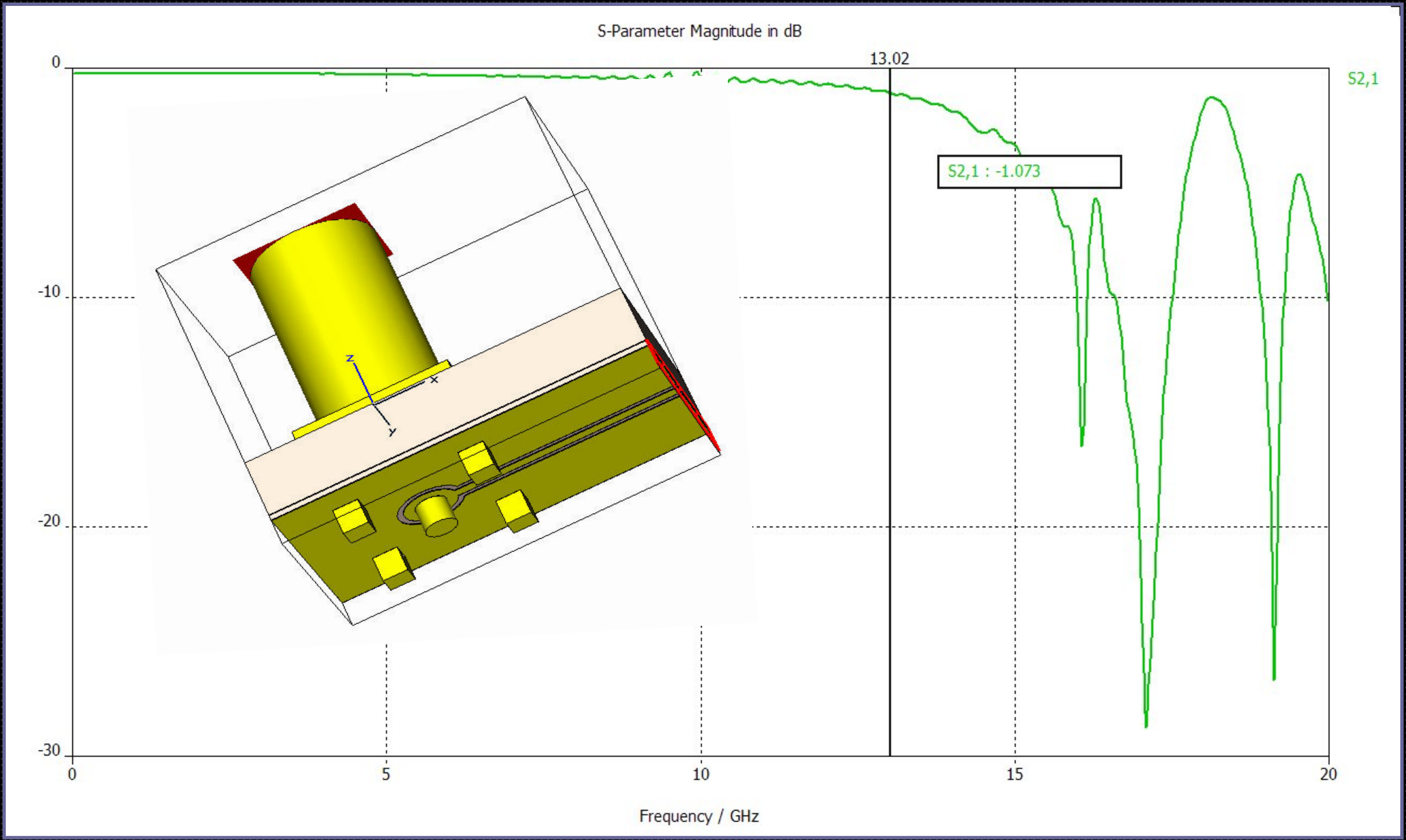
- VNA with time domain option to characterize existing cards

- TDR is extensively used to pinpoint impedance variations
- TDT is used to characterize rise time and delay

3D connector model



Improved design



Return path problems

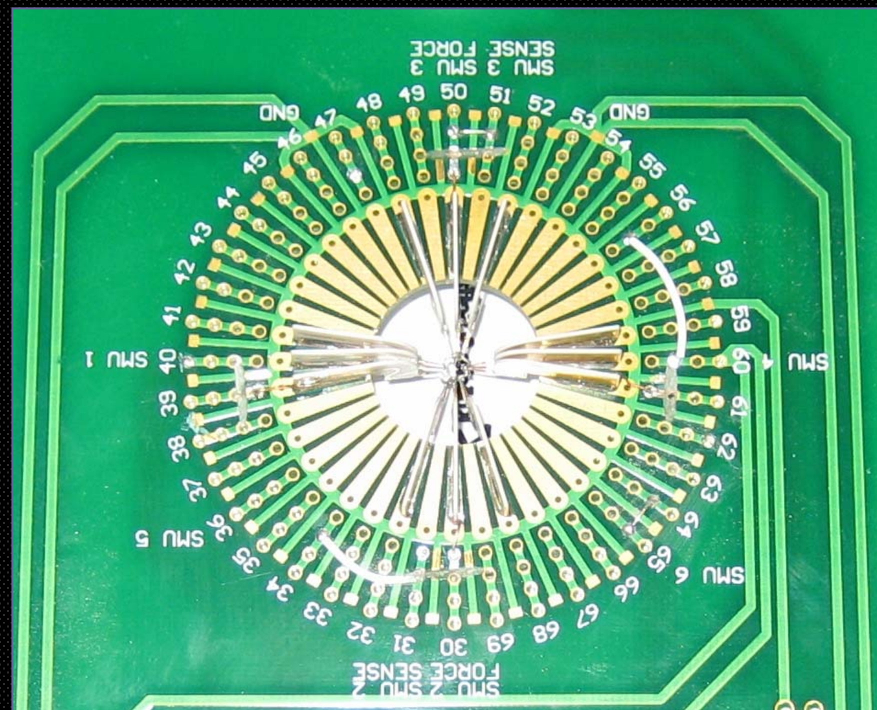
- Each impedance step along the connection will create reflection

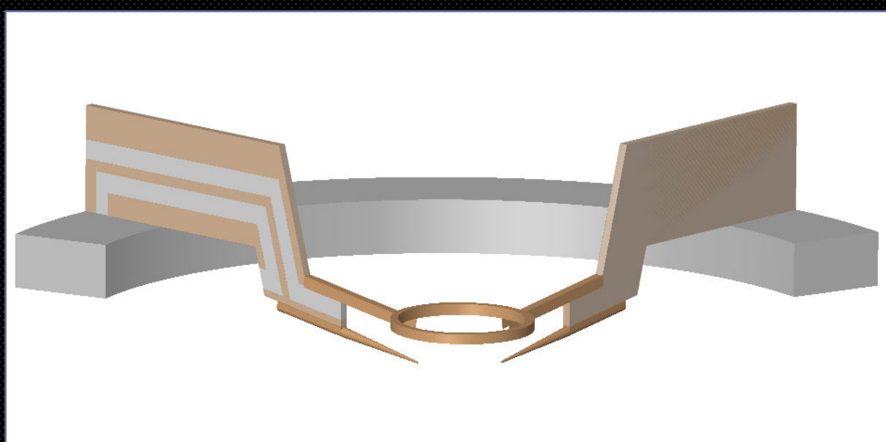
$$\Gamma = \frac{Z_L - Z_0}{Z_L + Z_0}$$

- It is desirable to reduce reflection to less than 10%.
- Major discontinuities are introduced on transition points such as connector to PCB and PCB to probe
- If DUT does not have ground pads close to signal path shorter return paths can be created between probes.
- Shorter return paths also decrease probe inductive behavior.

Return loop concept on blade cards

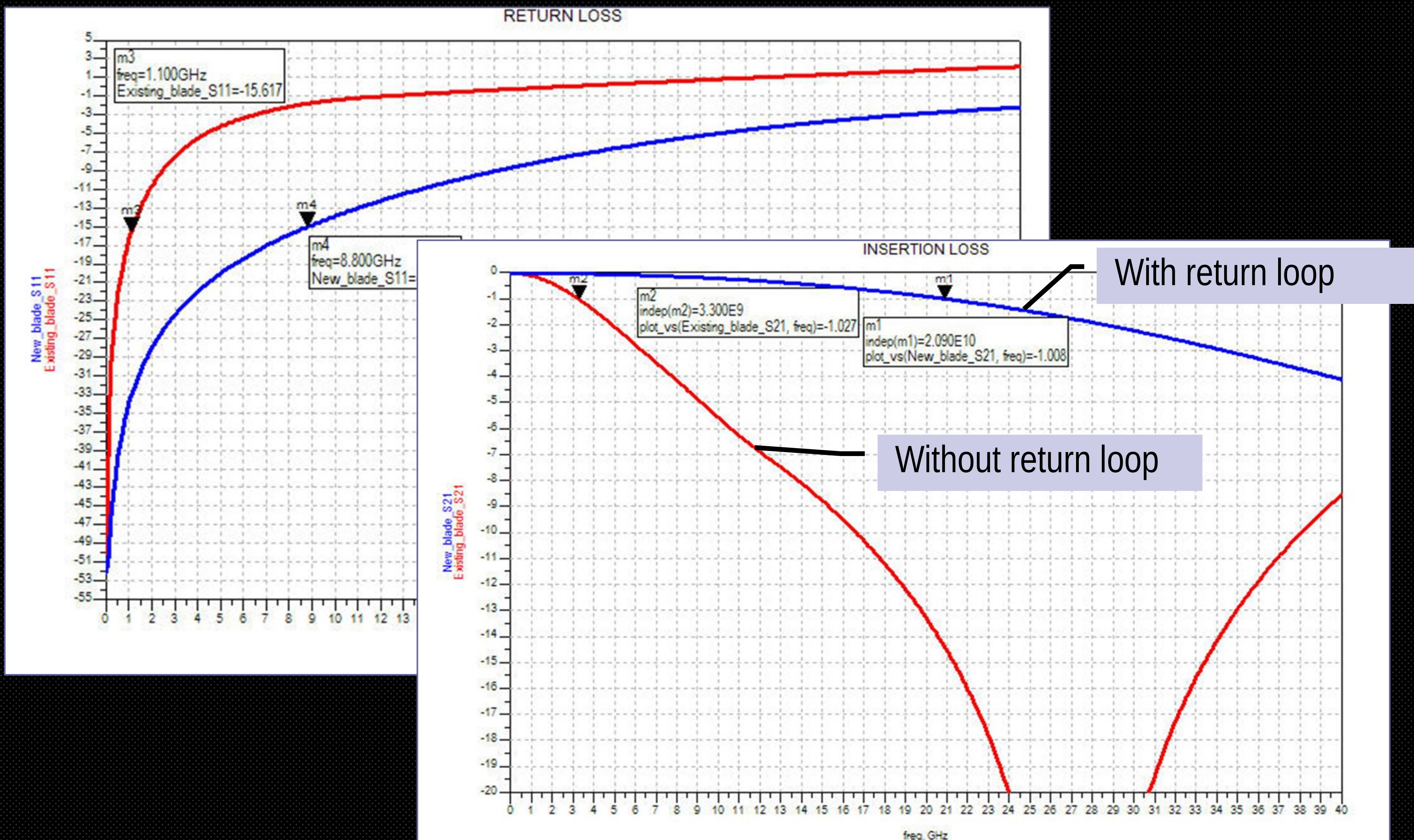
- Return path is created on top of the probes reducing probe tip inductive effects.
- Return path is reduced from periphery of the card to return loop





Patent pending

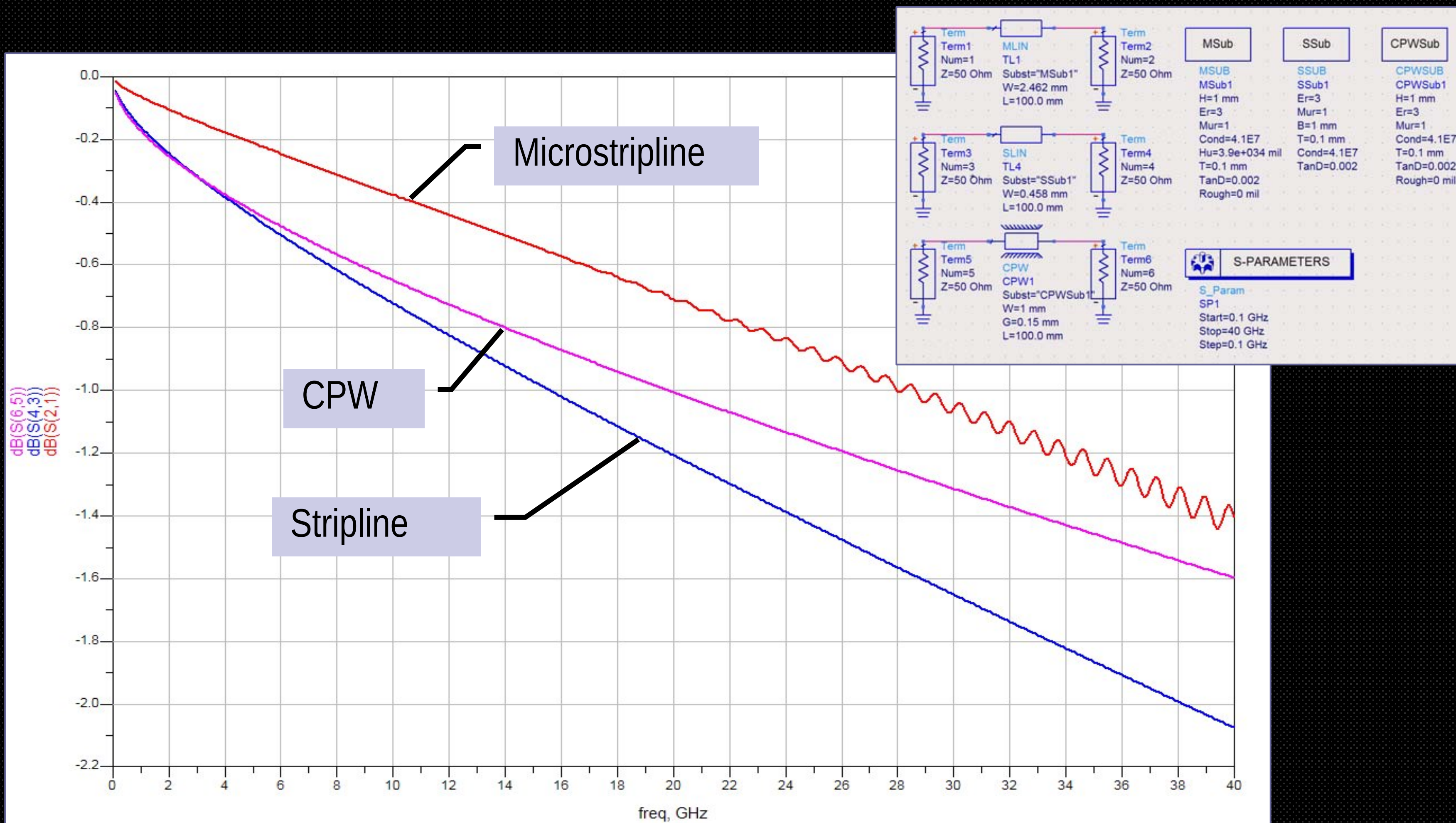
Return loop effect



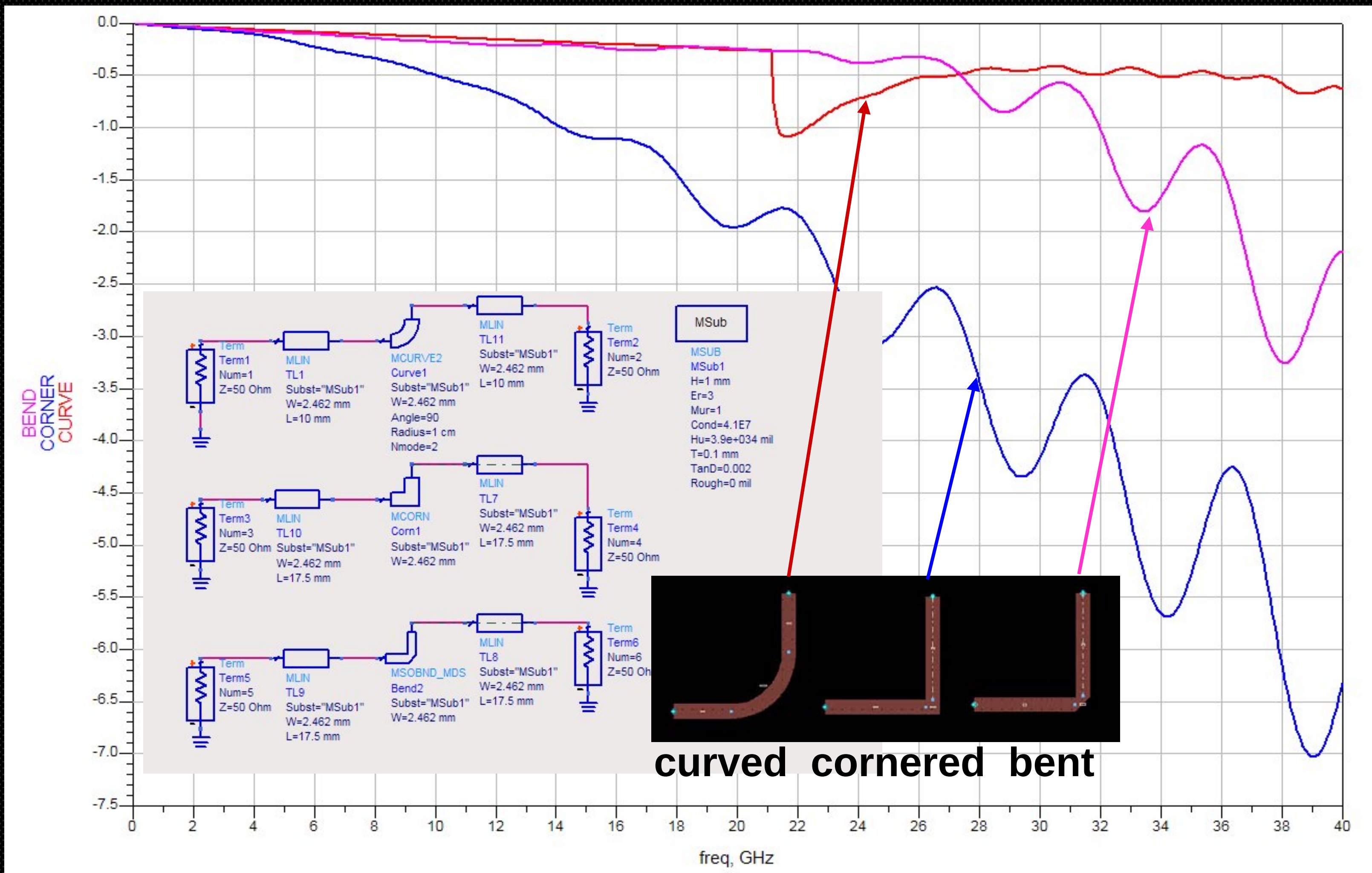
PCB losses

- PCB losses for short traces are minor contributors on bandwidth
- If there is no major reflections on probe card, then reducing PCB losses becomes important
- Dielectric losses rise proportionally with frequency
- If the loss tangent is less than 0.002, conductor losses are major contributor2
- Corner edge traces should not be used
- Via usage should be avoided
- Transmission line length should be minimized to reduce dielectric loss and conductor losses.

CPW (Coplanar waveguide), stripline, microstripline?



Curved, cornered or bent?

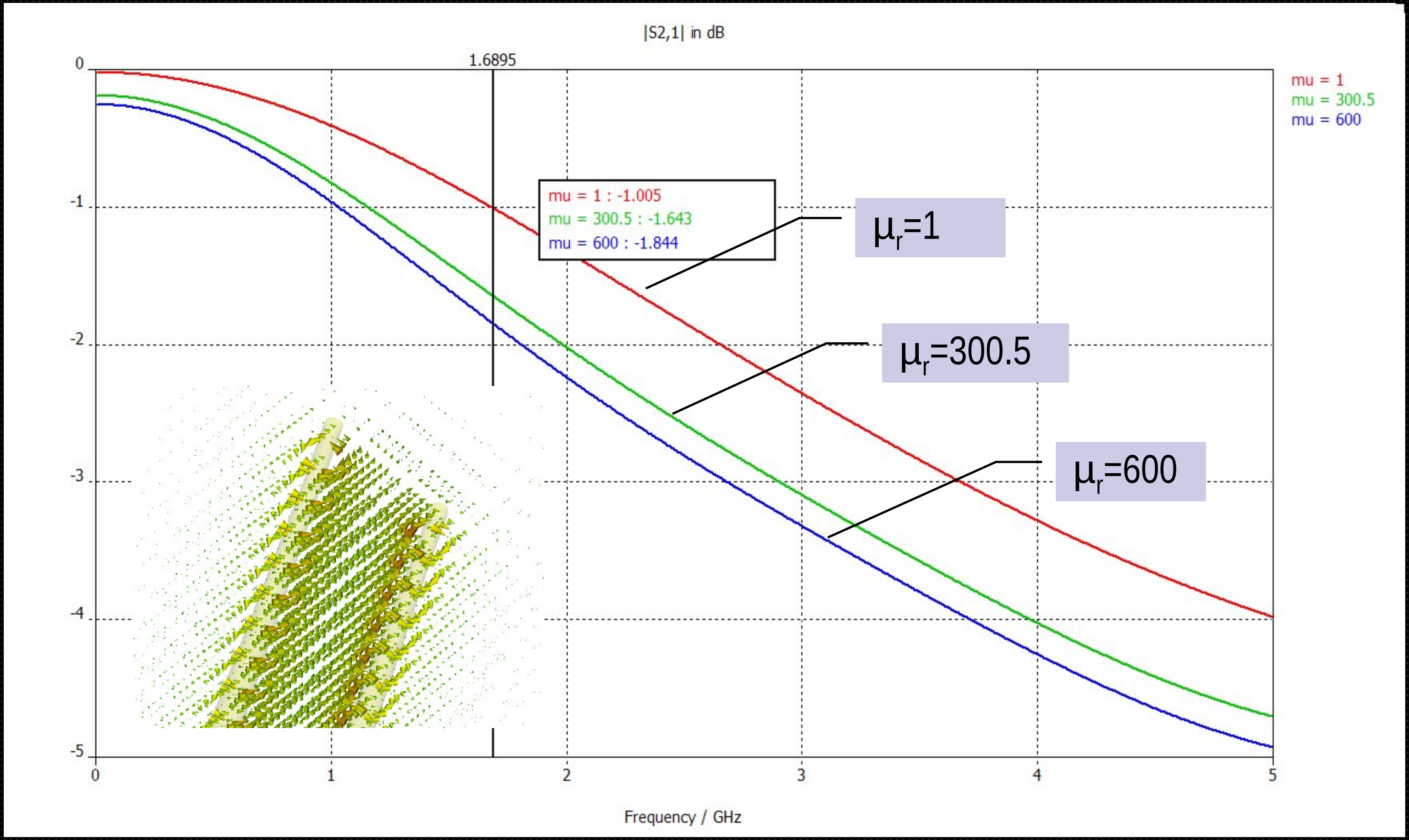


Materials effects

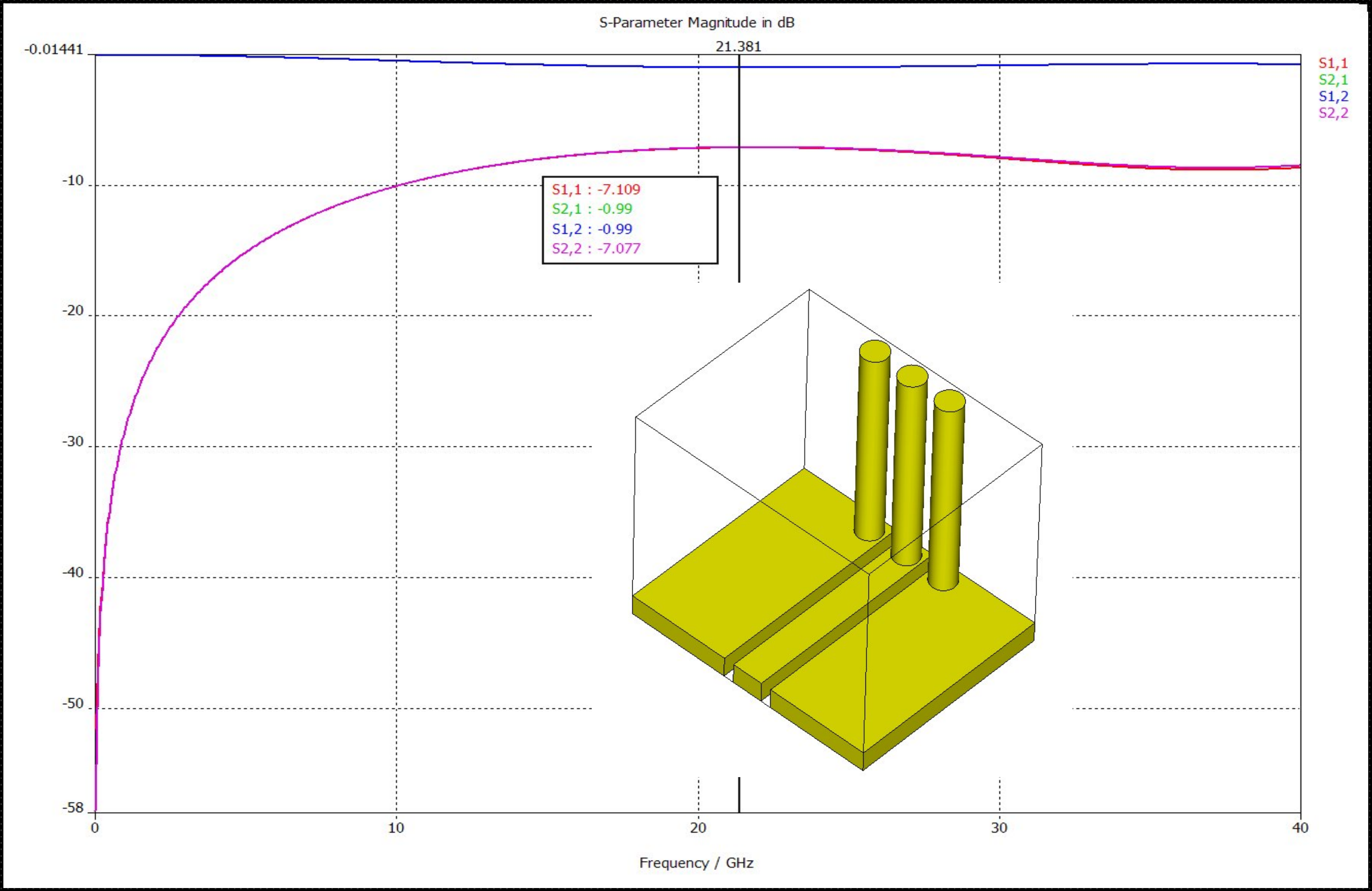
- High magnetic permeability materials such as nickel and steel increase inductance and creates delay on digital signals
- Magnetic fields should be confined to specific volume
- If not possible, usage of steel etc close to unconfined space should be restricted.

Air	1.00000037
Copper	0.9999833
Gold	0.99996
Aluminum	1.000021
Nickel	600
Tungsten	1.00008
Manganese	1.001

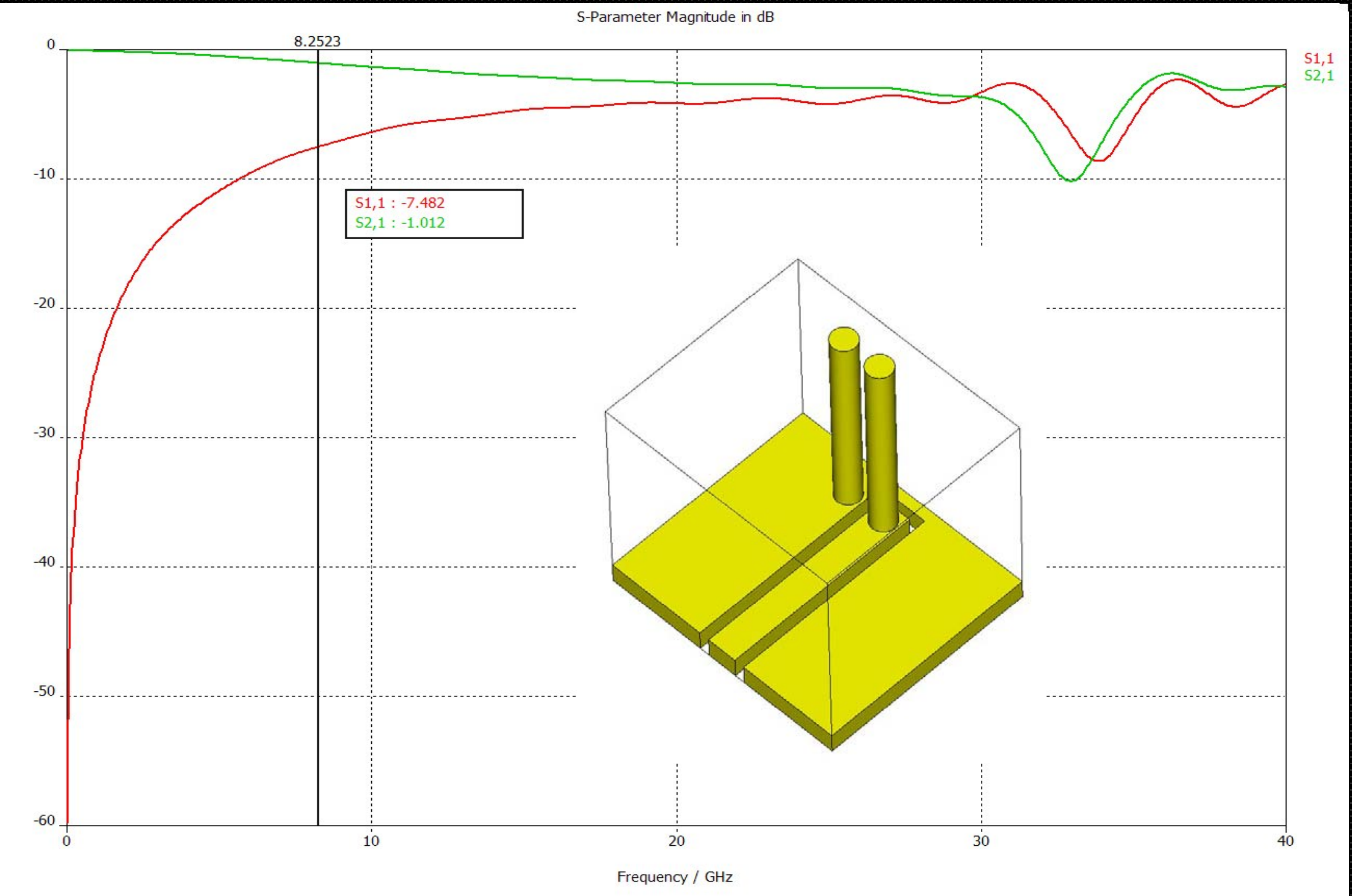
Effects of different probe permeability



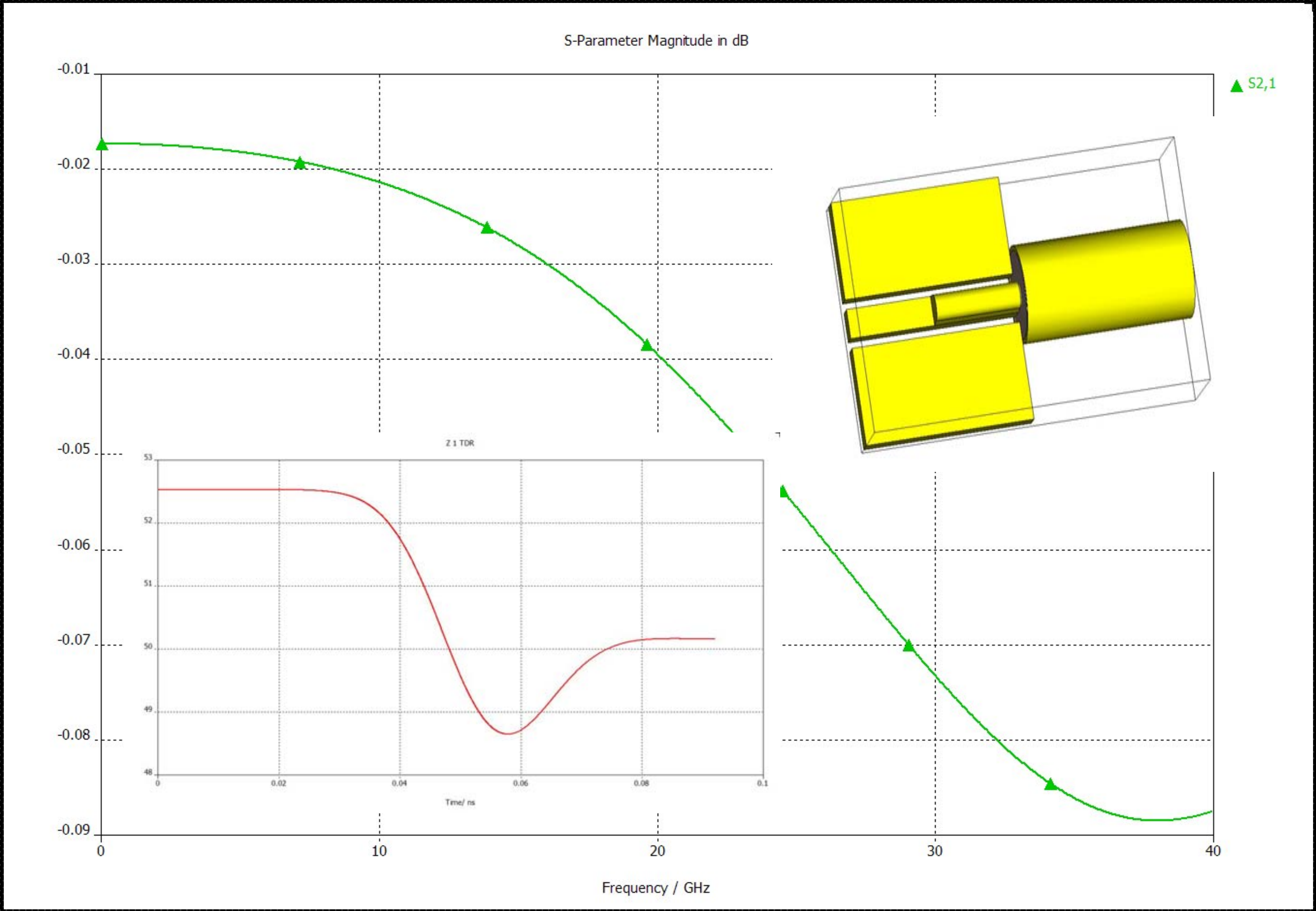
Probe termination (GSG)



Probe termination (GS)



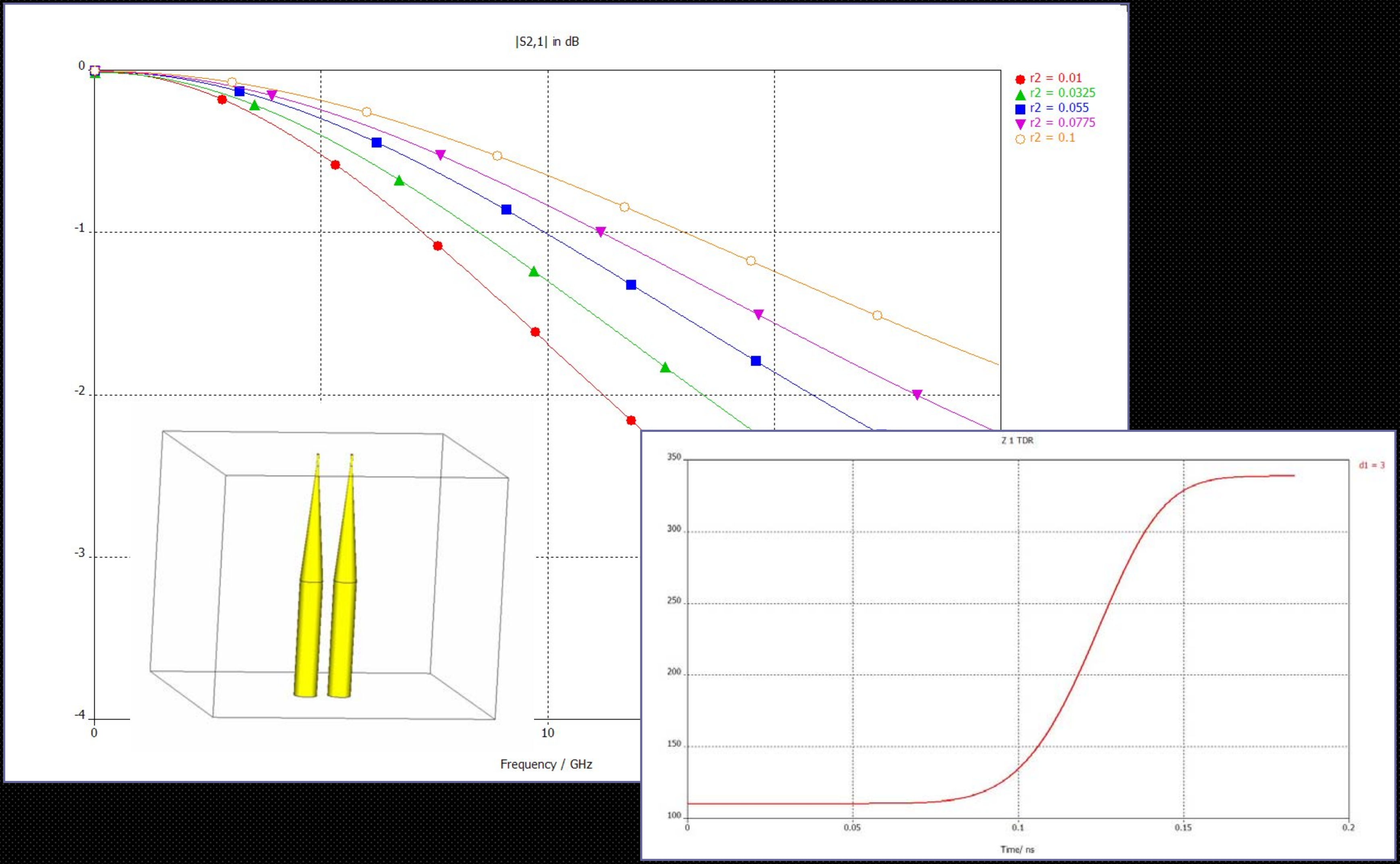
CPW to coax transition



Probe tip geometry effects

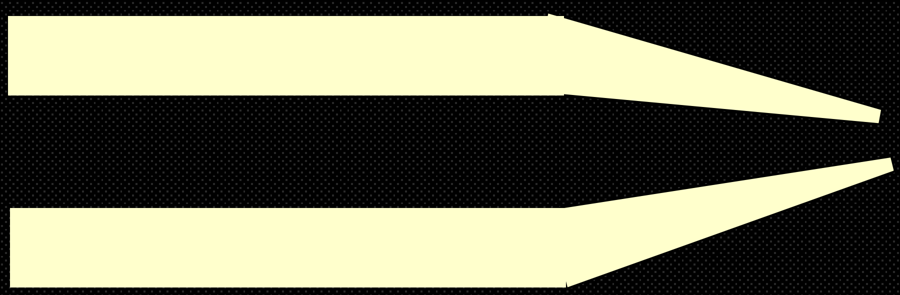
- Tapering of tips creates a impedance change, and in general, results in increased characteristic impedance compared to beginning line impedance
- It behaves as a low pass filter on S21
- Adjustment of probe tip angle is required to keep characteristic impedance constant.

Tip taper angle

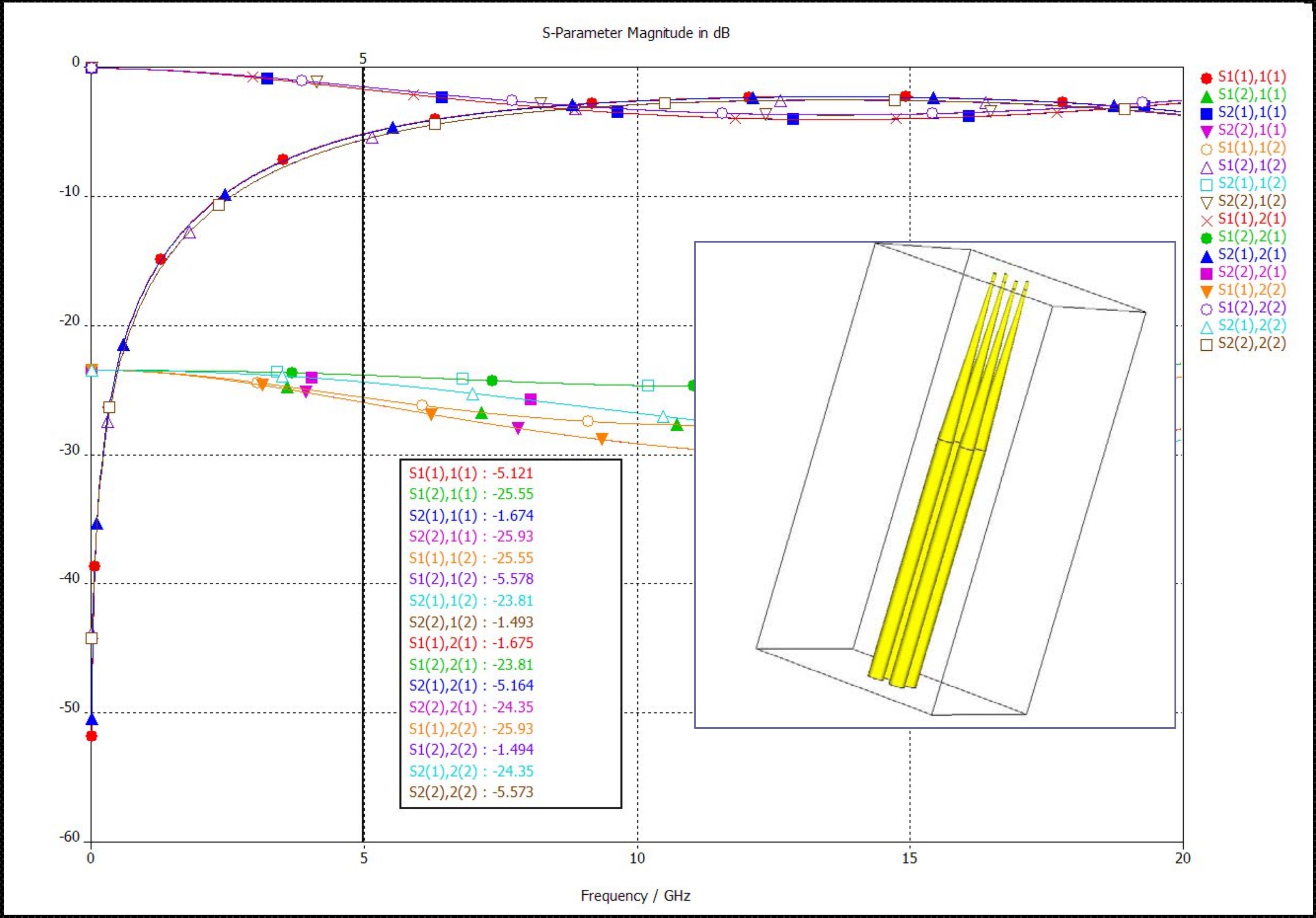


Cantilever probe placement

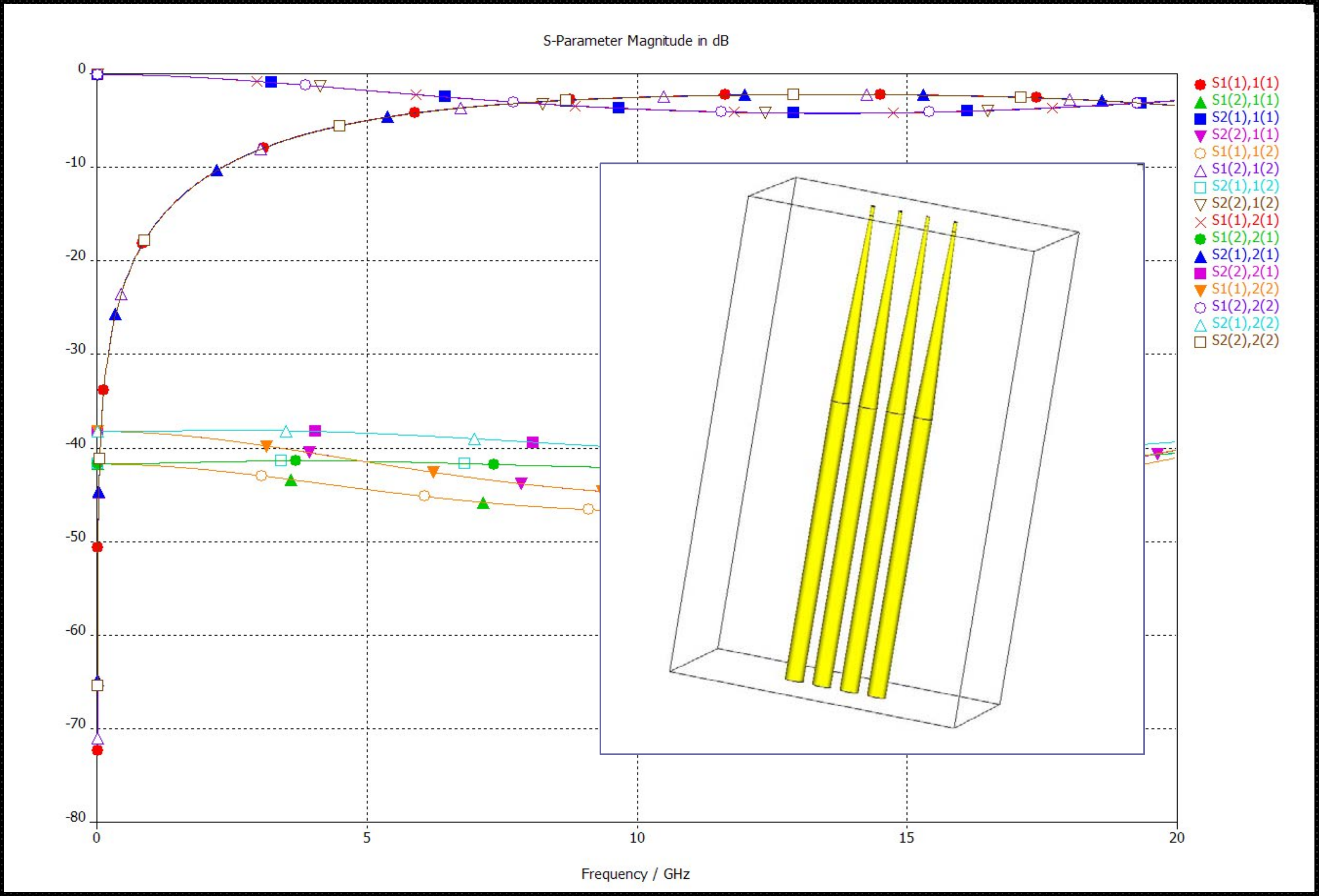
- Characteristic impedance is proportional to D/2r where D is the distance between two probes center to center and r is the probe radius
- So D/2r ratio should be kept same along the tapering to keep the characteristic impedance constant



Bandwidth is same but data rate is higher?



Crosstalk reduction



How much improved?

- According to Shannon-Hartley theorem

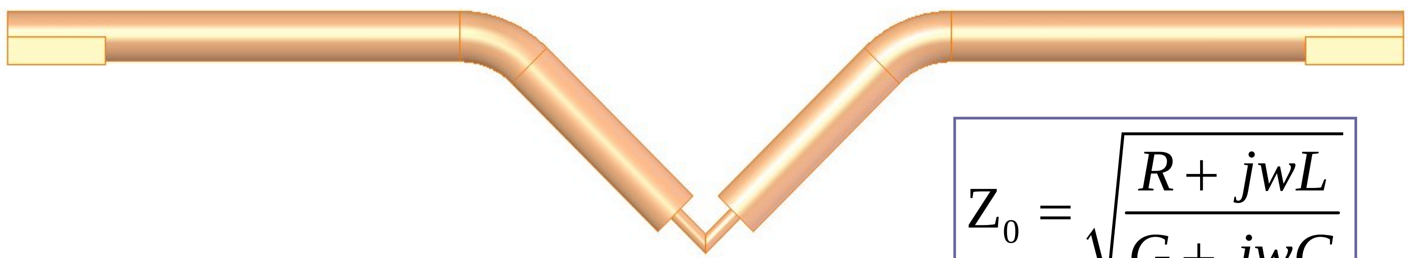
Channel capacity in bits per second:

$$C = BW \times \log_2\left(\frac{S+N}{N}\right)$$

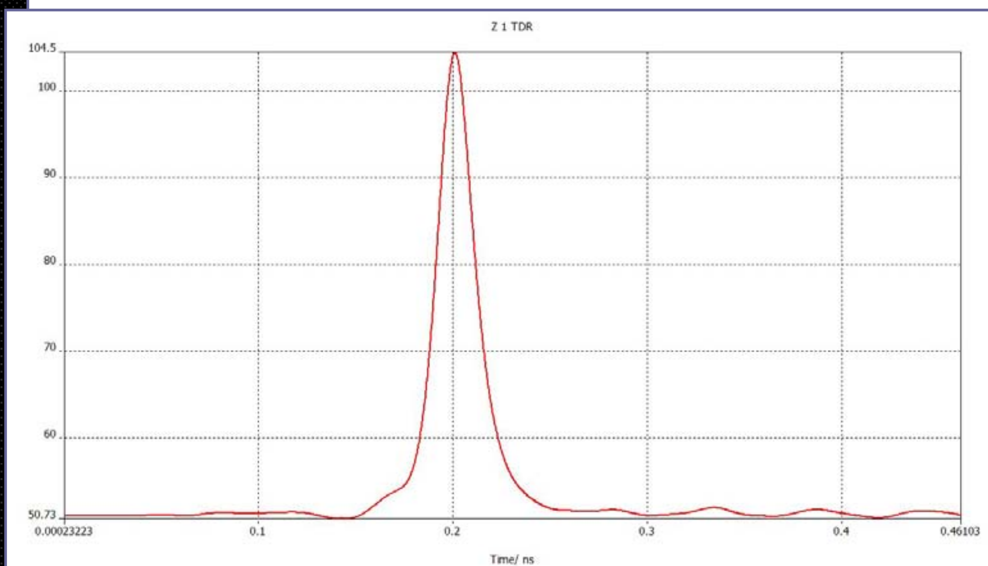
- From S/N=20 dB to S/N=40 dB

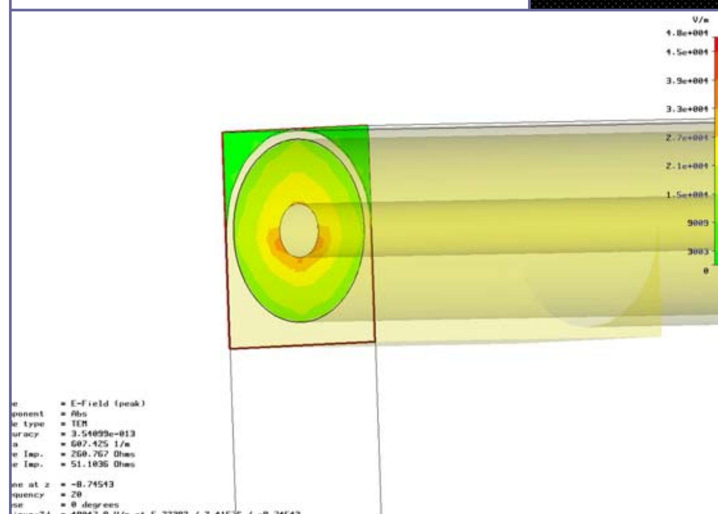
Data rate is improved 1.92 times although bandwidth kept same.

Using epoxy to reduce inductivity tips



$$Z_0 = \sqrt{\frac{R + jwL}{G + jwC}}$$





Summary

- Mechanical design
- PCB design
- Materials choices

All affect bandwidth and can be used to optimize probe card design.