

# Implementing Inkless Wafer Sort

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# Implementing Inkless Wafer Sort

- Introduction
- Benefits Why implement inkless wafer sort?
- Inkless process flow example
- Implementation goals
- Requirements key items for implementation
- Possible problems & solutions
- Summary

### Introduction

 Altera is a fab-less FPGA / programmable logic company and does wafer sort in San Jose and at off-shore foundries

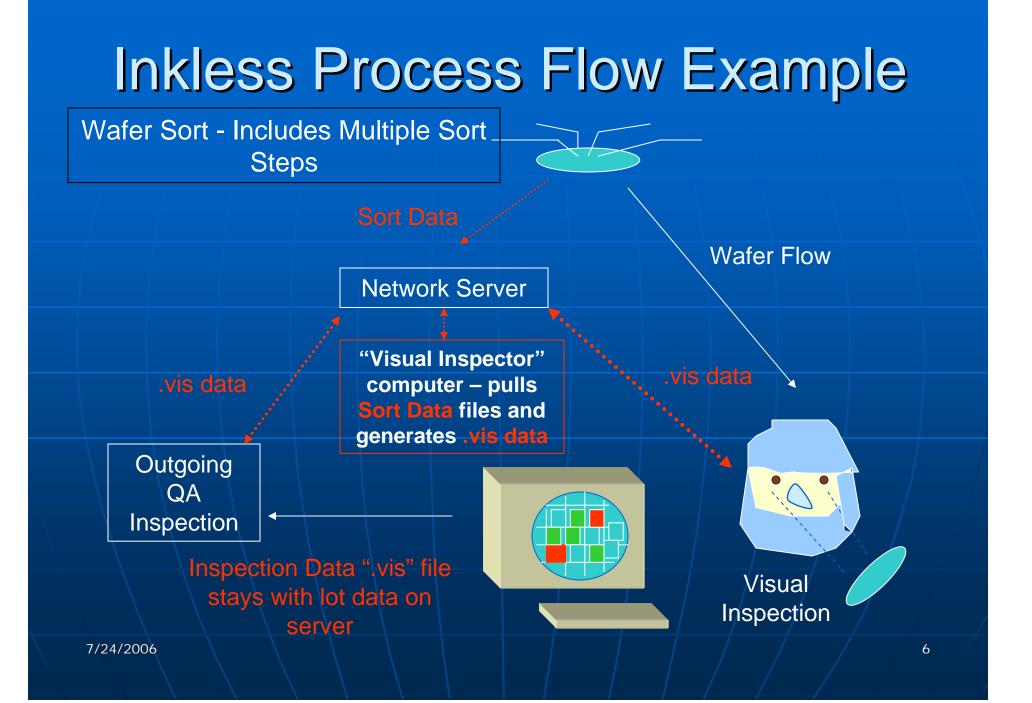
- Started out with in-line inking
- Progressed to off-line inking
- Decided engineering time better spent on eliminating inking issues

Process wafers from wafer sort to assembly without INK!

- Electronic Wafer Maps identify passing and failing dice on each wafer
- Visual Inspection rejects identified on wafer maps
- It is NOT a quick fix to "push" count variance problems onto assembly. (And you don't immediately say "good bye" to Xandex!)
- It is part of an ongoing wafer sort improvement process

#### **Benefits - Why Implement Inkless Wafer Sort?** Increased Productivity Reduced Cycle time. Eliminates inking step Eliminates ink cure time Eliminate rework due to inking errors Allows for good die recovery (no ink to remove) More assembly flexibility Speed binning die segregation Qualifications of non-passing dice Additional assembly "EPR" capabilities: binning, qualifications, sampling, etc. 7/24/2006

**Benefits - Why Implement Inkless Wafer Sort?** Increased quality No chance of inking incorrect dice or dripping ink on good dice. Reduce chance for wafer breakage and bump damage Solder-bumped wafers can be re-flowed if necessary Reduces count discrepancies Improves data systems

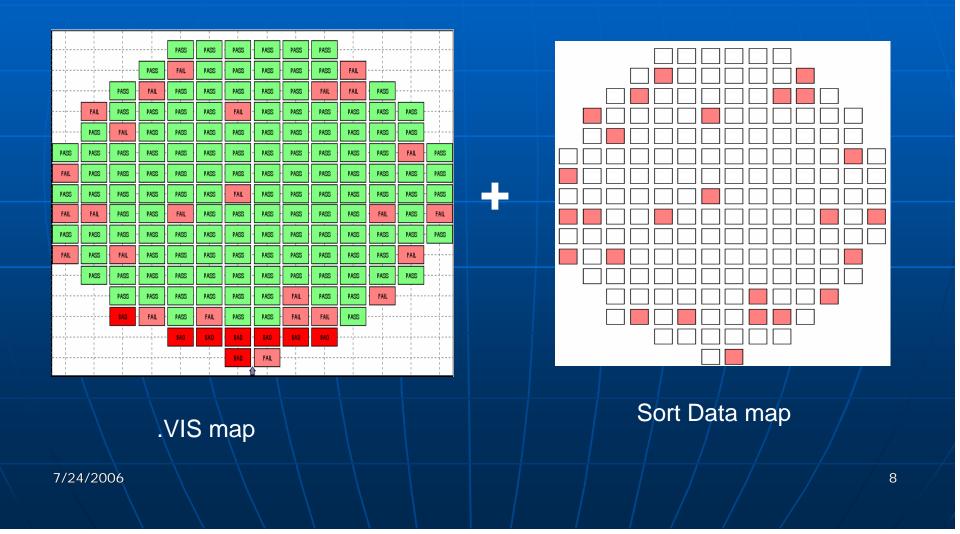


#### "Visual Inspector" Program for identifying visual defects

Visual Inspection

							Wafer:								
						N	otch Positi	on: 6:00							Passing
. 1															Failing
15 -					PASS	PASS	PASS	PASS	PASS	PASS	;				
14 -				PASS	FAIL	PASS	PASS	PASS	PASS	PASS	FAIL				
13 -			PASS	FAIL	PASS	PASS	PASS	PASS	PASS	FAIL	FAIL	PASS			
12		FAIL	PASS	PASS	PASS	PASS	FAIL	PASS	PASS	PASS	PASS	PASS	PASS		
11		PASS	FAIL	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS		
10	PASS	PASS	PASS	PASS	PASS	PASS	FAIL	PASS							
9	FAIL	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	
8 -	PASS	PASS	PASS	PASS	PASS	PASS	FAIL	PASS	PASS	PASS	PASS	PASS	PASS	PASS	
7 -	FAIL	FAIL	PASS	PASS	FAIL	PASS	PASS	PASS	PASS	PASS	PASS	FAIL	PASS	FAIL	
6	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS							
5	FAIL	PASS	FAIL	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	FAIL		
4 -		PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS		
3			PASS	PASS	PASS	PASS	PASS	PASS	FAIL	PASS	PASS	FAIL			
2			6AD	FAIL	PASS	FAIL	PASS	PASS	FAIL	FAIL	PASS				
1					8AD	6AD	6AD	8AD	8AD	8AD					
0							BAD	FAIL							
į							1								
	-6	-5	-4	-3	-2	-1	Ó	1	2	3	4	5	6	7	

 Visual Inspection file (.VIS) over-laid onto Sort Data files.



Wafer map used for assy ALTR EP1SXYZ13 N42675-01 9D008101.asm . . . . . . . . .  $\mathbf{1} \mathbf{X} \mathbf{1} \mathbf{1} \mathbf{1} \mathbf{1} \mathbf{1} \mathbf{X}$ TXTTTTTXX1. TYTTTT 77777 111211111111 XX11X111111X1X TTTTX 11111X11X. QX1X11XX1. 

Planner issues assy instruction using Manufacturing Control System

Manufacturing Control System notifies <u>summary</u> server to generate wafer maps

Lot, Wafer numbers, and selective assy decisions input by planner into Manufacturing Control System

Maps generated with .ldb and .vis files merged together Summary network server pulls .ldb and .vis files from specified product and lot # and runs *Mapgen* program to generate assy maps which are FTP'd to assy house

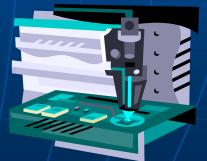
Map Data & Assy Report FTP'd to Assy House





Wafers are shipped to Assy House

Map Data and wafers combined during pick and place. OCR fab lot # and Wafer # matched with data to prevent errors. "X, @, and ." dice discarded. Bin -1 dice assembled.



#### Implementation Goals

#### Two Goals:

- 1) Satisfy Wafer Sort Area Customer
  - Prove data management system works
    - Off-line inking (1<sup>st</sup>)
    - Visual Inspection System (2<sup>nd</sup>)
- 2) Satisfy Assembly House Customers including Planners
  - Don't trade ink problems for inkless problems:
    - Die count discrepancies between Inventory Control Database and Wafer Sort Summary Database
    - Wafer map quality and transfer problems

Wafer Sort Area Customer

- Understand Sort Process Test Flow
  - How many sort steps are there?
  - Are there re-test steps?
  - Which sort steps affect yield?
  - How / where / when do lot WIP data get stored?
- Use OCR scribed or bar coded wafers
  - Test data should cross reference OCR lot number
- Establish robust Off-line inking process
  - Prove data system works verify inking quality correct dice inked, no count discrepancies
- Develop electronic wafer map inspection system
  - No Ink! Must "Mark" Visual Inspection Rejects and record data
- Start with one product and focus on making it work

- Assembly House Customers:
  - Understand Sort Process Data Flow
    - Where do Sort Data Originate?
    - Are there multiple Sort Sites?
    - Whose Sort Data?
      - Sort Vendor's?
      - Your company's testers?
    - Where / how does WIP system data get distributed to planners and assembly house?
    - Where are Sort Data Stored?
      - Sort Vendor / Fab / Your HQ (fabless model)?
    - Who maintains Sort Data?
    - How do you adjust for Count Discrepancies between WIP Control System and Sort Data Base?

Wafer Map Standard

- Use existing specifications
  - Wafer Fab / Sort Facility
  - Assembly house
- Assy Vendors must have procedures and equipment for inkless assy
  - Verify these:
    - Map standards
    - FTP capabilities
    - OCR capabilities
  - Avoid: "Sure we do inkless Blind Builds, Anyone?!"

#### Initial management buy-in

- Develop a Team Manufacturing Engineering, Materials Planning, Test Engineering, MIS, Wafer Sort and Assembly Vendors
  - Ongoing communication
  - Team leader
- Servers and Software
  - Wafer Sort Data file system
  - Map generation software system
  - Material Automation Software to execute map generation with die release order
- Develop manual map generation back-up system
- Run Sample Inkless Lot
  - Inspect wafer skeletons, compare with maps

• Make appropriate adjustments, run another sample lot

**Requirements - Key Items for** Implementation Develop monitoring system for quality improvement Track number of inkless lots processed Track number of issues Feedback results to team members Seek upper management buy-in Introduce more products as more success and knowledge evolve

#### **Possible Problems and Solutions**

- Problem Incorrect map / incorrect map data
- Solution Same data system used for off-line ink used for map generation. History of off-line inking success. Wafers are identified by Fab lot # and wafer #. Map data contain Product type, Fab Lot #s, sort lot #s, and Wafer #.
- Problem Map data fails to transfer to assy vendor
- Solution Data are stored on local server. TE and ME can regenerate and FTP or email maps as required. No assy will occur unless maps are FTP'd.
- Problem Edge dice on wafer aren't on wafer map
- Solution Develop map "padding" for unprobed edge dice

### Summary

- Inkless processing reduces cycle time and improves quality
- The goal is to satisfy two customers
  - Wafer sort area
  - Assembly house
- There are several key items for implementation
  - Sort data knowledge
  - Teamwork
  - Hardware
  - Software
  - Management approval

#### Implementing inkless processing is a continuous improvement process