



# **IEEE SW Test Workshop**

**Semiconductor Wafer Test Workshop**

## **Wafer level testing Challenges and opportunities Scope: CPU + Chipsets**

**June 3-6, 2007**

**San Diego, CA USA**



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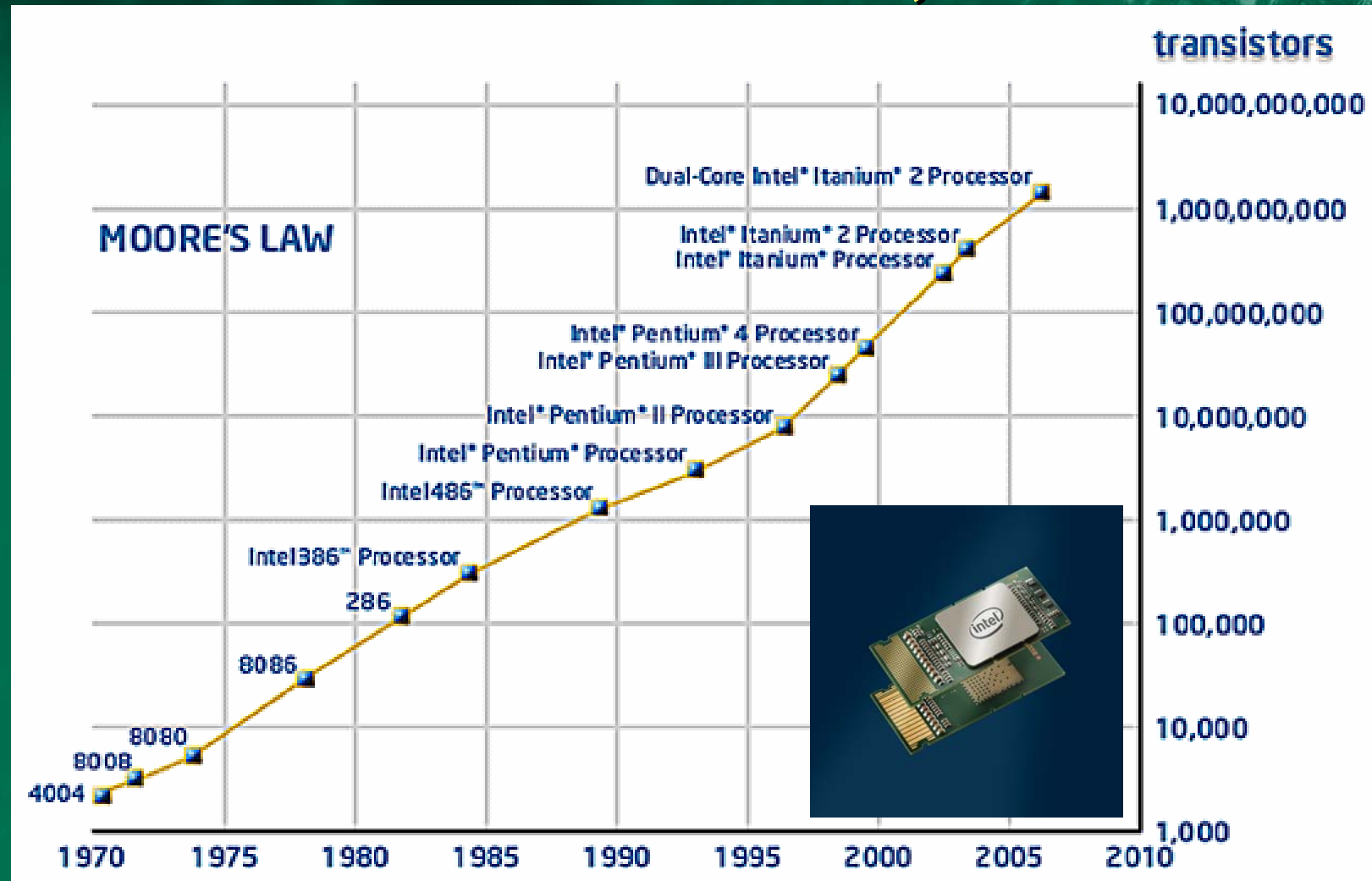
# Overview

- Moore's Law
- Test cost prediction from 1990s
- Equipment development impact: CMT
- Current cost projections
- Example of cost reduction through SIU
- Other vectors of test cost
- A word on collaboration
- Summary

Last  
10yrs

Future  
Challenges

# Moore's Law: Our friend, our challenge



<http://www.intel.com/technology/mooreslaw/index.htm>

How to test 2X transistors/2yrs cost-effectively with high quality?

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# Recapping the Last 10yrs

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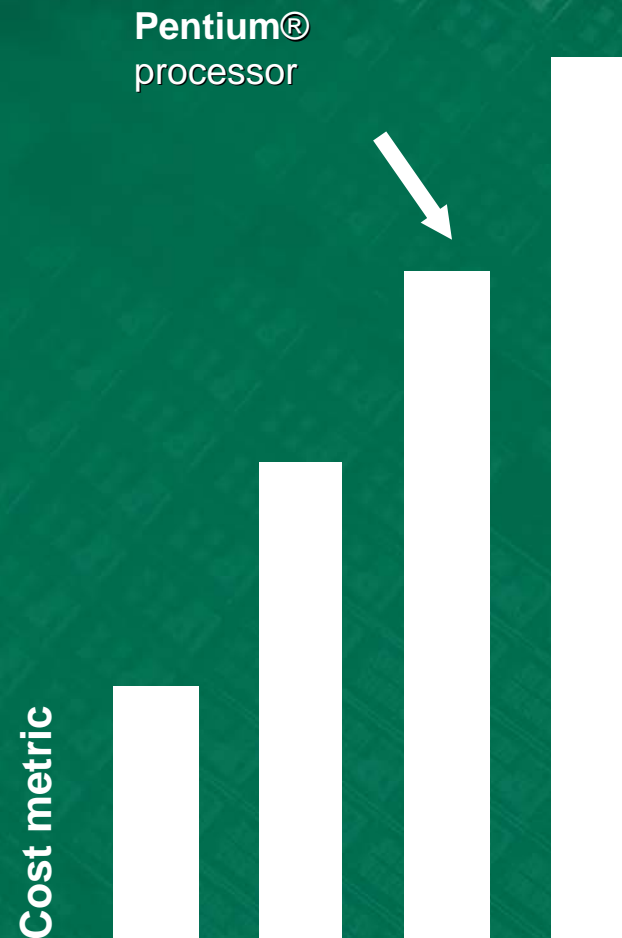
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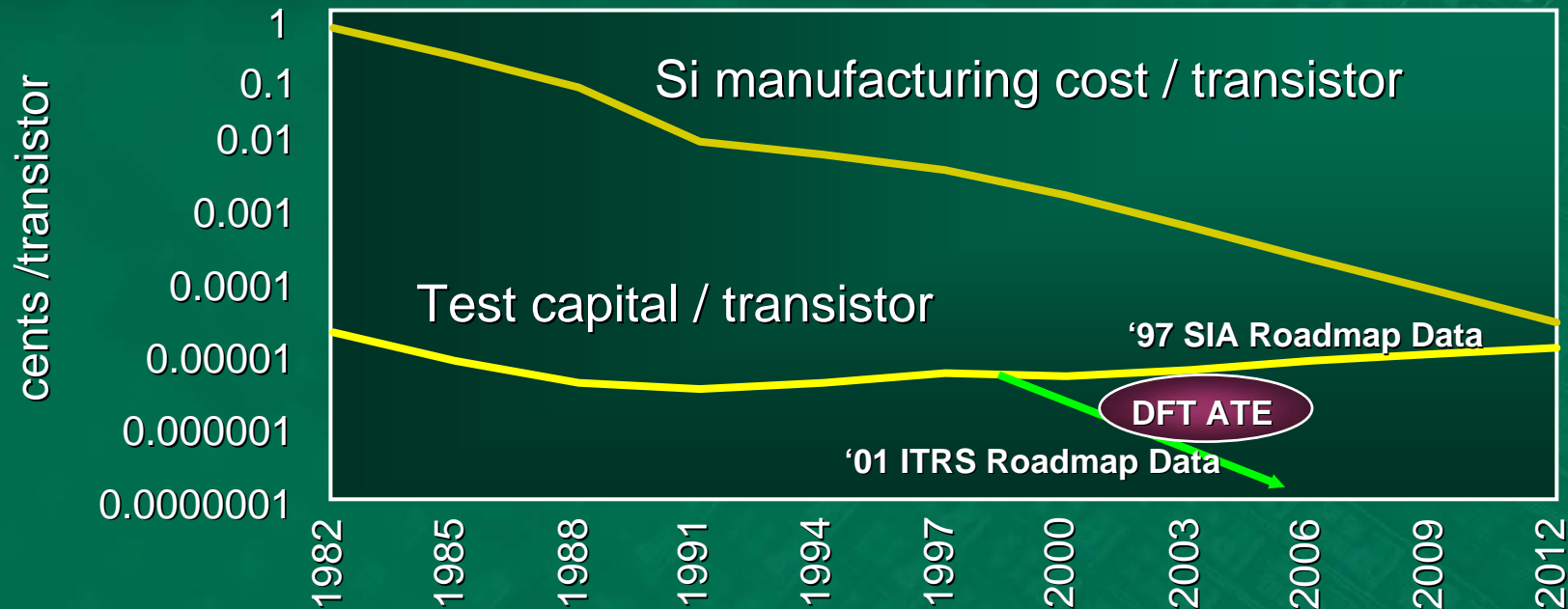
# Test Cost Trends: Circa 1997

Each generation:

- 2x transistors
  - test complexity increases
  - longer test time
- 2x performance
  - tester speed reqt increases
  - more expensive testers

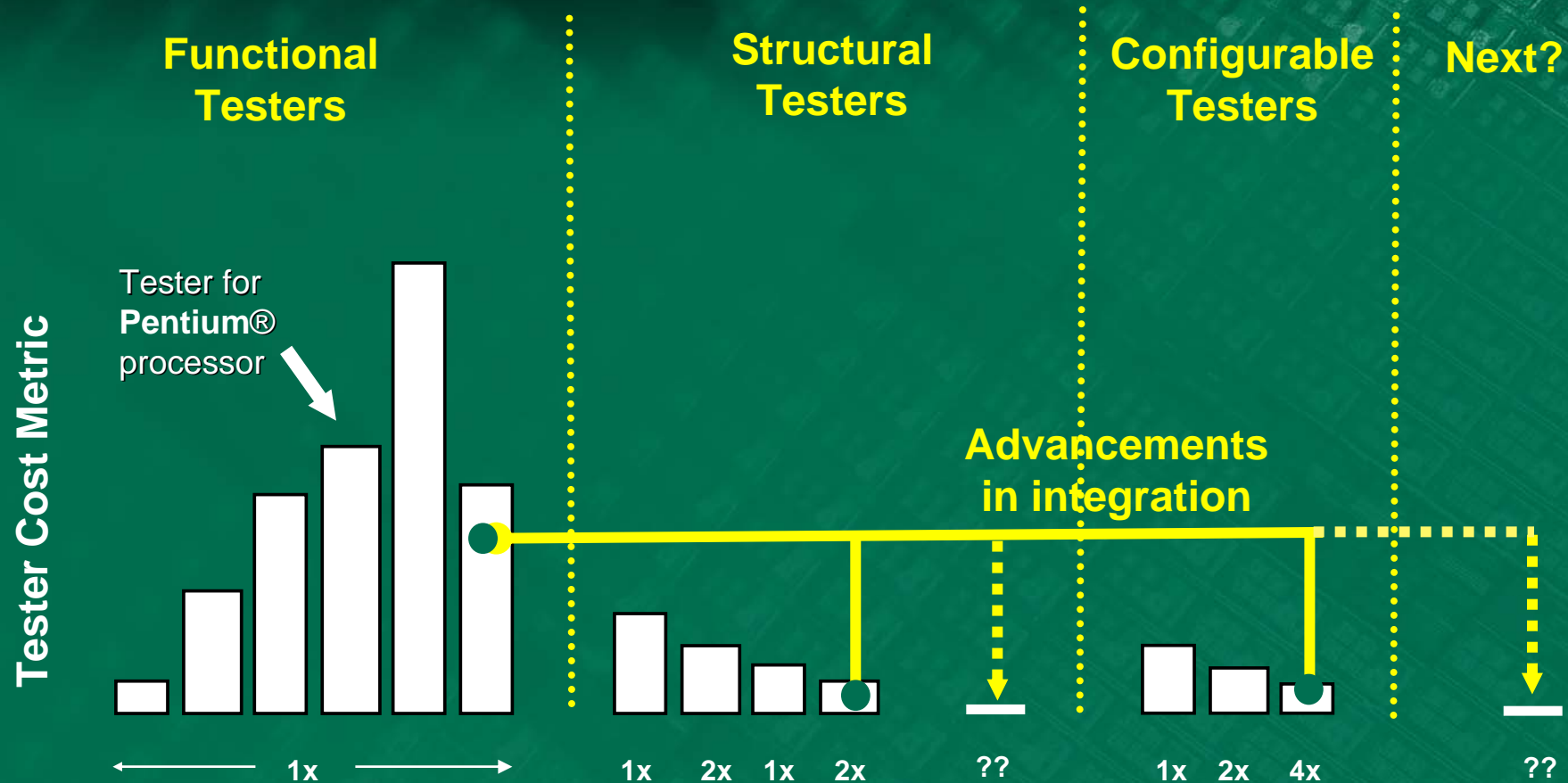


# 1997 SIA Roadmap – Alarming!



- 1997: Predicted per xtor test cost to exceed fabrication cost
- 2001: DFT & Structural Test reduce equipment cost & complexity
  - Lower requirements on I/O data rate, #IO, etc

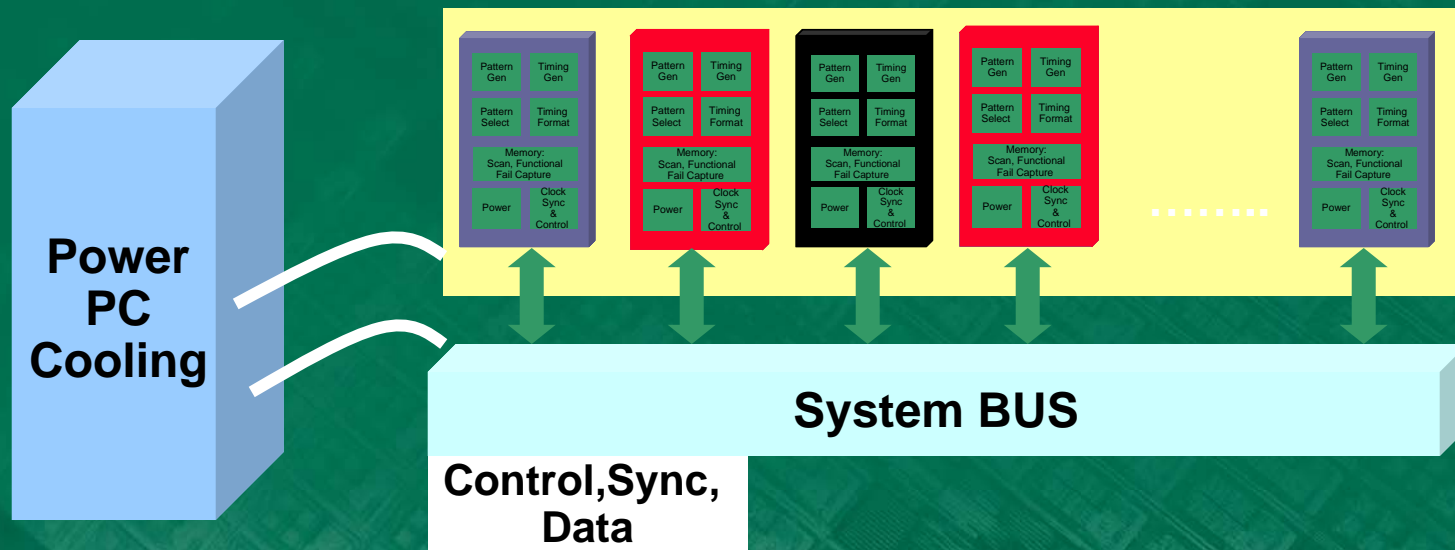
# 1. Developing New Tester Architectures



- Per site wafer tester is 1/10 of 1995 tester
- Distribute tests. Maximize on cheapest tester
- Introduce methods to confine requirements within tester capability
- Develop equipment for increased performance at lower cost

# Configurable Modular Tester (CMT) and Open Architecture

- Common tester shell with replaceable boards
  - True parallel test without any penalty
- Scalable system from commodity through high end
  - Adaptable to changing production demands (i.e. CPU, chipsets, communication products, ...)
  - Upgradeable as new test technology is developed





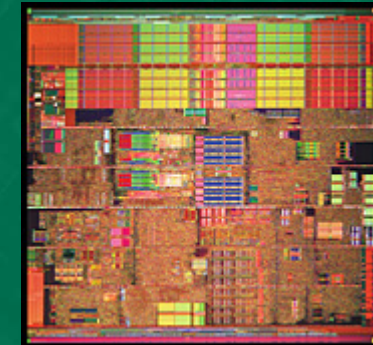
# Intel Test Cost Trends Today

Intel® Pentium® Processor  
on 350nm Technology

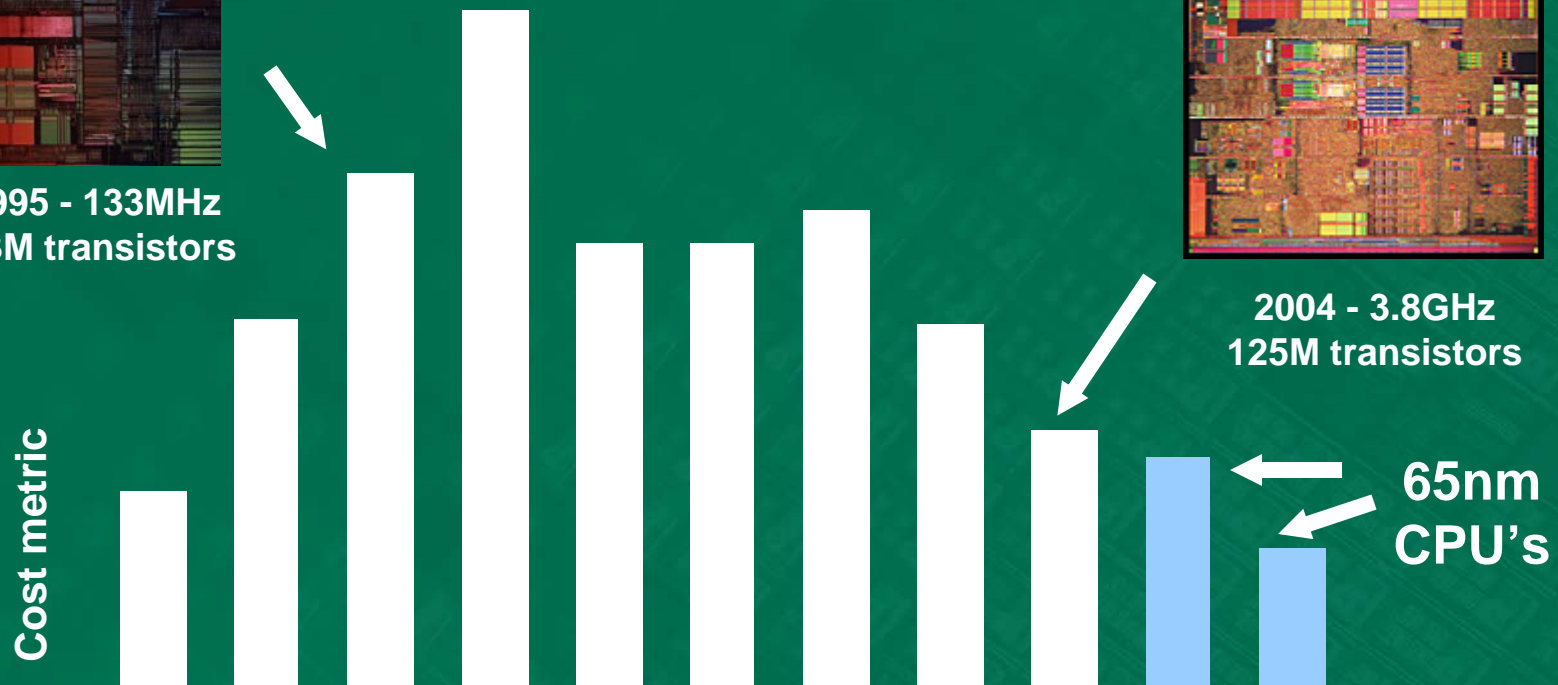


1995 - 133MHz  
3.3M transistors

Intel® Pentium 4® Processor  
on 90nm Technology



2004 - 3.8GHz  
125M transistors

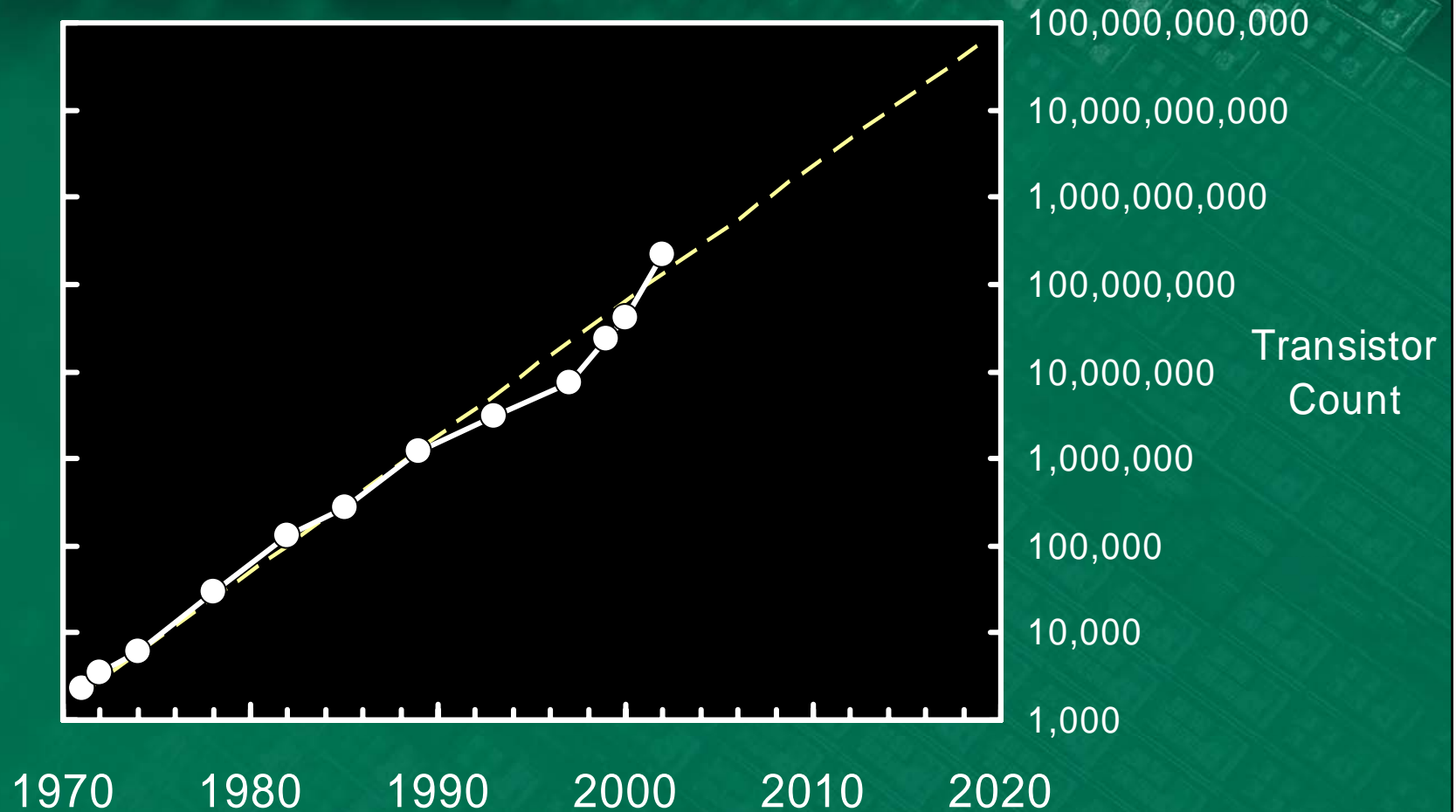


- 65nm CPU's have  $>\sim 80x$  as many transistors as Pentium® processor but cost less to test

**Cost increase projections  
from 1997 were effectively  
curbed with cooperative  
collaboration on Test  
equipment arch (and DFT)**

**But, going forward ....**

# Moore's Law is Alive and Well



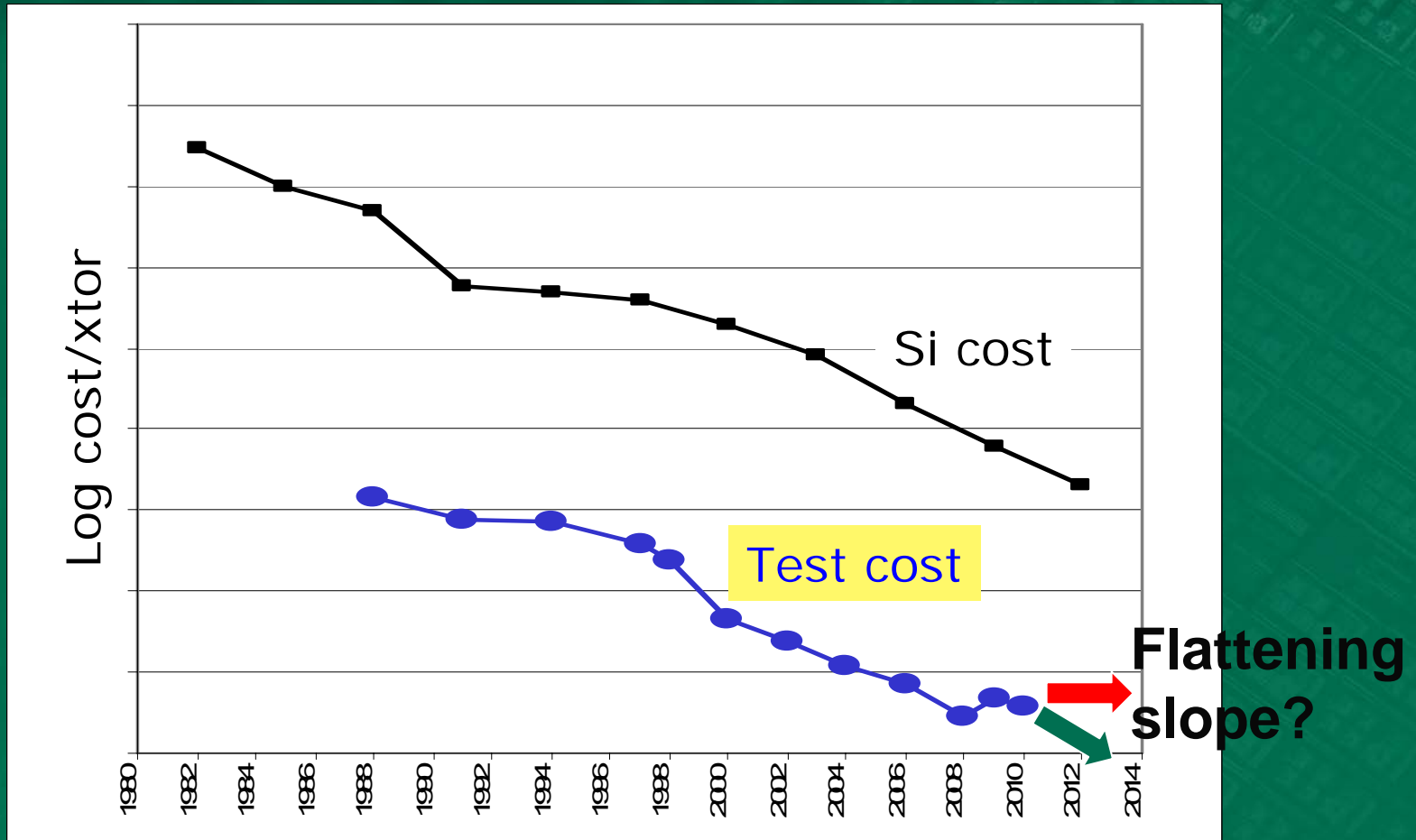
**Finding the path to 100 Billion transistor devices  
Need to reduce test cost/xtor by ~100X in 10-15yrs**

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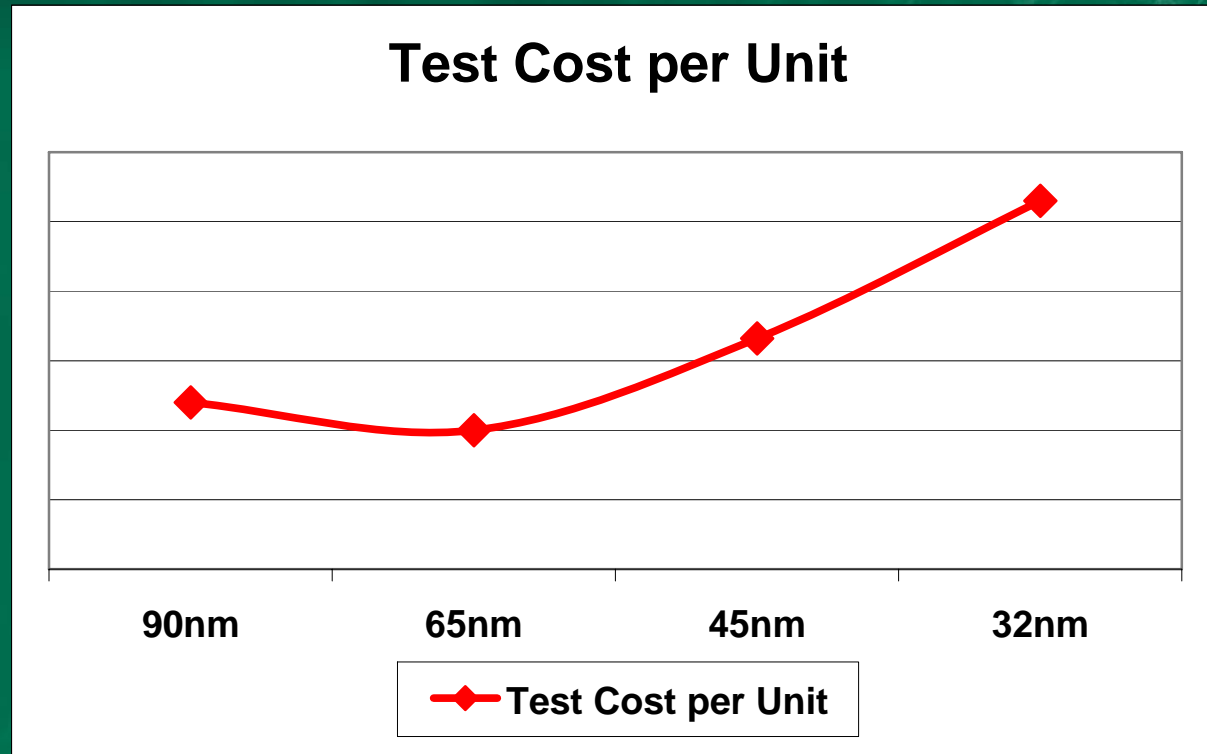
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# Disturbing trends re-emerging ...



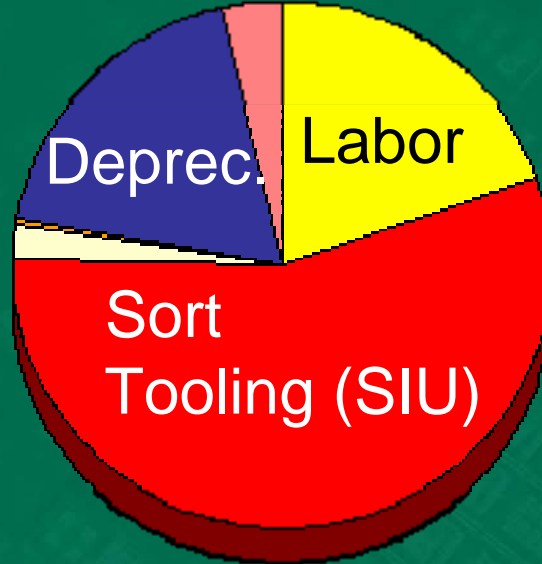
Need actionable plan to cut cost by 10x in ~5yrs

# Something needs to change ....



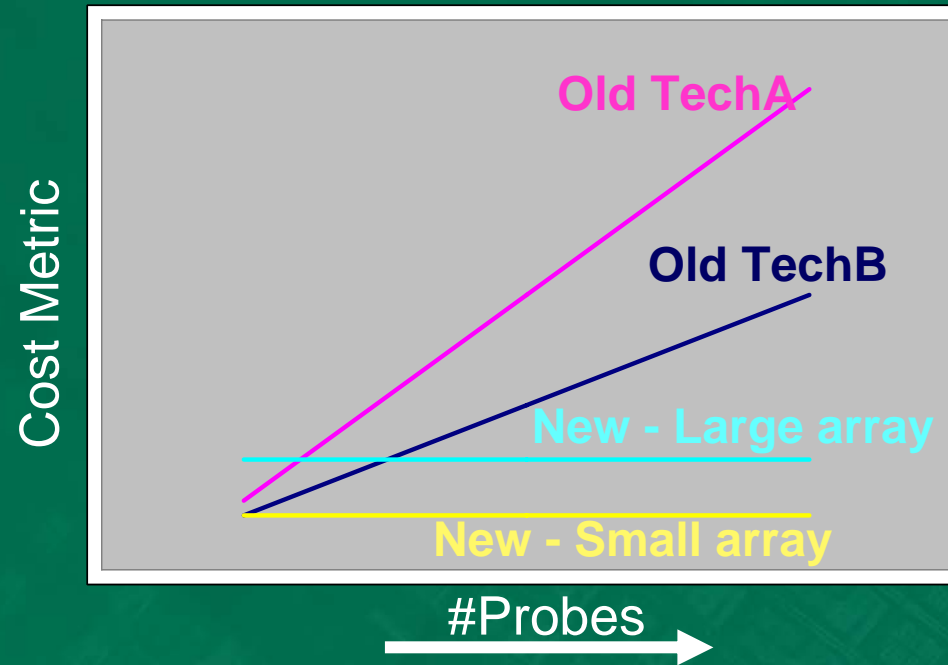
Need actionable plan to cut cost by 10x in ~5yrs

# Tooling >50% Sort cost



SIU costs need to be 1/10<sup>th</sup> current costs in ~5yrs

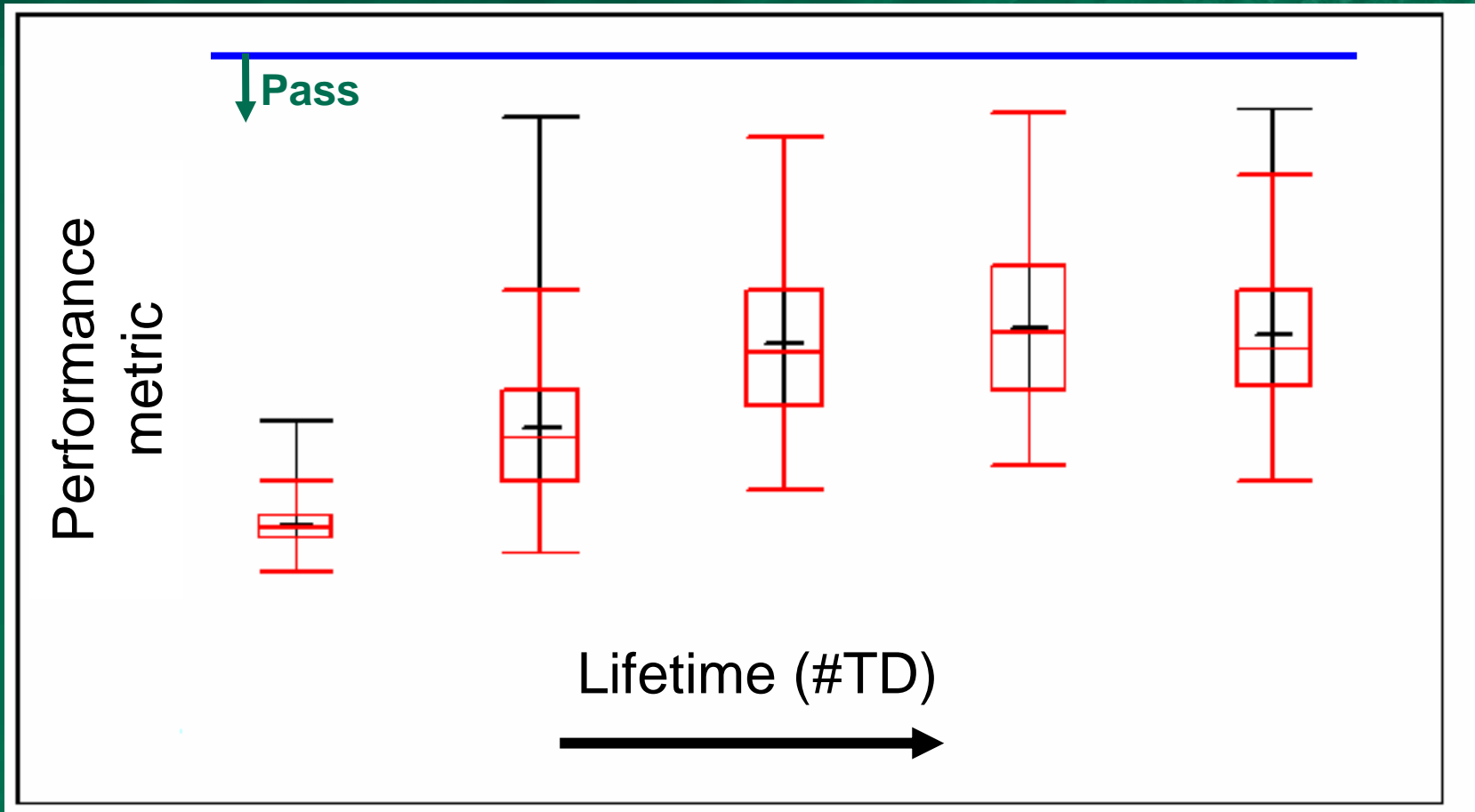
# Technologies with flatter cost structure desired, and they exist



- Expectation: Lower and relatively flat cost. But, ...
- .... Not an order of magnitude reduction. Yet.



# Proof of concept of performance



- Further development required ....

# Parallelism: More economical with flatter cost structure

	Run rate over 1X
2X	>1.x
3X	>2.x
4X	>>2.x

- Parallelism is worth pursuing
- Pick optimal level of parallelism
  - Benefits have not scaled previously because of disproportionate increase in SIU cost

# Known Good Die

Sort Correlation to Class

OK (Today)	Excellent (True KGD)
Probe C4 bumps	????

- Environmental differences a challenge:
  - Thermal, electrical (packaging, xIU), content
- Some can be addressed by improved SIU electrical capabilities

# Other cost levers

- Capital \$
  - Content
    - Do no more testing than required
    - Distribute content proactively across sockets.
  - Reuse or redefine level of integration in equip
- HC \$
  - Automation
  - Simpler process flow within Wafer Test
  - Robust technology
- Reducing need for capital and HC does not reduce tooling\$

# .... And don't forget

- Lead time
- Line item agility

FOR Faster response to:

- Rapidly changing customer demand
- Increased WIP velocity in fab

# Needs for next 10-15yrs

- Cost
- Lead time
- Agility

# Supplier and customer collaboration a must to win

- Agree on what to design + fabricate
  - Comprehend use condition and manufacturing requirements
- Make it
- Make it work in required use condition
- Improve

# Summary: Call to Action

- Reduce SIU cost to  $1/10^{\text{th}}$  in  $\sim 5$  yrs
- Collaboration key to achieving breakthrough results



# Q & A

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