IEEE SW Test Workshop Semiconductor Wafer Test Workshop

REYNAUD Vincent MESATRONIC

D.O.D. TECHNOLOGY® brings new evolutionary solutions in front end probing to face in pad reduction and probing contamination during intermediate level parametric test.

> June 3-6, 2007 San Diego, CA USA

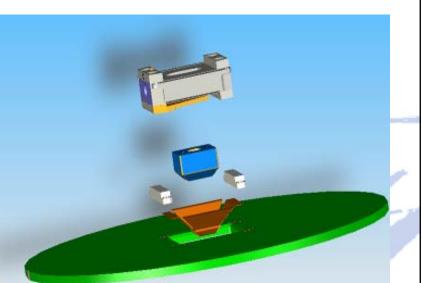


The D.O.D. TECHNOLOGY®

- Vertical technology
- Based on a semiconductor process
- Membrane technology
- Field adjustable probe force
- No alignment variation during Z movement
- Overdrive : 50µm +/-5
- Constrained reliable connection
- Shape : Mesatower
- Typical dimensions
 - Base diameter : 30 to 50 µm
 - Typical Contact diameter : 23 µm
 - Typical Overall height : 50 µm
 - Alignment accuracy +/- 2µm
 - Pad size : 35 µm
- Material : Hard Nickel alloy
- Shear resistant probes

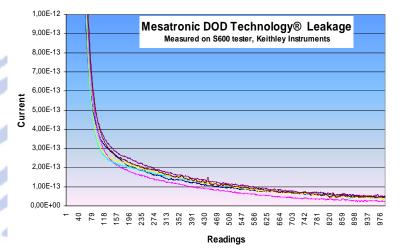
June 3-6, 2007

IEEE SW Test Workshop



Parametric DOD electrical results

- The Parametric DOD development program has involved Joint Development Agreements with Keithely Instruments and the CEA-LETI Research Laboratory.
- Leakage 10 fA/V
- Parasitic Capacitance
 60 fF



June 3-6, 2007

DOD Parametric main advantages

Probe marks / Contamination

Depth inside the pad :-0.4 μmHeight up on the pad :0.6 μmThe number and the size ofparticles removed from thepads is reduced comparedto a cantilever probe cards

Contact Resistance reliability

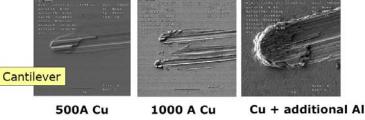
Contact resistance : 0.2 to 0.5 ohm on blank aluminum wafers

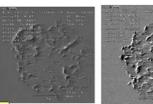
After 1 Million TouchDowns	
Path Resistance	$=2.3\Omega$
R _{contact}	$= 1.1\Omega$
standard deviation	$= 0.4\Omega$
yield	= 99.6%

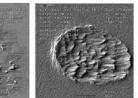
June 3-6, 2007

IEEE SW Test Workshop

Cantilever vs. DoD







DOD

4