IEEE SW Test Workshop
Semiconductor Wafer Test Workshop

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Design Considerations for Parametric-RF Probing in Production Test Environments

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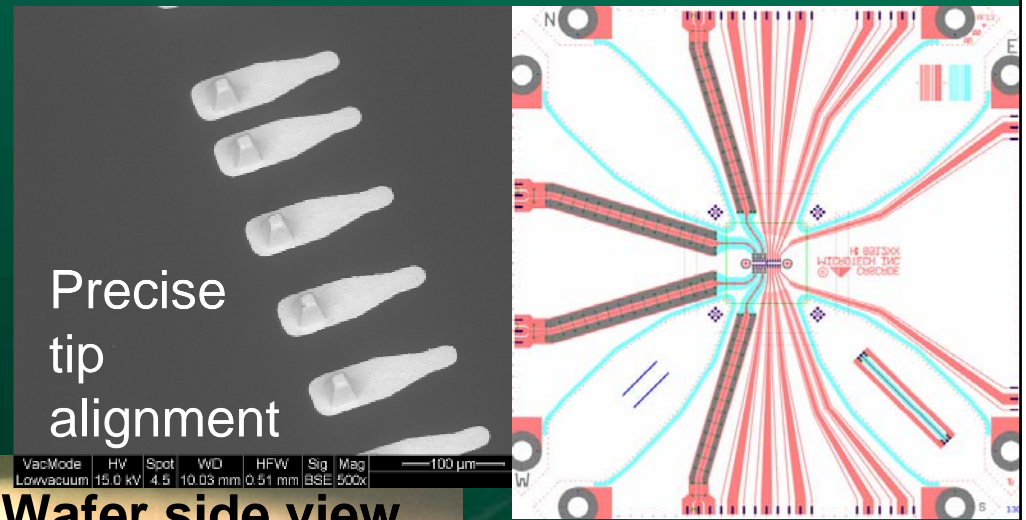
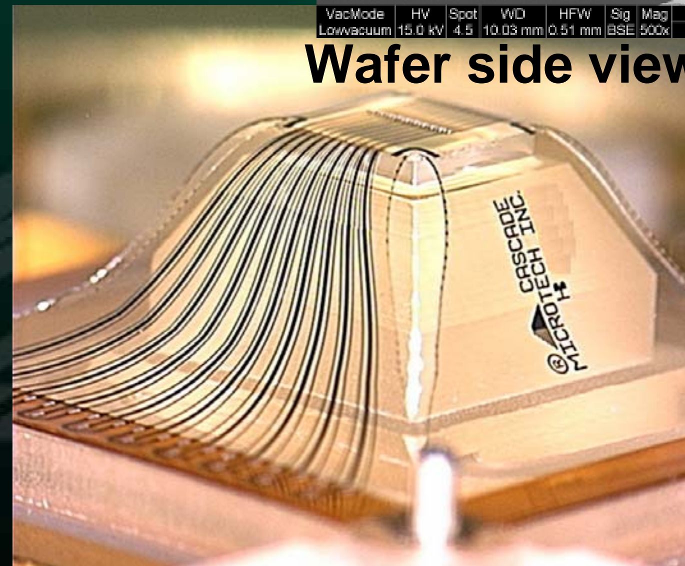
Pyramid Probe for DC + RF Parametric Test

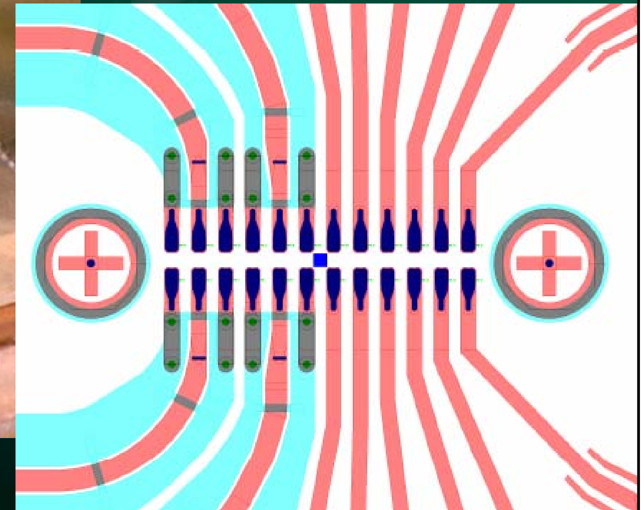
- Inter-die structures for parametric test
- Probe must provide low loss, low noise & low leakage paths to probe tips
- Signal traces are DC-guarded during measurement



- ATE systems include parametric + RF capabilities
- Membrane card supports both:
  - Low loss, lo leakage DC parametric
  - Controlled Impedance RF

Wafer side view

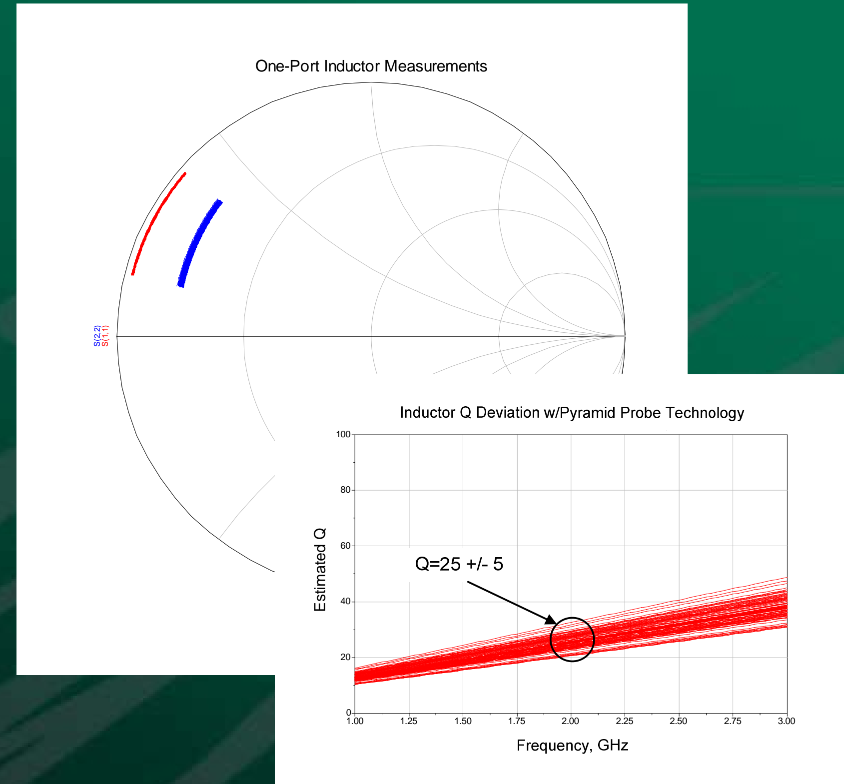




Probe Contact Resistance

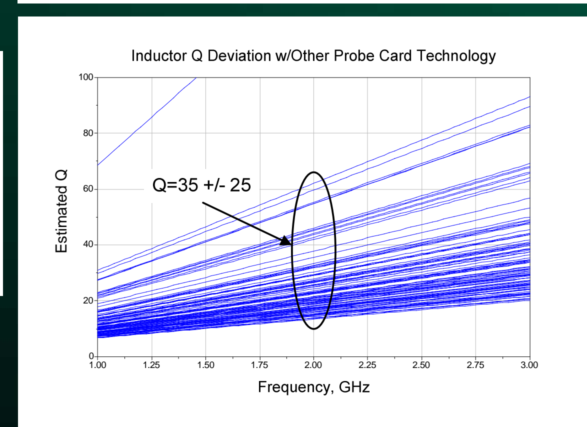
- Low contact resistance is important:
  - Stable resistance can be calibrated out;
  - *Variations* in contact resistance cannot be removed.
- Variations in contact resistance affect:
  - Resistance measurements
  - Device Q calculations
- Example: Inductor Q

Inductance	Path Loss	Frequency	Q
10nH	1 Ohm	150 MHz	9
2.2nH	0.8 Ohm	1 GHz	17
400pH	0.3 Ohm	3.5 GHz	30

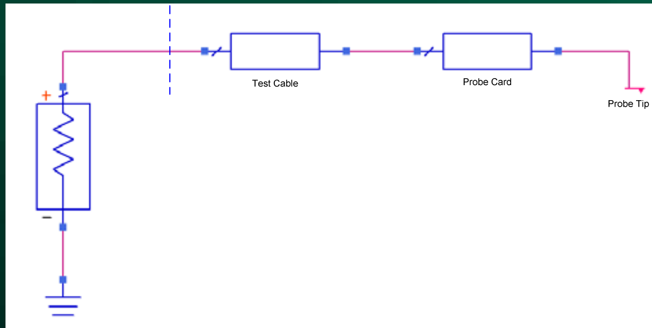


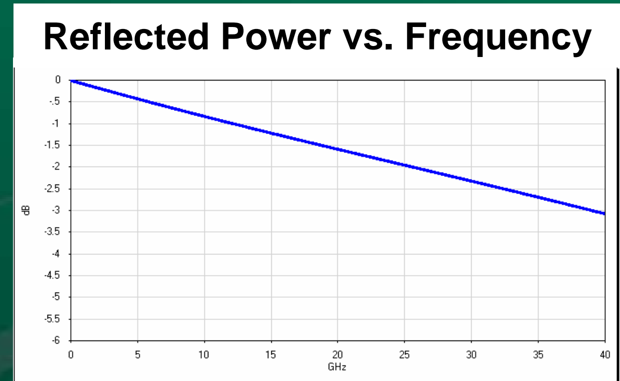
$$X_L = 2\pi f L$$

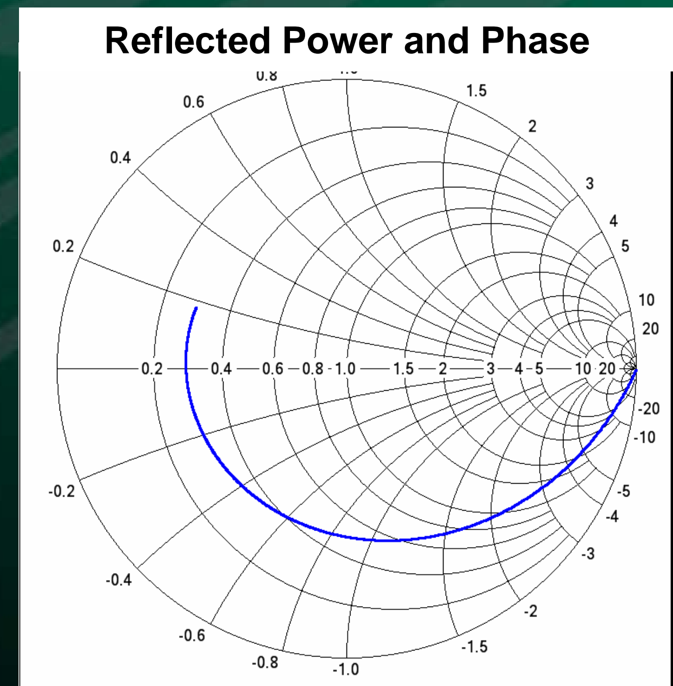
$$Q = \frac{X_L}{R}$$



RF Calibration







- Removing the anomalies from the measurement system
  - Eliminate electrical delay
  - Eliminate path loss
- Account for temperature, humidity, aging.
- Routine re-calibration required.
- *Measure only the device, not the probe card.*

- VNA: Vector Network Analyzer. Measures Reflected Power and Phase.
- *Calibration must be performed whenever anything between the VNA and the probe tip has been altered.*

- *(With RF calibration, the loss & delays shown here are characterized & removed).*