Design Considerations for Parametric-RF Probing in Production Test Environments
Outline

- Pyramid Probe Technology
- Parametric Measurements
- RF Parametric
- Design Considerations
  - Contact Resistance
  - Calibration
  - Probe Card Validation
Pyramid Probe Technology

- Full-custom to match die layout
- Thin film high-tech flex-circuit
- Controlled impedance transmission lines
Pyramid Probe for Parametric Test

- Inter-die structures for parametric test
- Probe must provide low loss, low noise & low leakage paths to probe tips
- Signal traces are DC-guarded during measurement

- Probe tips
- Guarded signal traces to probe tips
- Guarded circuit board interface

Wafer side view

Precise tip alignment
Parametric Test

- DC / AC Measurements
  - Resistance
  - Leakage current
  - Source impedance
  - Capacitance, inductance

- Techniques
  - C-V
  - I-V
  - HF C-V (to 100-300 MHz)

- RF Measurements (1-40+ GHz)
  - Active:
    - $F_t$, $F_{\text{max}}$
  - Passive:
    - Inductors, Capacitors
    - Q

- Techniques
  - RF C-V, I-V
  - Network Analysis
    - (S-Parameters)
RF Measurements

- $F_t$ – Active device frequency of unity gain
- $F_{\text{max}}$ – Maximum oscillation frequency
- $Q$ – Reactance vs. passive losses

Device Gain vs. Frequency

![Graph showing device gain versus frequency](image)
Combining Parametric & RF Measurements

- ATE systems include parametric + RF capabilities
- Membrane card supports both:
  - Low loss, low leakage, DC parametric
  - RF: Controlled impedance, low loss
- Probe card layout matches on-wafer test structures
Probe Contact Resistance

- Low contact resistance is important:
  - Stable resistance can be calibrated out;
  - *Variations* in contact resistance cannot be removed.
- Variations in contact resistance affect:
  - Resistance measurements
  - Device Q calculations
- Example: Inductor Q

<table>
<thead>
<tr>
<th>Inductance</th>
<th>Frequency</th>
<th>$X_L$</th>
<th>Resistance</th>
<th>Q</th>
</tr>
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<tr>
<td>10nH</td>
<td>150 MHz</td>
<td>9.4 Ohm</td>
<td>1 Ohm</td>
<td>9</td>
</tr>
<tr>
<td>2.2nH</td>
<td>1 GHz</td>
<td>13.8 Ohm</td>
<td>0.8 Ohm</td>
<td>17</td>
</tr>
<tr>
<td>400pH</td>
<td>3.5 GHz</td>
<td>8.8 Ohm</td>
<td>0.3 Ohm</td>
<td>30</td>
</tr>
</tbody>
</table>

\[ X_L = 2\pi fL \]

\[ Q = \frac{X_L}{R} \]
Probe Contact Resistance

- Example: Inductor Q
  - One-port ($S_{11}$) calibrated
  - False-positive Q possible due to low $R_{\text{contact}}$ during calibration.

![Inductor Q Deviation w/Pyramid Probe Technology](image1)

![Inductor Q Deviation w/Other Probe Card Technology](image2)
RF Calibration

- Removing the anomalies from the measurement system
  - Eliminate electrical delay
  - Eliminate path loss
- Account for temperature, humidity, aging.
- Routine re-calibration required.
- Measure only the device, not the probe card.

- Calibration must be performed whenever anything between the VNA and the probe tip has been altered.

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Calibration Techniques

- Cable Calibration:
  - Mechanical Standards:
    - Short, Open, Load, Thru…., ECal, etc.
- Port Extensions:
  - Extend reference plane to the probe
  - Subtract estimated (linear) path loss
- Fixture De-embedding:
  - Characterize path loss for each port
  - VNA augments error-set with this data
- Tip Calibration:
  - Probe onto standards:
    - Short, Open, Load, Thru….
  - Advanced algorithms characterize the errors. Correction factors are stored in the VNA.
- **Parametric RF test requires high accuracy, repeatable measurements.**
Impedance Standards for RF Calibration

- Useful for tip calibration, probe card validation
- GSG 100um Standards:
  - Shorts, thru paths, 50 ohm loads, etc.
- Other structures to match popular probe configurations:
  - Varying pitch
  - Varying topology (GSGSG, etc.)

- Use GSG probe configuration

- Match pad layout to standards, whenever possible.

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Establishing a Plan for Calibration

- Choose your calibration algorithm:
  - SOLT, SOLR, LRM, LRRM, etc.
- Have appropriate standards available:
  - ISS mounted on tester
  - ISS on wafer
  - Standards fabricated on wafer
- Establish a calibration schedule
- Determine where the calibration will be implemented:
  - VNA, embedded, PC, etc.
- Validate calibration & probe card assembly:
  - Probe onto known standards
  - Sample structures
- Test the entire procedure with known standards.

- General purpose ISS:
  - Sea of gold, 50 ohm loads.
  - Miscellaneous resistive loads
Probe Card Validation

• Calibrate to the probe tips:
  – SOLR allows for a general purpose thru.
  – LRRM:
    • Highly repeatable measurements.
    • Requires a perfect thru-path.
• Validation:
  – Verify calibration by landing onto known standards.
  – Example: Perfect Short, after an SOLR calibration.

- Smith chart reveals one dot.
- Magnitude Power (dB) plot reveals all energy is reflected.
  (The loss variation is minimal).
Probe Card Validation

- Inductor & Capacitor:
  - Inductor appears as a short at DC.
  - Capacitor appears as an open at DC.
Incorrect Standards

- Poor calibration:
  - When a short is not a short:
    - (left side of Smith chart)
  - When an open is not an open:
    - (right side)
  - Calibration should never reveal “gain”
Incorrect Calibration

- Example: Long, open transmission line.
  - General pattern matches expectations.
  - Calibration is poor.
- Verify expectations on the Smith chart.
  - Magnitude power may not reveal enough information.
Probe Card Validation

- Open Transmission Line stub:
  - Two calibration examples:
    - Good cal reveals little or no loss through 40 GHz.
    - Other calibration reveals ~1 dB loss at 40 GHz.
Conclusion

- Parametric RF Test establishes improved methods for process monitoring:
  - Device characterization.
  - At-frequency component validation.
- Establish a plan for calibration.
  - Establish a location for calibration standards within the ATE.
  - Know and understand the limitations of your measurements.
- Validate your probe card with something other than your DUT.
  - Develop experience with the system to assure that calibration functions as expected.