IEEE SW Test Workshop
Semiconductor Wafer Test Workshop

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Xandex, Inc.

Theory and Test Methods for Board-to-Board Interposer Technologies

Topics

- What is the function of a board-to-board interposer?
- Contact Probability
- How is an electrical connection made?
- Testing methodologies
- Commercially available solutions

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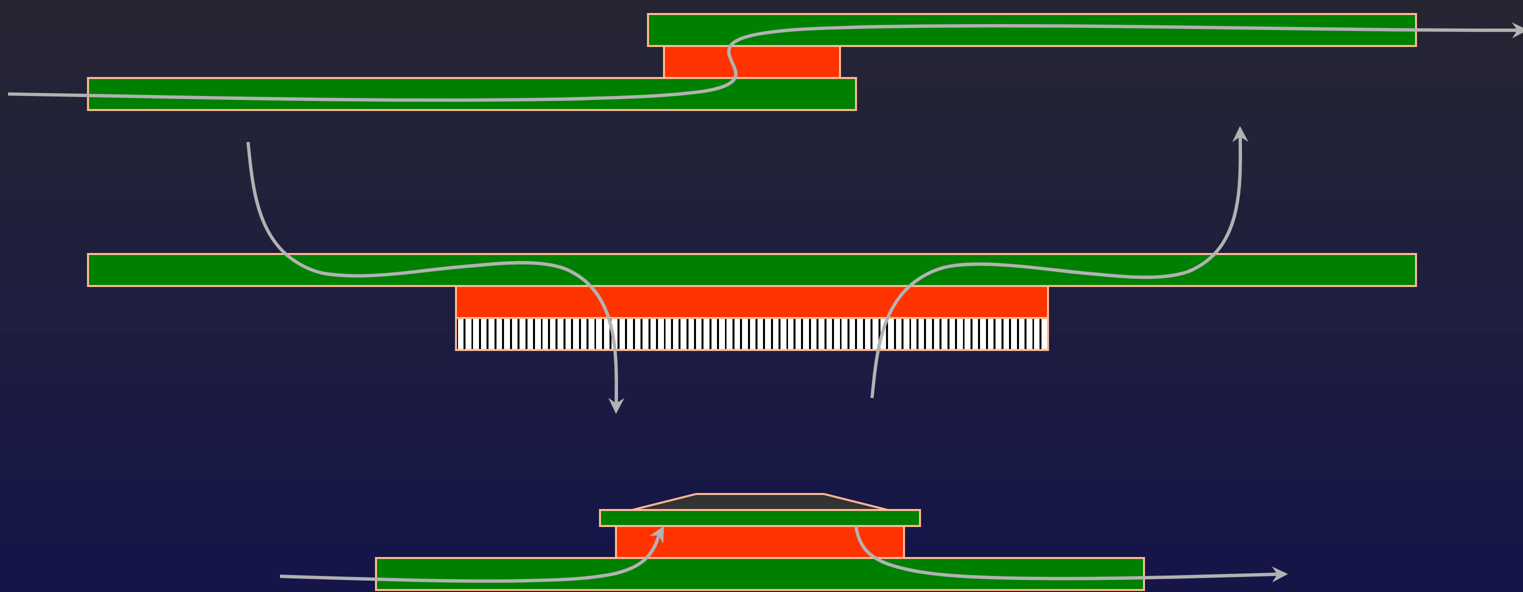
What good are they?



They connect things

Topics

- What is the function of a board-to-board interposer?
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- Testing methodologies
- Commercially available solutions

So what's so hard about that?

- It's all about the probabilities –
  - '80s Trillium tester used 640 spring pins – any 5σ-performance interconnect solution would work

*http://www.swtest.org/swtw_library/2004proc/PDF/S01_03_Sinsheimer.pdf

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    - 1,000,000 / 6400 = 156 DPMO or 5.1σ or a Cpk of 1.7
    - That's a reasonable expectation of an off-the-shelf spring pin*

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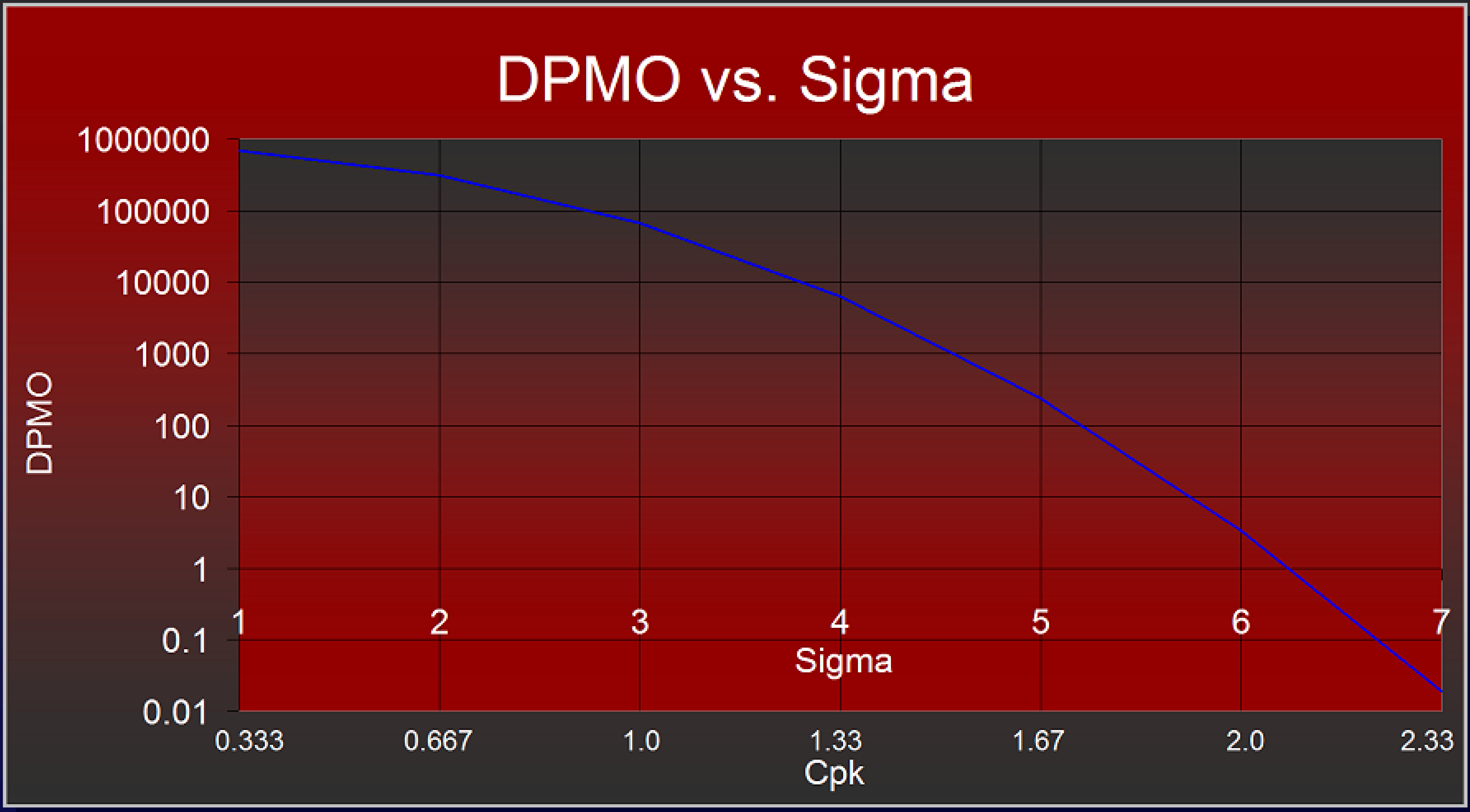
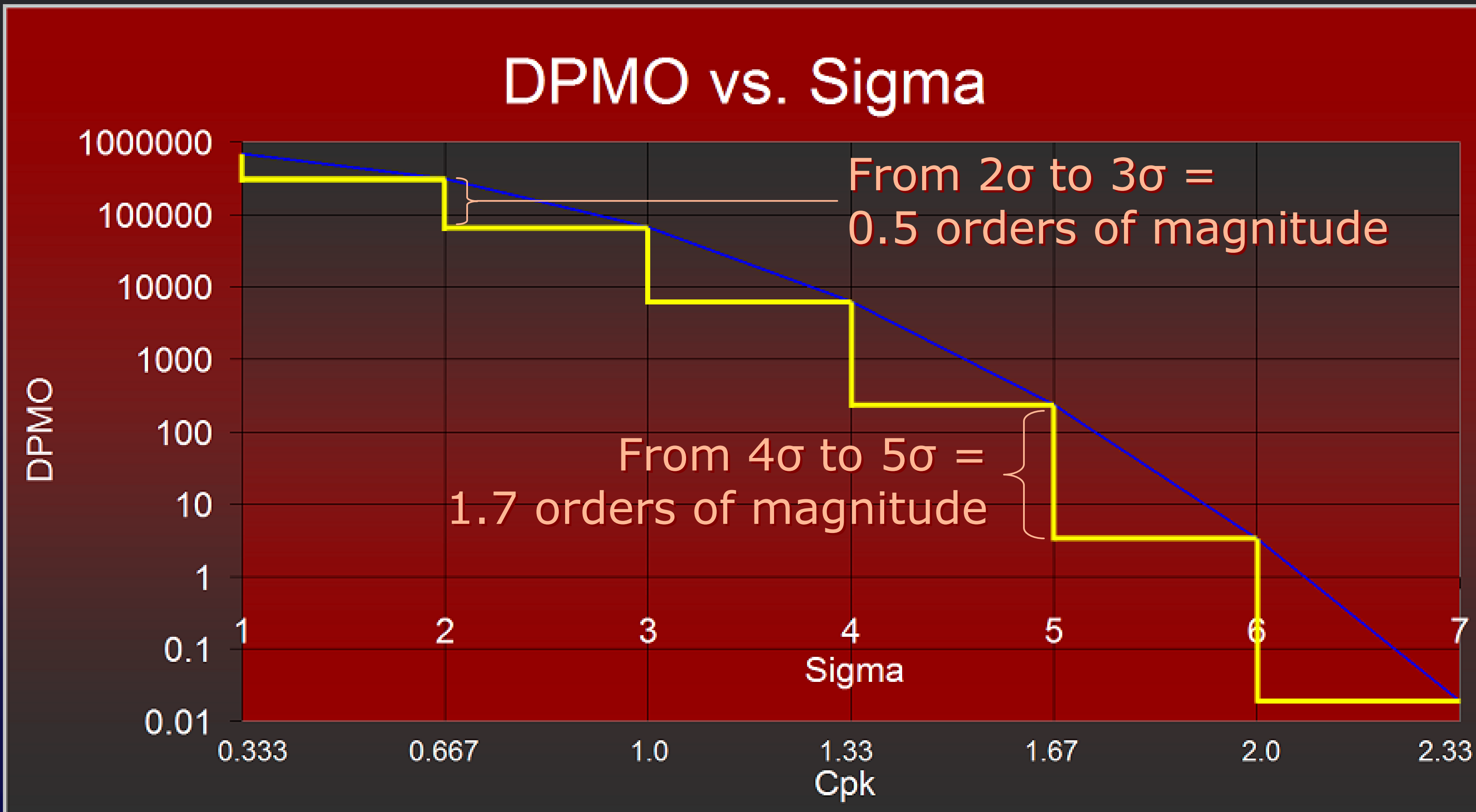
In case you're too young to know what a Trillium Pogo™ tower looked like

This 640-pin interface was sufficient to test the Intel '386 microprocessor generation, as well as the early '486's

Quick statistics review

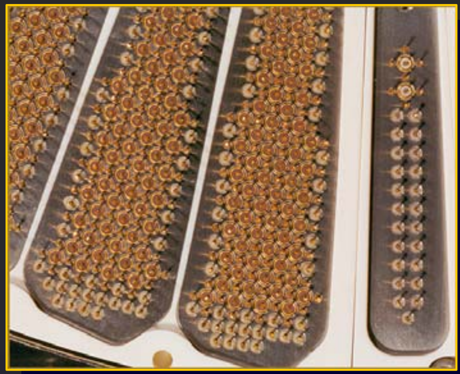
Process σ	DPMO	Cpk
1	691,462	0.333
2	308,538	0.667
3	66,807	1
4	6,210	1.33
5	233	1.67
6	3.4	2
7	0.019	2.33


DPMO vs. Sigma
DPMO
1000000
100000
10000
1000
100
10
1
0.1
0.01
1
2
3
4
5
6
7
Sigma
0.333
0.667
1.0
1.33
1.67
2.0
2.33
Cpk



DPMO vs. Sigma
1000000
100000
10000
1000
100
10
1
0.1
0.01
DPMO
From 2σ to 3σ =
0.5 orders of magnitude
From 4σ to 5σ =
1.7 orders of magnitude
1
2
3
4
5
6
7
Sigma
0.333
0.667
1.0
1.33
1.67
2.0
2.33
Cpk

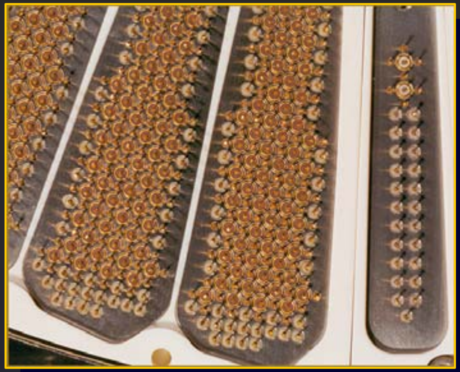
So what?



- Agilent V4400 spring probe interface* had 7290 spring pins
  - Will 5σ interconnect technology work?
    - 7290 x 0.000233 (5σ DPMO) = 1.7
      - i.e. failure to fully connect about 40% of the time

*http://www.swtest.org/swtw_library/2001proc/PDF/S6_04.pdf

So what?



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  - Will 5σ interconnect technology work?
    - 7290 x 0.000233 (5σ DPMO) = 1.7
      - i.e. failure to fully connect about 40% of the time
  - One “open” every <u>20</u> probe card docks
    - 5.85σ performance (Cpk 1.95) is required**

*http://www.swtest.org/swtw_library/2001proc/PDF/S6_04.pdf
**S01_03_Sinsheimer.pdf, loc. cit.

It only gets worse

- Agilent V5400 interface has 22.5k contacts
  - 5σ-class performance <u>will not work</u>
  - Allow one open every <u>40</u> probe card dockings
  - That's 1.1 DPMO, or 6.25σ, or a Cpk of 2.08

This is getting difficult

And worse

- One next-gen ATE wafer probe interface architecture requires 186,600 connections
- To be functional, contact technology must meet:

<0.134 DPMO / $>6.7\sigma$ / >2.2 Cpk

Topics

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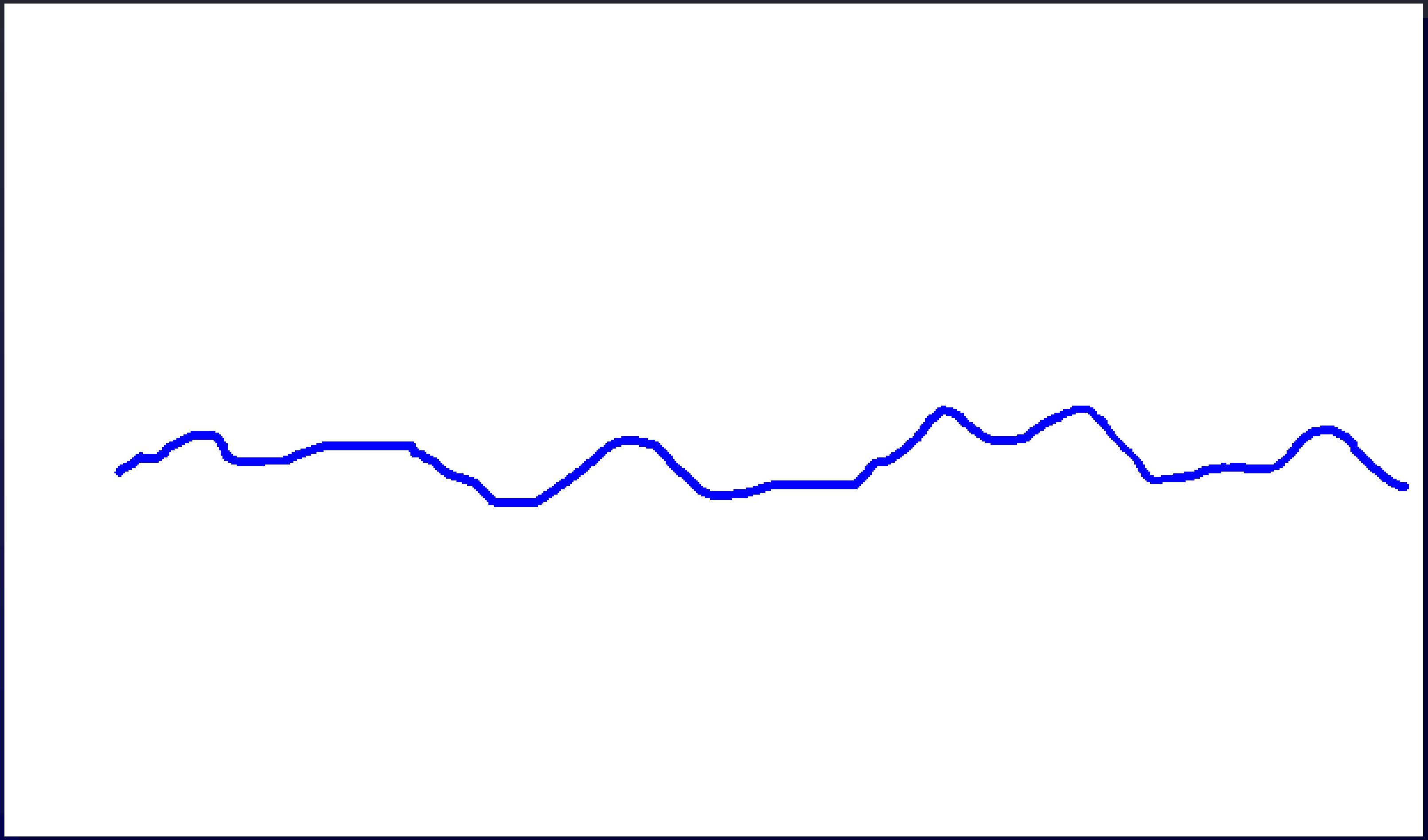
So what's the problem?

- Jam two pieces of metal together, introduce a voltage difference and then the current flows, first time, every time.

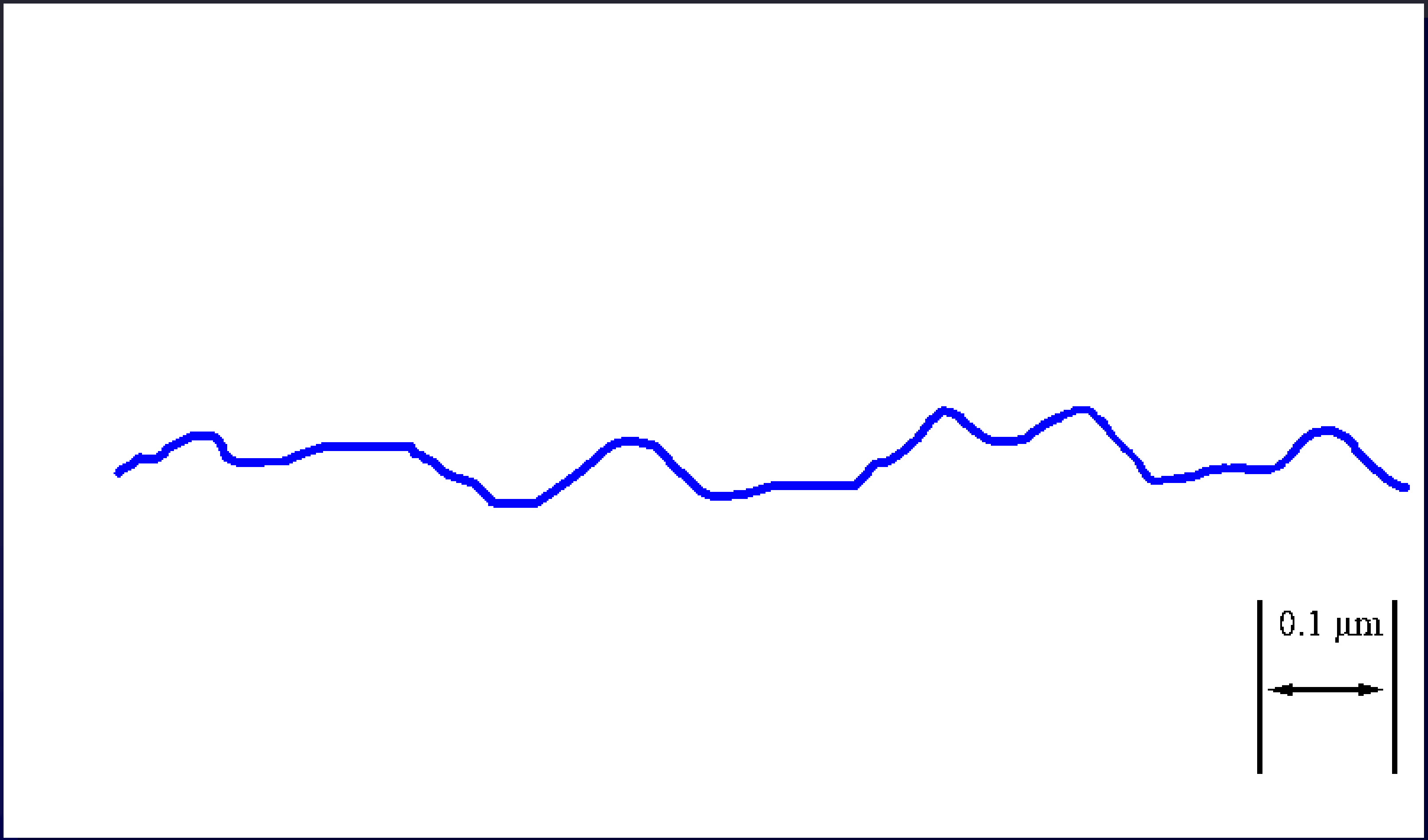
Right?

A surface

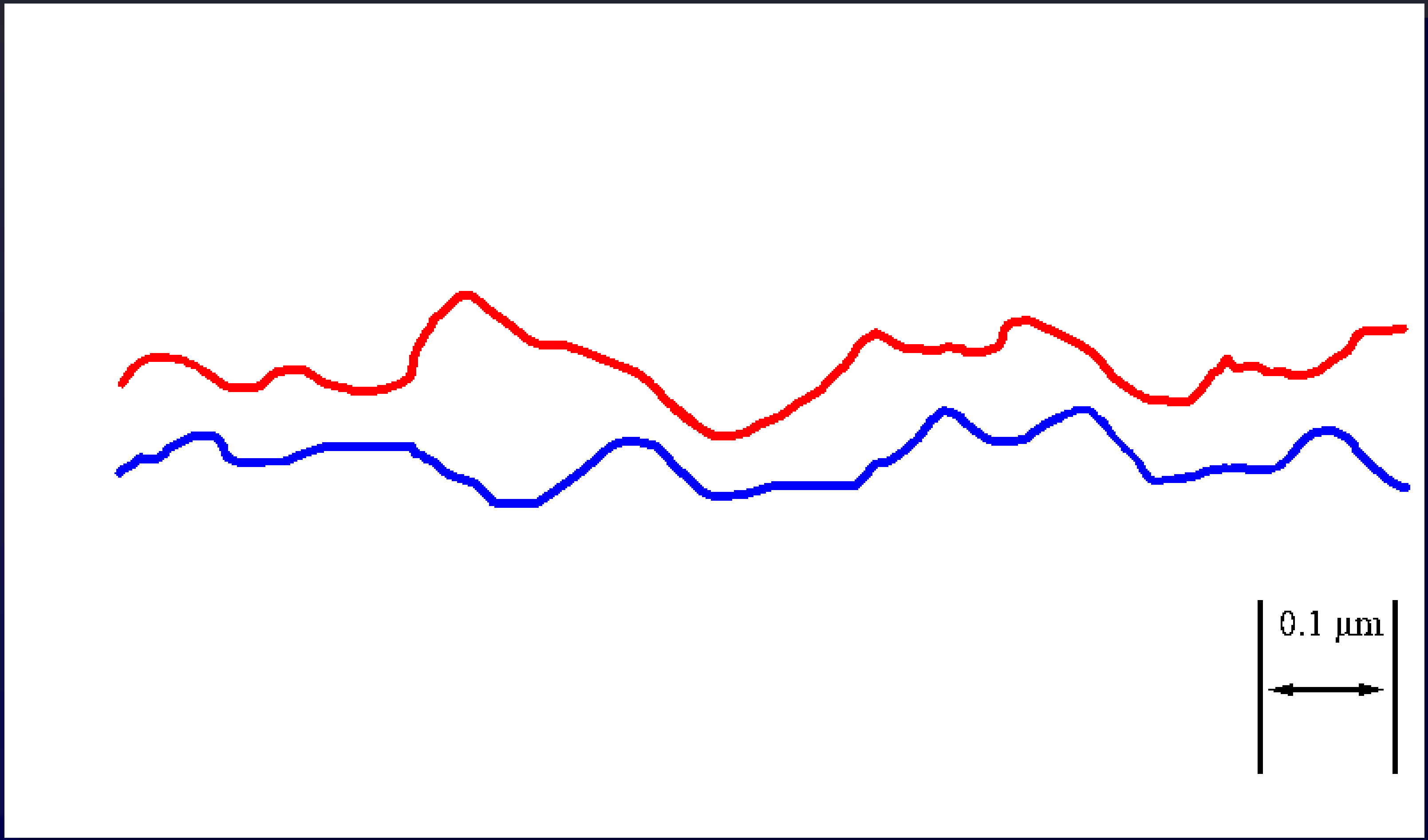


A mirror smooth surface

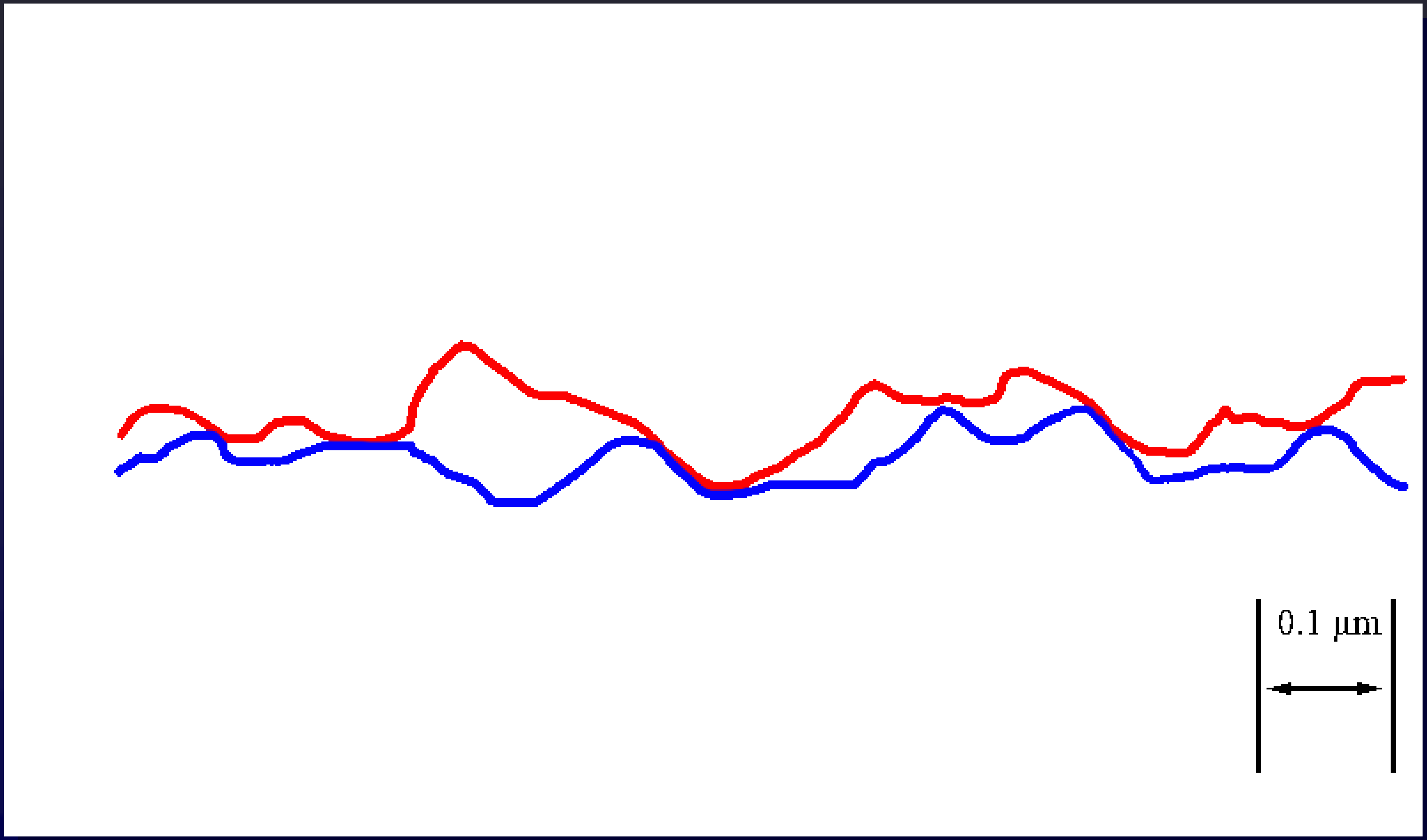
Note: Heavy-service contact gold plating is 1.3 μm (50 μ-in) thick



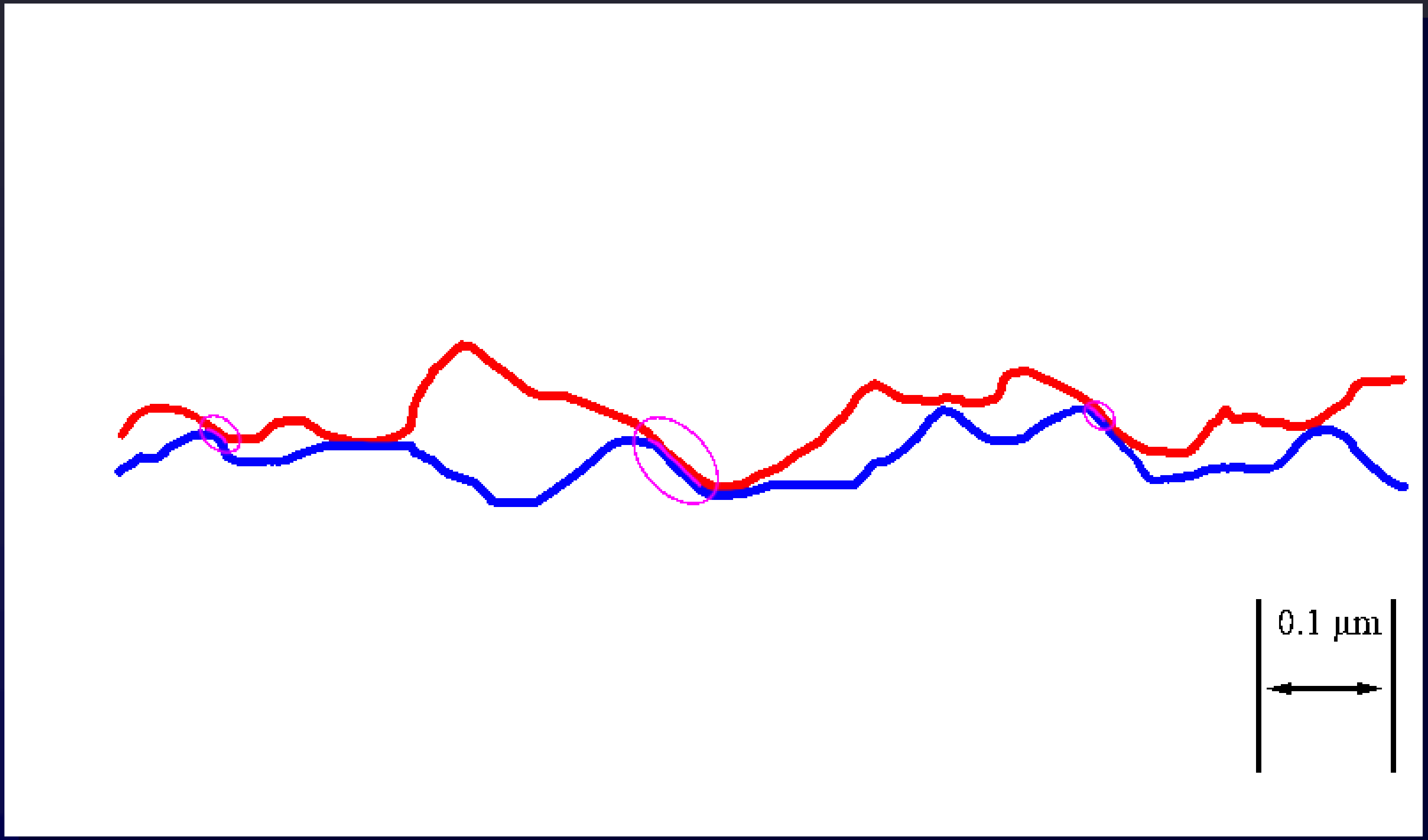
Another surface



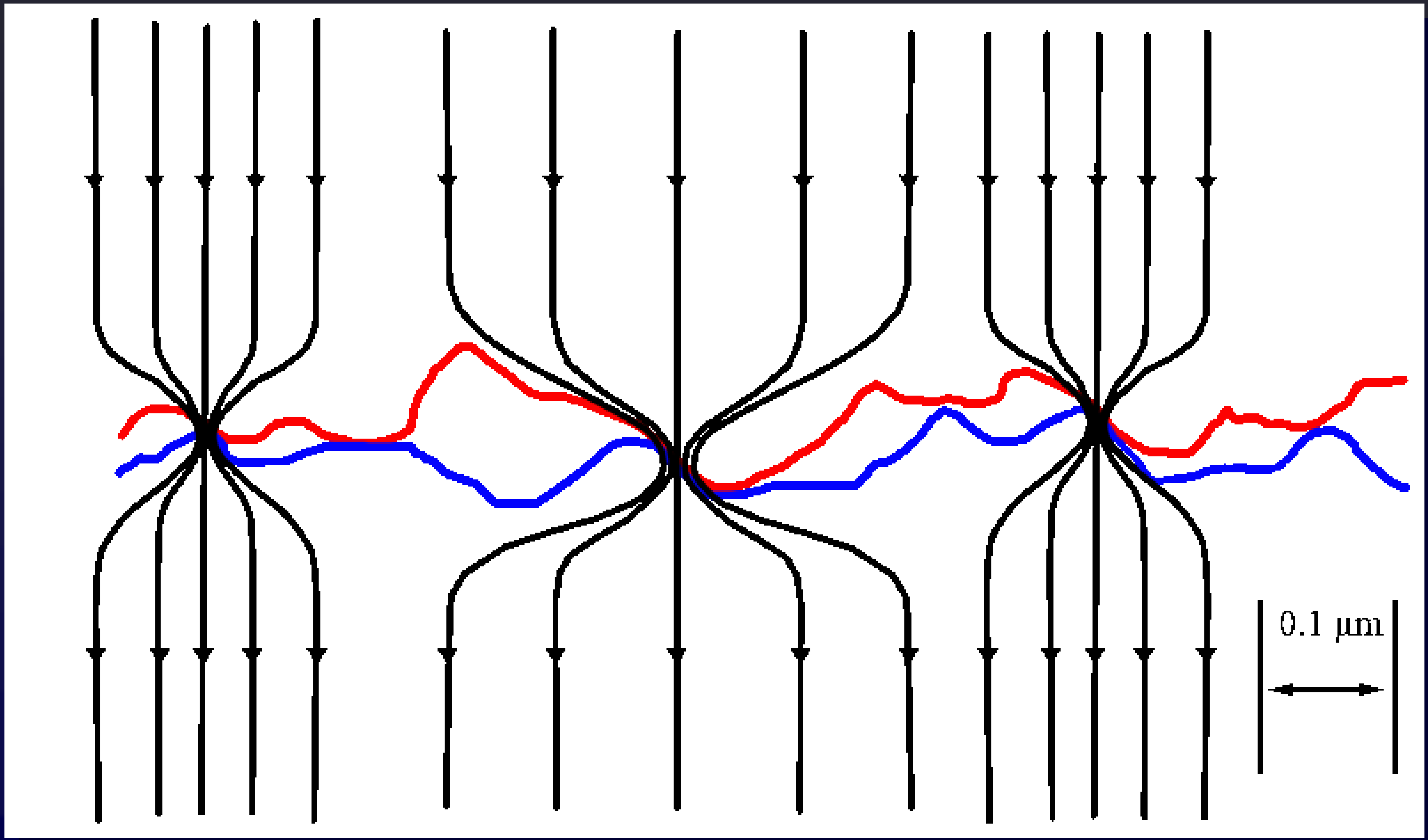
They meet



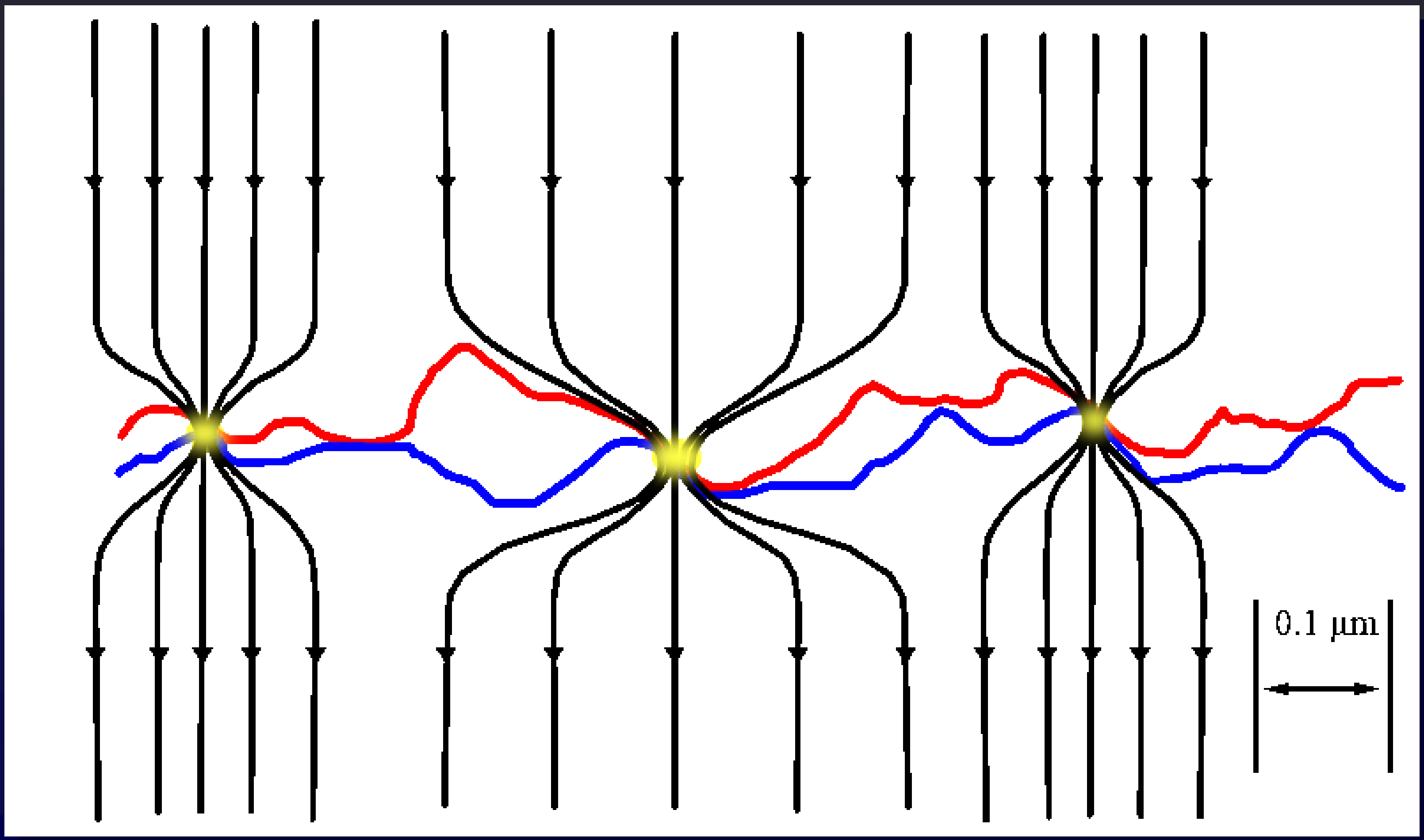
There's pressure – >250,000 PSI (1720 MPa)



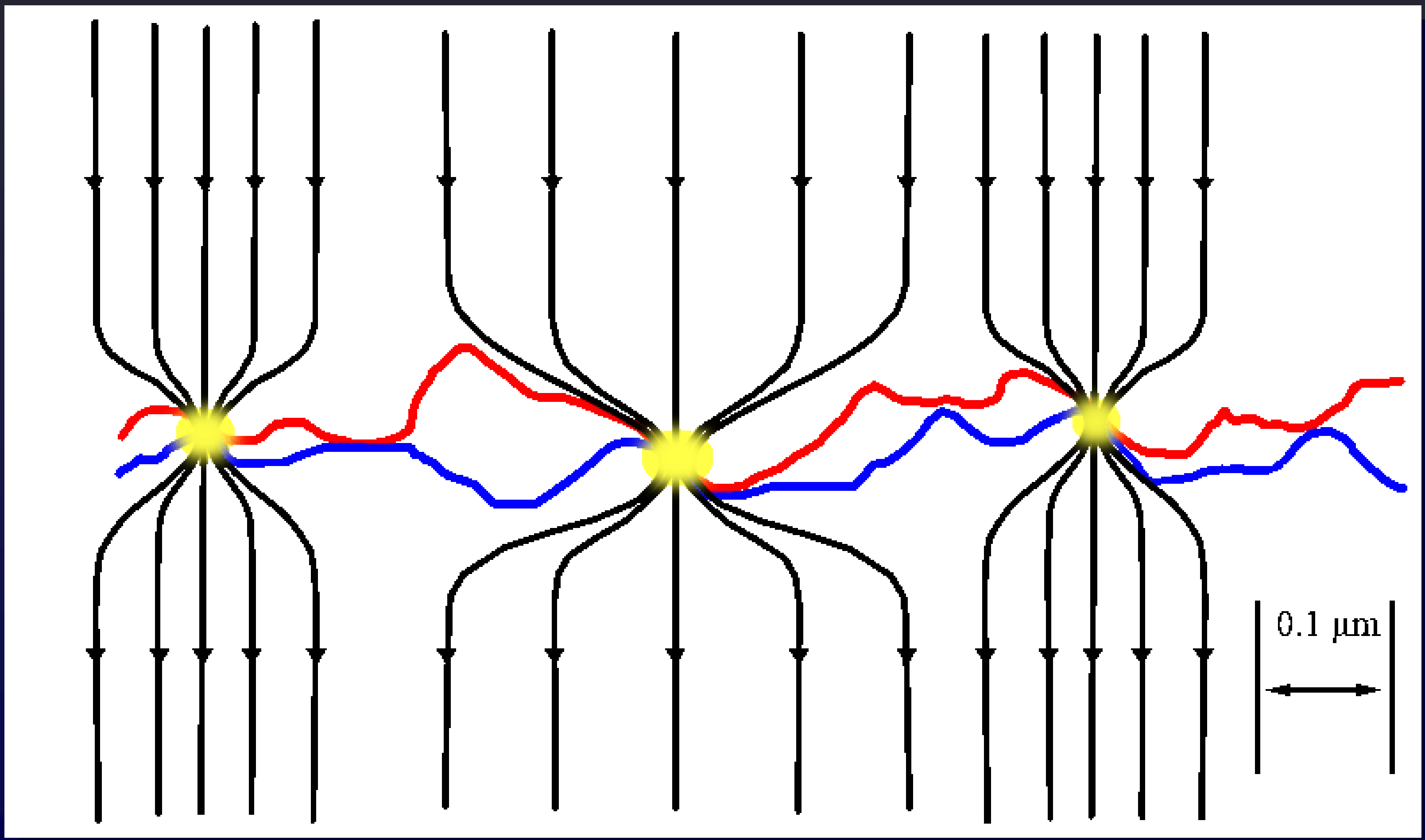
With a voltage difference, there's current flow



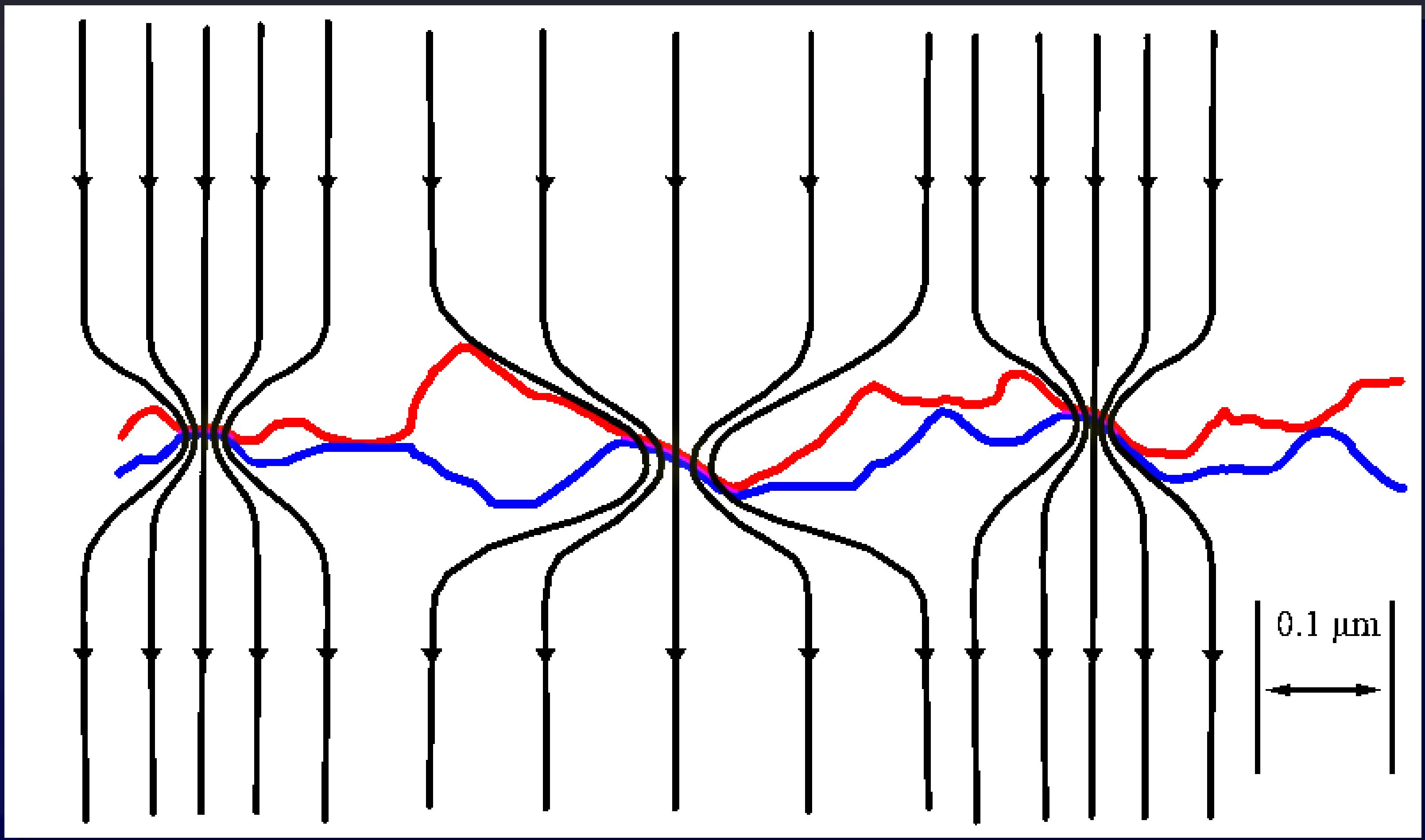
Things are getting hot



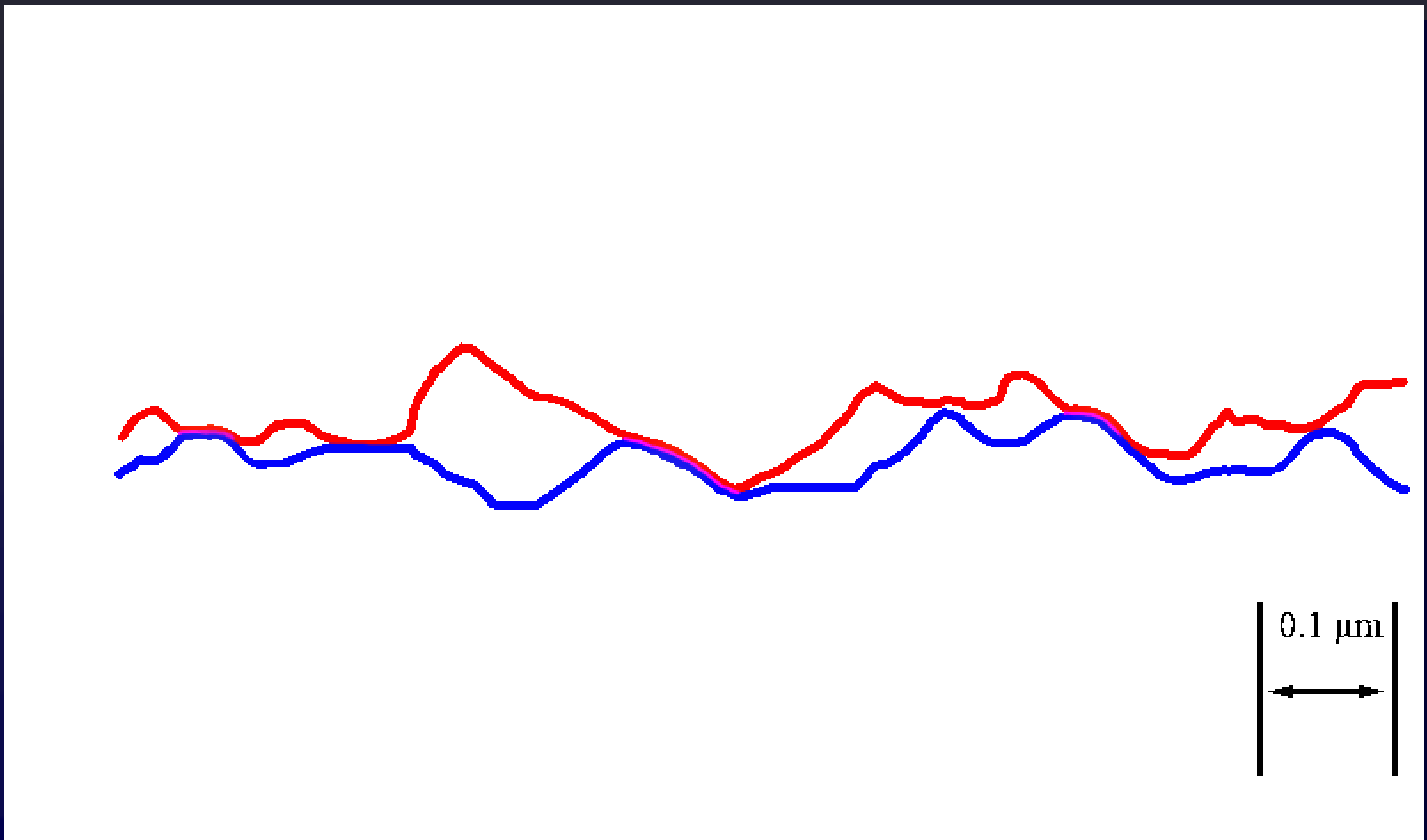
Really hot (sintering may also be occurring)



Equilibrium is reached

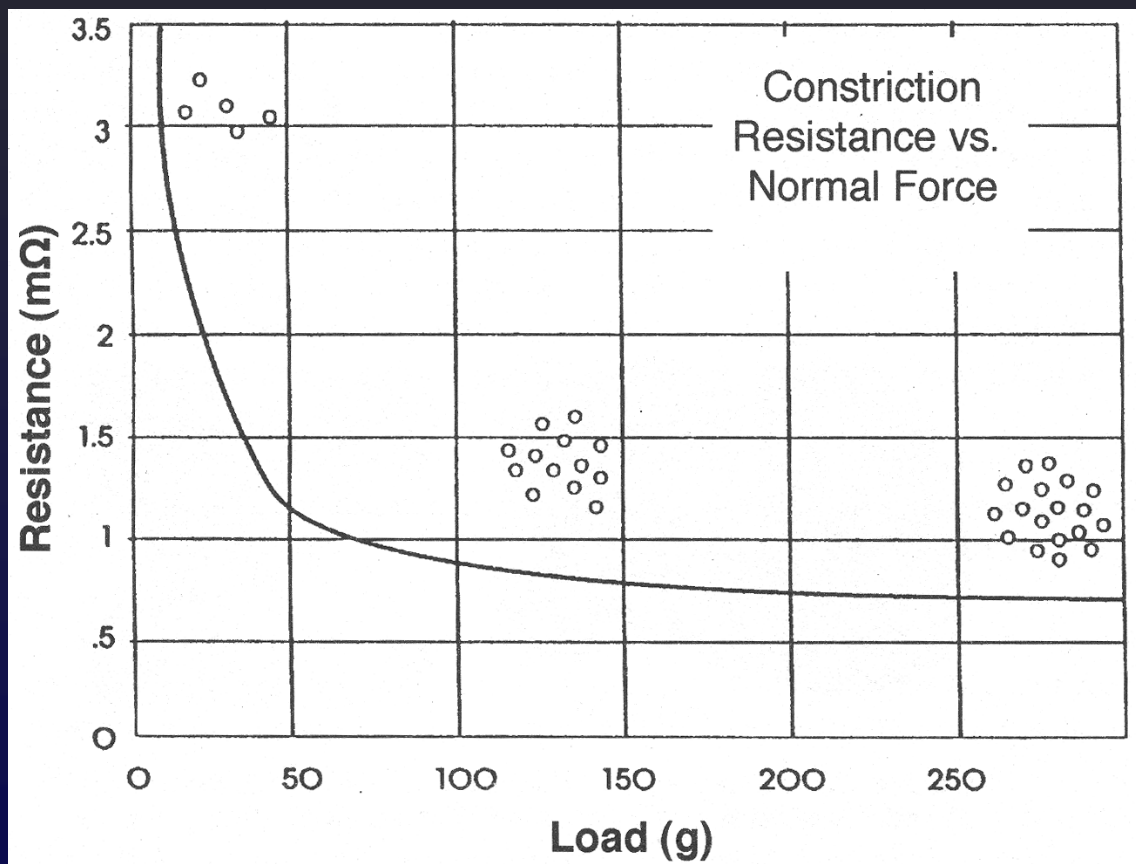


Surfaces are bonded



Let's put it all together

Force required to make contact



Images on this and the next slide from: *Electronic Connector Handbook* by Robert Mrockzkowski

α-spots (asperities)

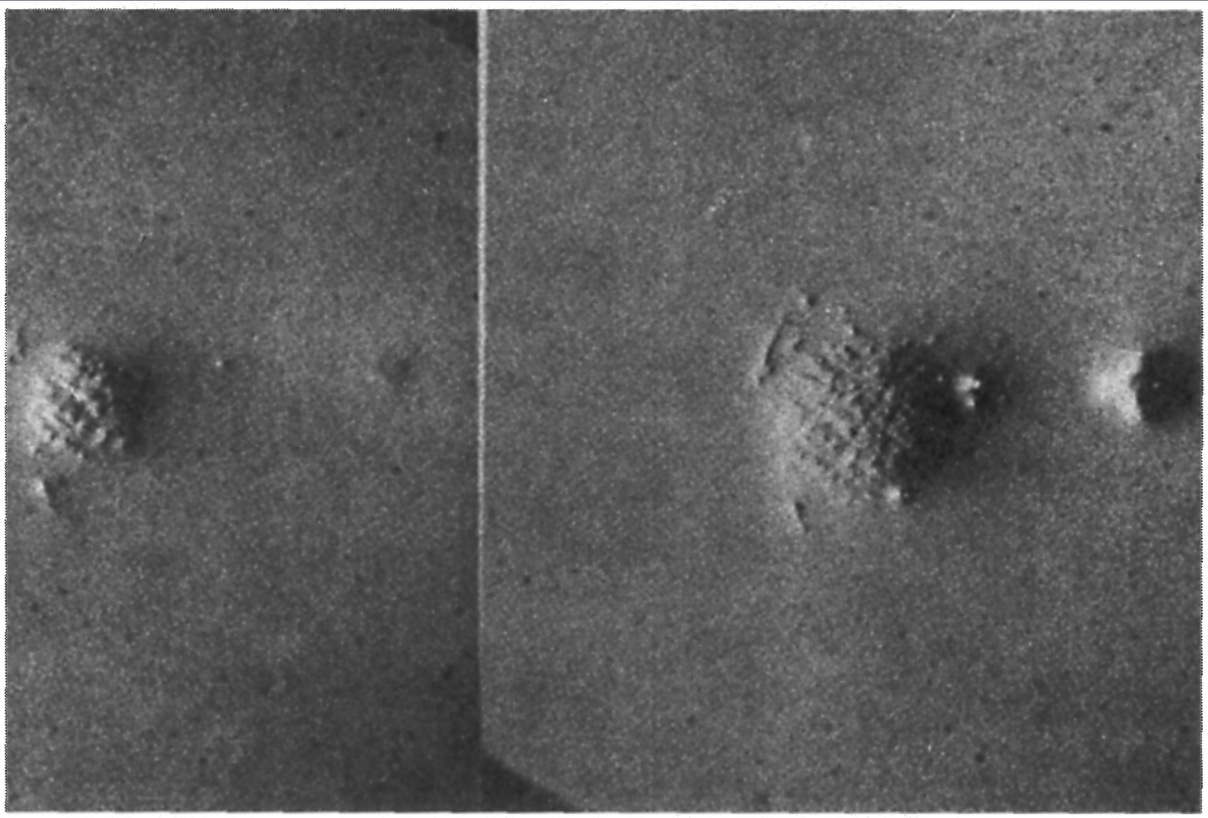


FIGURE 2.4 Variation in a-spot size and distribution as the load is increased from 20 to 80 g. *From Ref. 5.*

Again, so what's the problem?

It looks simple enough:

α-spots + voltage + pressure = current?*

Anyone should be able to do that – right?

Important Note: Contact material selection <u>very strongly influences the results achieved</u>

*http://www.swtest.org/swtw_library/1998proc/PDF/S01_kister.PDF

Topics

- What is the function of a board-to-board interposer?
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So you've got a candidate interposer, is it the right one?

- It depends:
  - What is the required, or acceptable:
    - Working range?
    - Reliability?
    - Current carrying capacity (ampacity)?
    - Bandwidth?
    - Crosstalk requirements?
    - Cost (both per unit and NRE)?
    - Complexity of technology application?
    - etc.

Working Range / Compliance

- This is a complex concept:
  - "Regardless of manufacturing / process variation, the DCR of this electrical interface must always be ≤50 mOhms."
  - There are many potential sources of misalignment / warp / out-of-plane conditions

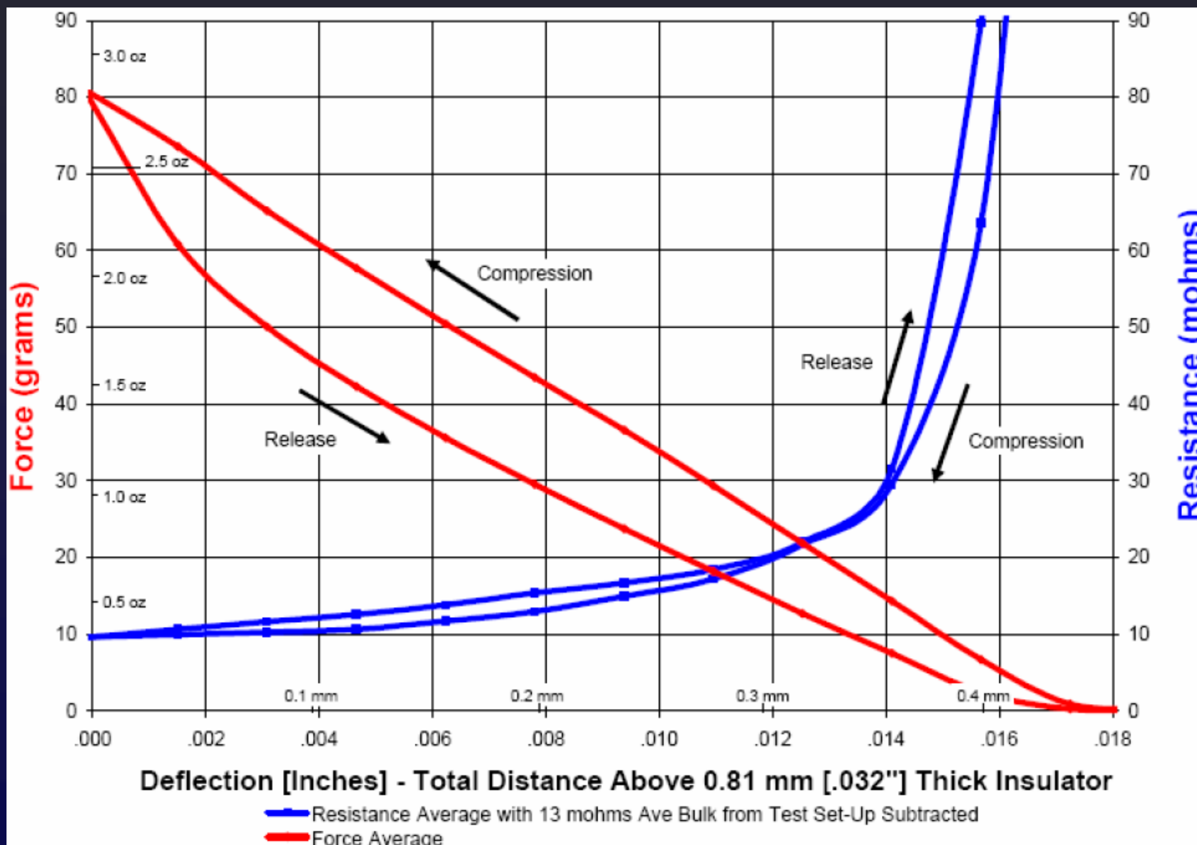
One source of WR problems: board flatness

- IPC 6012B paragraph 3.4.3 states:

“. . . The printed board shall have a maximum bow and twist of 0.75% . . . ”

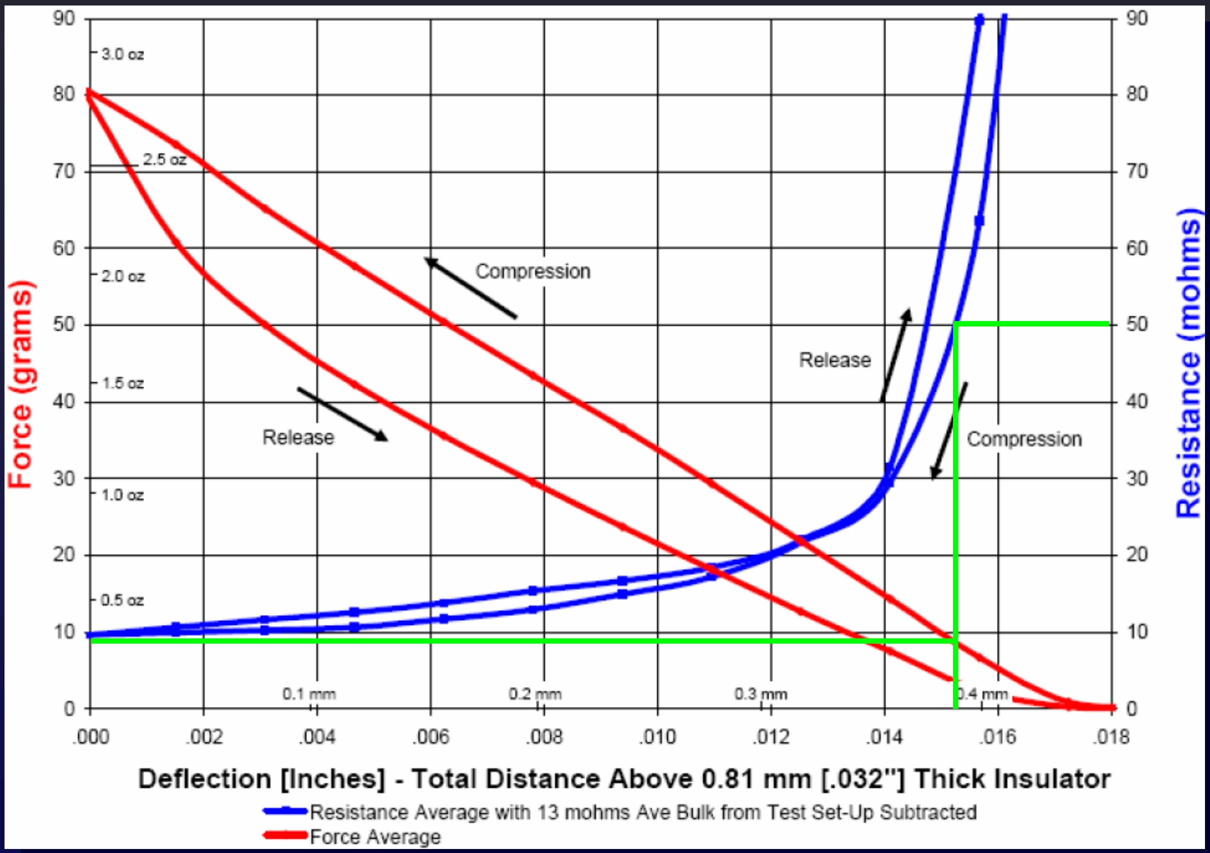
- Equivalent to 7.5 mils per inch (75 µm/cm).
  - This is the “tight” spec’, reserved for surface mount component boards

Example Working Range vs. Force diagram



Cinch "IQ" Contact

Example Working Range vs. Force diagram



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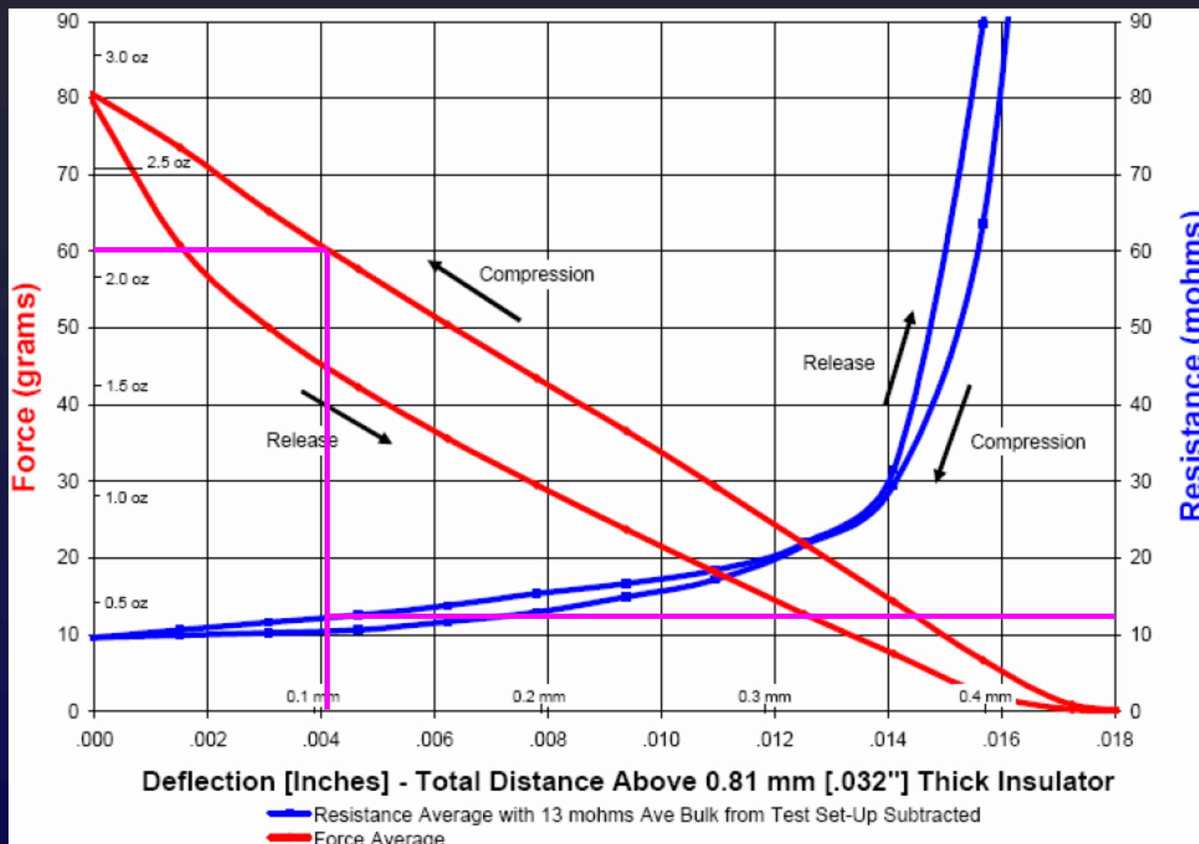


Cinch "IQ" Contact

Working Range measurement technique

- Instron or equivalent force-vs.-displacement mechanism
- *Standardized* 4-wire / Kelvin test boards
  - Boards should test multiple contacts, the more the better
- DC Resistance instrumentation
  - Should record data automatically

Reliability

- Requirement depends on nature of application
  - High cycles (>5000 for lifetime)
  - Low cycles (<50 for lifetime)
- Highly parallel application?
  - See Contact Probability discussion

Target cycle count

- For a wafer probe interface:
  - Assume three probe card changes / day (once per shift)
  - 365 days / year
  - Three year product life

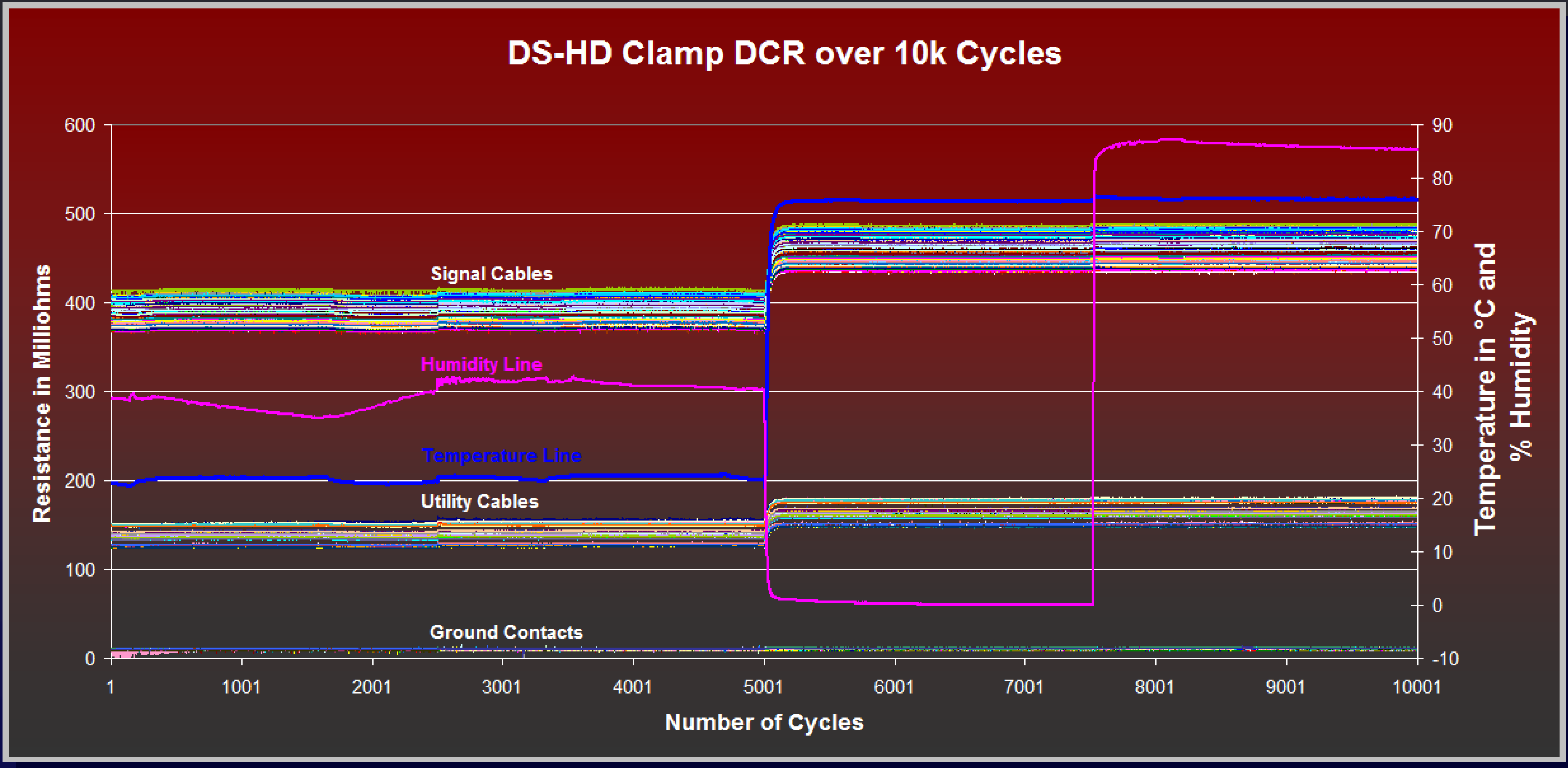
3 (shifts) x 365 (days) x 3 (years) =
3285 mate/demate cycles

Reliability test methods

- Cycling
  - 10,000 cycles
    - up to 75° C / 85% RH
    - Cycle time is approximately 5s
- First touch
  - 5 minutes closed, 55 minutes open
    - 75° C / 85 % RH environment
    - >65 hours / cycles

Important Note: For accurate test results the clamping fixture must not vibrate the assembly under test

Cycling



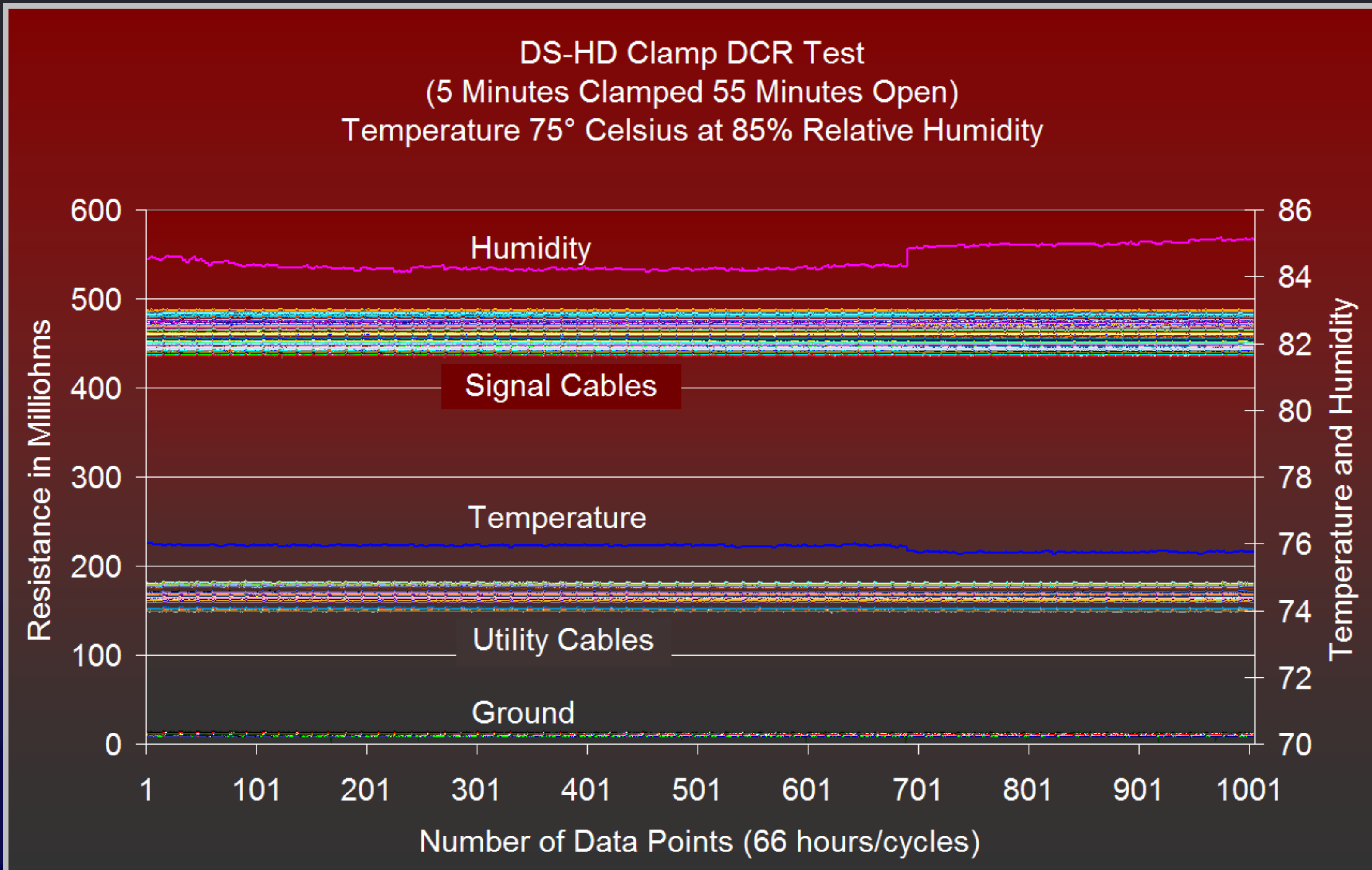
DS-HD Clamp DCR over 10k Cycles
Signal Cables
Humidity Line
Temperature Line
Utility Cables
Ground Contacts
Resistance in Milliohms
Temperature in °C and % Humidity
Number of Cycles
600
500
400
300
200
100
0
90
80
70
60
50
40
30
20
10
0
-10
1
1001
2001
3001
4001
5001
6001
7001
8001
9001
10001

Probability Implications

- <1 failure in 5.76E6 opportunities
  - Equivalent to <0.17 DPMO
  - >6.6σ
  - Cpk >2.2
- Well, *sort* of . . . .
  - Resistance failure is not a Gaussian distribution problem *, so therefore the classical definition of σ doesn't <u>really</u> apply
  - But DPMO does – and can be related back to σ

*http://www.swtest.org/swtw_library/2002proc/PDF/S04_01.pdf

First Touch


DS-HD Clamp DCR Test
(5 Minutes Clamped 55 Minutes Open)
Temperature 75° Celsius at 85% Relative Humidity
Humidity
Signal Cables
Temperature
Utility Cables
Ground
Resistance in Milliohms
Temperature and Humidity
Number of Data Points (66 hours/cycles)
600
500
400
300
200
100
0
86
84
82
80
78
76
74
72
70
1
101
201
301
401
501
601
701
801
901
1001

This is the most difficult test

- Only one technology tested using this method has cleanly passed – and many have not

One more DCR test

- Clamp 'n Hold
  - Use Model:
    - left in the clamped condition for weeks, months or even years
    - extremes of temperature and/or humidity
    - interposer must work first time, every time
  - No real way to accelerate this test – just have to wait it out

Other tests

- Mechanical conformity to design
  - Do the samples match the print?
  - Under load, are the contact points in the correct location?
- Storage
  - Can the interposer technology survive the anticipated storage conditions?

More tests

- Contamination
  - The real world's a dirty place – even in a clean room
  - Scrub. Either the contact technology has it – or it doesn't
    - If no scrub, must have extremely hard, sharp features to pierce surface contamination
  - Make it dirty – does it still work?

And more tests

- Insertion Loss
- Insulation Resistance
- Ampacity
- Inductance
- Return Loss
- Impedance
- Cross Talk

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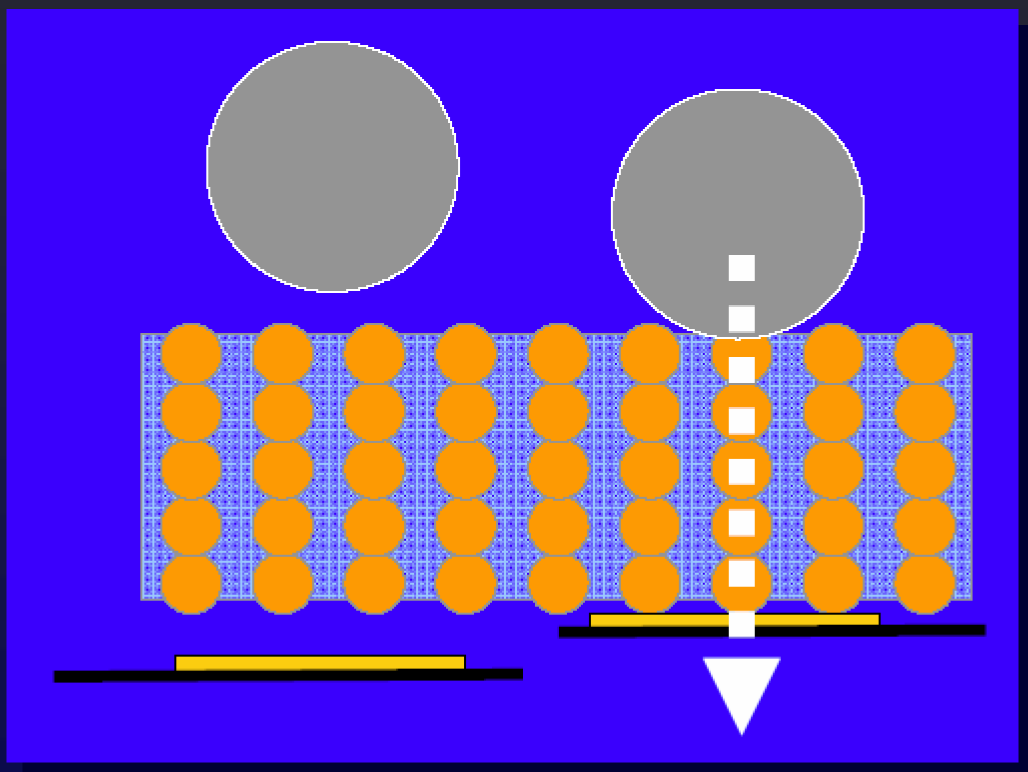
Creating a robust interposer is actually pretty difficult

– And it depends what you want/need

- 9 different species of interconnect technology from >30 companies:
  - Elastomeric – discrete conductive elements
  - Elastomeric – wire
  - Elastomeric – particles
  - Bending Beam
  - Spring
  - Contact-on-flex
  - Random Wire Bundles
  - Rocking Beam
  - Spring Pins

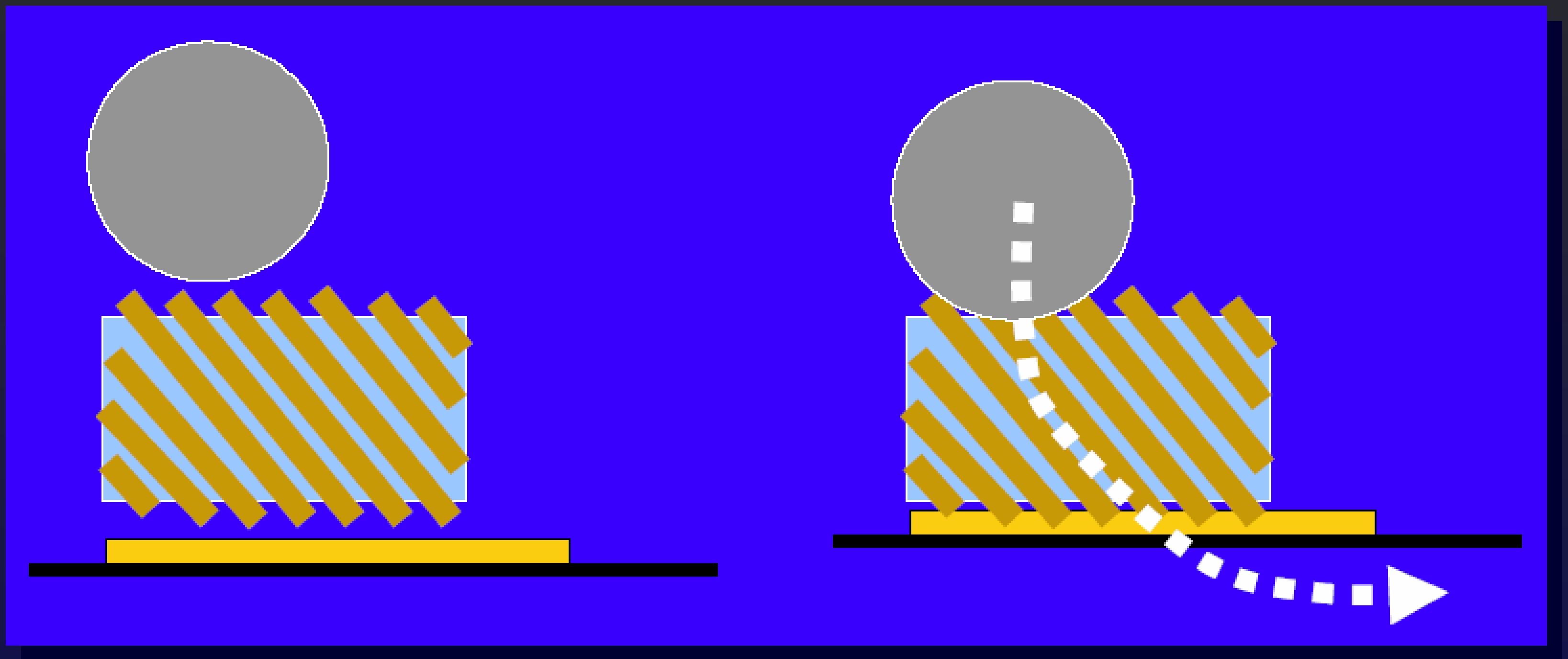
Elastomeric – discrete conductive elements



- ISCTech "ISC"
- JSR "MFPCR"
- Paricon "Pariposer"

Image from: "Elastomeric Contacts – Reliable enough for Production?" BiTS 2007

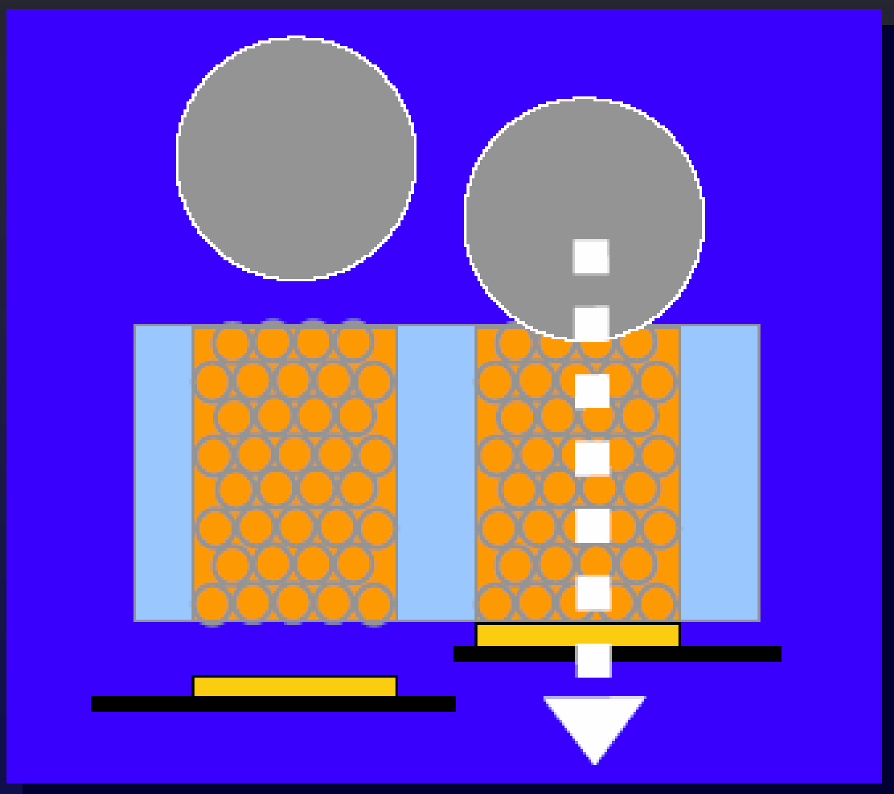
Elastomeric – wire



- FujiPoly "W", "FG-S"
- Shin-Etsu "GB-matrix", "MT-P"

Image from: "Elastomeric Contacts – Reliable enough for Production?" BiTS 2007

Elastomeric – particles



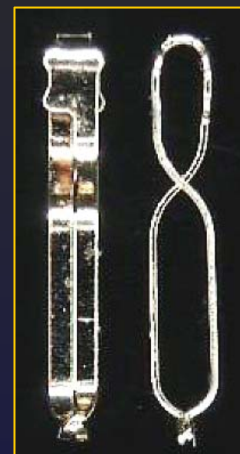
- Phoenix Test Arrays "Silmat"
- Shin-Etsu "RP"
- Tyco "HXC125"
- Various other "Zebra" technologies

Image from: "Elastomeric Contacts – Reliable enough for Production?" BiTS 2007

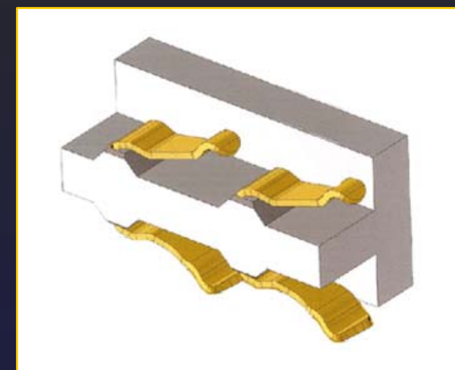
Bending beam

Amphenol
"cLGA"

Cinch "IQ"



Gryphics
"Dual Loop"

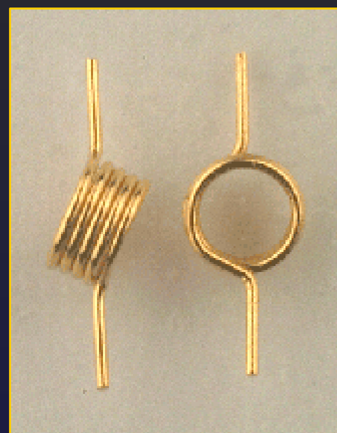


Teledyne
"MicroConn"

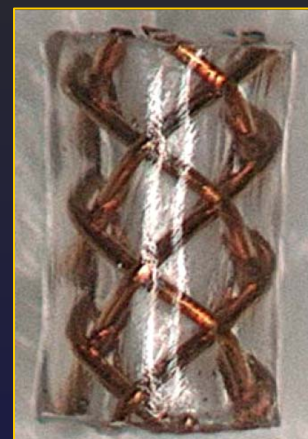
- Antares "Quatrix"
- Aries "Microstrip"
- Neoconix "PC Beam"

Note that there are others in this category (Tyco, FoxConn) vying for the low-cycle "Socket T / LGA 775" market. Huge volume, ultra-low cost (after $$$$$NRE)

Spring



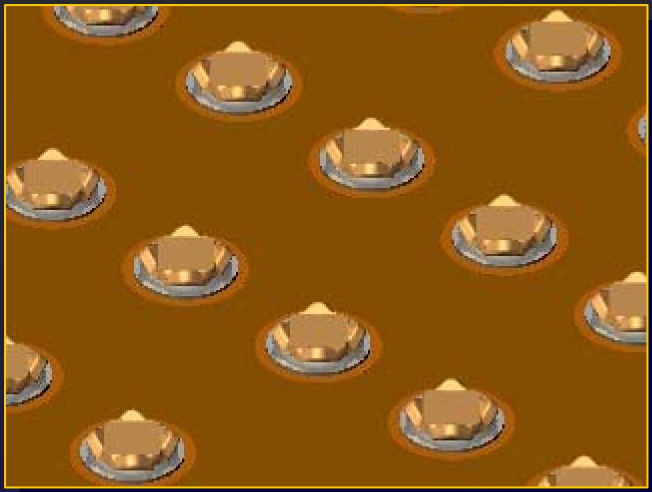
Ardent "RC"



HCD "SuperButton"

- Che-yu Li and Company "BeCe"
- HCD "SuperSpring"

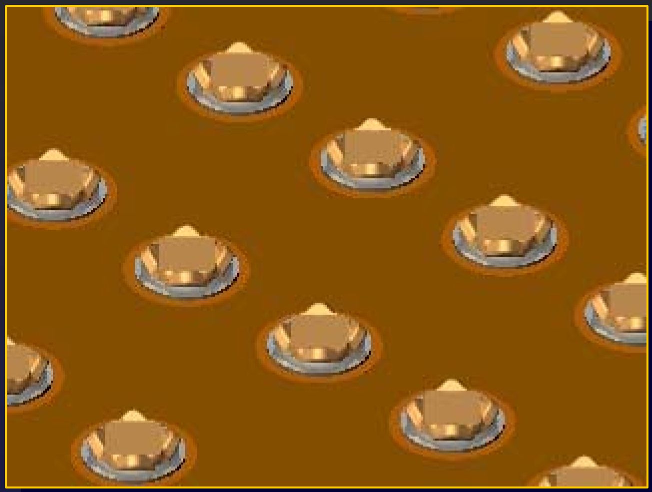
Contact-on-flex



Amphenol – InterCon Systems "C-Byte"

- Giga Connections "CDP" (particle interconnect)
- Delphi Gold Dot

Contact-on-flex



Amphenol – InterCon Systems “C-Byte”

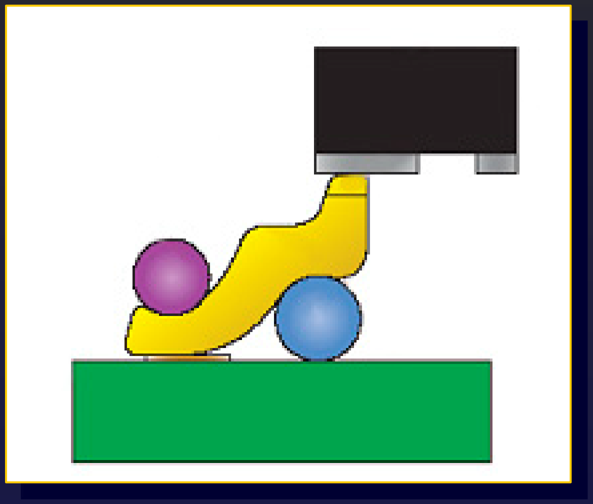
- Giga Connections “CDP” (particle interconnect)
- ~~Delphi Gold Dot~~

Random wire bundles

Cinch “CIN::APSE”

- Tecknit “Fuzzbutton”

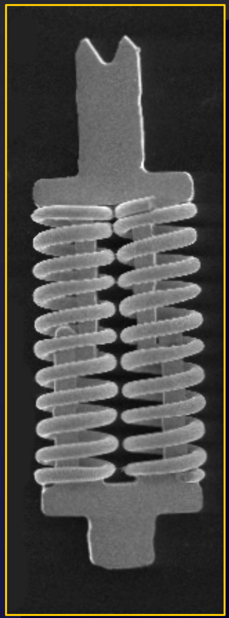
Rocking beam



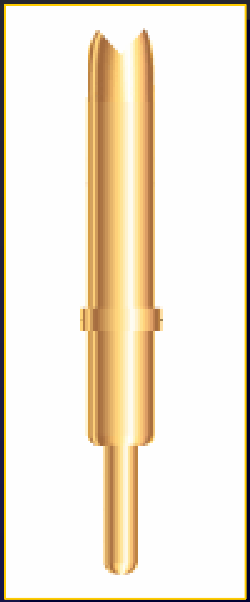
Johnstech "ROL200"

- Antares "Kalypso"
- Yamaichi "Y Shaped SMT Contacts"

Spring pins



ECT Gemini 4
(0.4mm pitch)



IDI 101001
(0.5mm pitch)

- And many, many, many others

Conclusion

- Contact physics specifically and interposers generally are very complex
- Many, many variables must be considered when selecting an interposer technology
- Very careful, thorough testing must be performed to validate/verify your selection

Conclusion, cont.

- Be nice to your probe card vendor – the problem is even more difficult on the other side of the probe card

Acknowledgements

Xandex staff:

- John Hiatt (Senior QA Engineer)
- Fred Morgan (Engineering Technician)
- John Wood (Senior QA Engineer)