Parallel Sort Process and its Challenges

Sabita Roy Warren Crippen Sean McClure Sayed Mobin Intel Corp. Intel Corp. Intel Corp. Intel Corp.

June 2007



OBJECTIVE

Share learning on initial development of 2 DUT (by-2) parallel probing process utilizing Wedge Buckling Beam probe card technology on Copper Bumps

OUTLINE

Introduction

- Technical issues discovered in developing the first 2 DUT probing process with Wedge Buckling Beam (WBB) on Cu Bumps
- Characterizing the issues from the observed effect
- Addressing the challenges
- Conclusions

INTRODUCTION

Motivations for parallel sort → (i) Sorting multiple dice simultaneously; Improves through put efficiency compared to a single DUT

(ii) Lower total cost compared to single sort testing

Goal→ Establish a by-2/Cu/WBB solution

Prior technology delivered probing process for by-2/FBB on PbSn bumps

by-2 sort on WBB/Cu bump is a new probing process with associated challenges

Initial Development Uncovered Key Challenges

Docking consistency of probe card to prober

Site to site discrepancies in in-line path resistance

Understanding/Characterizing the Challenges



Worst Case Scenarios:

Semiconductor Wafer Test Workshop-2007

Inconsistent docking leads to inconsistent planarity across the probe field. This can lead to differences in site to site sort performance



Fig.2- Inconsistent CFL to FRP Contact

Characterization of Contact Quality between CFL and FRP ◆ Determining quality of contact ◆ Conducted pressure paper experiment ◆ Under normal docking condition ◆ Evaluated paper color change ◆ Light color → poor contact; deep color → good contact



Pressure Paper

CFL covered by the pressure paper

Fig.3- Contact between CFL and FRP

Pressure Paper Study – Determination Contact Quality

Semiconductor Wafer Test Workshop-2007



a) No-contact → Pressure paper attached with CFL



b) Good Contact → Red dots = good quality contact between FRP/CFL



C) Uneven contact→ Red incomplete dots



d) Poor Contact→ No dots = no contact



e) Pressure paper calibration curves

Initial Development Uncovered Key Challenges



Docking consistency of probe card to prober

Site to site discrepancies in in-line path resistance

Rapid degradation of probe tips → short SIU lifetimes

Semiconductor Wafer Site to Site Difference in Path Resister Werkshop-2007



 Max Cres delta between sites ~15 - 20%

Die average Cres distribution – product X



Die average Cres distribution – Test Vehicle Y •Normalized max delta (TV material) is ~15 - 20%

•Site to site routing path length difference is a fraction (~ 8%)

•Discrepancy is not fully understood yet

Initial Development Uncovered Key Challenges

Docking consistency of probe card to prober

Site to site discrepancies in in-line path resistance

Rapid degradation of probe tips \rightarrow short SIU lifetimes

Rapid degradation of Probe tip for Parallel Sort

- ✤ Significant Probe tip degradation → life time is about order of magnitude less for by-2 sort
- Minimal Probe tip degradation for by-1 sort



Site Level Break out of Cres

Semiconductor Wafer Test Workshop-2007

Cres started increasing only at site-2 Overall Cres increases due to increased Cres of Site-2



Die average Cres distribution on Cu bump (TV wafer)

Probe Card Expires due to Increased Cres

Semiconductor Wafer Test Workshop-2007



Die average Cres distribution on Cu bump



Site level die average Cres distribution

Life time order of magnitude less → exceeds Cres goal
High Cres at Site-2 → shorter SIU lifetime

Potential Resolutions of the Challenges

Semiconductor Wafer Test Workshop-2007

Challenges – (i) Site to site discrepancies in in-line path resistance (ii) Life time Degradation

FEA was used to select an improved probe head design

- This demonstrates resolution of probe tip degradation
- Cres was also shown to be improved
- This analysis was validated via experimentation



Schematic of Z deflection for site-1/site-2

Contour plot illustrates differences in Z deflection between site-1 and site-2

Potential Resolutions of the Challenges

Challenge -- Docking consistency of probe card to prober

Insuring specifications for both FRP and CFL are compatible so that even in worst case material condition, contact is of sufficient quality to insure good sort

CONCLUSIONS

Major challenges of parallel sort on WBB/Cu bump discussed

Docking consistency can be achieved by consistent specifications between CFL and FRP

Site to site difference of in-line path resistance and life time to be validated with improved design