IEEE SW Test Workshop
Semiconductor Wafer Test Workshop

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Chief Marketing Officer

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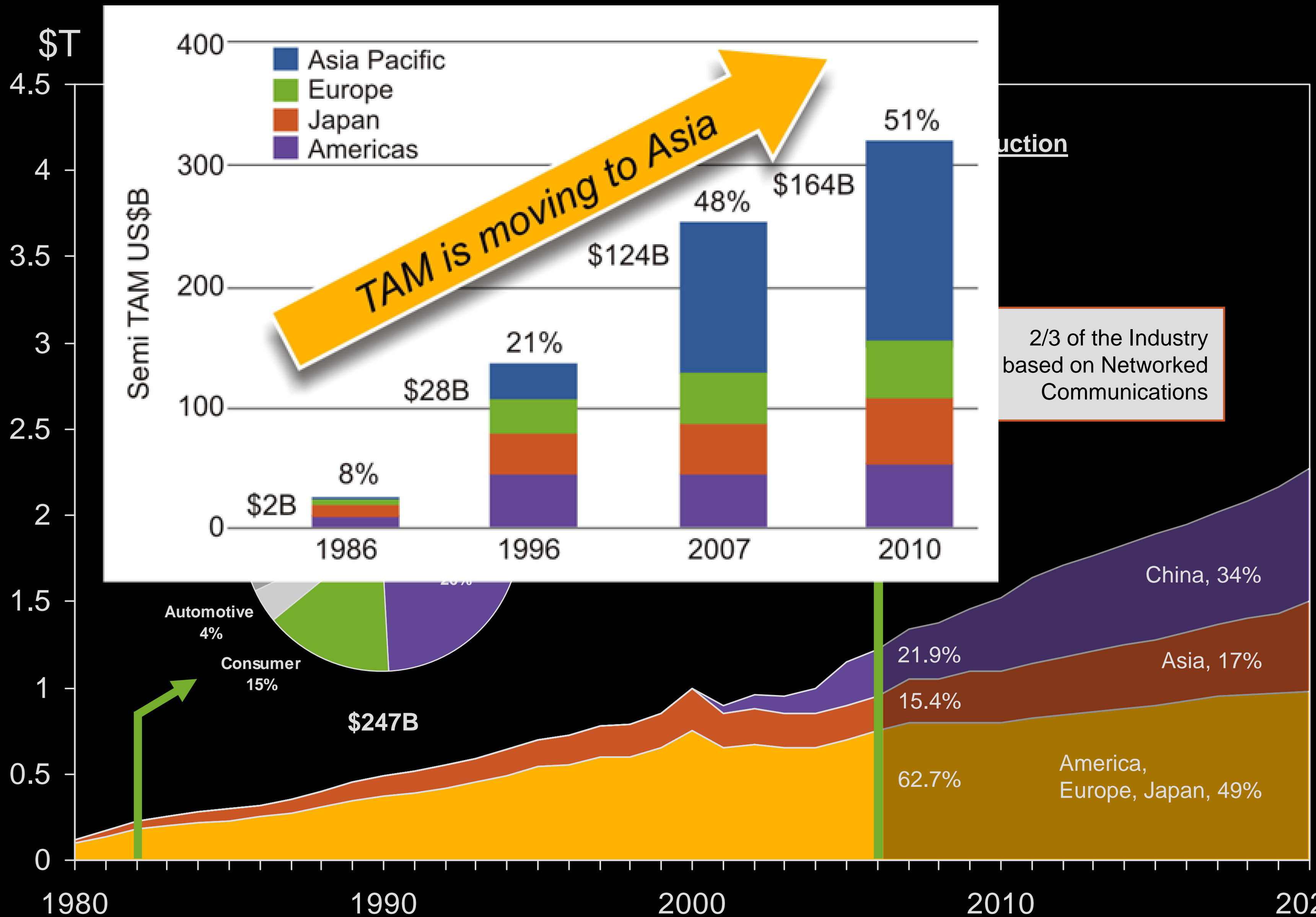
Consumers in the Drivers' Seats

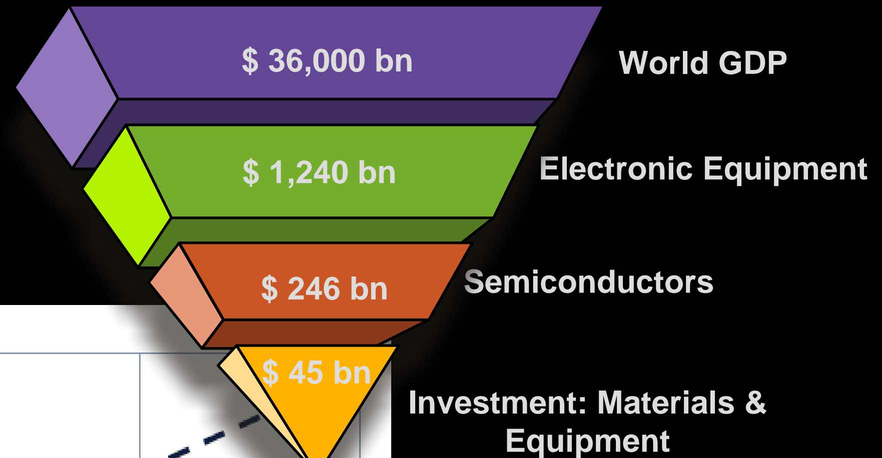
The Global Electronics Industry



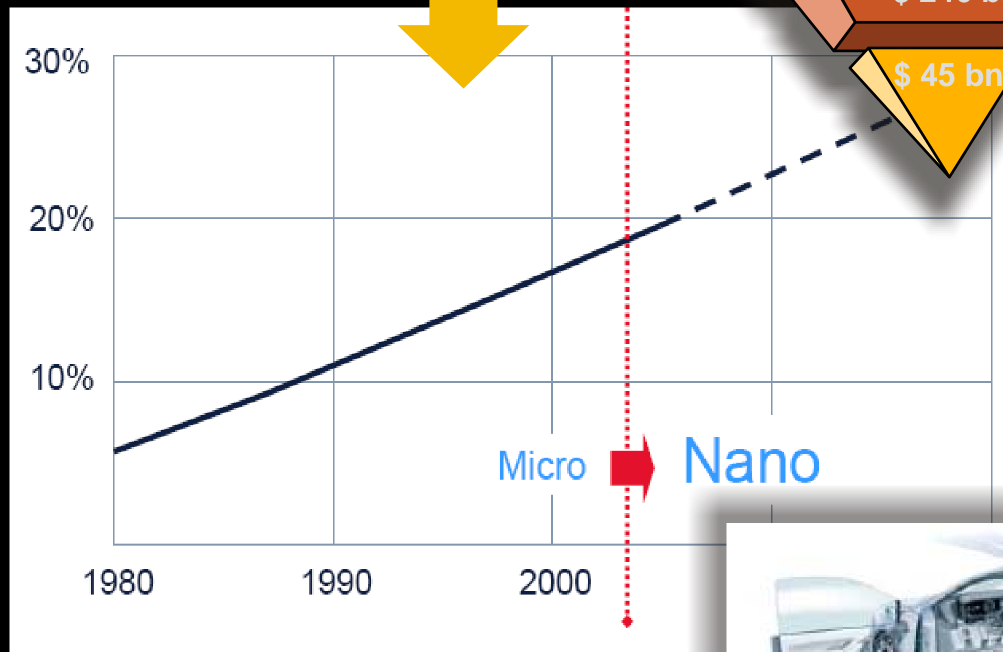
The Pervasiveness of Semiconductors

Semiconductors underpin all business sectors

End products' ever-growing dependence on semiconductors



Semi-conductor content (% of end product value)



Source: Medea+

The Prevailing Laws – Moore

More than Moore: Application-Driven Process Diversification

Analog/RF

Passives

HV Power

Sensors
Actuators

Biochips

Moore's Law: Scaling

CPU

Memory

Logic

130nm

90nm

65nm

45nm

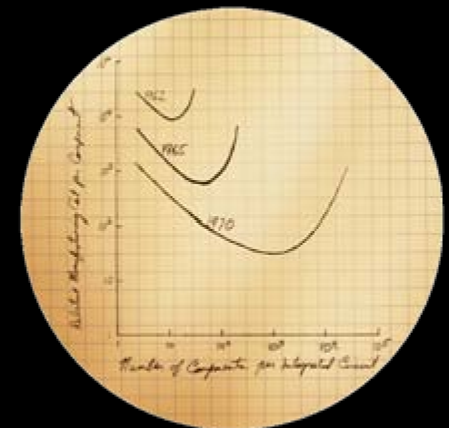
32nm

22nm

Combination → Higher Value Systems

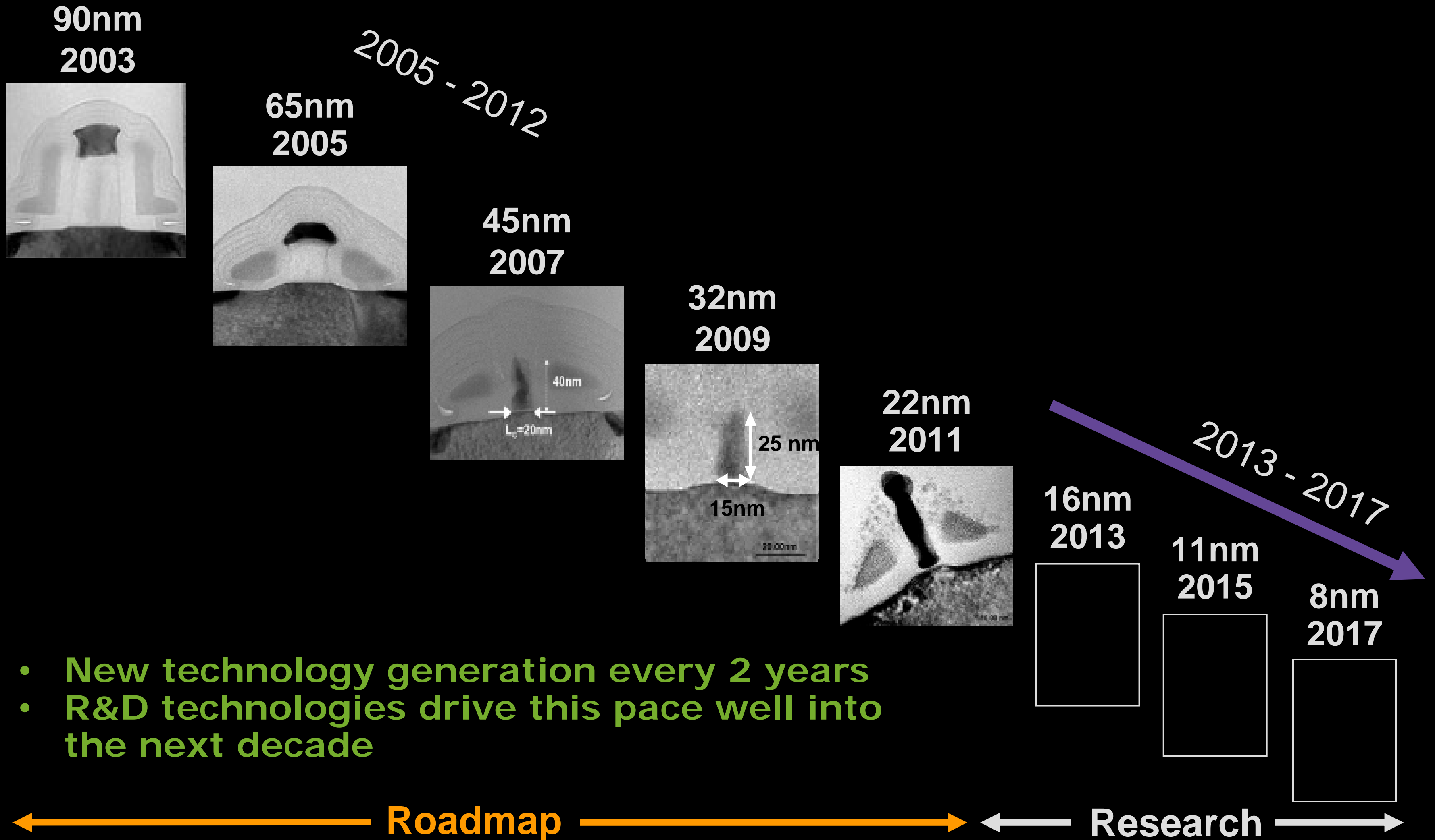
Interfacing &
Interacting with
Environment

Digital Data
Processing
& Storage



Source: ITRS, Intel

Silicon Future

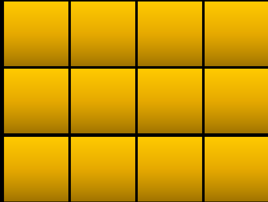


Source: Intel

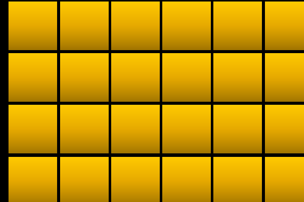
The Prevailing Laws – Amdahl

Increasing Throughput through Parallelism

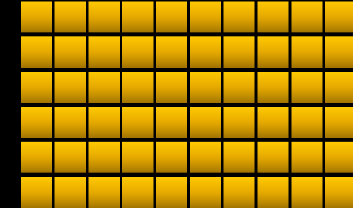
12 Cores

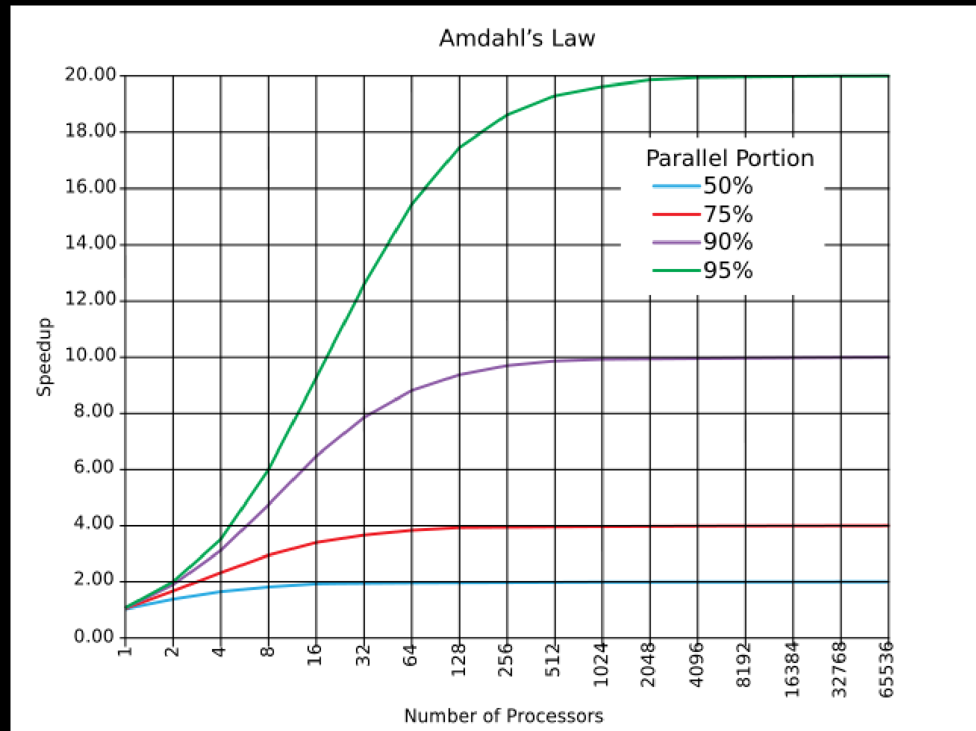


48 Cores



144 Cores

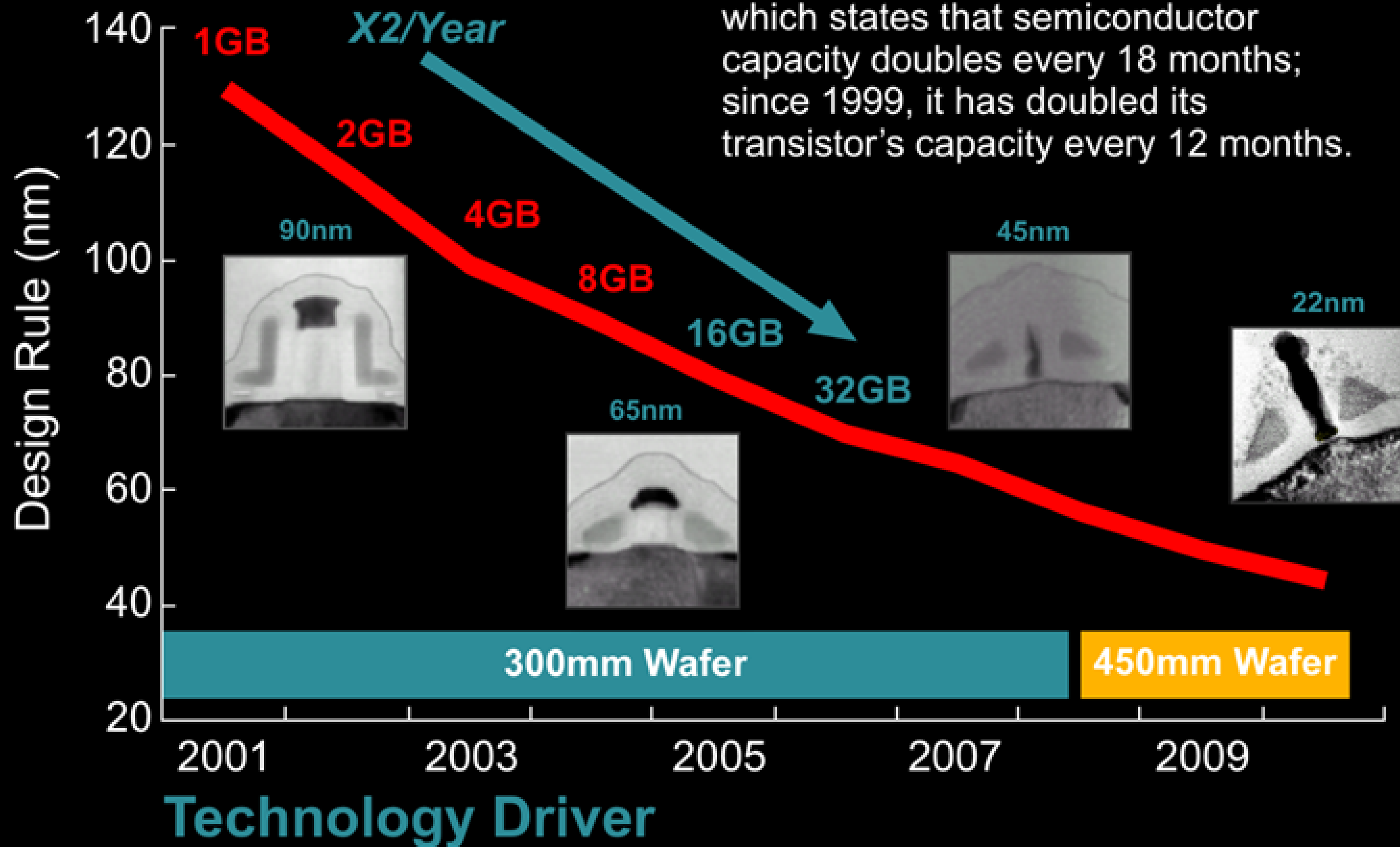




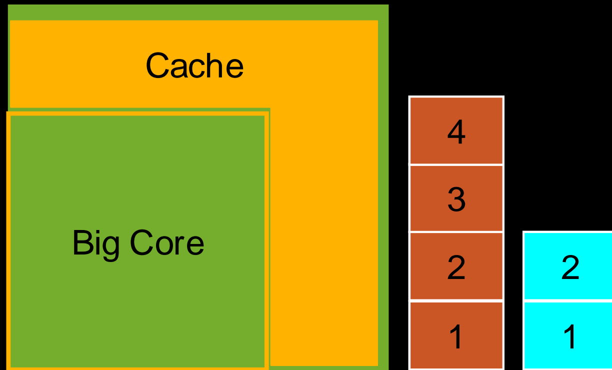
Parallel Speed-Up= 1/(Serial% + (1-Serial%)/N)

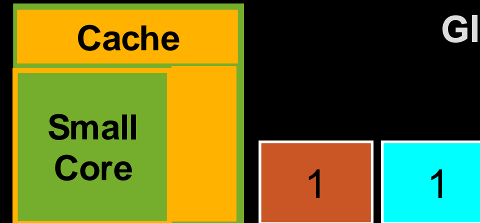
N= number of cores

Nano-scale Semiconductor Devices

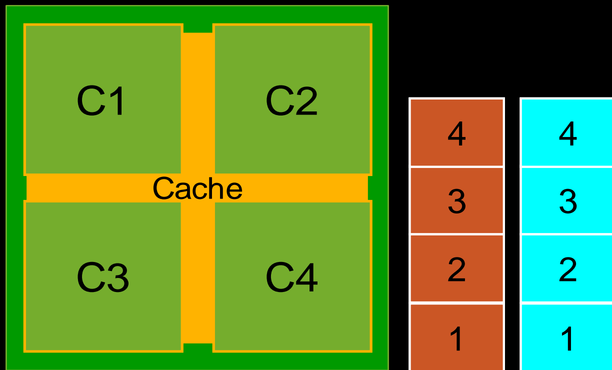


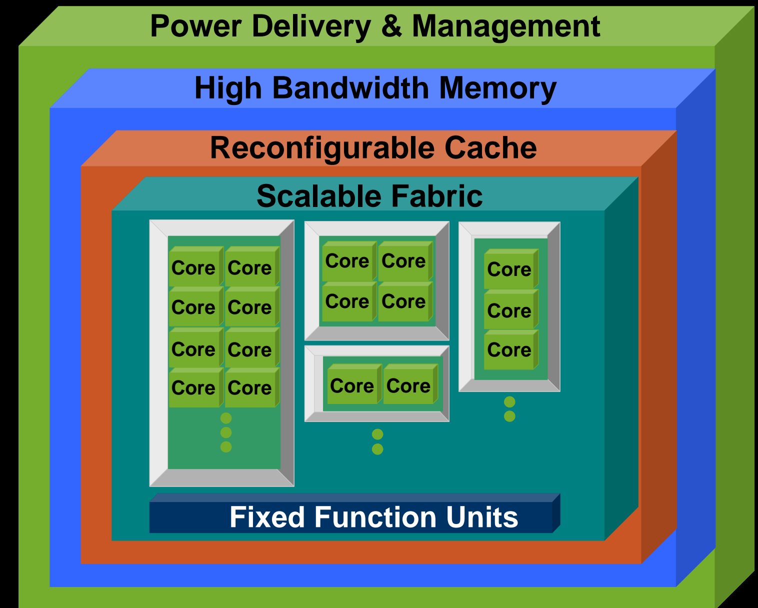
MPU to Multi-Core SoC Trend





Homogeneous Array of Cores
Fixed Function Units
Global Coherency Hardware





Multi-Core is more power-efficient
Power ~ Area
Single-Thread Performance ~ Area *.5

Source: Intel, www.intel.com

More than Moore

More than Moore: Application-Driven Process Diversification

Analog/RF | Passives | HV Power | Sensors Actuators | Biochips

Moore's Law: Scaling

CPU | Memory | Logic

130nm
90nm
65nm
45nm
32nm
22nm
.
.
.

Combination → Higher Value Systems

Digital Data Processing & Storage

Interfacing & Interacting with Environment

Source: ITRS, Intel

Qualcomm vs. Intel

Pocketable Computer

Fairbanks/Anchorage

Snapdragon Processor

Nokia's N800 Internet Tablet

Vs.

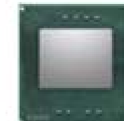
MID

Menlow Architecture

Silverthorne Processor

Menlow-based UMPC Platform

Intel Core 2 Duo



Intel Core 2 Duo

Standard size in Mac AirBook

Mac AirBook

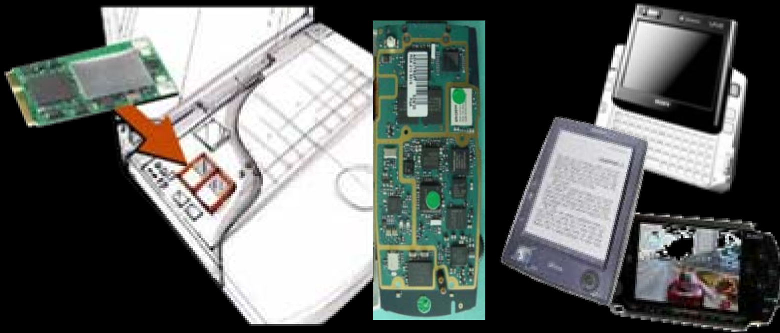
Source: Core Logic 2008

3 Imperatives For Mobile Internet

1

Innovation in Distribution:

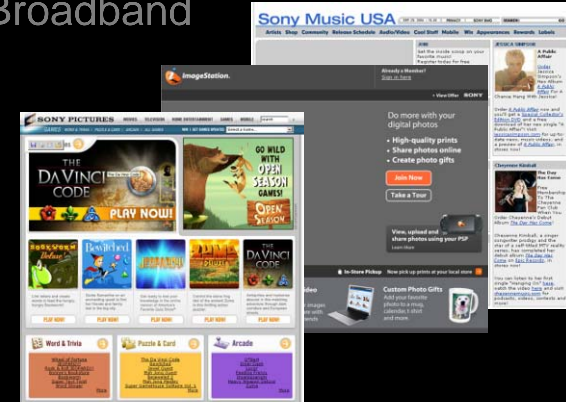
- *Chipsets: Single chip WiFi + WiMAX*
- *Devices: Embed chipsets in mass market laptops and consumer electronic devices*
- *Distribution: Leverage consumer electronics sales distribution channels*



2

Innovation Multimedia Solutions:

Visual Centric, Interactive, Personal Broadband



3

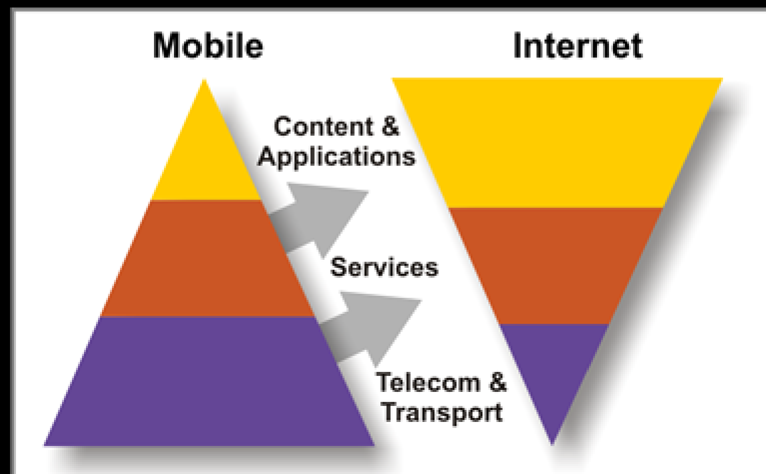
Affordable Service:

Pay as You Go, Pre-paid, or Monthly Subscription

Source: XOHM

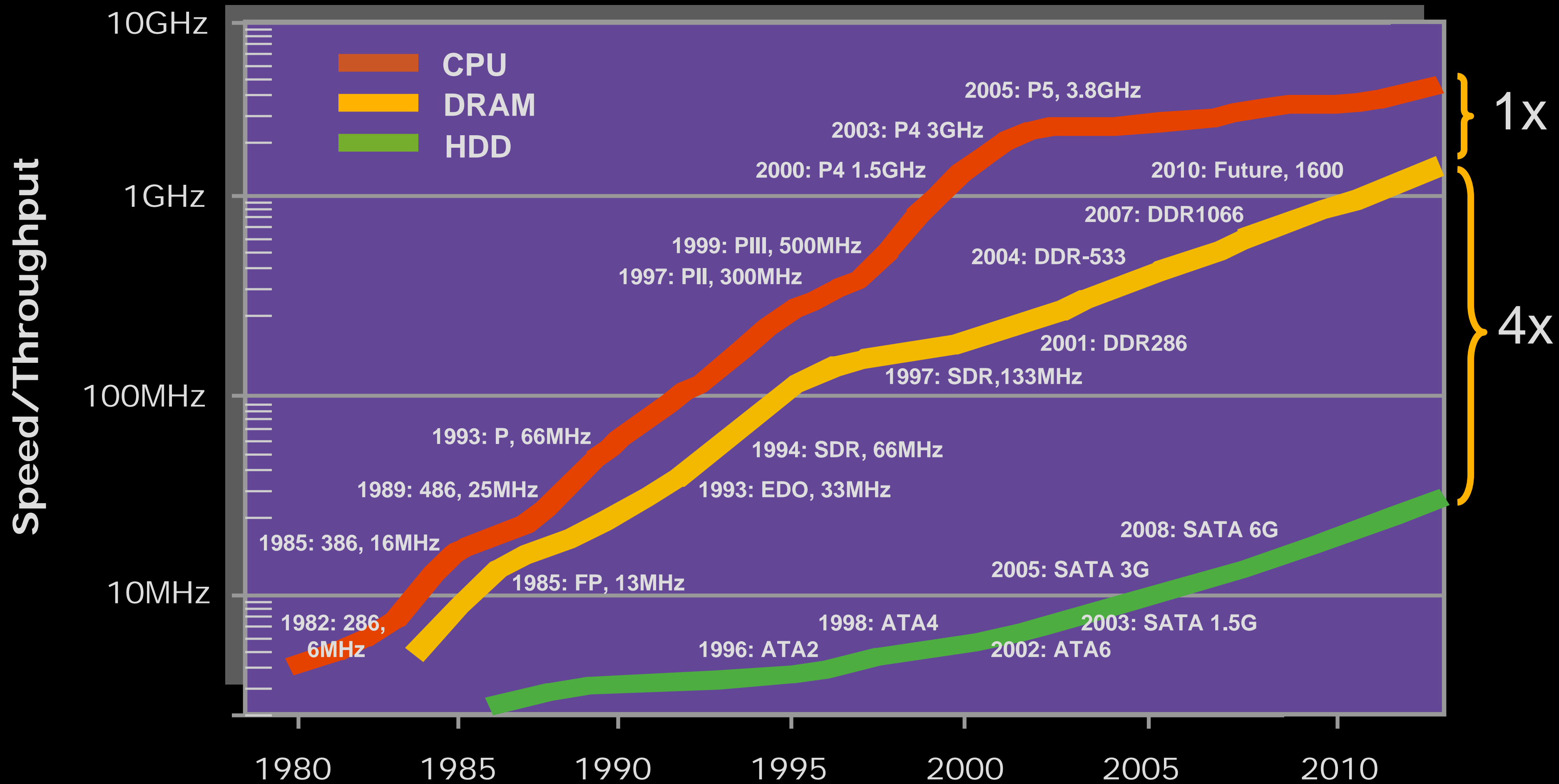
The WiMAX Ecosystem

Mobile Internet User
Mobile Devices
Applications
Service Delivery Providers
Network Operator
Network
Silicon
MOBILE INTERNET ECOSYSTEM



System Performance Bottleneck

Performance gap between DRAM and Storage is 4X greater than between DRAM and CPU



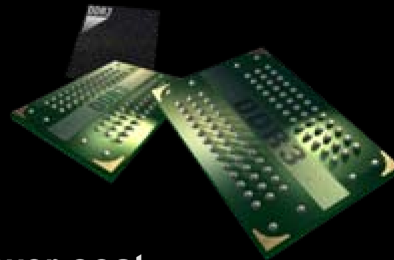
Source: Samsung 2007

System-in-a-Package vs System-on-a-Chip

Market Forces | **Requirements** | **Integration Solutions**

Mobilization

- Higher reliability
- Lower noise
- Multipurpose
- Lower power
- Better heat dissipation



Higher Performance

- Lower cost
- Smaller size
- Lighter weight
- Time-to-market

System-in-Package

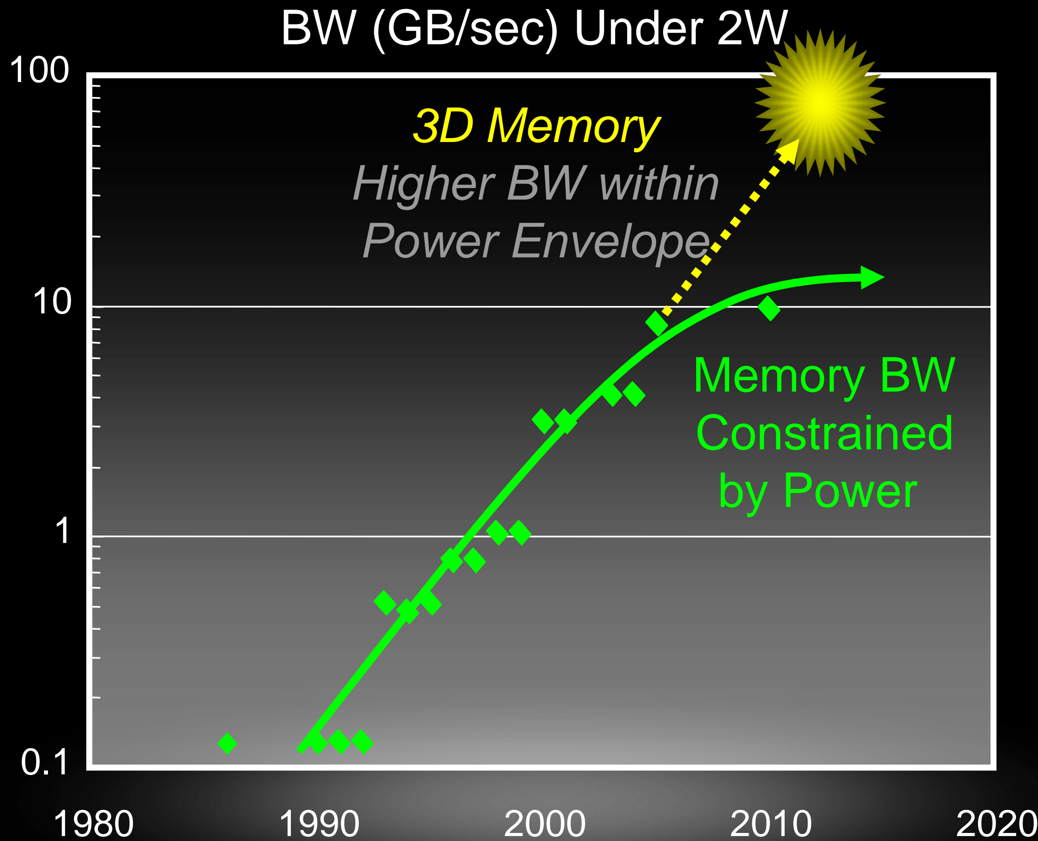
- Lower NRE
- Building block Si
- Multiple sourcing
- Simple IP integration
- Faster time-to-market
- Yield management system

System-on-a-Chip

- Highest performance
- Lower cost in high volume
- Smallest size
- Higher NRE
- Process integration limitation
- Longer incubation time

Source: STATS ChipPAC

Increasing Memory Bandwidth (BW) *to Keep Pace*

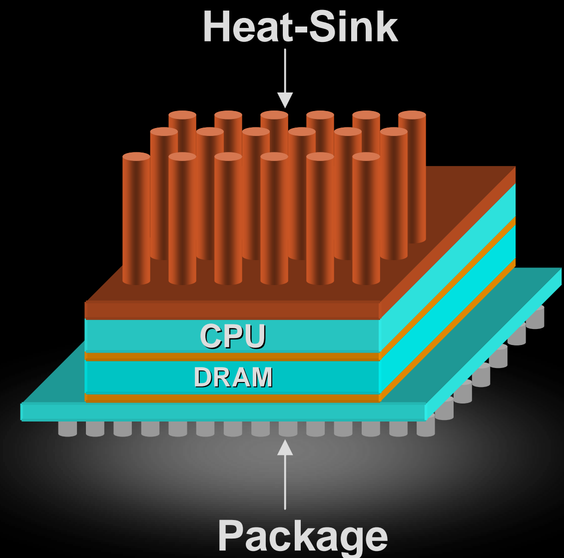


3D Memory Stacking

Power and IO Signals Go Through DRAM to CPU

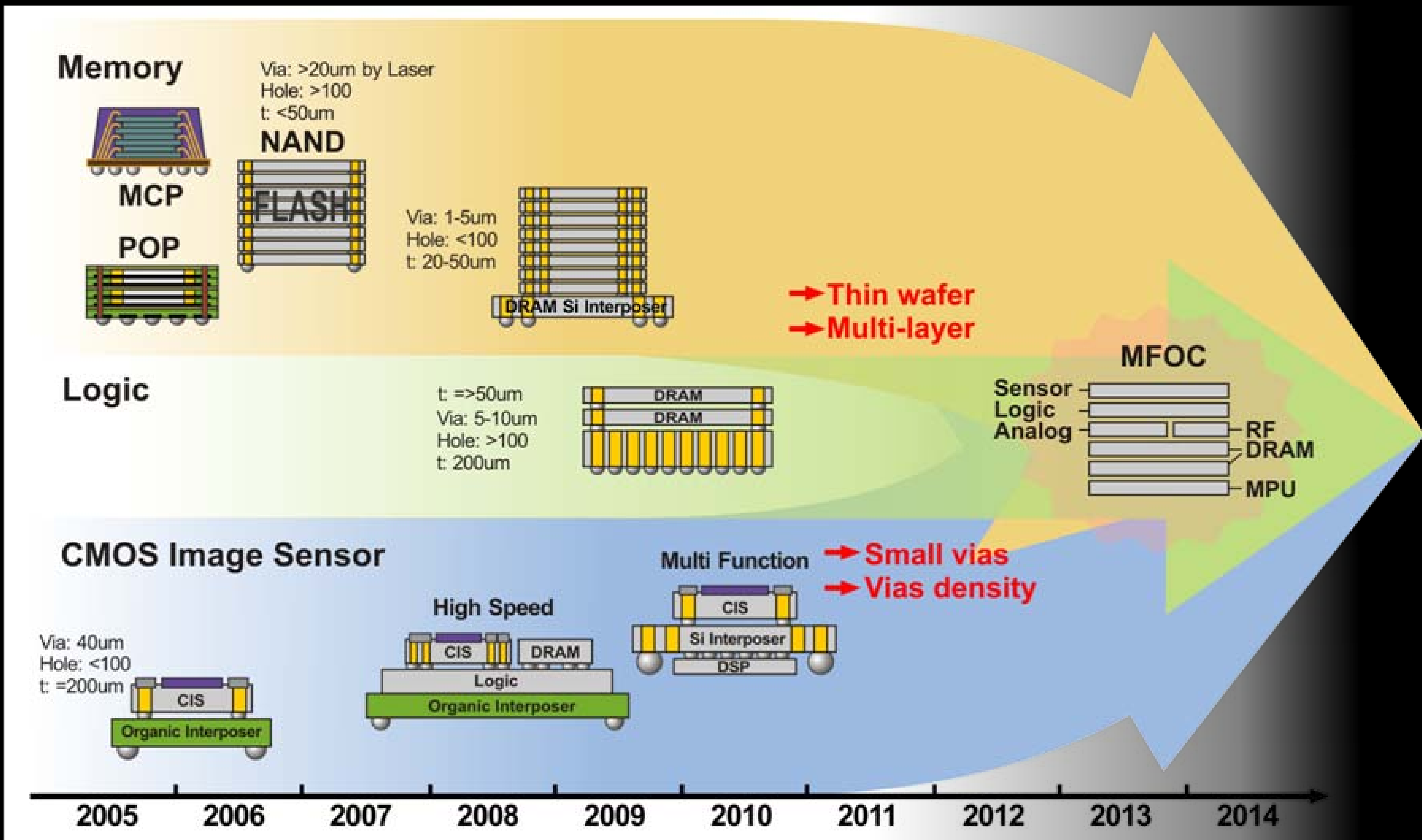
Thin DRAM Die

Through DRAM Vias



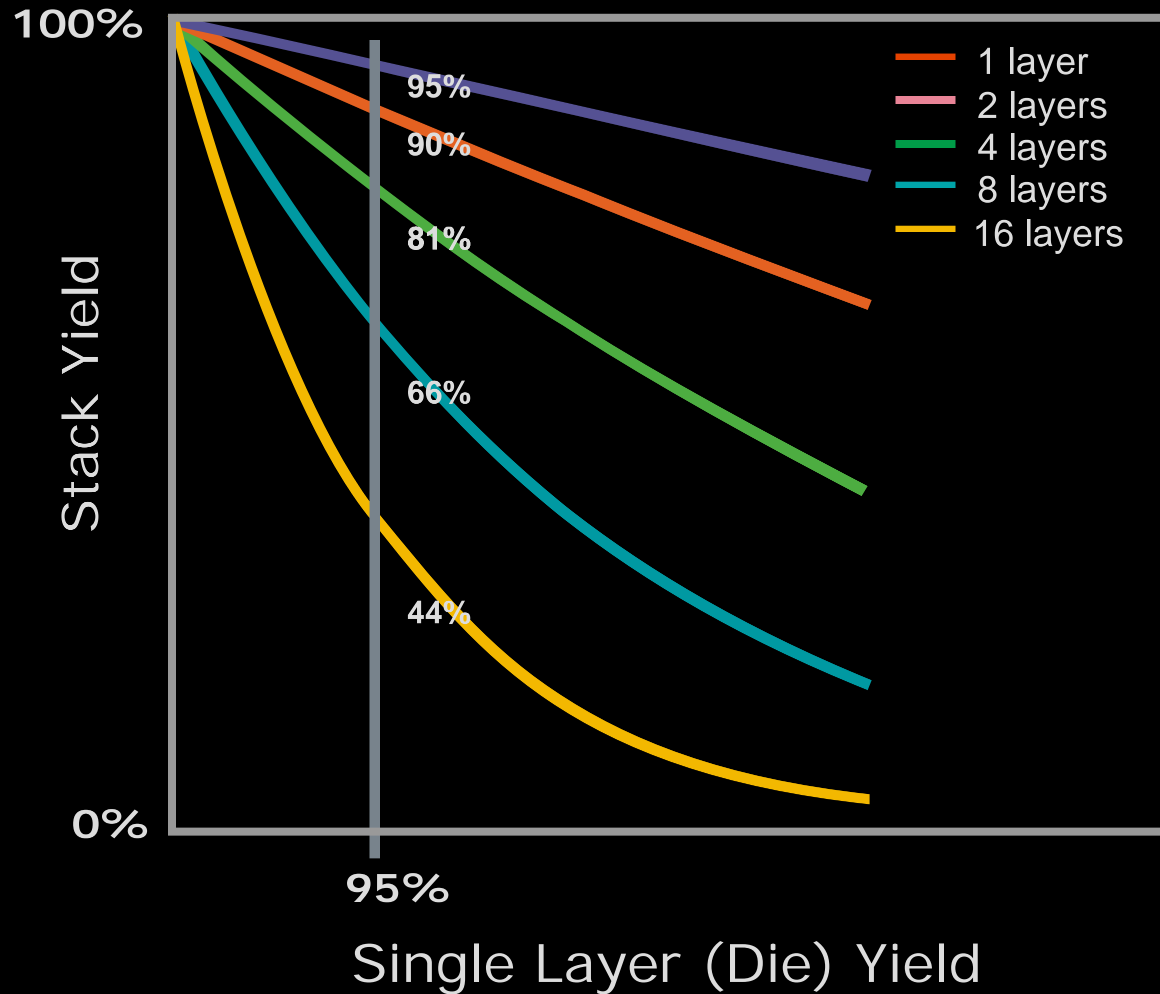
Source: Intel

3D-IC Market and Roadmap



Source: YOLE Développement 2007

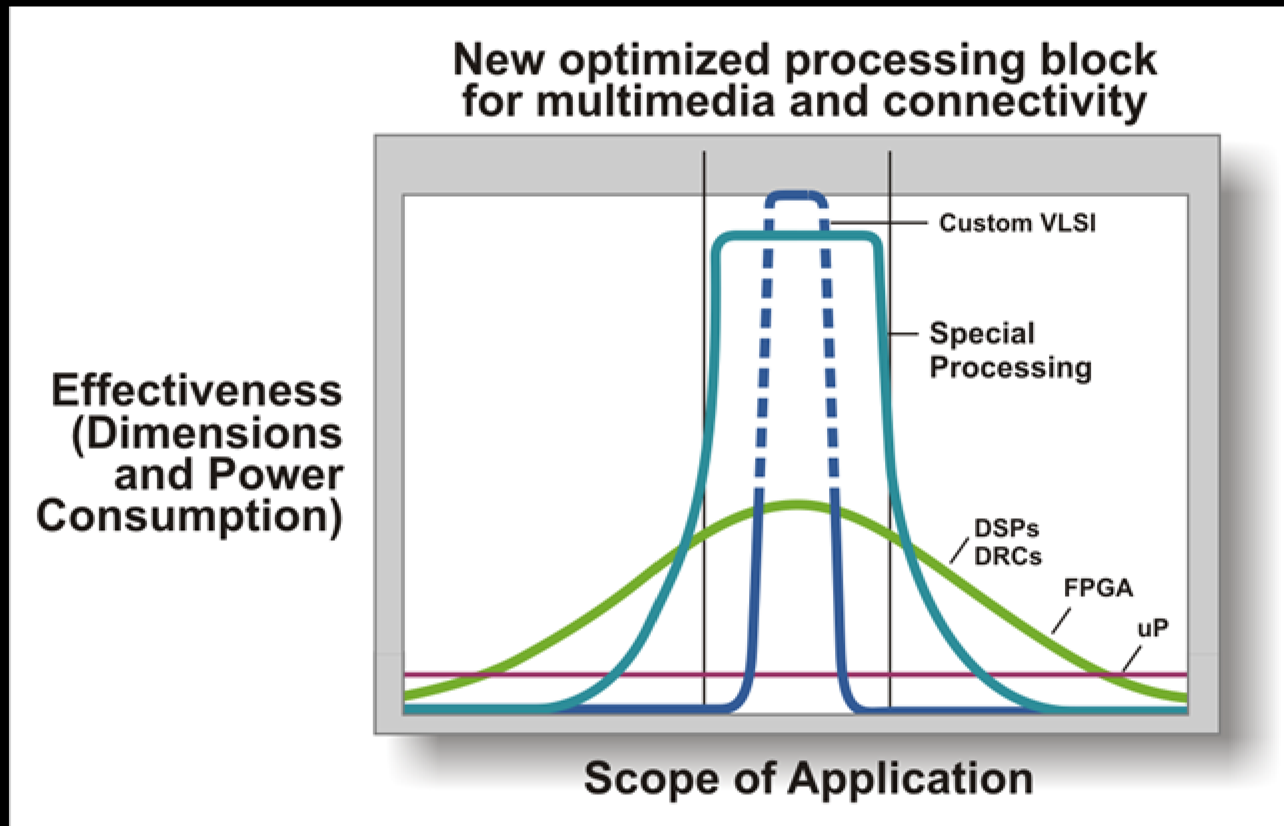
Motivation!!



Source: Lewis and Lee 2007

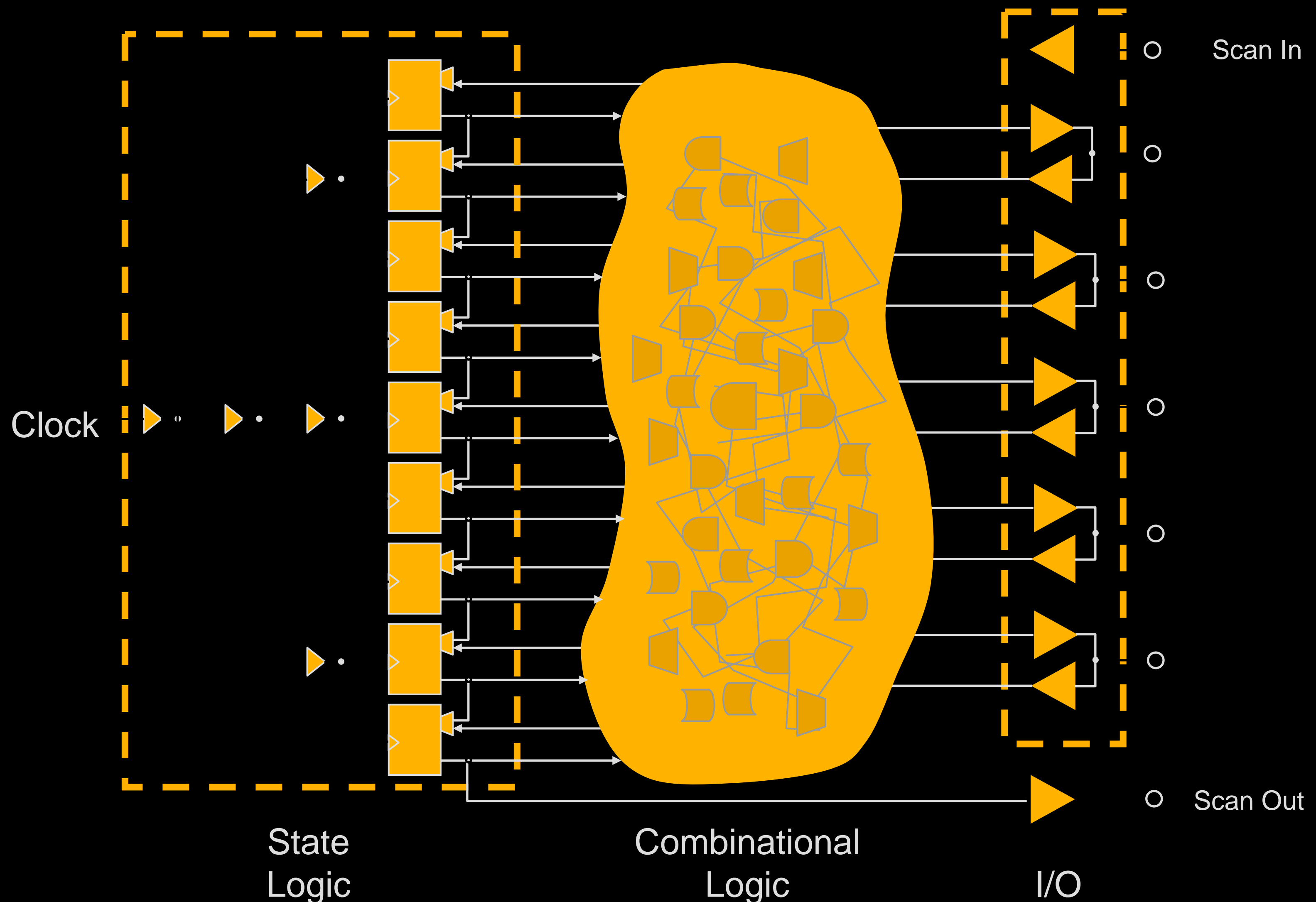
The Evolution of SoC Platform

- System-level design for faster time to market and efficiency
- Development of standard platform solution with flexible architecture
- Ideal core development

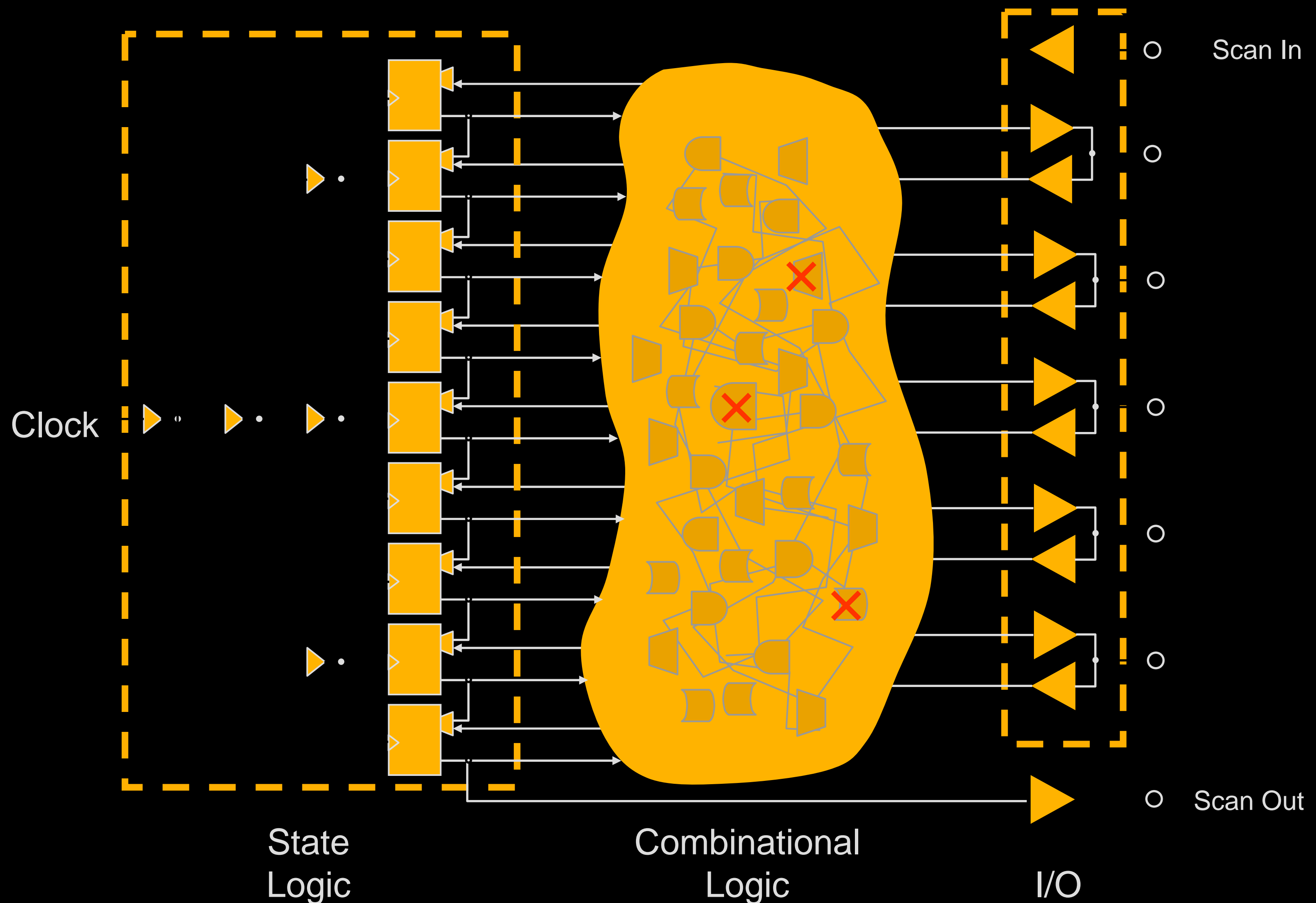


Source: Core Logic 2008

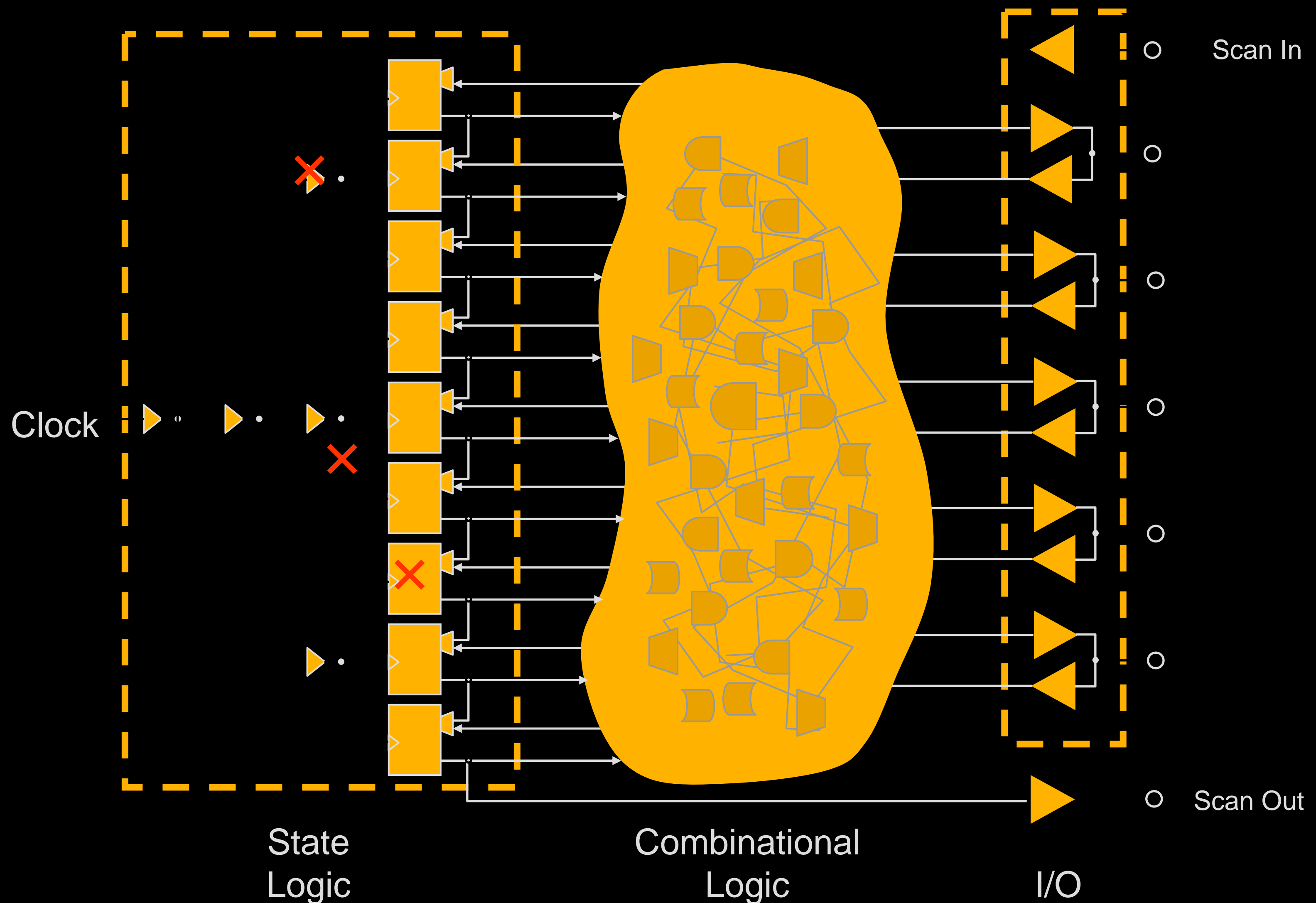
DFT Provides Access to the Combinational Logic Using the State Logic



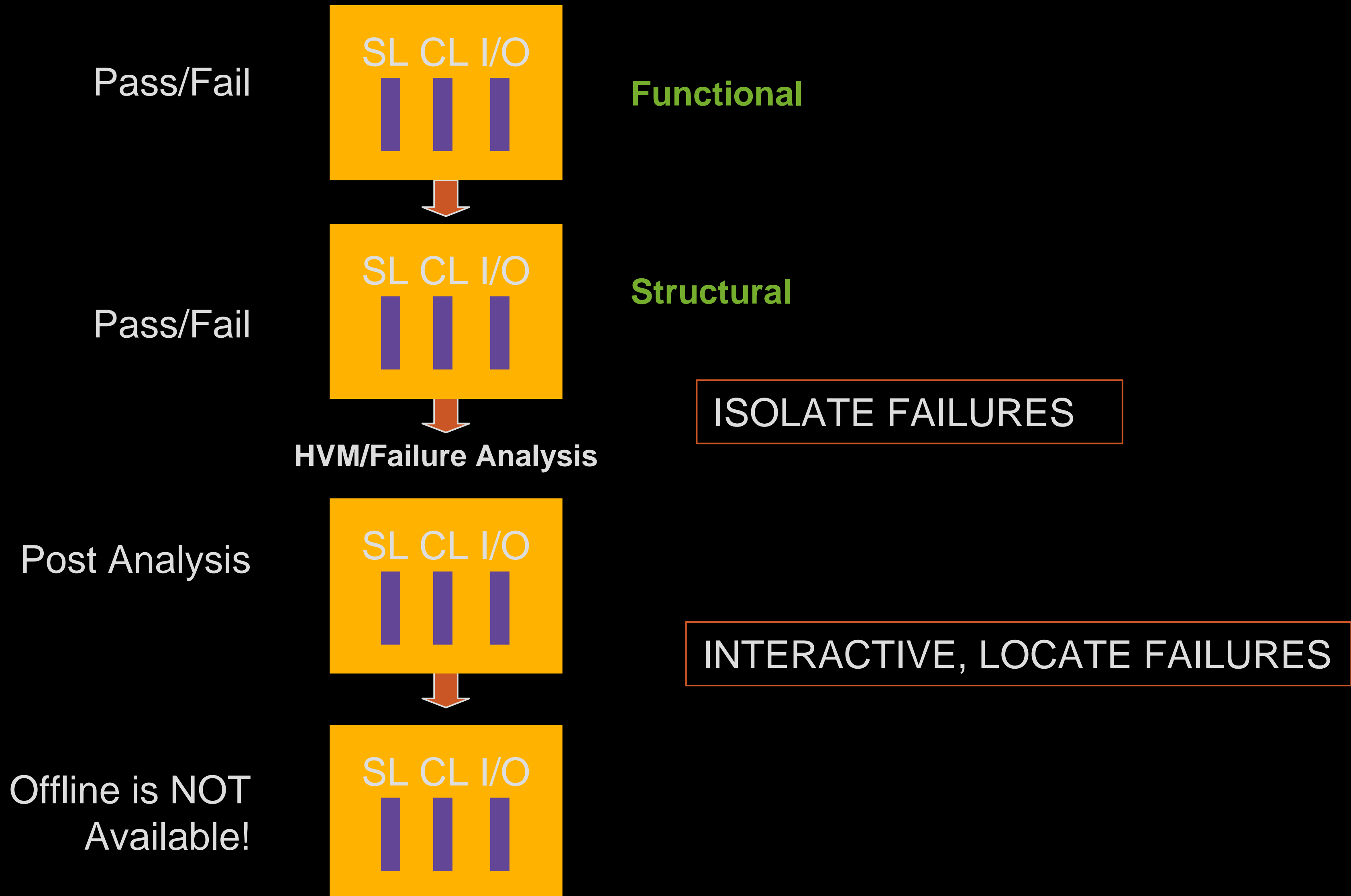
Post-Fault Simulation – Works OK for Combinational logic



But What Do You Do When the Fault is in the State Logic?



Evolution of the Tester



Integrated Solution for Accelerated Yield Ramp Linking Design to Silicon

Encounter Test True-Time ATPG

Generate test patterns

High coverage tests
for sub 90nm defects

V93000 Environment

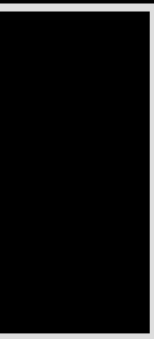
Capture failure data

Zero overhead data logs
for hundreds of failures

YieldVision

Triage failing die

Efficient data analysis to harvest most
representative failures



Encounter Diagnostics

Volume analysis

Identify systematic sources of
yield loss (logical & physical)

Encounter Diagnostics

Precision analysis

Identify most representative
die causing yield loss (logical)

Encounter Diagnostics

Physical correlation

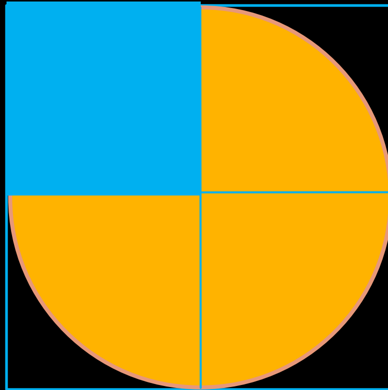
Identify layout feature causing
yield loss

PFA

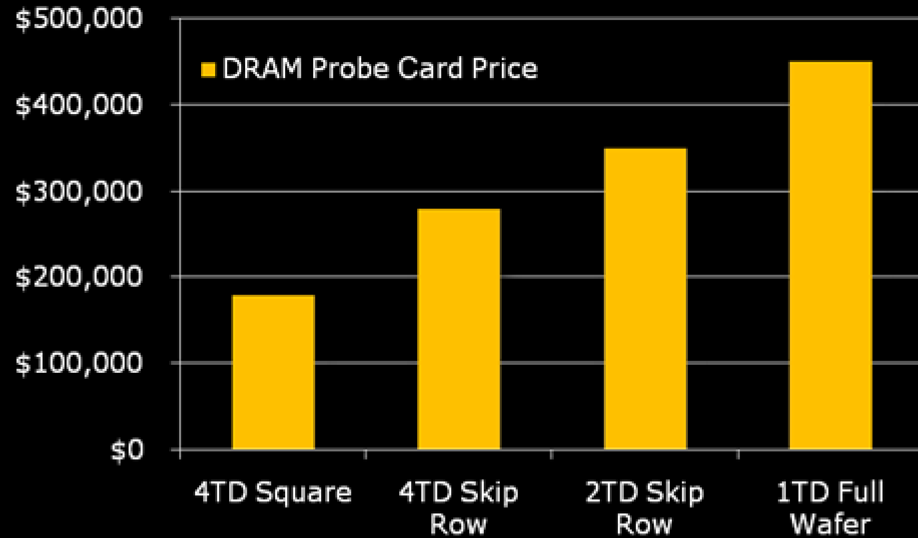
Highest probability die
with X-Y locations
confirms diagnosis

Source: Cadence, Verigy

DRAM Test Cost vs. Parallelism

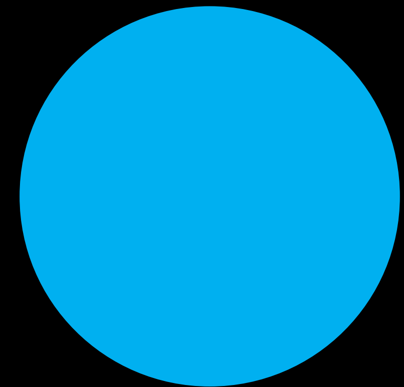


4TD Square
Normalized $1.00 CoT/die



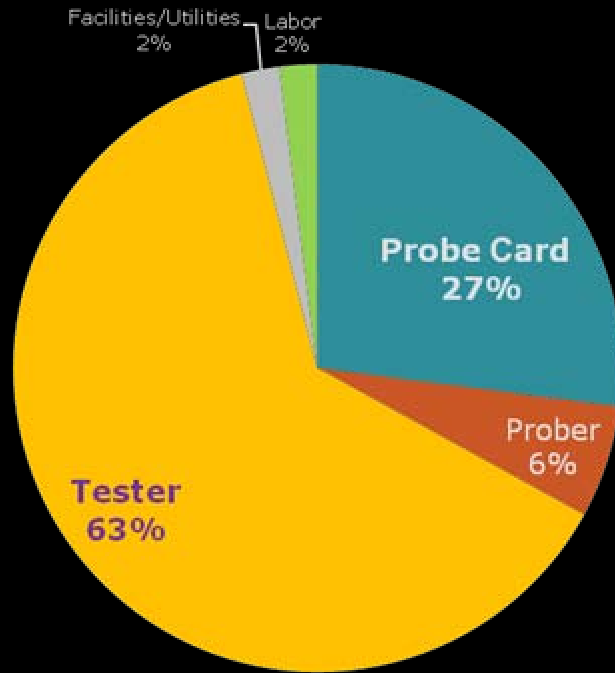
4TD Skip Row
$0.84 CoT/die

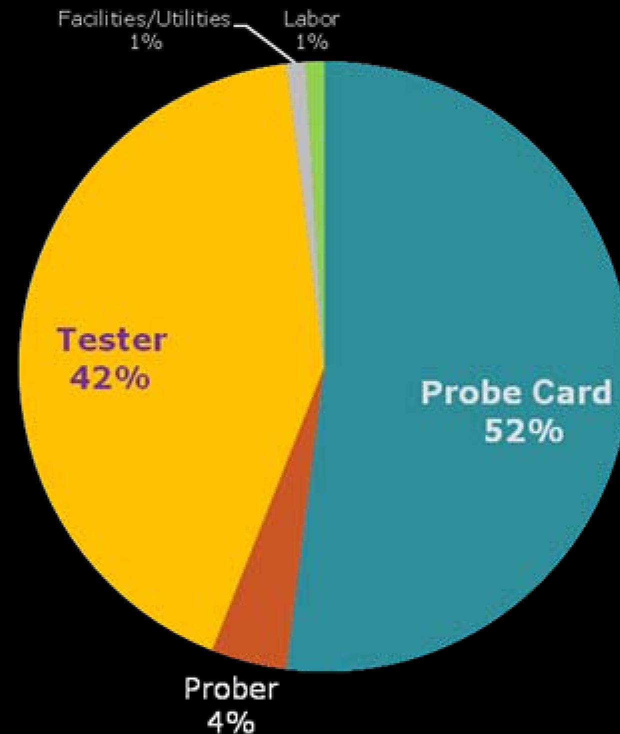
2TD Skip Row
$0.62 CoT/die



1TD – Full Wafer
$0.42 CoT/die

DRAM Test Cell Cost Breakdown – 1990s – 2000s





1997
Parallelism ~32 die/touchdown

2010E
Parallelism ~512 die/touchdown

Source: Verigy, Micron Marketing

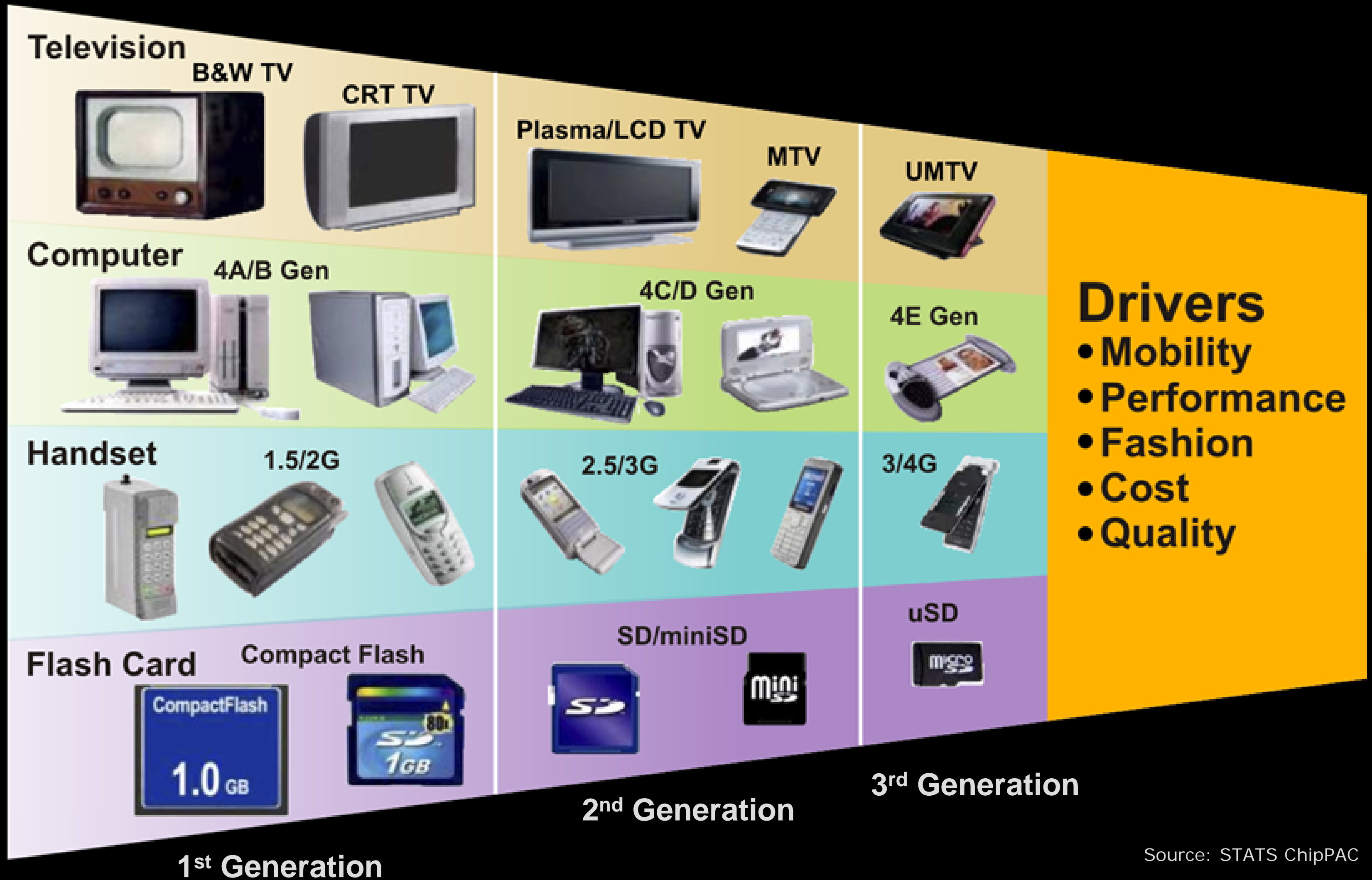
Overall Challenge to the Industry

Our future has a critical need for innovation and collaboration – across the boundaries of design, test and fabrication – to support the "faster", "more" and "cheaper" that are the requisites of the consumer economy.

THANK YOU!

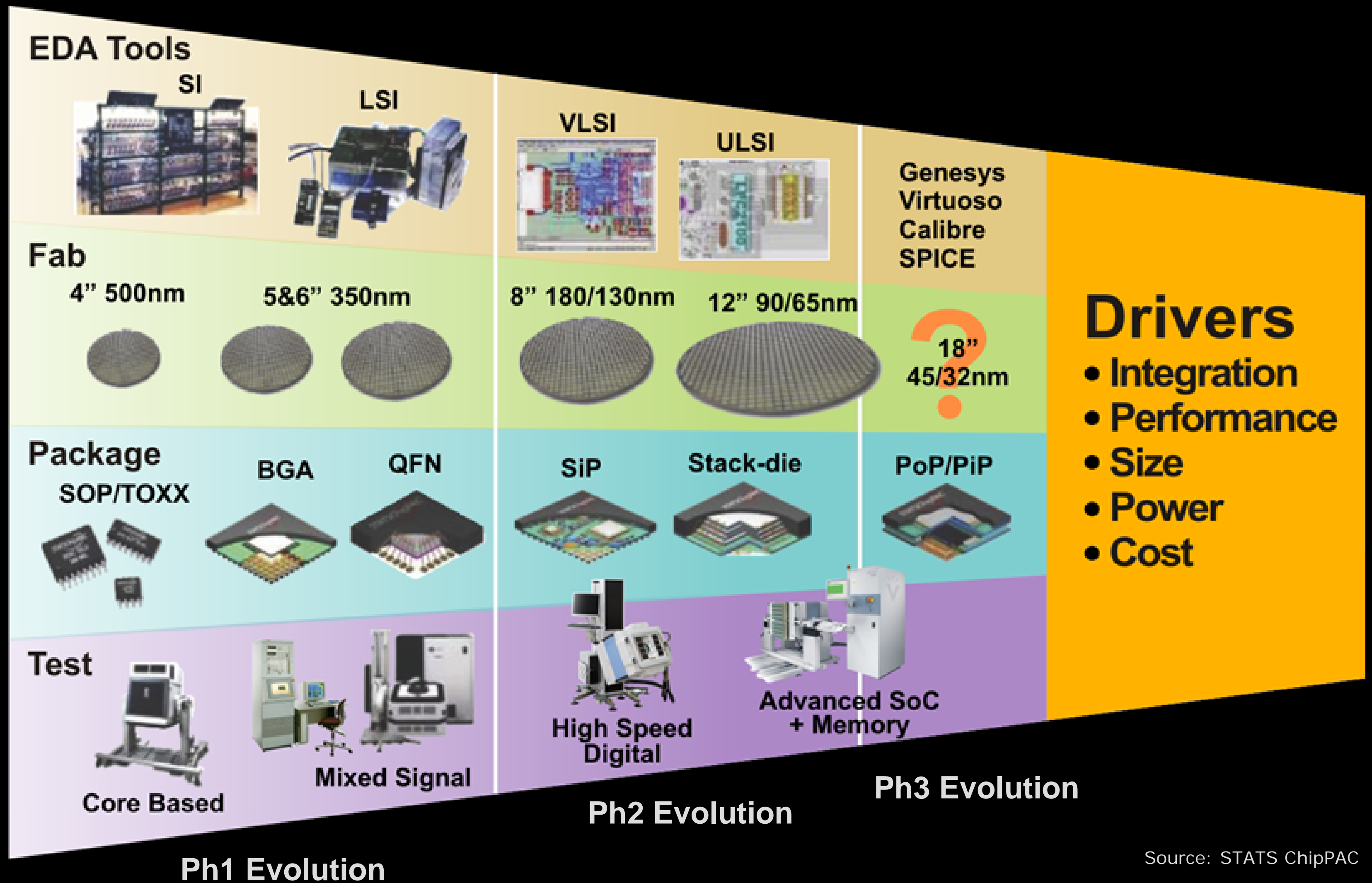
Back Up Slides

Rapid Technology Change & Consumerization



Source: STATS ChipPAC

Rapid Technology Change & Consumerization



Source: STATS ChipPAC