

**IEEE SW Test Workshop**  
Semiconductor Wafer Test Workshop



**Keith Imai**  
Semiconductor Test Consortium (STC)

***Tangible Value Can be  
Realized by Standardizing  
Probe Interfaces***



**June 8-11, 2008**  
**San Diego, CA USA**

# ***STC at a Glance***

- Global non-profit industry organization
- Main objective: develop & deploy value-added open test standards to benefit the industry
- Innovative collaboration initiated through technical, industry-driven Working Groups
- Diverse membership of leading companies, innovators & universities throughout the semiconductor supply chain

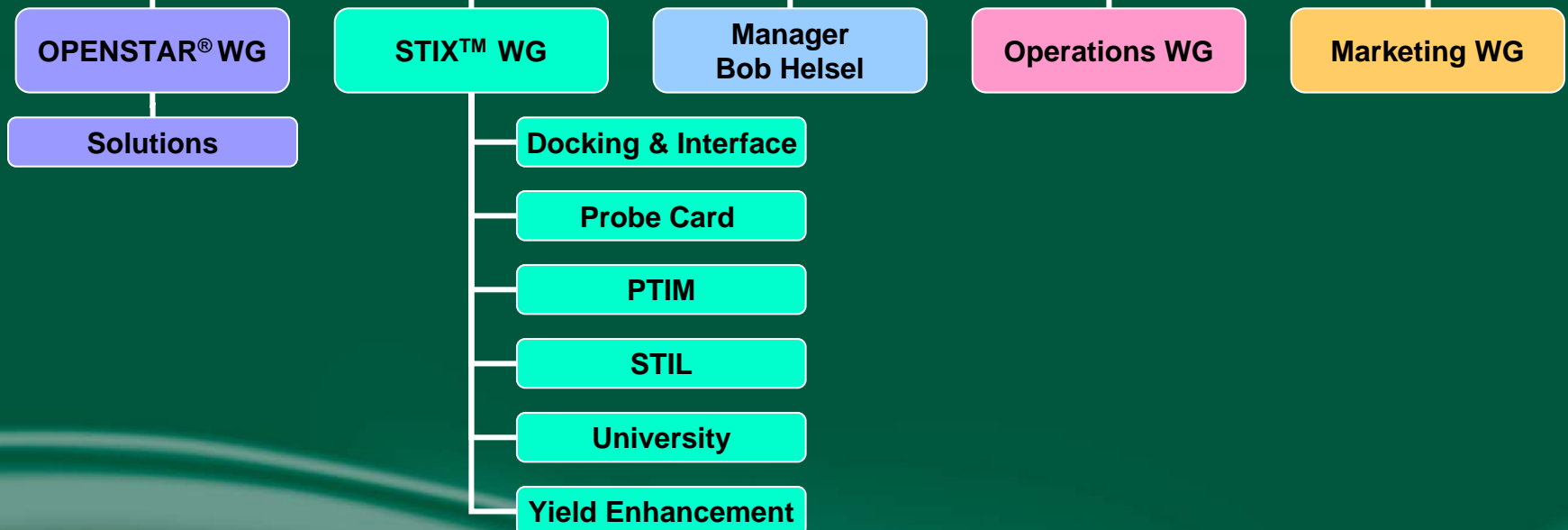


# Diversified Board

## STC Board of Directors

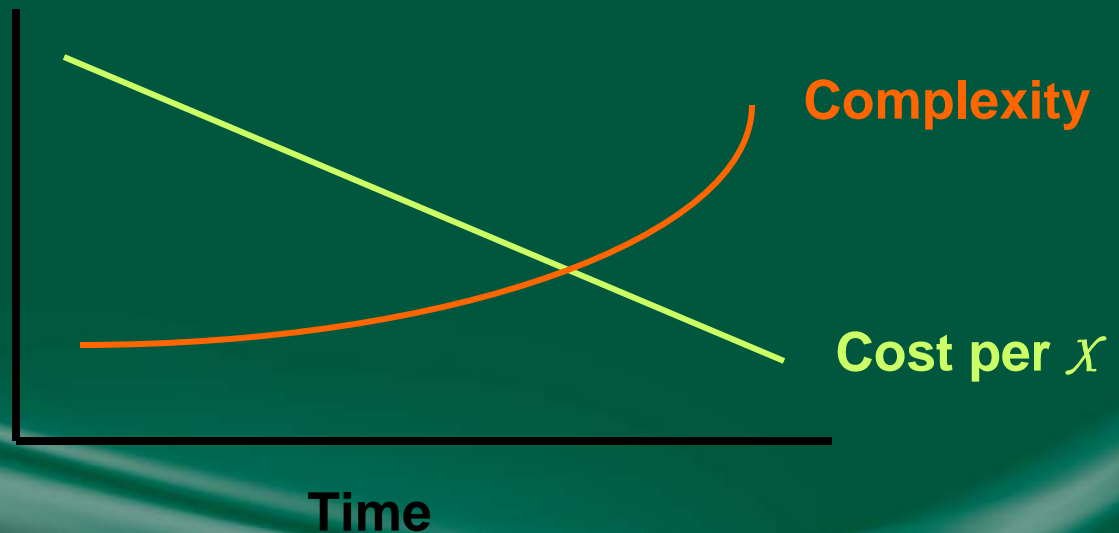
Chairman: Don Edenfeld (Intel)  
Co-chairman: Hideyuki Aoki (Renesas)  
Co-chairman: Klaus Luther (Infineon)

Billy Antheunisse (Texas Instruments)  
Paul Roddy (Advantest)  
Steve Wigley (LTX)



# Consumer Driven Market

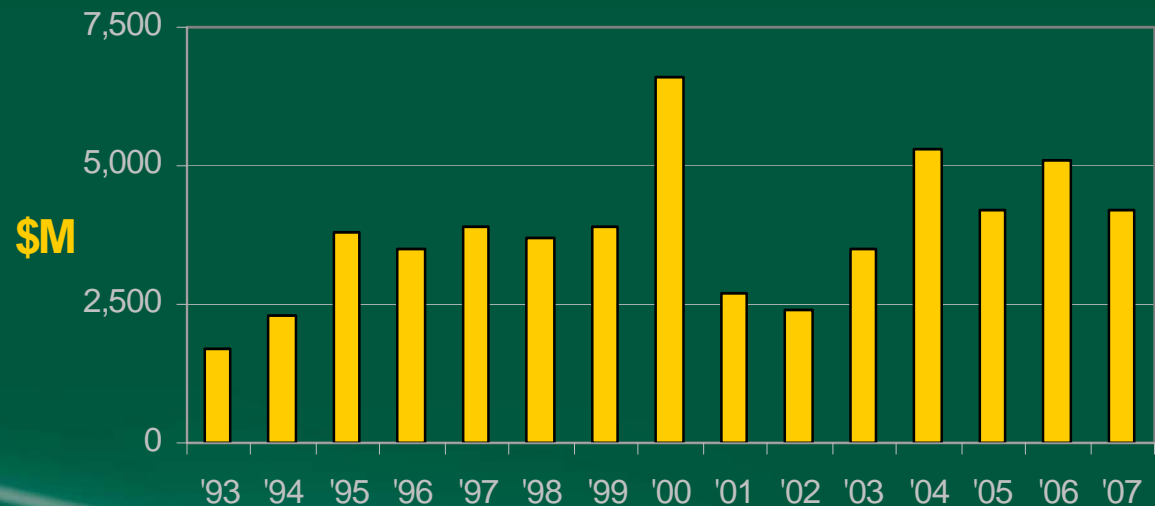
- Places great strain on supply chain
  - Time to market/volume/profitability is critical
  - Reduced total cost of test is a necessity
  - Device technology & integration are increasing
  - Product life cycles are shortening
  - Test requirements are increasing exponentially



# ***Volatile Industry Dynamics***

- Chaotic market is detrimental to supply chain
- Everyone's resources are stretched
  - Efficiencies & economies of scale are critical

**Semiconductor Test System Market**

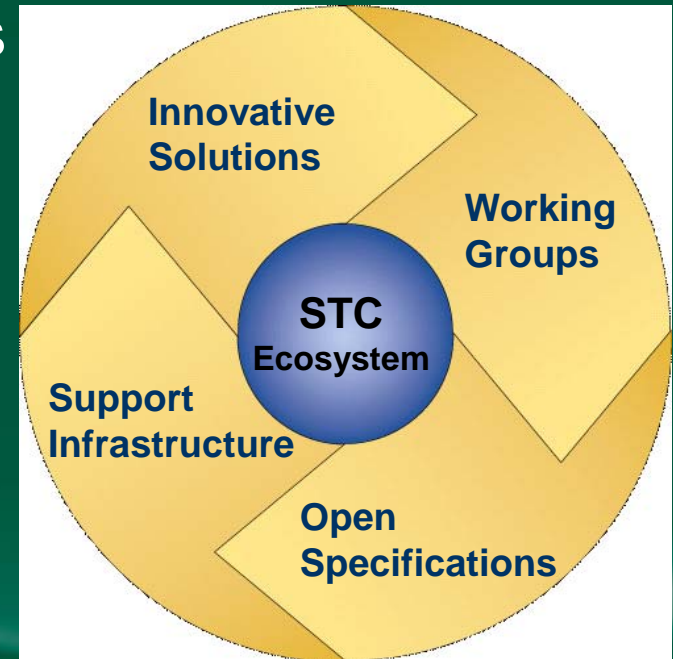


Source: Prime Research Group



# ***Collaborative Solutions are Necessary***

- Synergistic ecosystem elements
- Infrastructure enables quick solution deployment
- True open specifications:
  - Fully leveraged throughout supply chain
  - Enable “best-in-class” solutions
  - Facilitate innovation
  - Drive economies of scale

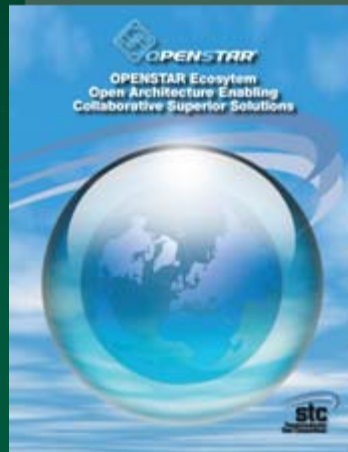


# STC Evolution



## Phase I Launch

- Established corporate infrastructure & core Working Groups
- OPENSTAR® specs published
- Achieved critical mass



## Phase II Traction

- 1<sup>st</sup> Third Party module developed
- OPENSTAR® specs improved
- Established new Working Groups



## Phase III Expansion

- STIX™ formalized
- Continued focus on providing value to industry
- Additional Working Groups forming



# ***STIX™ Expansion***

- “Semiconductor Test Interface eXtensions”
  - For areas around ATE





# STIX™ Enabled Opportunities

## Training

Test Engineers  
Product Engineers  
Techs & Operators

## Corporate Integration

ATE specs to Design rules  
ATE to Planning system

## Program Development

Test Programs  
Characterization Programs  
Test Vectors  
Data Collection

## "Black box" ATE



## Software

ATPG Tools  
Design to Test Tools  
Conversion Tools  
Virtual Test Tools

## Factory Integration

Hardware Specs  
Calibration  
GUI Interface

## Hardware Support

Probe Cards  
Mechanical Docking  
Load Boards  
Spares Inventory



# ***Probe-centric Groups***

***Hardware Support***  
***Probe Cards***  
***Mechanical Docking***  
***Load Boards***  
***Spares Inventory***

- Probe card WG
  - Japan driven
- Prober task team
  - Part of DIWG
  - Europe driven



# PCWG & DIWG Members



Never stop thinking



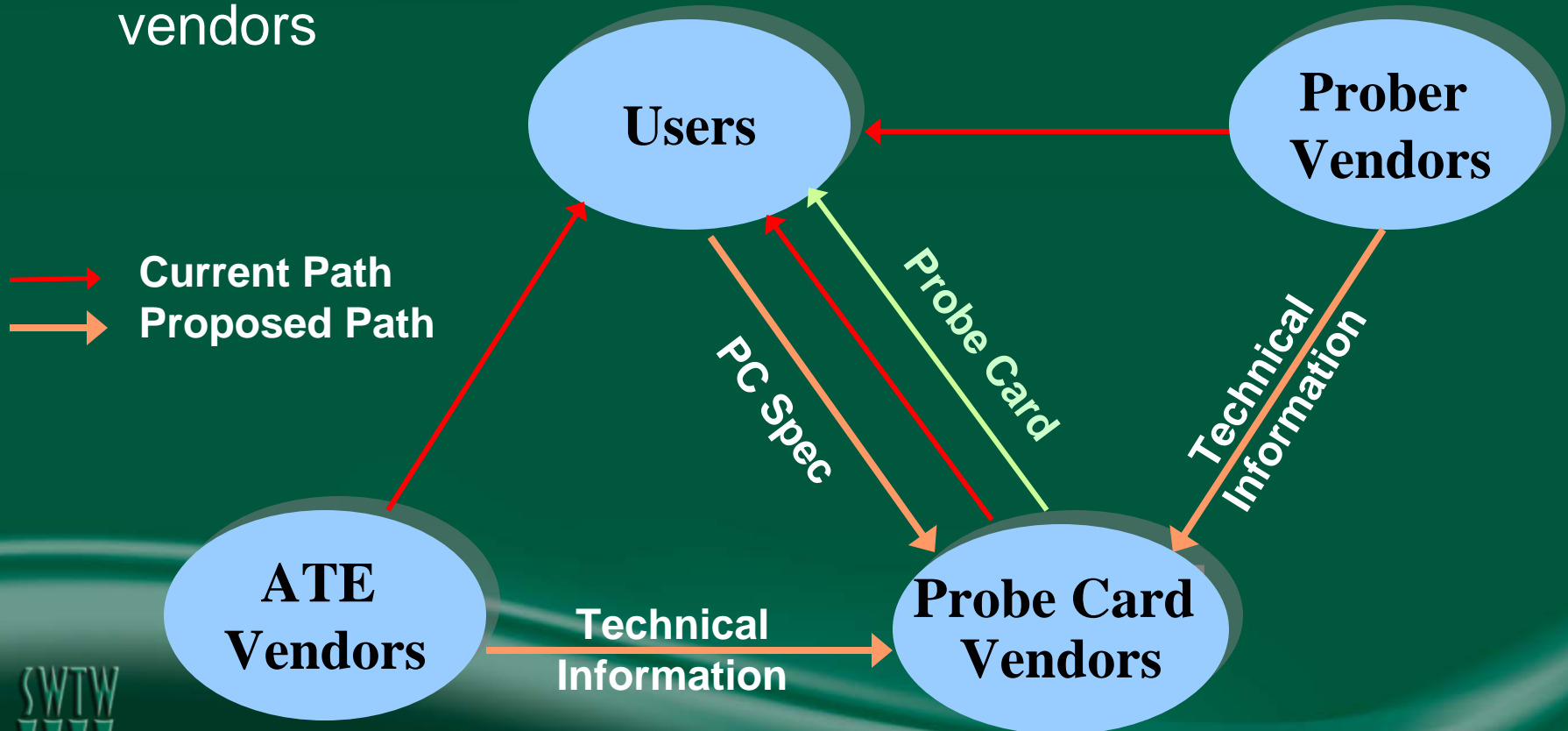
# PCWG

- Efforts initiated by Japanese members
  - Goals: shorten time to procure probe cards & standardize path
  - Achieved general consensus on key points & documentation
- First Japan/US WG meeting – March 13
  - Follow up meeting June 6 at GSC
- Vote on Rev. 0 specs ~ Q3'08



# Probe Card Order Placement Path

- Users no longer need multiple contacts
- Probe Card ordering info is managed between vendors
- Users can get up to date and controlled info from vendors



# Automatic Deployment of Documented Work Instructions

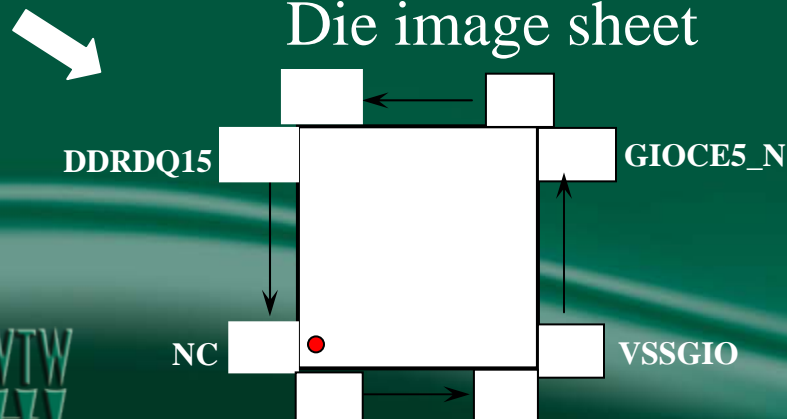
## User Input

Pad		Map of Probe point		Signal Path Spec.	
No.	NAME	X ( $\mu\text{m}$ )	Y ( $\mu\text{m}$ )	Net List	Signal Attribute
213	DDRAD0				
210	DDRAD1				
215	DDRAD10				
224	DDRAD11				
228	DDRAD12				
230	DDRAD13				
212	DDRAD2				
221	DDRAD3				
219	DDRAD4				
216	DDRAD5				
218	DDRAD6				

## Pad order sheet

Pad		Map of Probe po	
No.	NAME	X ( $\mu\text{m}$ )	Y ( $\mu\text{m}$ )
1	VSSC1		
2	VSSHDMI		
3	TOUTP_A		
4	TOUTN_A		
5	REXT_A		
6	VDDC2		
7	PXNC_A		

## Die image sheet



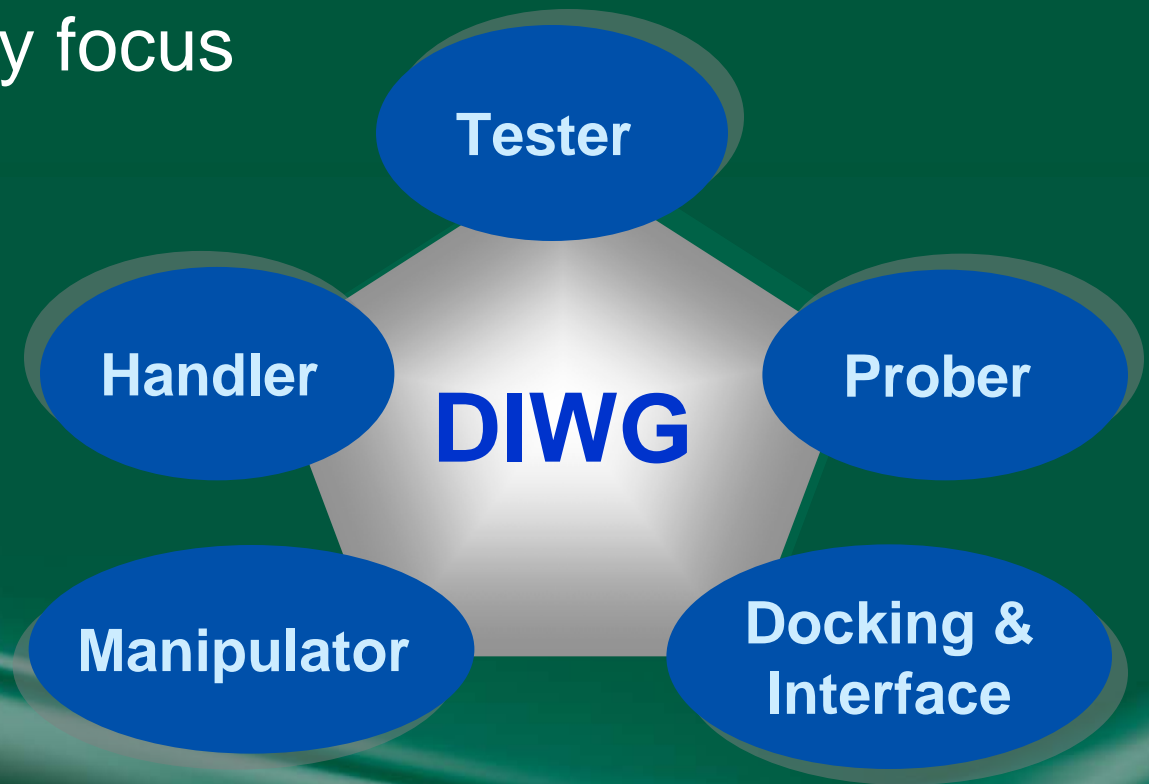
## Power Plane sheet

262	VSSDDR	0V3
265	VSSDDR	0V3
271	VSSDDR	0V3
48	VSSGIO	0V4
56	VSSGIO	0V4
68	VSSGIO	0V4



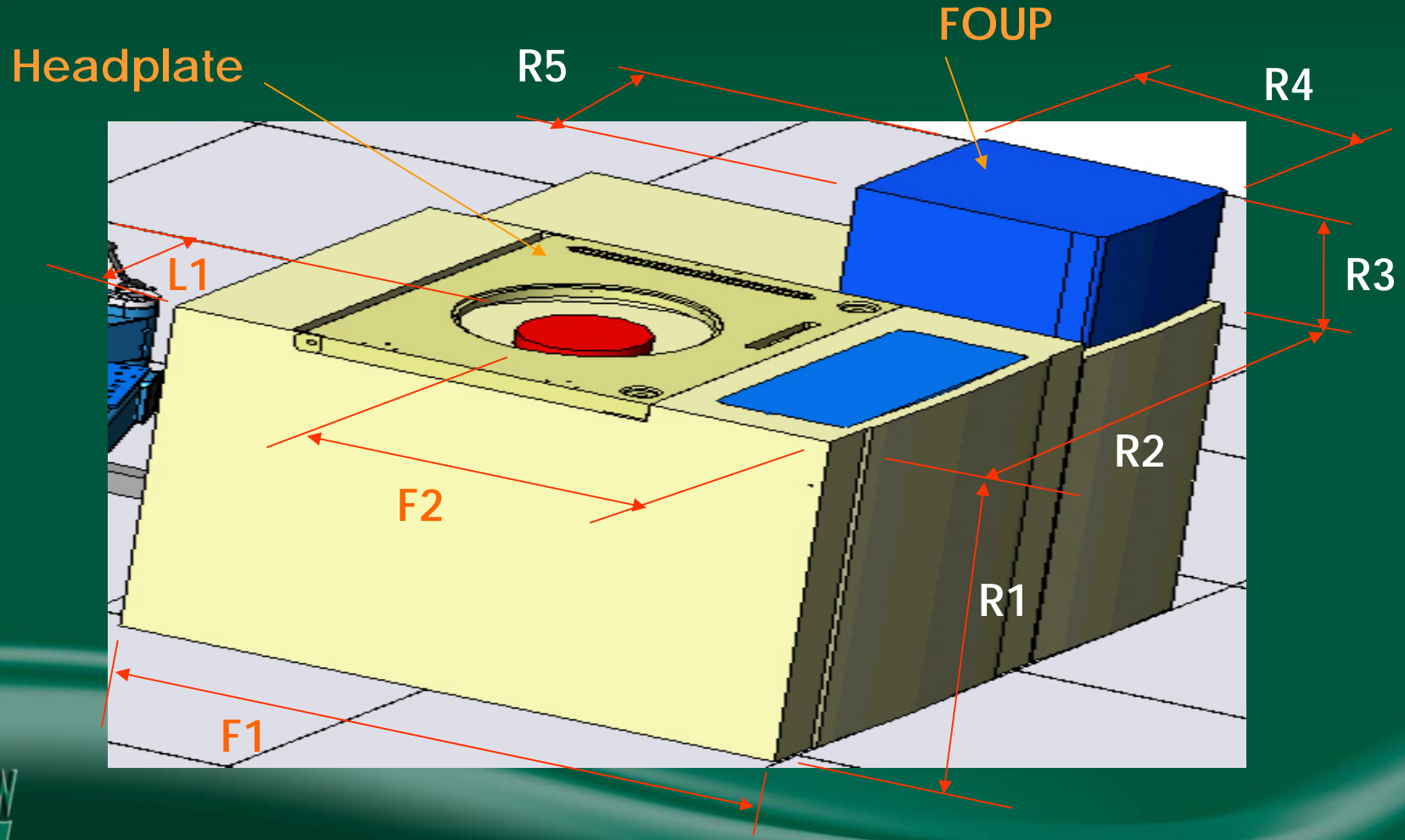
# ***DIWG: Task Teams***

- Formed Jan. 2007 in Europe
- First documents completed Oct. 2007
  - Terminology focus



# Prober Outline

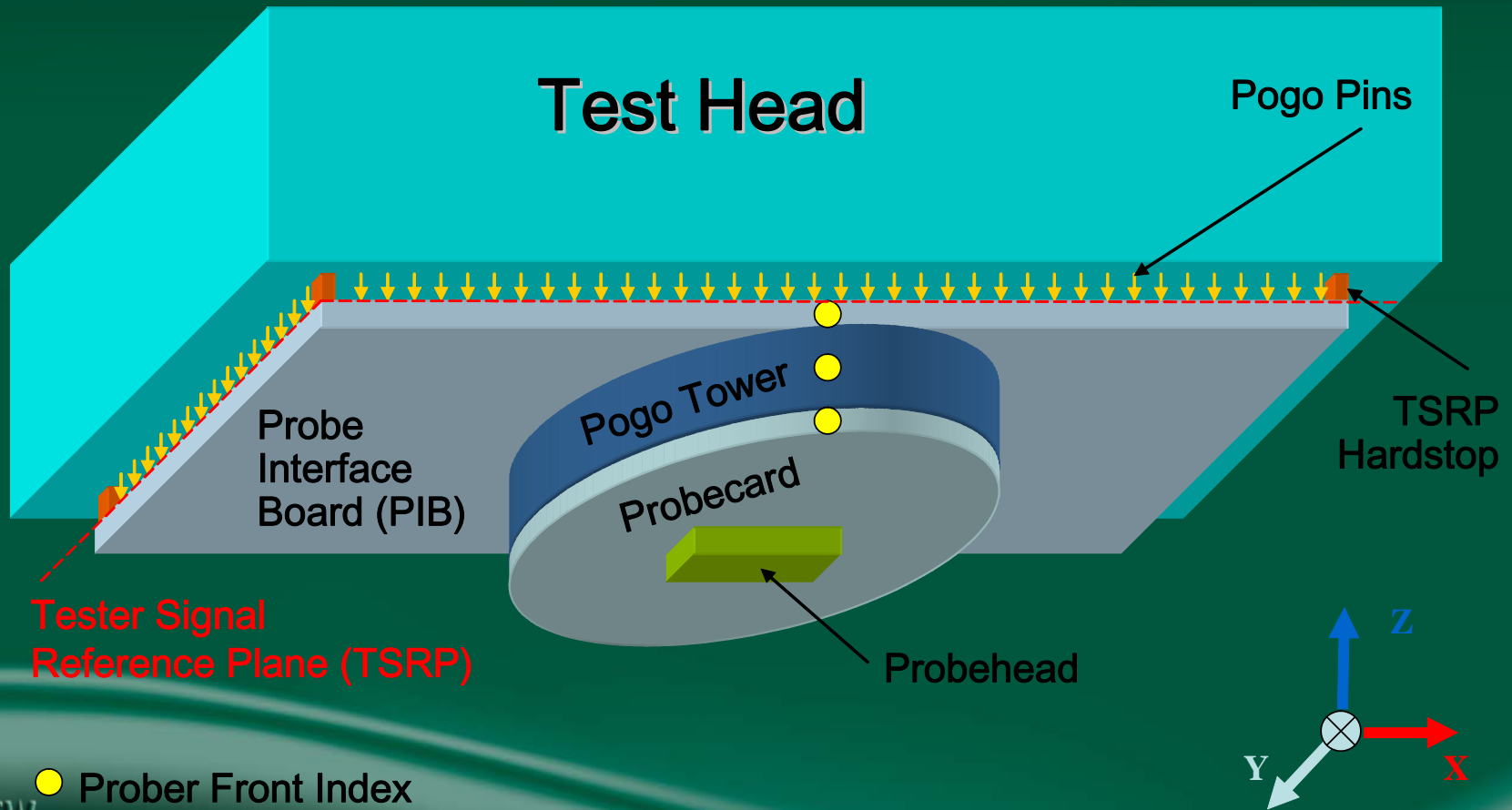
- Standardized naming conventions are key





# Sort Interface Terminology

- Multiple drawings for various implementations



● Prober Front Index



# 2008 Worldwide Calendar

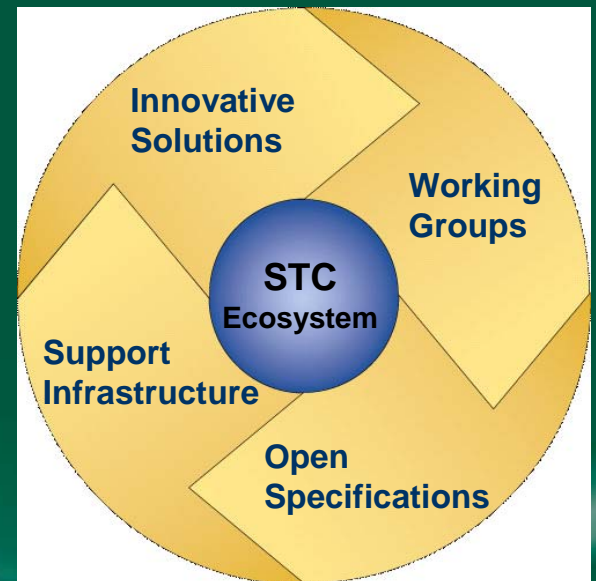
- 19 global activities
  - 5 regional meetings
  - 5 industry events
  - 4 major shows
  - 4 event meetings
  - 1 GSC
- Details on web site
  - [www.semitest.org](http://www.semitest.org)

Month	Japan	Asia	Europe	USA
Jan. 2008				ISS (Half Moon Bay) Jan. 15
			GM @ Infineon Jan. 31	VLSI Chip Insider Live. Jan. 16
Feb.				
March	GM - Tokyo March 26	Semicon China Mar. 18-20		GM (Austin) Mar. 13
Apr.				
May			@ ETS (Italy) May 25-29	
June	Global STC Conference: June 4-6 in San Diego, CA			
				SWTW June 8-11
July				Semicon West July 15-17
Aug.				
Sept.	GM Sept. 24	Semicon Taiwan GM/Dinner event ~Sept. 9-11	Reliability conference Ingolstadt, Germany Sept. 29 - Oct. 1	GM (Boston?) Sept. 18
Oct.			Semicon Europe Dinner meeting Oct. 8	Dinner event Oct. 27
				ITC - Santa Clara Oct. 28-30
Nov.				
Dec.	GM/Dinner event Dec. 4			
	Semicon Japan Dec. 3-5			



# ***STC Value Proposition***

- Active Working Groups focused on driving value-added solutions to industry
- Synergistic ecosystem enables timely, cost-effective solutions to meet dynamic market challenges
- Membership is open to all
- [www.semitest.org](http://www.semitest.org)



*Thank you  
for your attention*

