IEEE SW Test Workshop
Semiconductor Wafer Test Workshop

**Gert Hohenwarter**
GateWave Northern

# Effect of ground return path on timing accuracy

GateWave Northern, Inc.

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# Objective

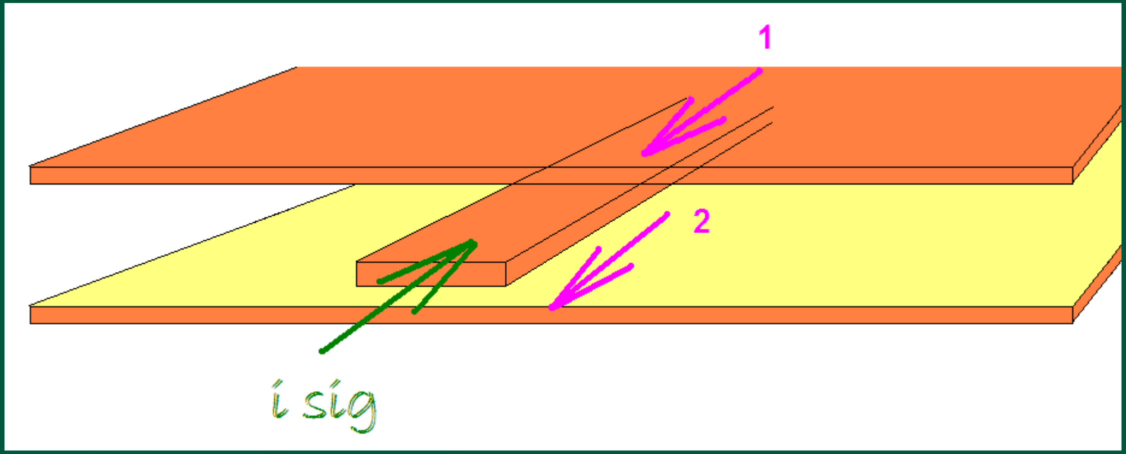
- Review problem of ground path
- Identification of trouble spots
- Assessment of individual impact
- Demonstrate significance
- Summary

# Approach

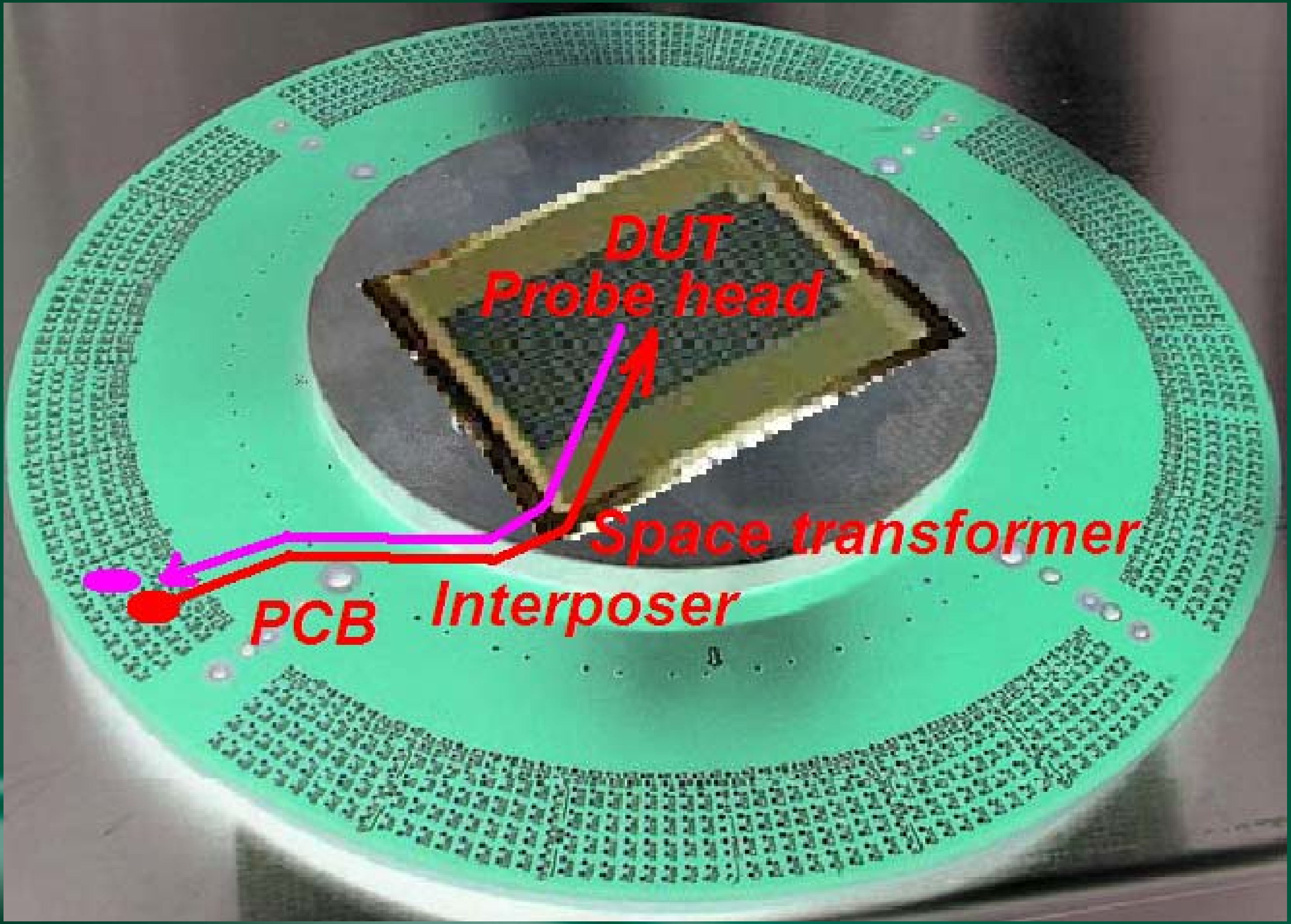
- Examine complete signal path in a probecard
- Develop models (FEA, SPICE)
- Use models to evaluate impact of changes
- Provide select measurement results to corroborate models

# Problem

- Signal in transmission line needs a return path
- This path must be located physically close to the signal
- Disruptions/detours add inductance and therefore delay

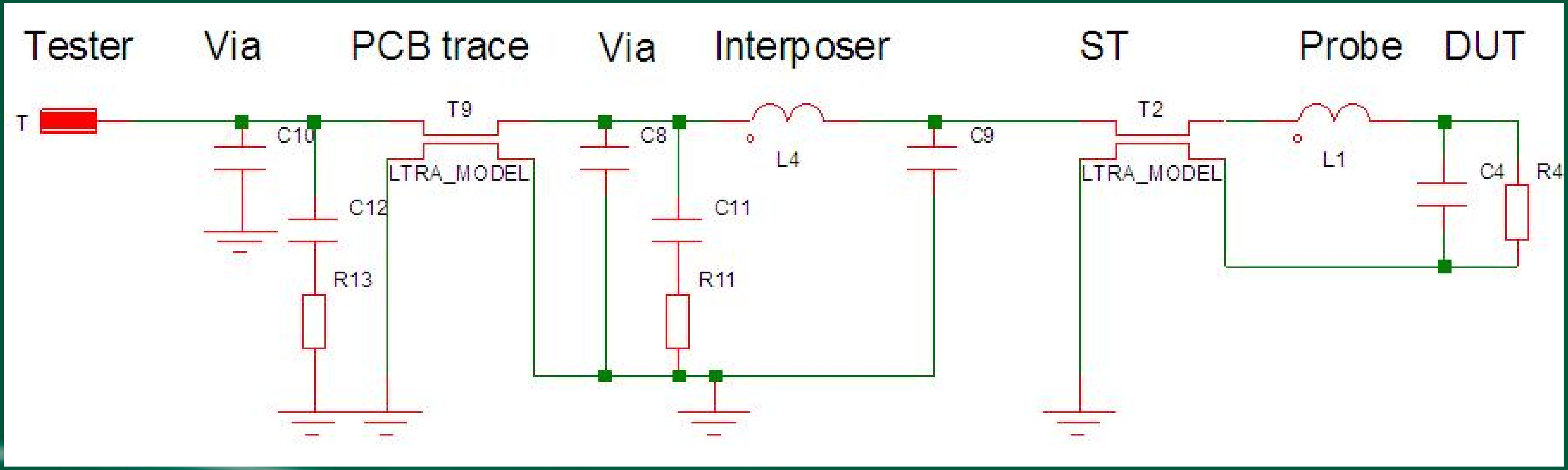


# Probe card signal path



# Probe card signal path

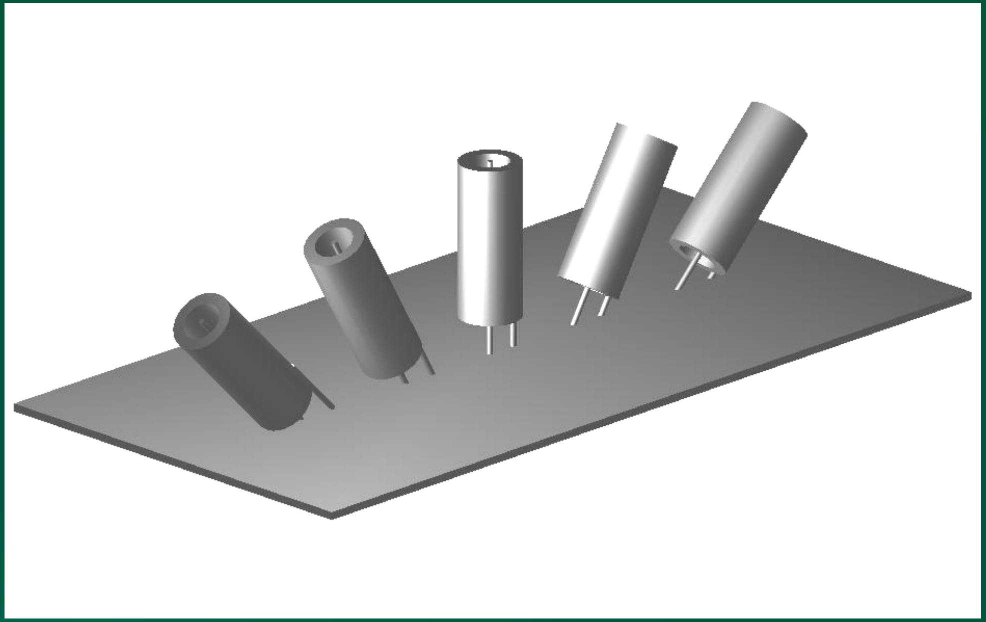
- The signal path in the probecard begins at the perimeter with a tester connection and ends at the probe tip with a connection to the DUT




Alongside the signal path a ground return must be provided

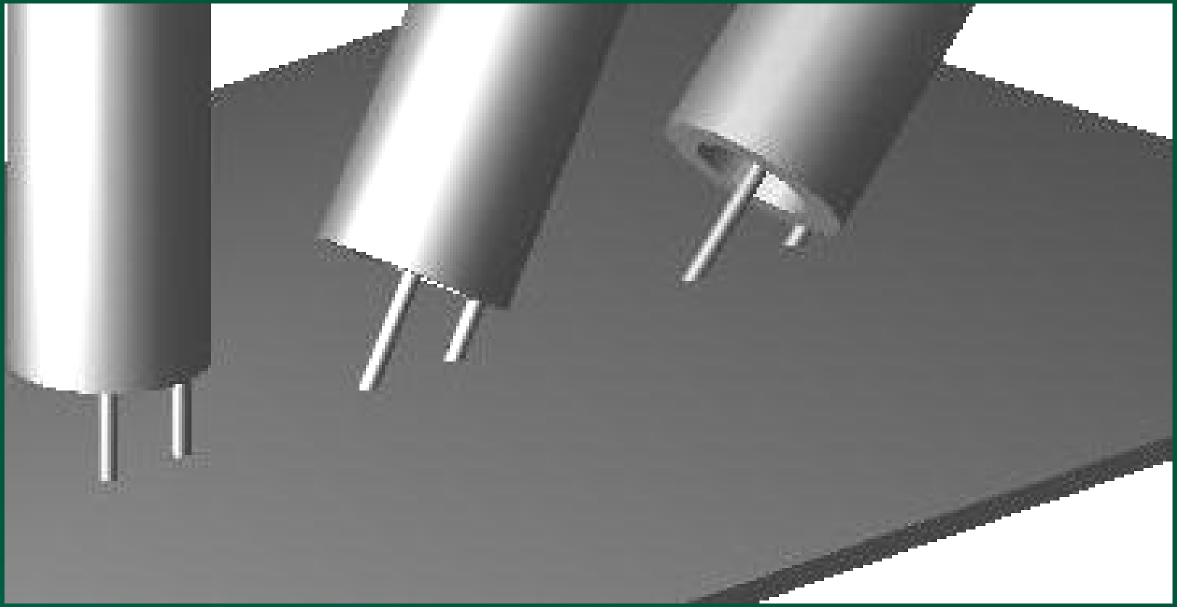
# Follow the signal…..

- Timing verification begins at the tester connection with a time domain reflectometer and a test probe…..



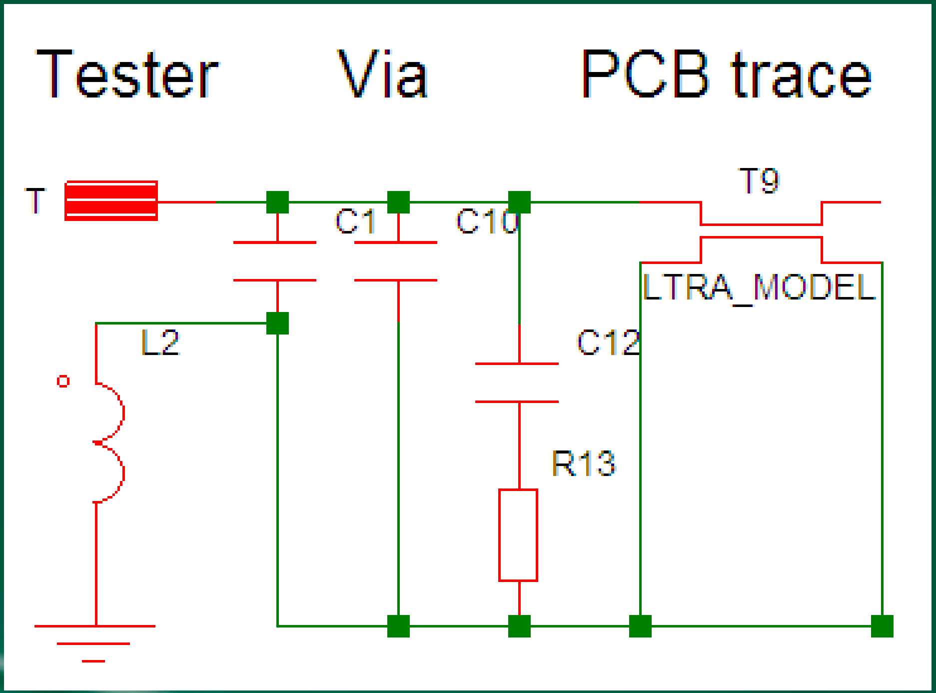
# …through the probe…..

- Common probes often have a fixed signal contact and movable connection at ground:



# Consequences

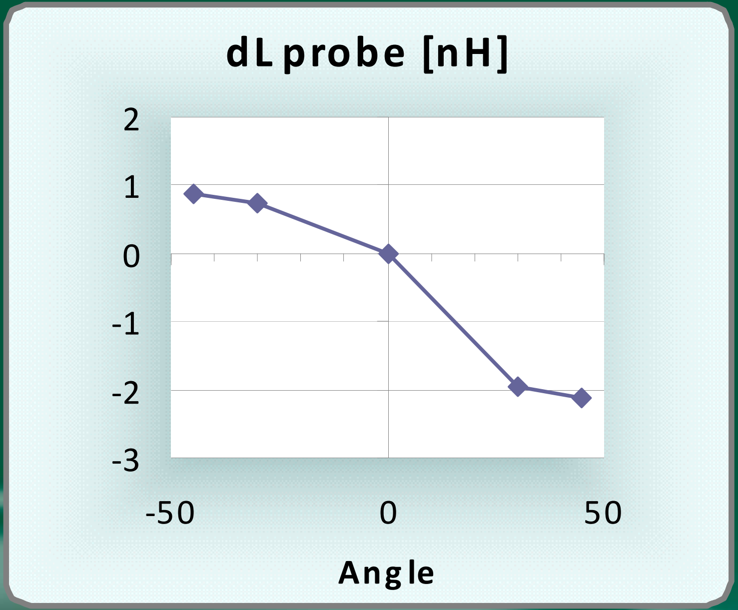
- Ground path inductance changes
- Signal path capacitance changes



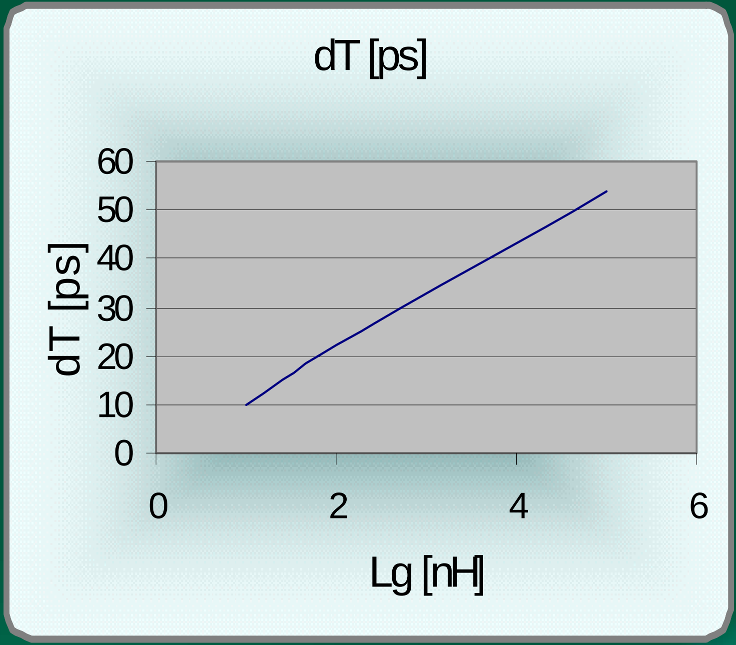
# Consequences

- Ground path inductance changes
- Signal path capacitance changes
- Delay changes

FEA analysis

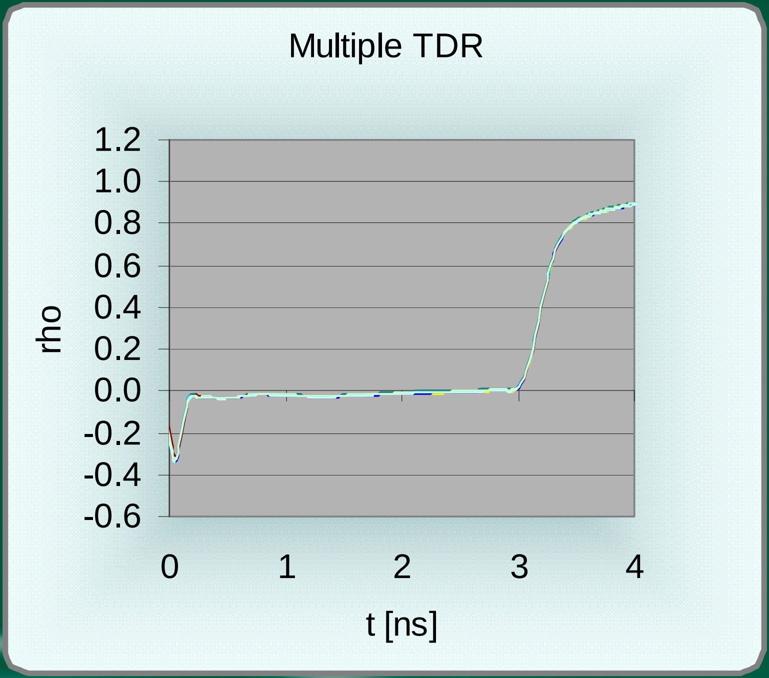


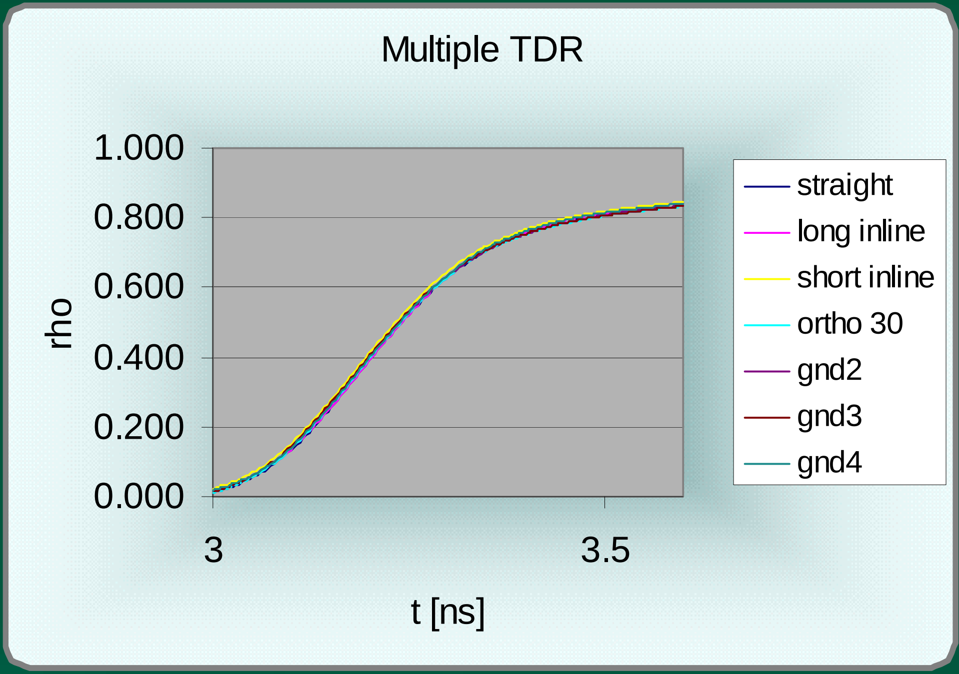

SPICE model



# Verification

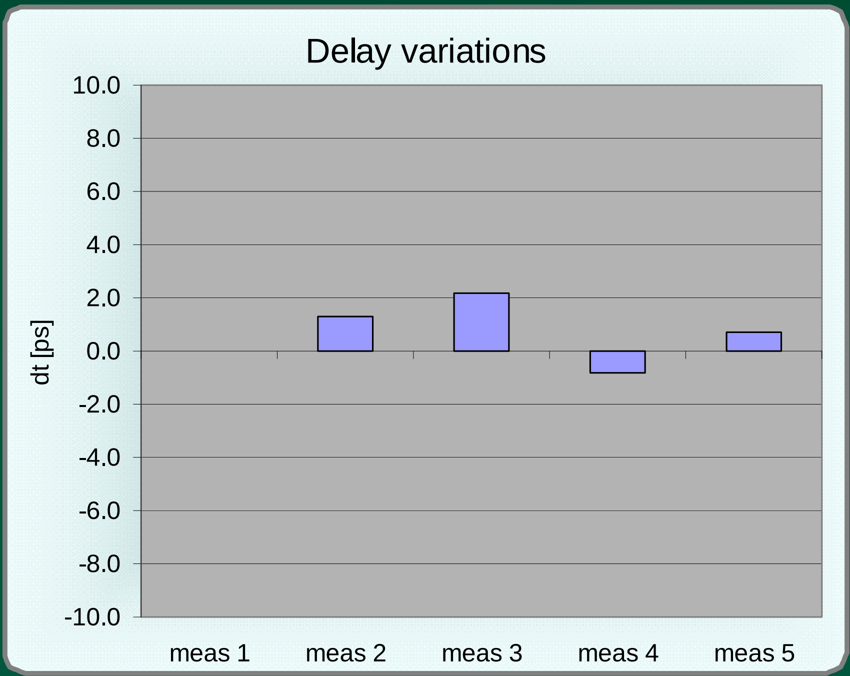
- Measurement at actual probecard PCB
- At first glance everything is fine….



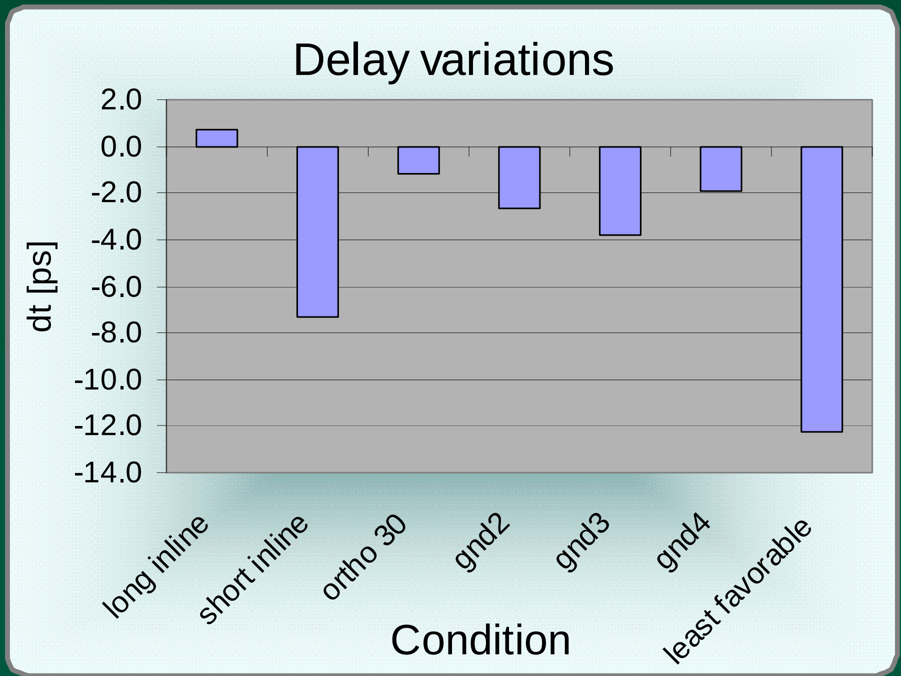
# Delay extraction

- When processing the data, differences become noticeable




Measurement to measurement

(probe straight)




For different probe positions

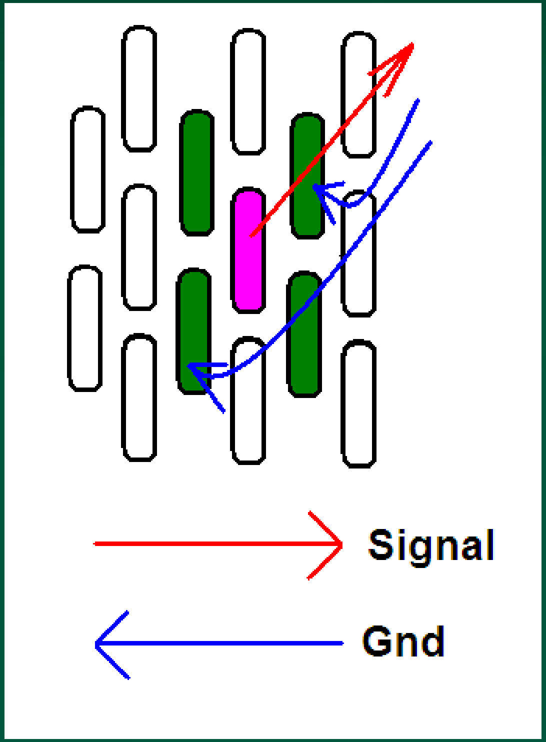
**dT counter: ->**

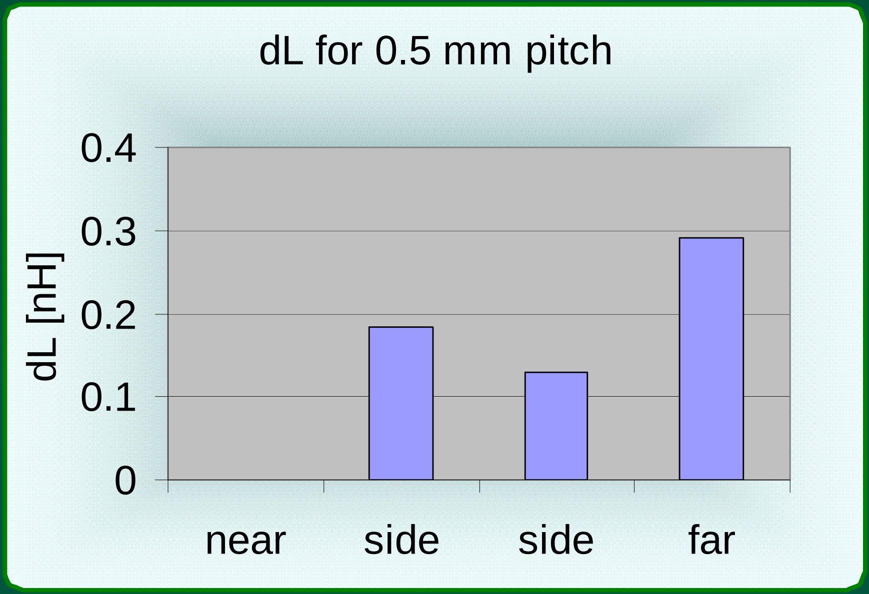
| | | |
|---|---|---|
| dT = | 5 | ps |
| **dT tot=** | **5** | **ps** |

(average, not max. dT)

# Follow the signal…..

- Ground via selection (only one ground via present for each case):



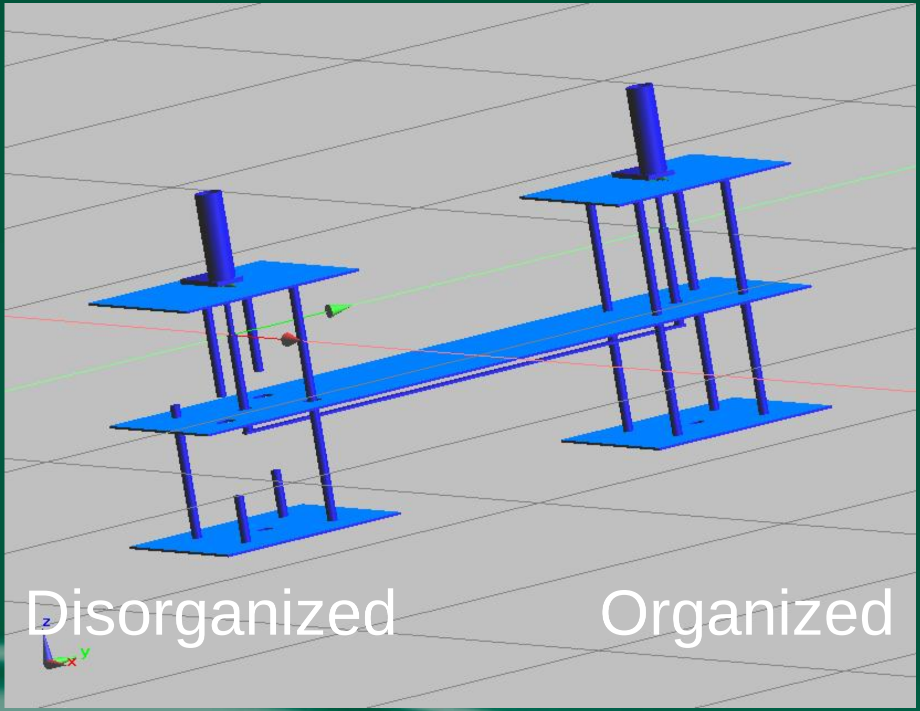



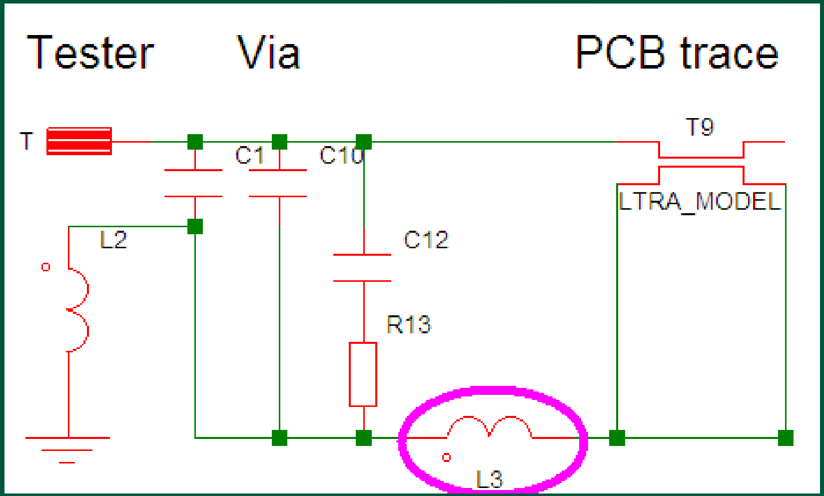

Inductance difference for 0.5 mm pitch

| | | |
|---|---|---|
| dT = | 3 | ps |
| **dT tot=** | **8** | **ps** |

# Follow the signal…..

- The signal travels into the PCB through a connector and returns through an array of vias:

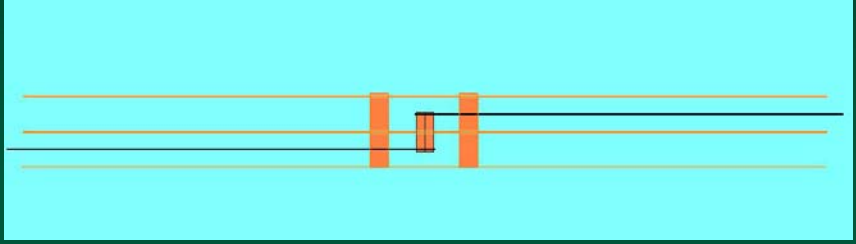


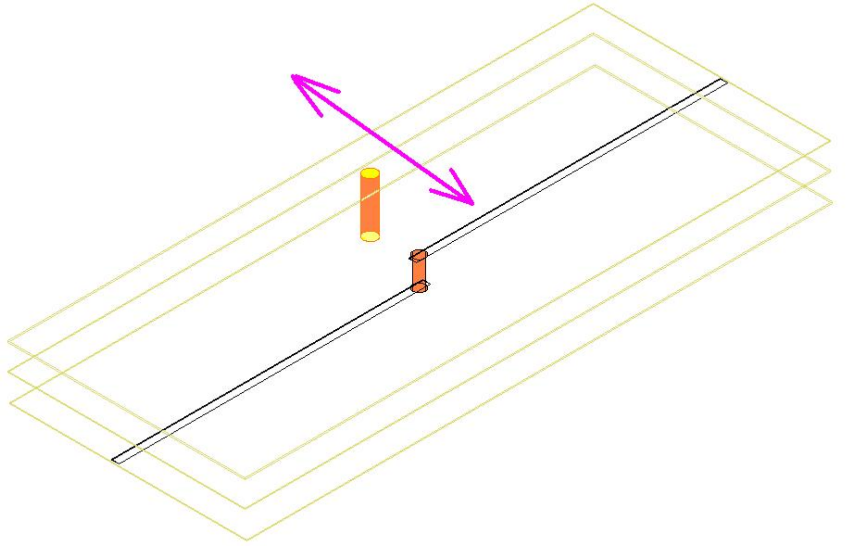



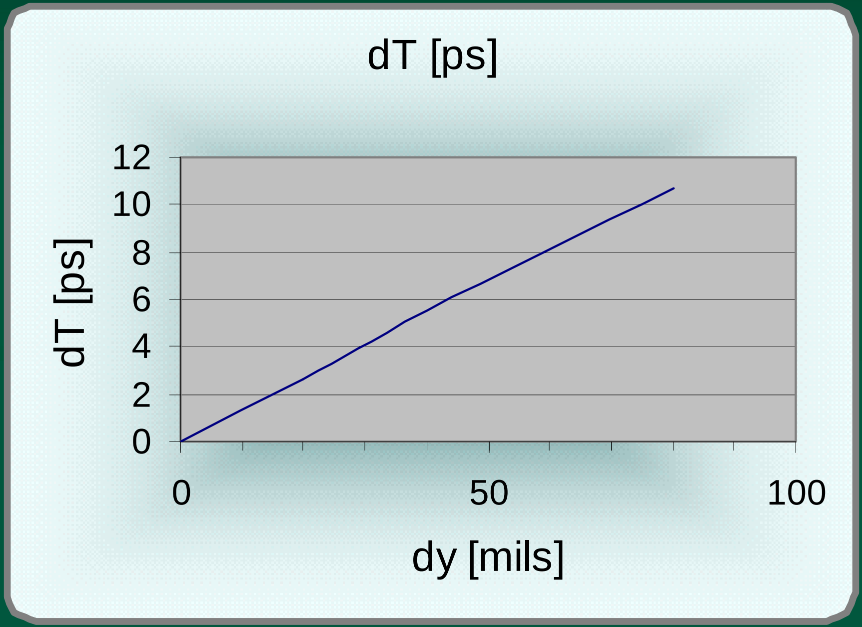

| | | |
|---|---|---|
| dT = | 10 | ps |
| **dT tot=** | **18** | **ps** |

# Follow the signal…..

- PCB via position (vias must be provided near level shifts):





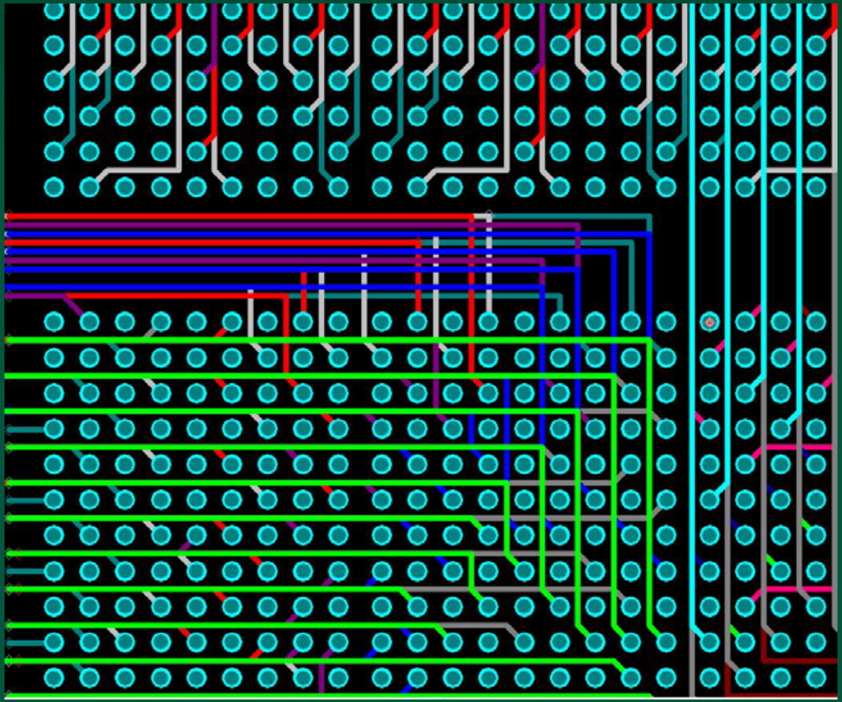



Inductance change as a function of lateral via position

| | | |
|---|---|---|
| dT = | 5 | ps |
| **dT tot=** | **23** | **ps** |

# Follow the signal…..

- Ground planes are disrupted in LGA/interposer area



Inductance per unit length changes

If traces get close to via antipads, capacitance per unit length changes, too

Example (inductance only):

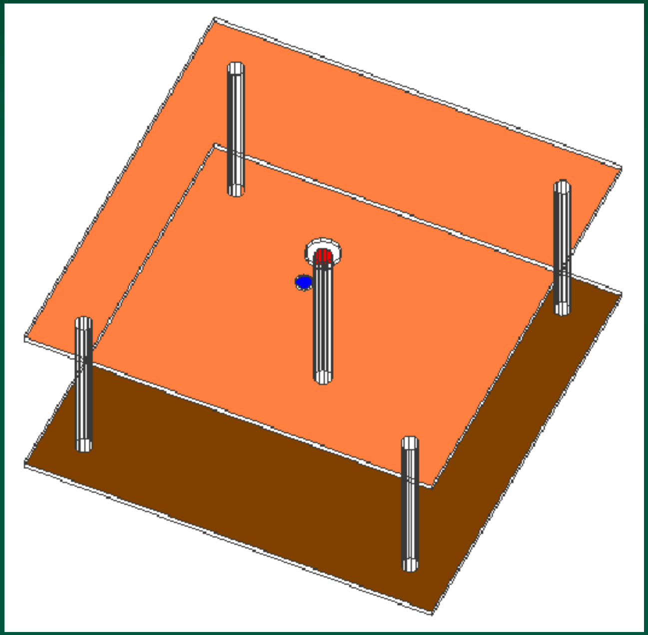
Uniform array of 1mm pitch vias

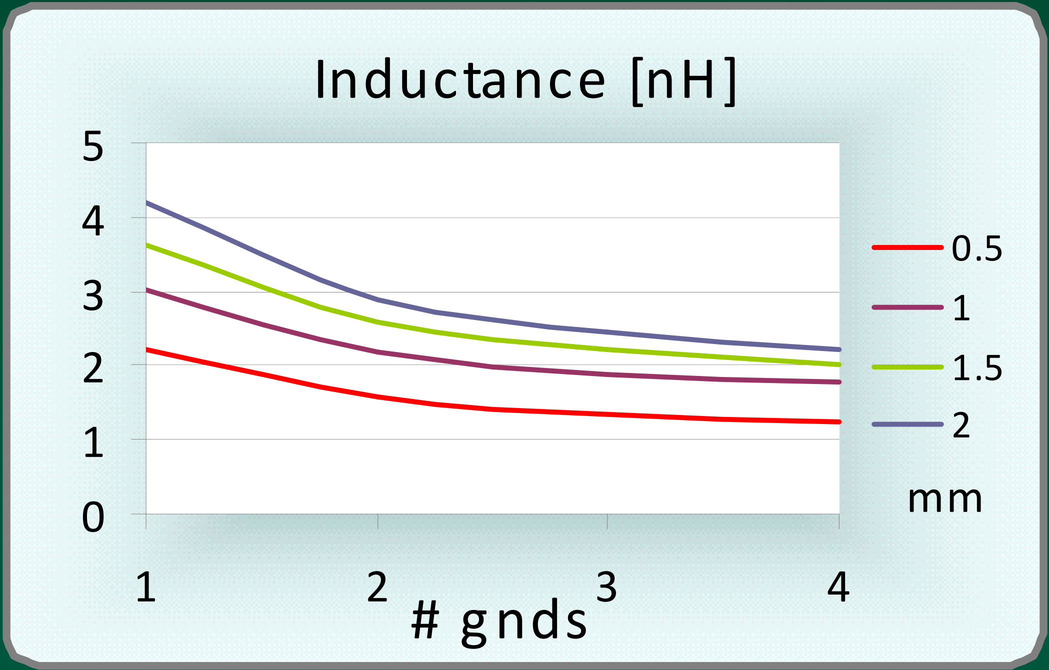
Ground path inductance changes by 12% for a 40 mm long path

| | | |
|---|---|---|
| dT = | 16 | ps |
| **dT tot=** | **39** | **ps** |

# Follow the signal…..

- Ground via positions in the interposer contact array



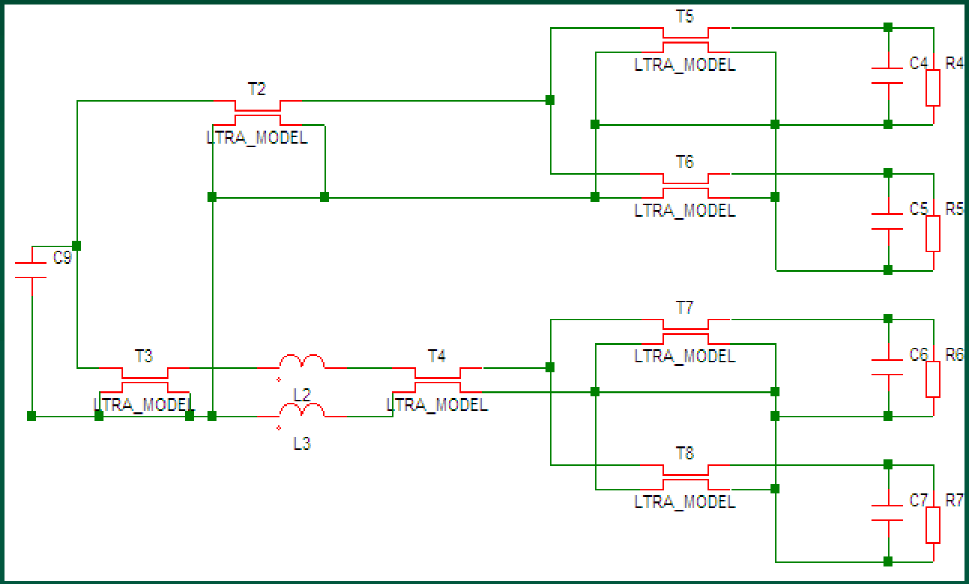


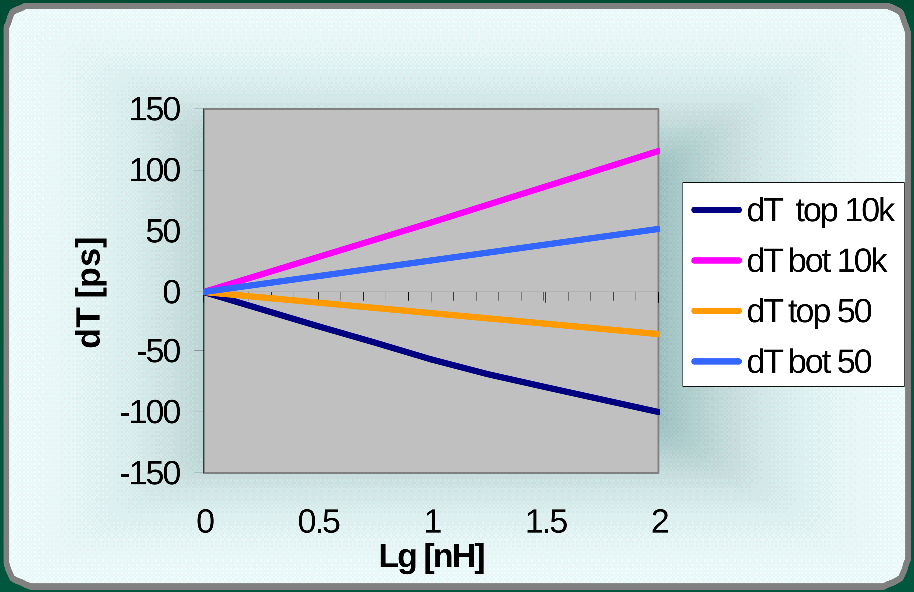

Inductance as a function of via distance from signal and number of ground vias

| | | |
|---|---|---|
| dT = | 10 | ps |
| **dT tot=** | **49** | **ps** |

# Follow the signal…..

Delay change as a result of branch imbalance in ground path



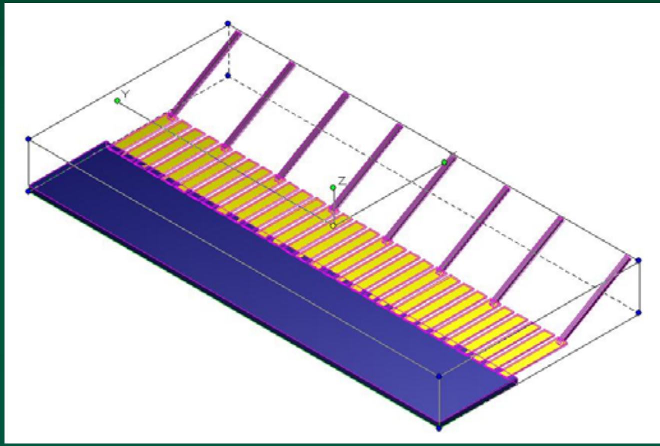




Different load conditions result in different delay changes

| | | |
|---|---|---|
| dT = | 30 | ps |
| **dT tot=** | **79** | **ps** |

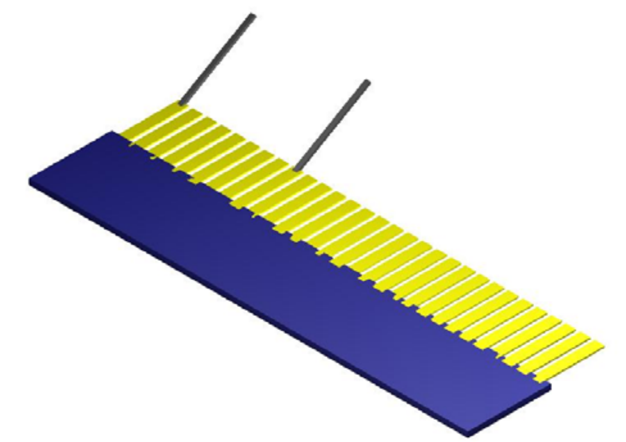
# ....to the DUT

Delay change as a result of grounding configuration at the DUT



Dense ground

With typical dimensions assumed the inductance difference for the two different configurations is 0.88 nH

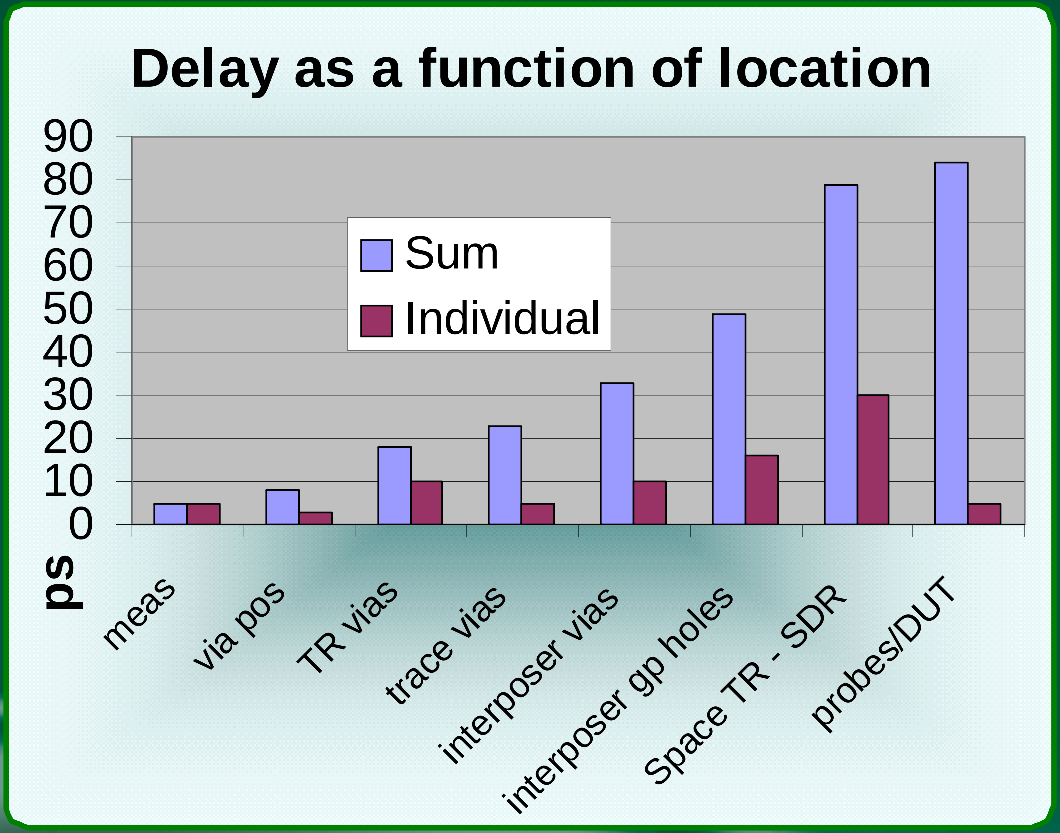


Sparse ground

| | | |
|---|---|---|
| dT = | 5 | ps |
| **dT tot=** | **84** | **ps** |

# Overall changes

Graphic representation of relative change as a function of where change occurs

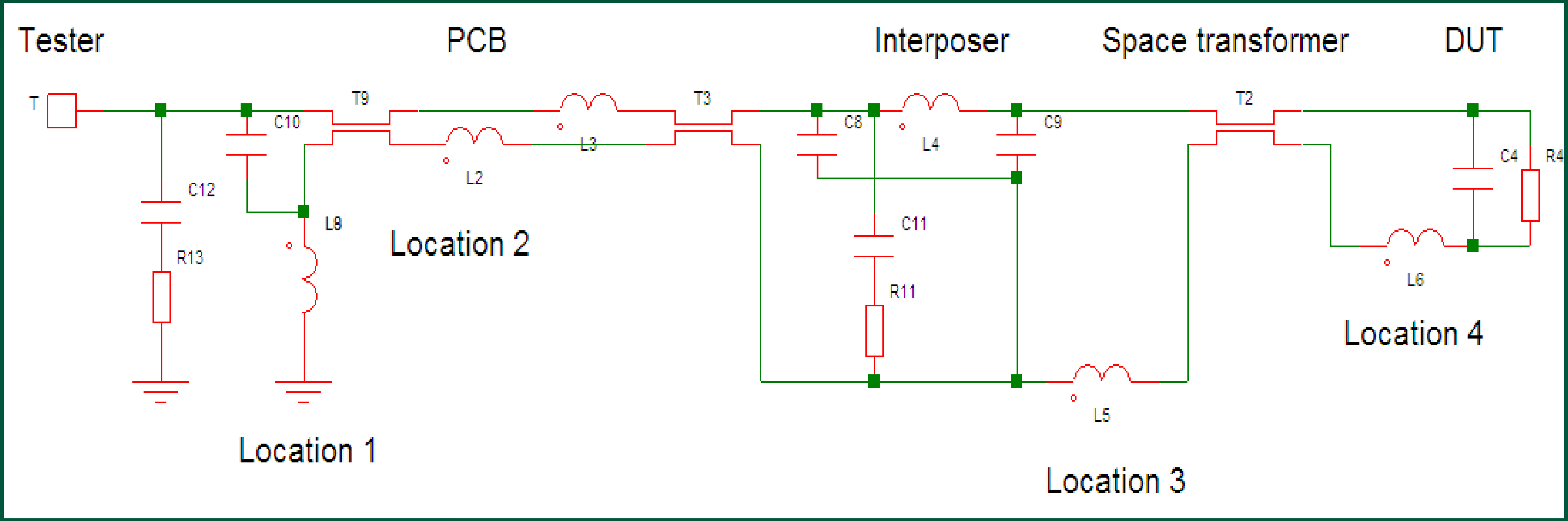



Comment:

Line length matching to within 20 mils results in an inaccuracy of 3.5 ps

# The impact of location

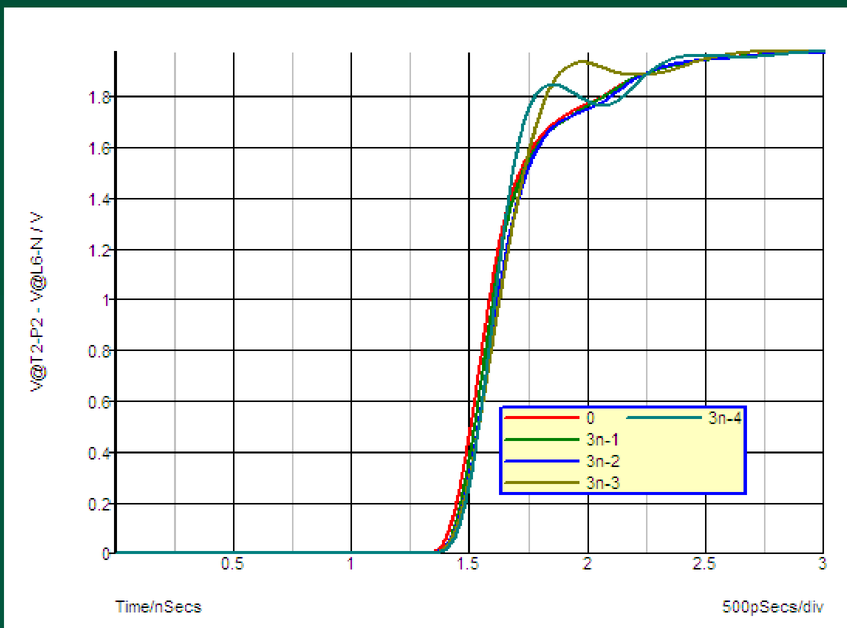
Delay change as a result of inductance change at different locations along the signal path



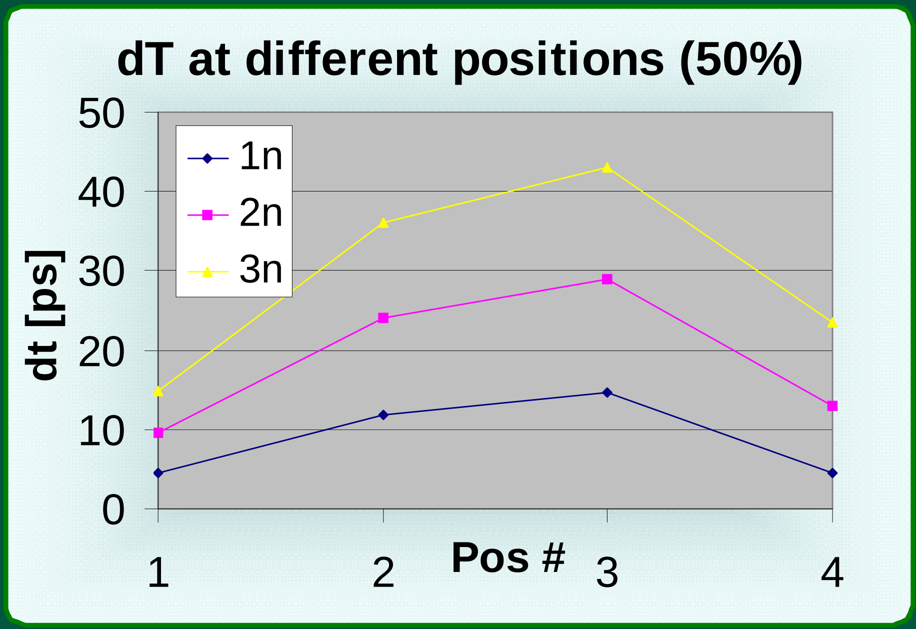

Approximate equivalent circuit of signal path

# The impact of location

Delay change as a result of inductance change at different locations along the signal path



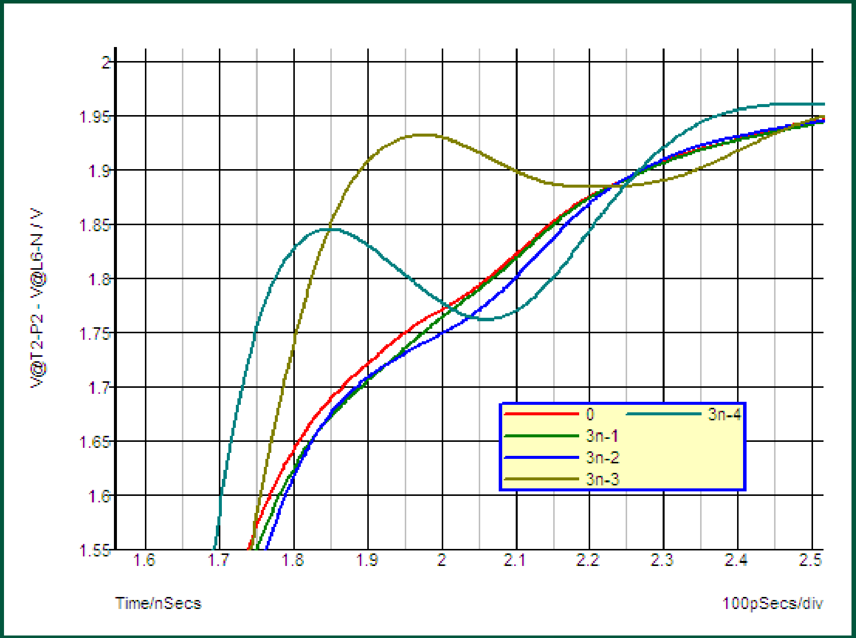

Signal at DUT (SPICE simulation)



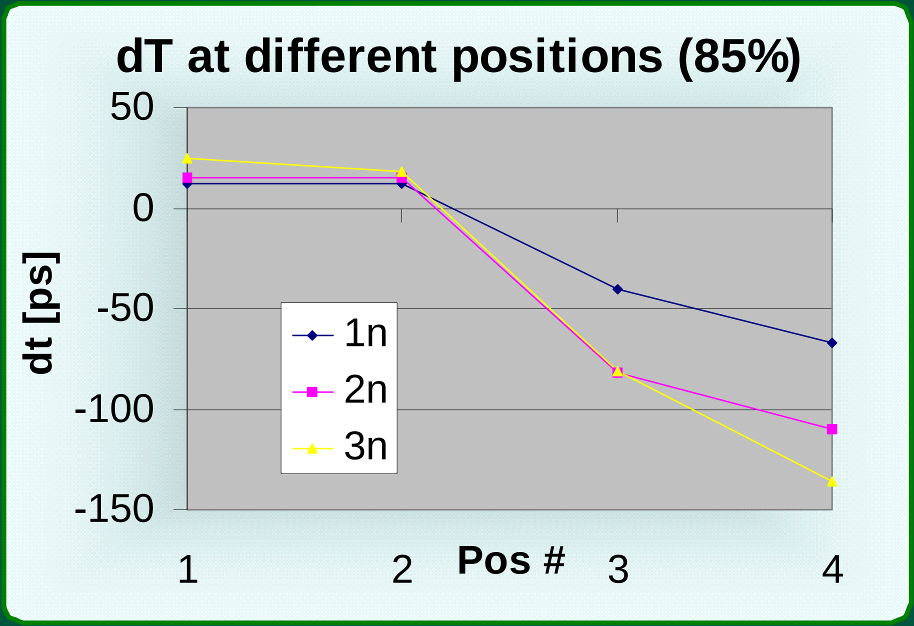

Delay change

# Waveform change

Wave form changes as a result of inductance change



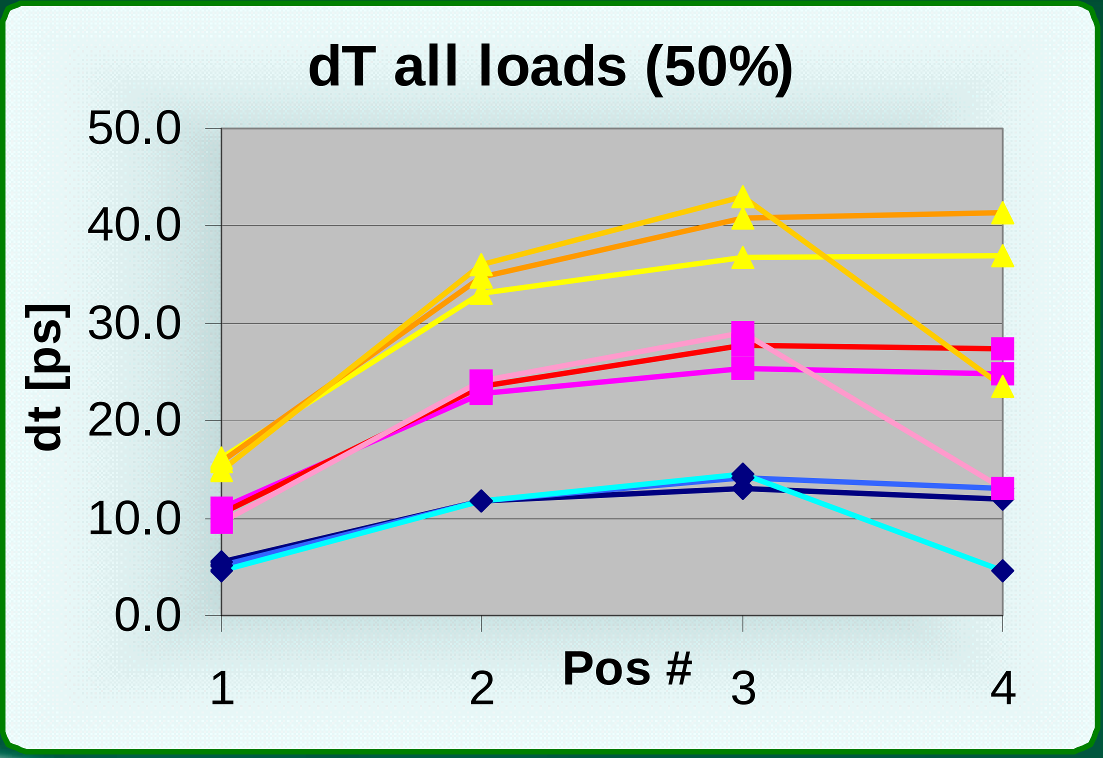

Signal at DUT (SPICE simulation)




Delay change

# Different loads

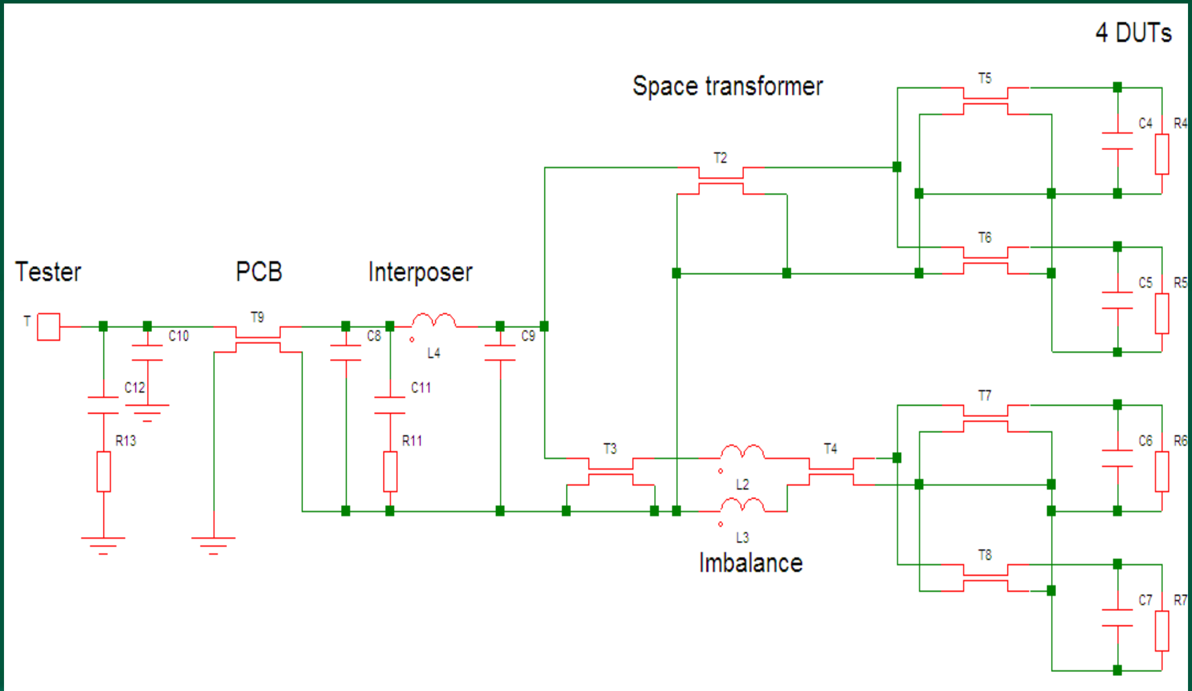
Delay change for 3 different cases (10kOhm 2pF, 150 Ohm 2pF, 50 Ohm)



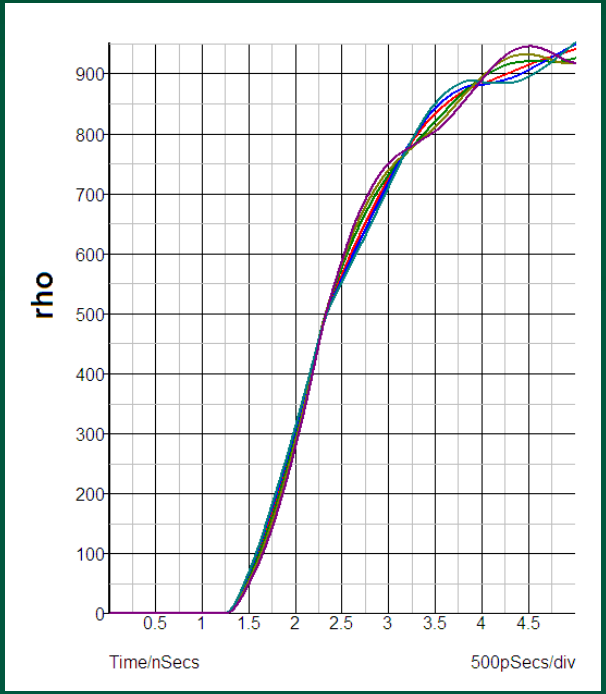

Load has additional impact on skew

# Shared resources

Delay change as a result of inductance change in case of split lines/ shared drivers



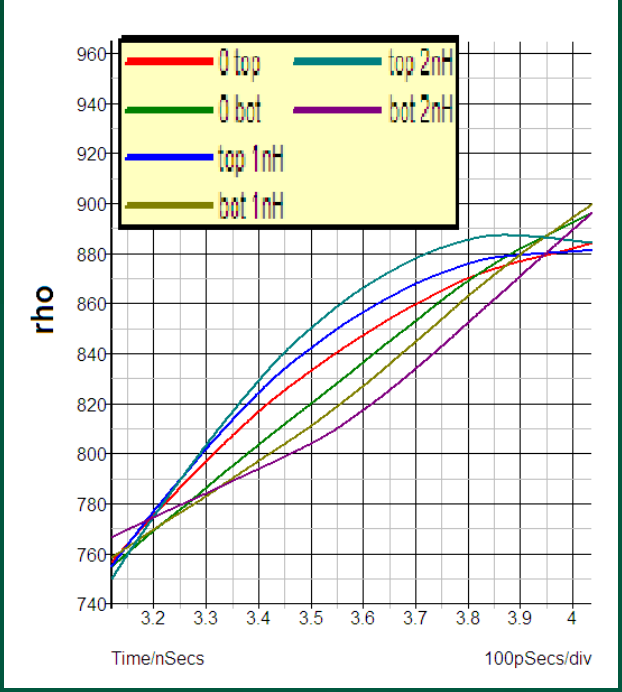

Simplified equivalent circuit




Signal change

# Shared resources

Delay change as a result of inductance change in case of split lines/ shared drivers




| | | Delay change | | |
|---|---|---|---|---|
| | | Unperturbed branch | Perturbed branch | |
| nH | 0 | 0 | 0 | ps |
| | 1 | -54 | 56 | ps |
| | 2 | -76 | 117.5 | ps |

Delay change at 85% level

Delay change at 85% level

(10kOhm/2pF load)

# Summary

- Overview to problem of ground path provided
- Timing accuracy is sensitive to location of ground discontinuity
- Timing accuracy depends on architecture of signal delivery system
- Budgeting should be performed
- Compensation seems possible, if trends are known
- Other contributions to timing arise from line length matching, fabrication variances such as dielectric constant changes, coupled sections, transitions and other discontinuities on the signal itself and must be accounted for separately. These contributions have NOT been taken into account here, yet a significant skew has already accumulated …..

**Thank you!**