

IEEE SW Test Workshop

Semiconductor Wafer Test Workshop



Jay Kim, PE (jay.kim@westernst.com)
Western Specialty Technologies, LLC
Jae-Ha Lee (luis.jhlee@fineinstrument.com)
Fine Instrument Co., Ltd.

New Probe Card Architecture – Ceramic without MLC



June 6 to 9, 2010
San Diego, CA USA

20th 2-0-1-0
ANNIVERSARY

Outline

- **MLC-free Probe Card**
- **Building “FI” Probe Card**
- **“FI” Probe Card Example**
 - CMOS Image Sensor
 - 300mm Full Wafer
- **Signal Integrity**
- **Summary**



“Make things as simple as possible, but not simpler”

Albert Einstein



June 6 to 9, 2010

IEEE SW Test Workshop

3

MLC

- **MLC: Multi-layer Ceramic**
 - HTCC (High Temperature Co-fired Ceramic)
 - LTCC (Low Temperature Co-fired Ceramic)



Probe Cards with MLC

- **Advantages**

- Throughput

- Due to increased parallelism

- Yield

- Consistent contact with device pads*

- **Challenges:**

- Cost

- Custom design & fabrication of MLC

- Lead time

- Multi-layer (as many as 20+) “green tape”



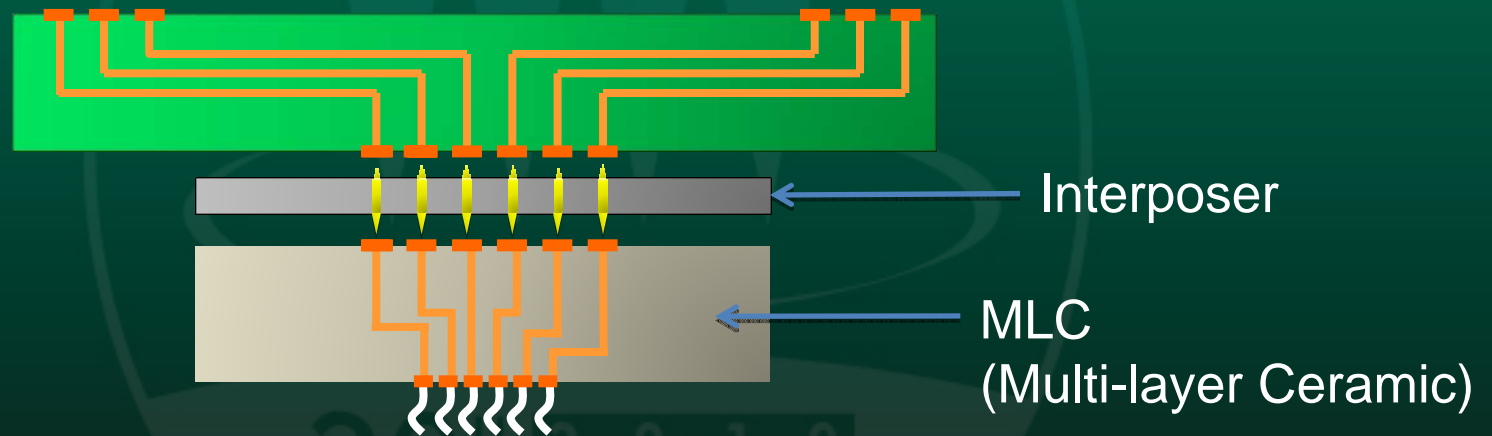
New Probe Card without MLC

- **Goal**

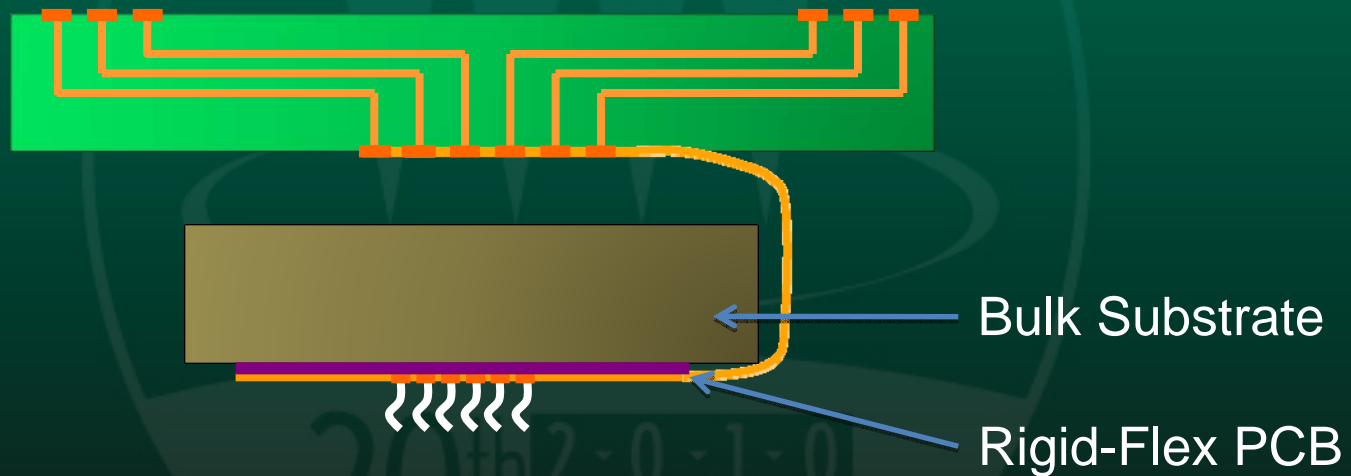
- Maintain parallelism & reliability advantages, while overcoming cost & lead time challenges of the MLC-based probe card.



Typical Probe Card with MLC



“Fine Instrument” Probe Card - without MLC



- ✓ Bulk Substrate
- ✓ Rigid-Flex PCB

- ✓ No Interposer
- ✓ No MLC



“FI” Probe Card

- **Rigid Flex PCB**
 - Improved signal integrity
 - Modular construction
- **Bulk Substrate**
 - Wide selection of available substrates
 - CTE Match
 - Mechanical fabrication only
 - Lead time



“FI” Probe Card

BUILDING “FI” PROBE CARD



June 6 to 9, 2010

IEEE SW Test Workshop

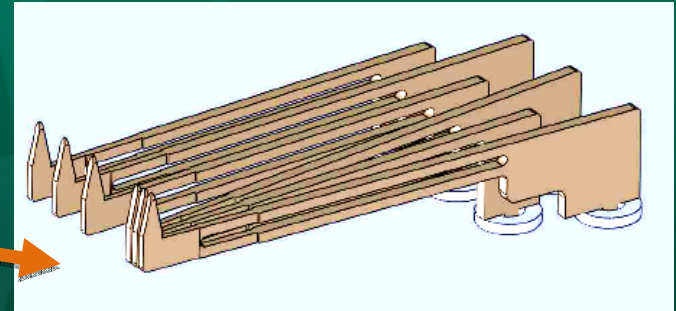
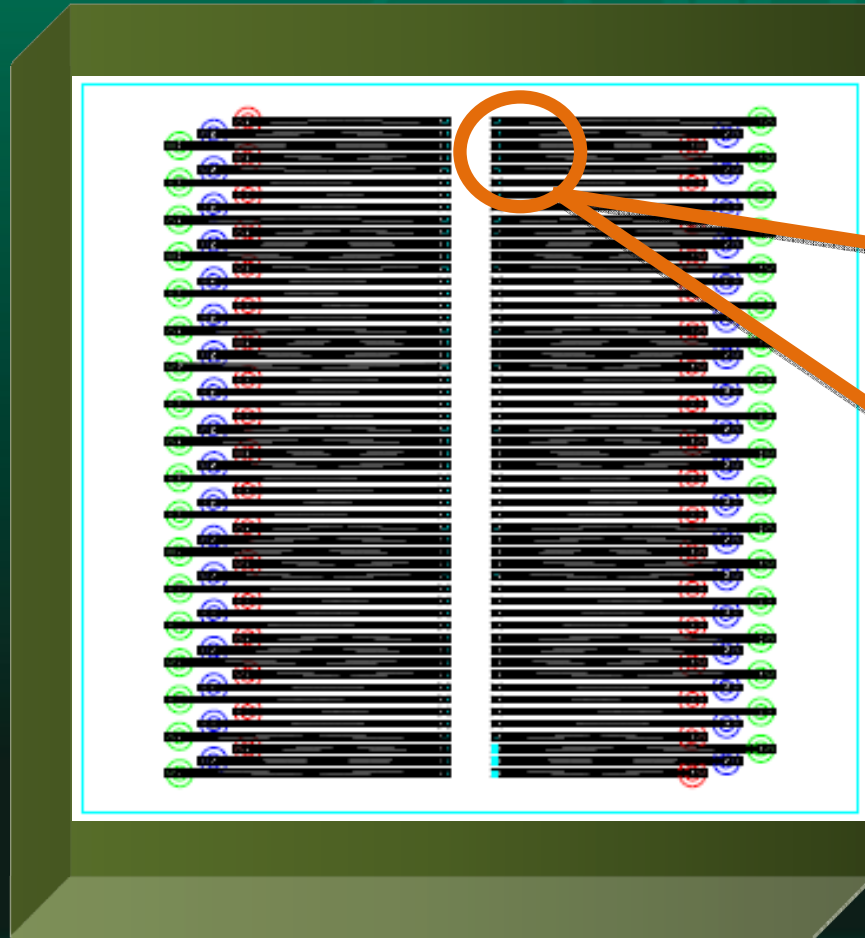
10

Building “FI” Probe Card

- **Select Contact Material**
 - MEMS
 - Micro Cantilever: 2 – 3mm
- **Select Bulk Substrate**
 - Match CTE with wafer
- **Design Rigid-Flex Circuit**
 - PCB design & fabrication



Contact Selection

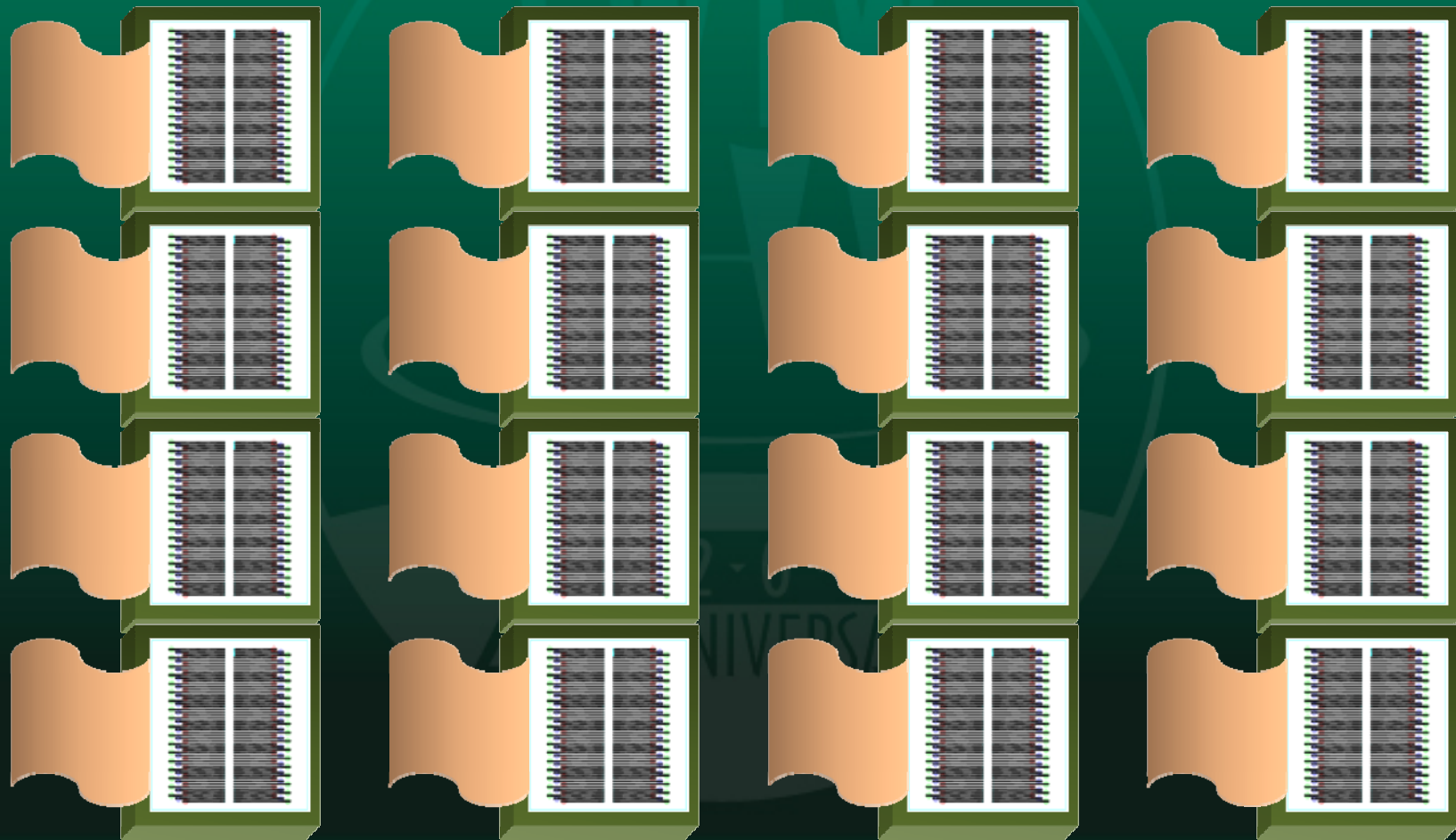


MEMS



Micro Cantilever

Modular Site



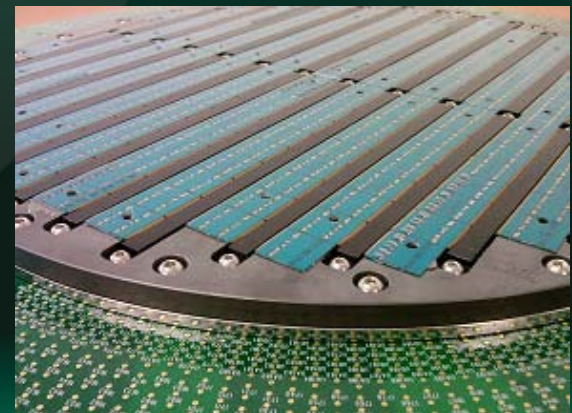
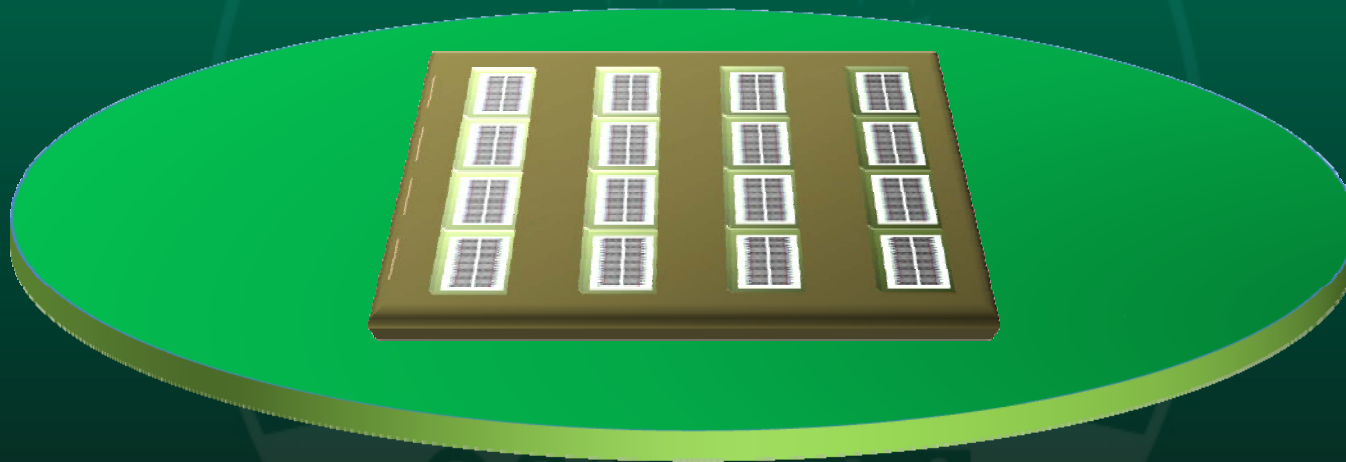
June 6 to 9, 2010

Bulk Substrate – No MLC



June 6 to 9, 2010

Finished Probe Card – No MLC



June 6 to 9, 2010

IEEE SW Test Workshop

15

“FI” Probe Card Example

- **CMOS Image Sensor Probe Card**

- Light port on each site (through-hole in the middle of each device location)
- Multi-die: 32 devices in parallel
 - Higher parallelism, if ATE support is available

- **300mm Full Wafer Probe Card**

- 1 touchdown (for flash); 4 touchdown (for DRAM)
- Single probe card for both hot (90 deg C) and cold (-40 deg C)



“FI” Probe Card Example

CMOS IMAGE SENSOR PROBE CARD

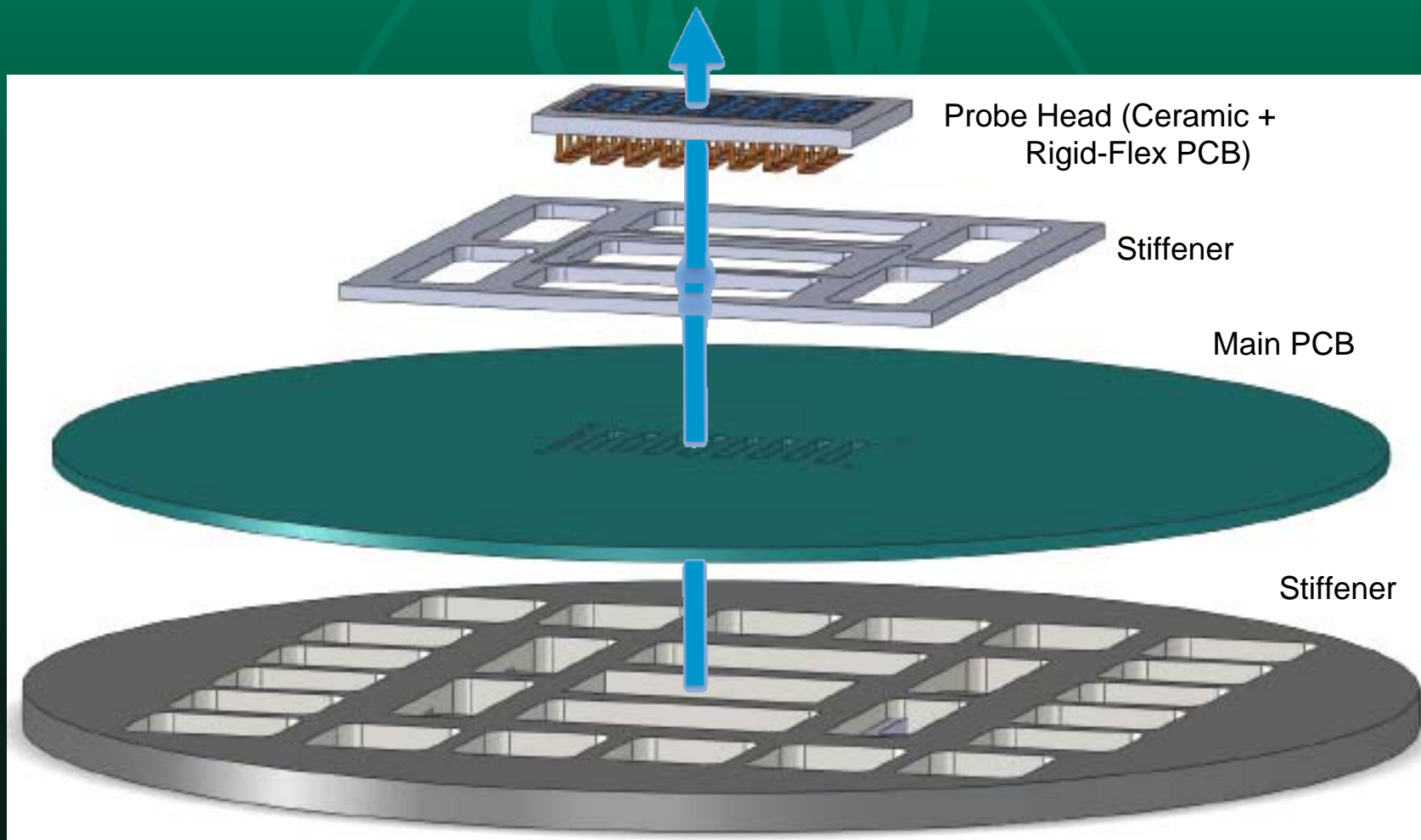


June 6 to 9, 2010

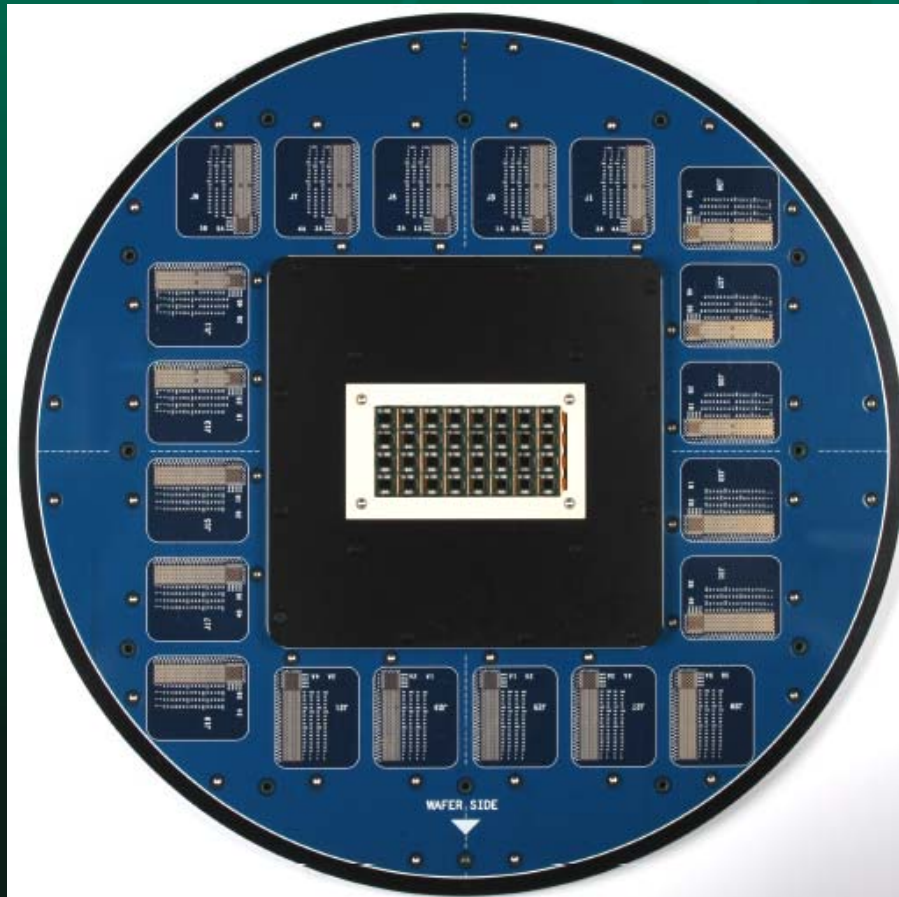
IEEE SW Test Workshop

17

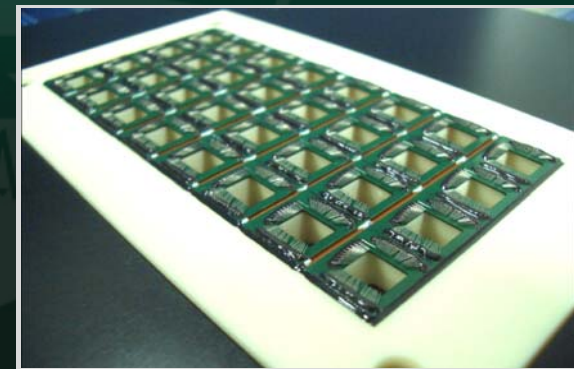
CMOS Image Sensor Probe Card



Probe Card for Image Sensor



- ✓ Multi-site: 32 (4 x 8)
- ✓ Light port on each site



“FI” Probe Card Example

300MM FULL WAFER PROBE CARD

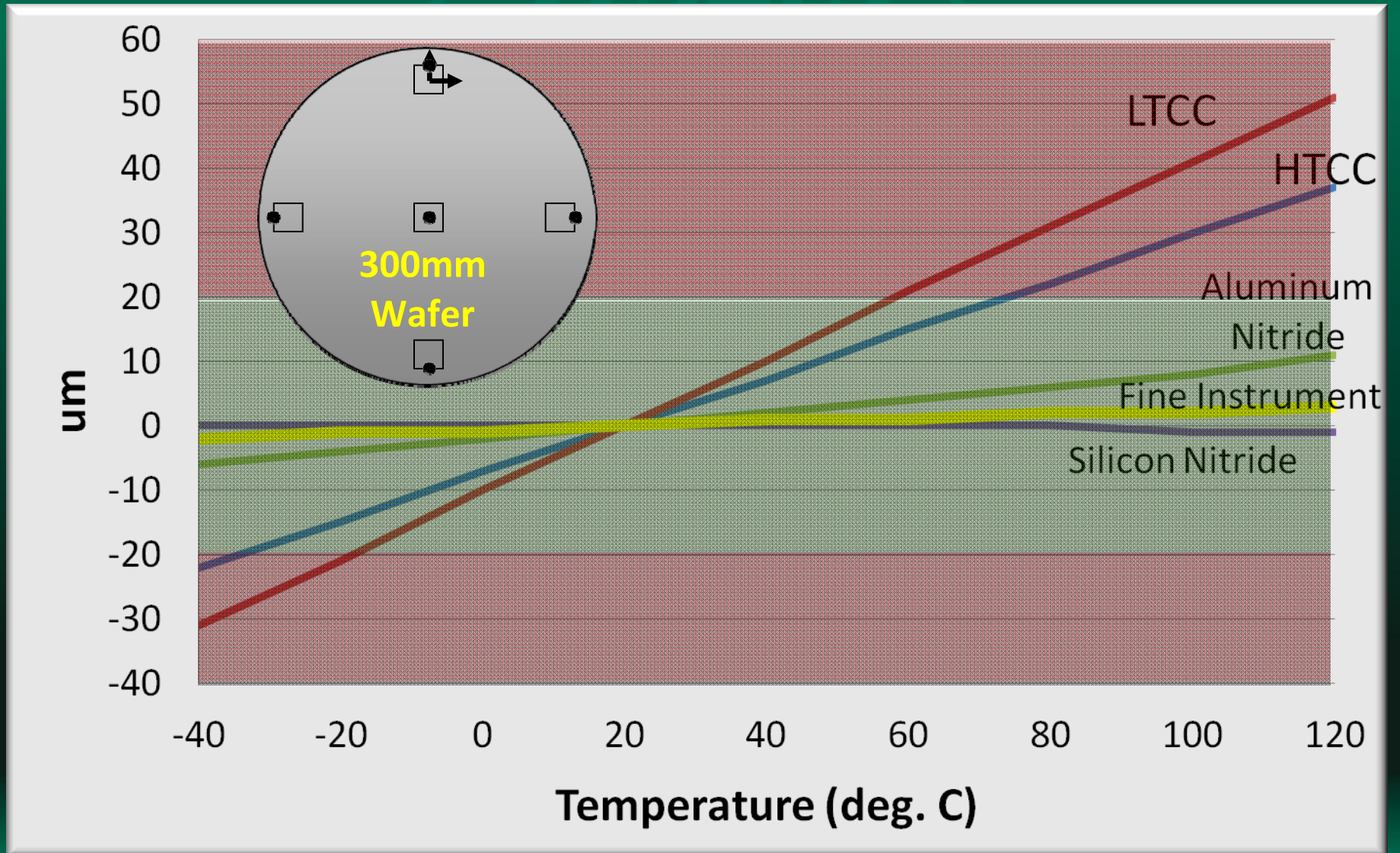


June 6 to 9, 2010

IEEE SW Test Workshop

20

Temperature vs. Probing Error

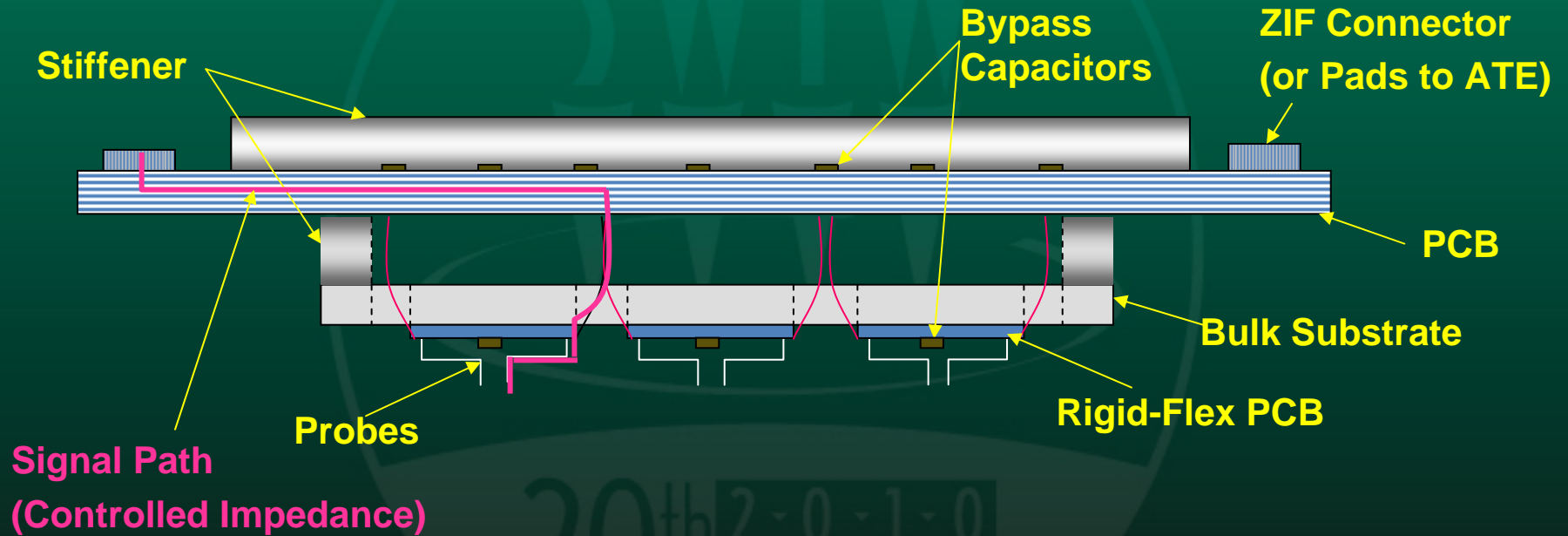


Substrates for 300mm Probing

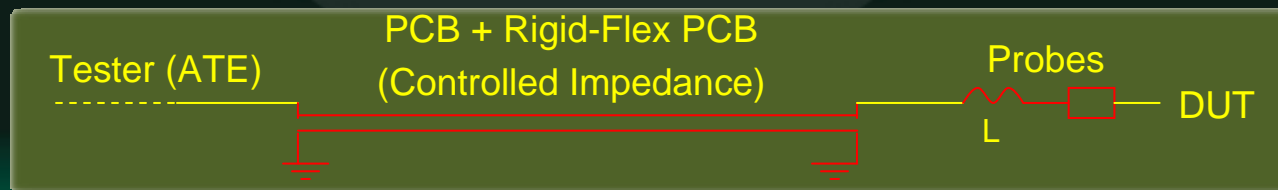
- **Suitable for full 300mm application (good CTE match with wafer)**
 - Aluminum Nitride (AlN)
 - Silicon Nitride (Si₃N₄)
- **Limited (Localized or small temperature range) substrate application (due to CTE mismatch on 300mm wafer)**
 - HTCC (High Temperature Co-fired Ceramic, Al₂O₃)
 - LTCC (Low Temperature Co-fired Ceramic, Al₂O₃)



"FI" 300mm Probe Card Structure



Signal path is fully impedance controlled

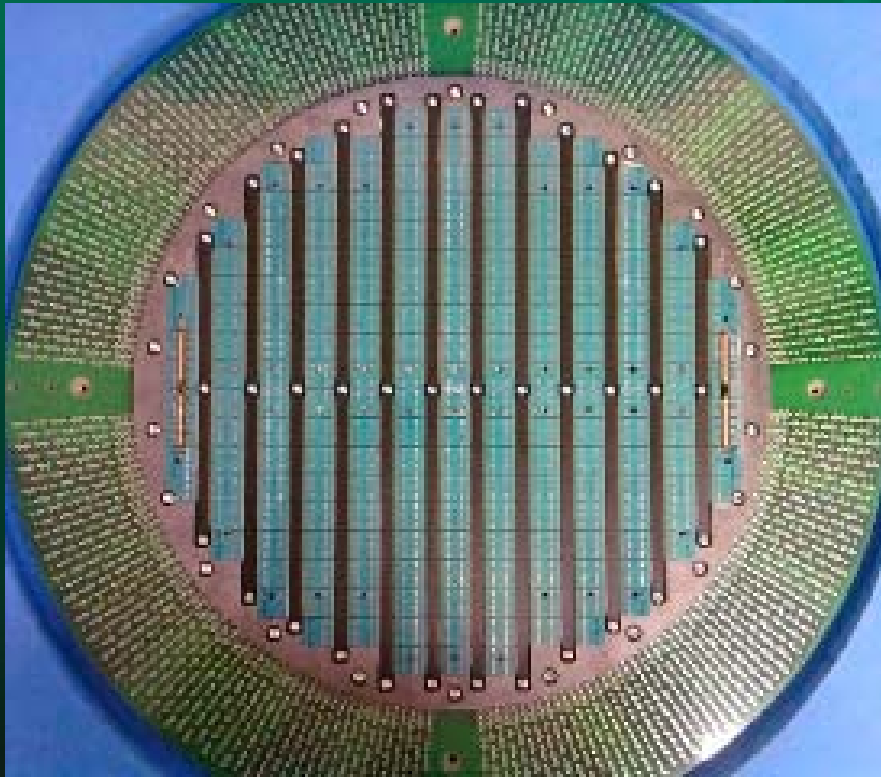


“FI” Probe Card

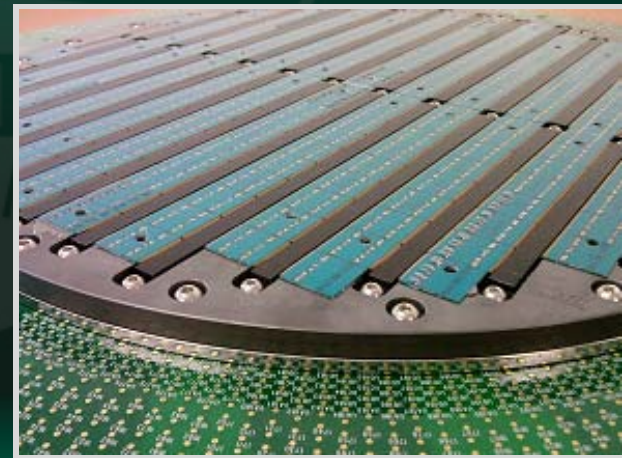
- **Impedance controlled signal path**
 - No interposer:
 - No extra inductance
 - No extra contact resistance
 - High speed / high signal integrity
- **Modular construction**
 - Readily scalable for high throughput (2x, 4x, etc.)
 - Selection of best CTE matched material
 - Single probe card for both hot (90 deg C) and cold (-40 deg C)



“FI” 300mm Probe Card – No MLC



- ✓ Full wafer, single touchdown
- ✓ 10,000+ contacts
- ✓ -40 deg C to +90 deg C



“FI” Probe Card Example

“FI” PROBE CARD SIGNAL INTEGRITY



June 6 to 9, 2010

IEEE SW Test Workshop

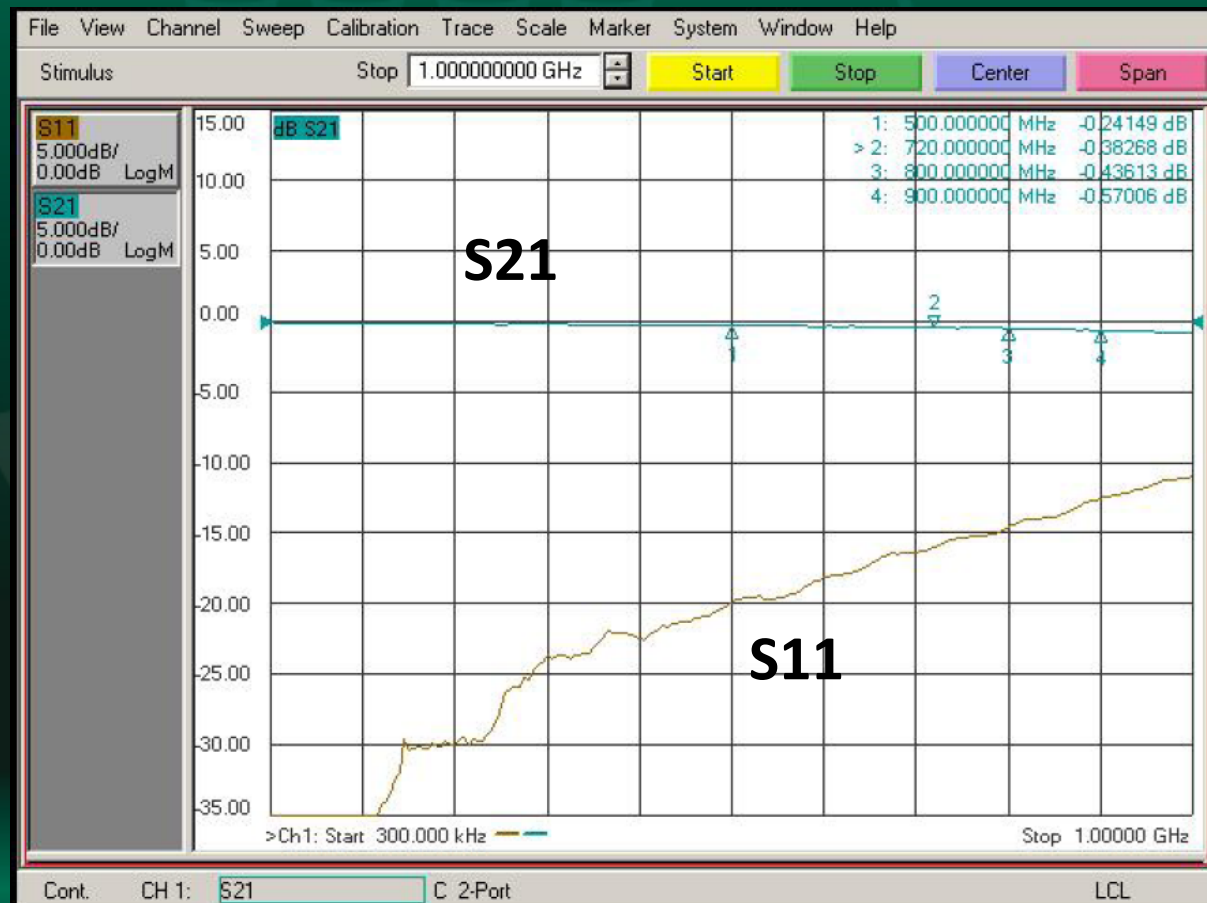
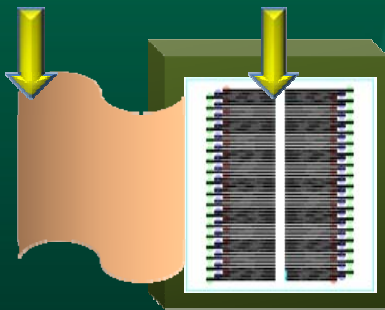
26

Signal Integrity for Probe Block

Probe Block:

S21 (transmission / insertion loss) >> 900MHz @-1dB

S11 (reflection / return loss) > 500MHz @-20dB



June 6 to 9, 2010

IEEE SW Test Workshop

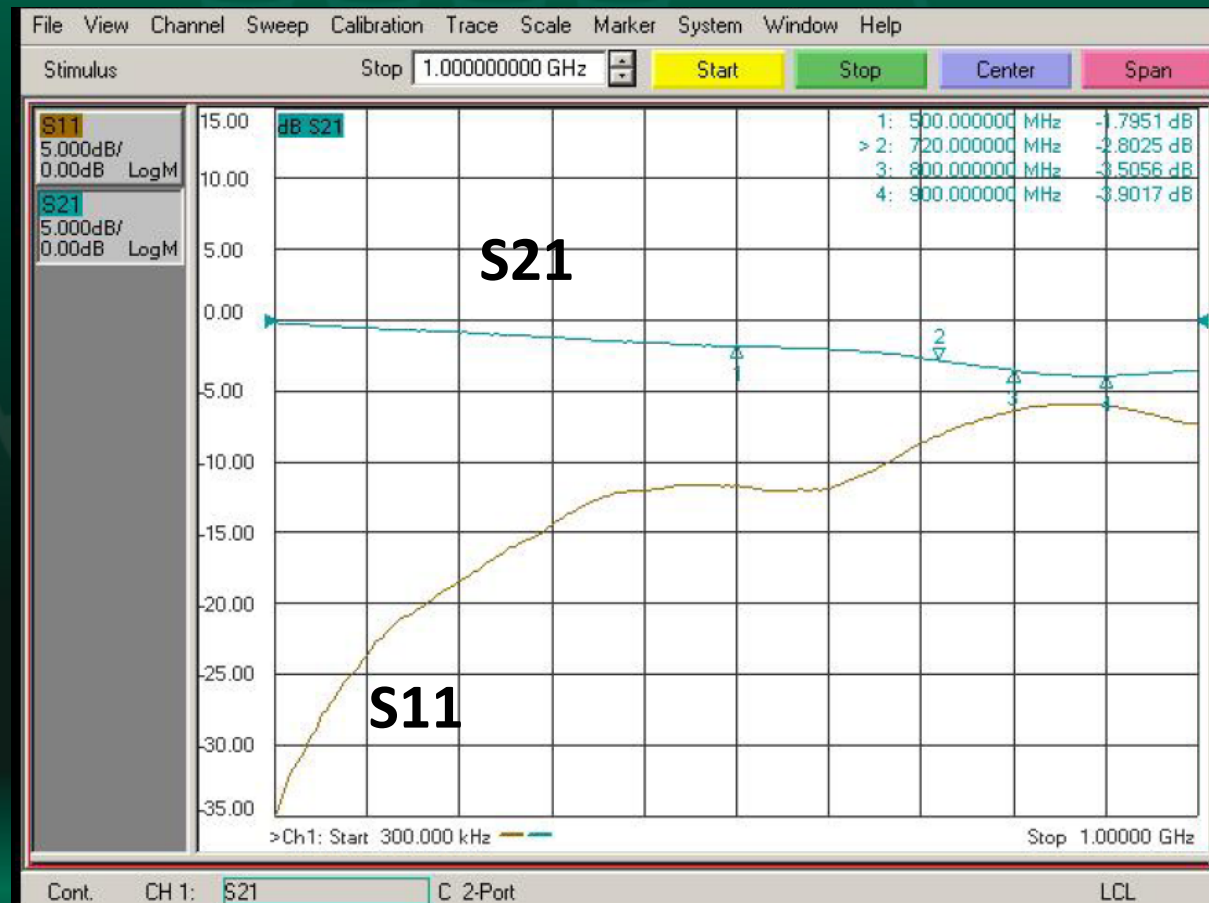
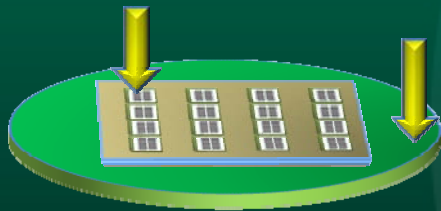
27

Signal Integrity for Probe Card

Probe Card:

S21 (transmission / insertion loss) > 720MHz @-2.8dB

S11 (reflection / return loss) > 400MHz @-15dB



June 6 to 9, 2010

IEEE SW Test Workshop

28

“FI” Probe Card Capability

	Description
Alignment (X,Y)	+/- 10 um
Planarity (Z)	+/- 15 um
Working Temperature	-40 °C ~ 120°C
Pin Force	~ 1.2 gf/mil (selectable)
Tip Diameter	< 10 um
Minimum Pad Pitch	50 um
Impedance	50 Ω (customizable)



“FI” Probe Card

- **MLC-free, New Probe Card Architecture**
 - Bulk Ceramic Substrate
 - Choice of CTE matched material for full wafer contact
 - Shorter lead time
 - Rigid-Flex PCB
 - Signal integrity
 - Expandability (higher parallelism)
 - Shorter lead time
 - Probing contact
 - Choice of contact material
 - Repairable at individual pin & DUT



Summary

- **New probe card architecture, using bulk ceramic -**
 - Overcomes challenges of traditional MLC probe cards.
 - Lead time
 - Cost
 - Improves on advantages of MLC probe cards
 - Parallelism
 - Reliable contact



Appendix

PATENTS



June 6 to 9, 2010

IEEE SW Test Workshop

32

Patents related to “FI” Probe Card

- **Patents have been filed or issued (Korea, Taiwan, International PCT):**
 - Manufacturing method of probe array
 - Probe assembly
 - Probe assembly and manufacturing method of probe card
 - Probe card and manufacturing method
 - Pin array frame used for manufacturing of probe card
 - Probe pin for probe card and manufacturing method

