

IEEE SW Test Workshop

Semiconductor Wafer Test Workshop



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Adaptive test on wafer level

focus on: test-time reduction (TTR)

20th 2-0-1-0
ANNIVERSARY



June 6 to 9, 2010
San Diego, CA USA

Introduction

- **What is Adaptive test?**
 - Modify test content/flow based on results
- **Examples of adaptive test**
 - Dynamic change test limits (DPAT)
 - Reduce amount of tests
 - Make test plan based on PCM data
 - Smart Sample Probe
- **ITRS (Salland Engineering, contributes)**
 - International Technology Roadmap for Semiconductors



Why do we test in the 1st place?

- **What if the wafer-fab would produce 100% perfect product?**
 - No need for testing at wafer level.
 - Most of us would not have a job!
- **Lucky for us; there is enough process variation during wafer fabrication!**
 - This makes wafer test mandatory.



Cost of test

- **Cost of test still grows**
 - More complexity in the devices
 - More pins, higher density
 - More expensive ATE
- **Challenge to reduce cost without concessions to the quality**
 - Invest in Dynamic Test-cell Controller
 - Gain all advantages (not just TTR)

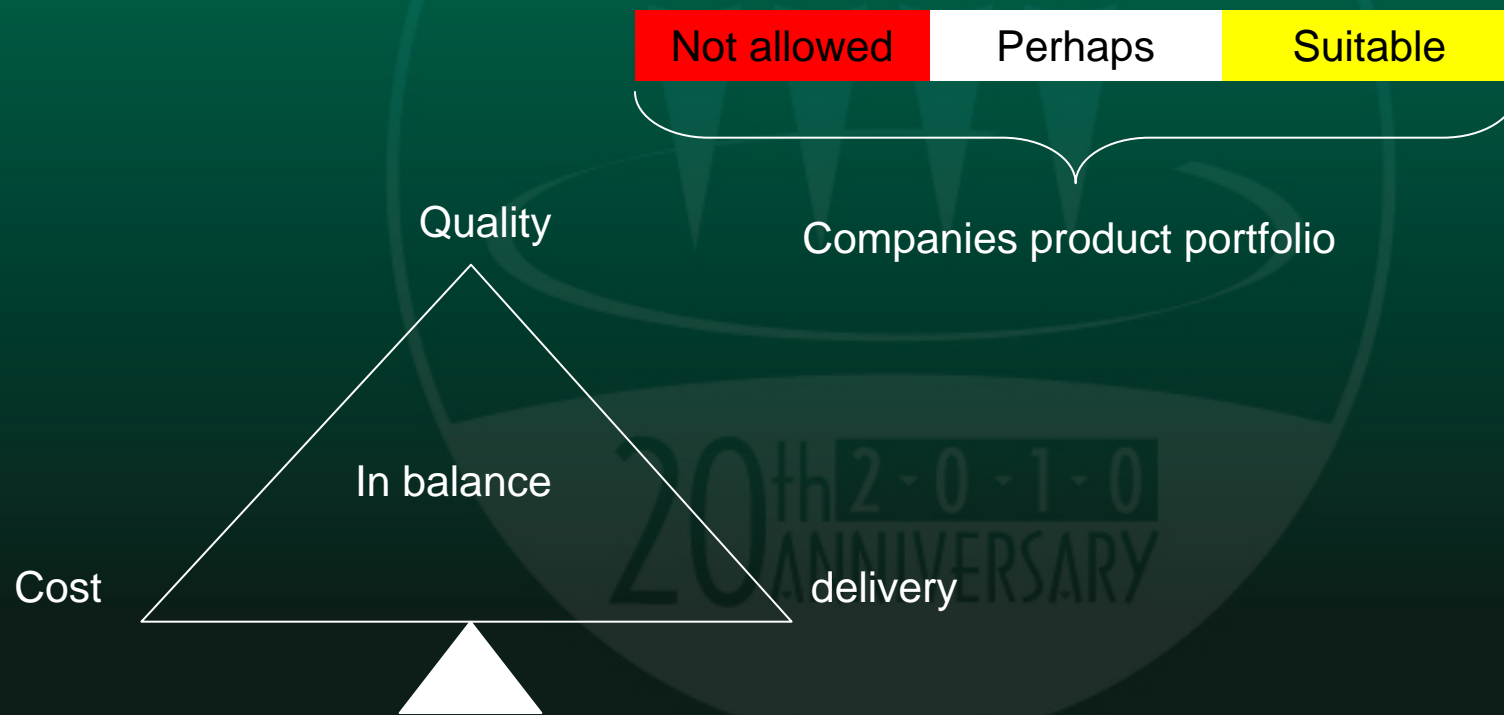


Suitable device types

- **Not all devices are suitable for adaptive test**
 - Test coverage needed at all times (Automotive)
 - New product or new technology
 - (not enough data available yet)
 - Effort is higher than profit
 - Low volume production



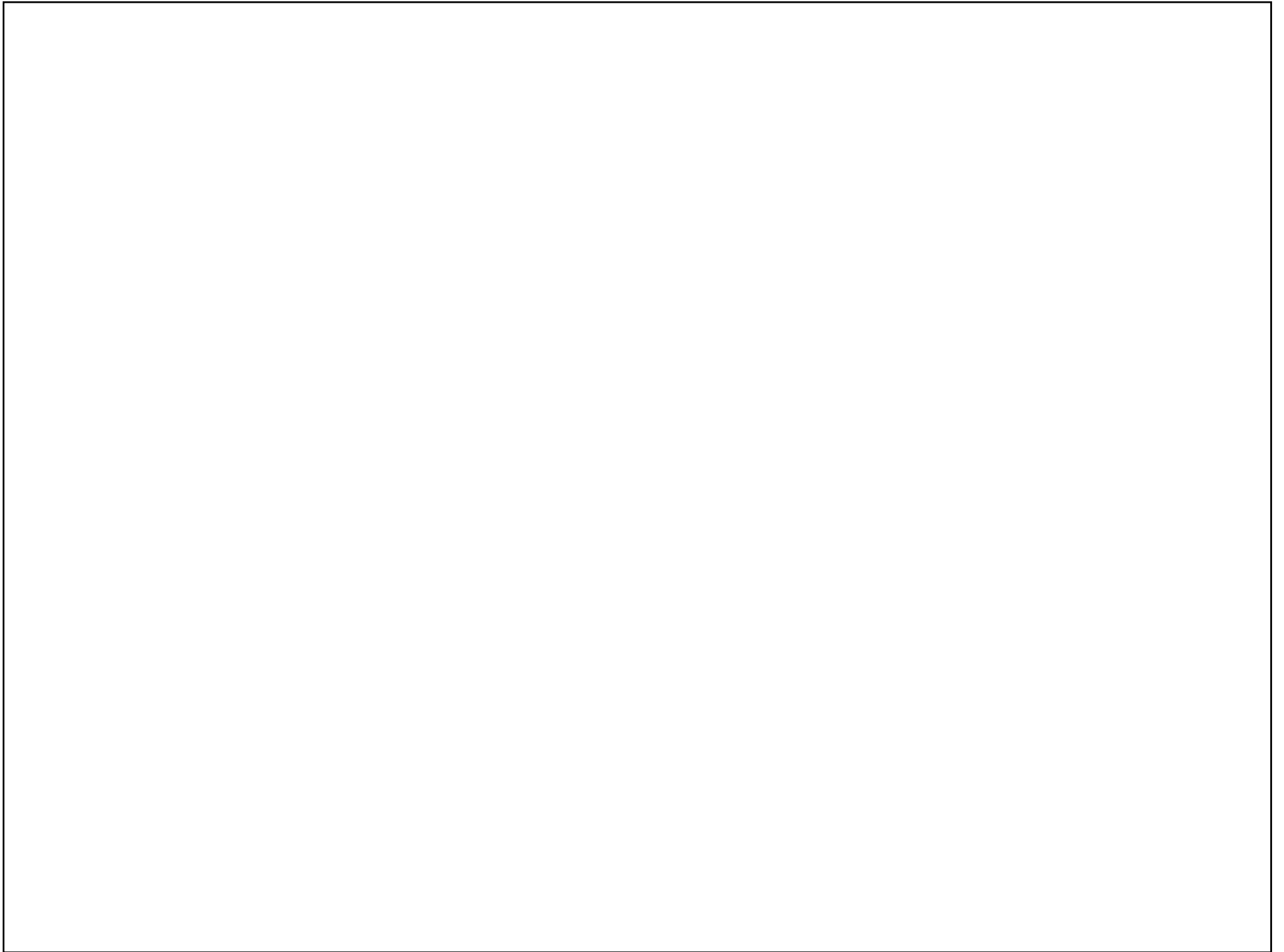
All about balance



Test

- **When do you recognize the picture?**
- **In total 80 boxes**
 - 1st ; 5 boxes; 94% reduction
 - 2nd ; 9 boxes; 89 % reduction
 - 3rd ; 13 boxes; 84% reduction





Objectives / Goals

- **Reduce test-time**
 - Have at least 20% TTR
- **No concessions towards quality**
 - Less than 20 PPM difference in yield
- **Recipe controlled;**
 - All adaptive TTR instructions are stored in a TTR-Recipe
- **Useable over wide range of products**
 - Mixed signal & analog
- **Traceability of how each die is tested**
 - Special identifiers (adaptive test-flow pass bins)
 - Know values used for switching



Methods

- **Detect redundant tests/data**
 - In order to create reduced test-flow's
- **Have multiple decision criteria (recipe-content)**
 - Validation towards the lot
 - Tests to monitor (used for switch decisions)
 - Area's over the wafer
 - Watch-dog test
- **Real-time analysis and decisions**
 - Activate the “switch”
 - Real Time data analysis (test-data validation)



Preparation

- **Redundancy analysis required (on historical data)**
 - Results will vary over the wafer surface
 - (geographical connected)
- **Reduce number of tests**
 - Which are suitable?
- **Test-flow creation**
 - Multiple test flows
- **Correlation analysis**
 - Remaining tests should correlate with full flow



Redundancy

- **When is a test redundant?**
 - When it does not contribute by it self, to the end result.
- **Why are there redundant tests in the first place?**
 - Creating a test-program is to cover all specified parameters.
 - for new product it is not clear yet, how tests are “connected” (and could end-up as being “redundant”)
- **How to detect redundant tests?**
 - Use a redundancy analysis software tool
 - Output is: a list with “skip-candidates”



Test-flow creation

- **Create reduced test-program (s) “TTR Test Flows”**
 - Use skip candidates list
- **Not all tests can just be skipped**
 - Waiting loops (for the DUT to stabilize)
 - Set-up information (to bring the DUT in a certain condition)
 - Essential test coverage (“must be” test, used also for switch indicator)
 - Watchdog test
- **Correlate each test in the “TTR Flow” to the Full-Flow**
 - To make sure no quality impact
 - Should bring same reading regardless the “Flow” (TTR or Full)

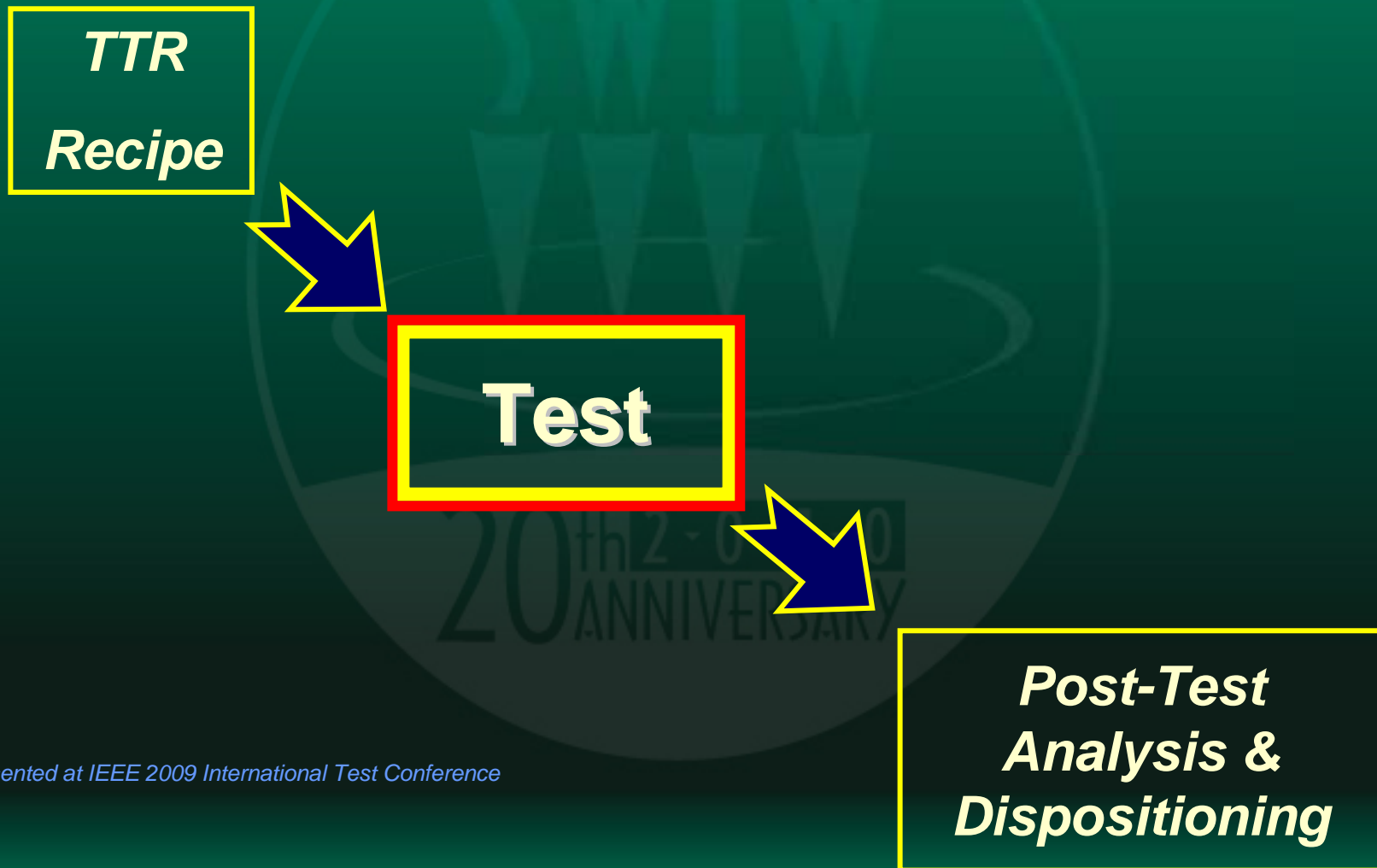


Watchdog test

- **Monitor the stability of the product & process**
- **Should be a representable test**
 - To validate the measured values (good contact)
 - Real time SPC
- **Secure the quality of process**
 - Watch for “Trend”
 - Guard band value’s set by historical data
- **Can never be switched off!**
- **When out of control;**
 - Return to full test flow



Adaptive Test Flow



Presented at IEEE 2009 International Test Conference



June 6 to 9, 2010

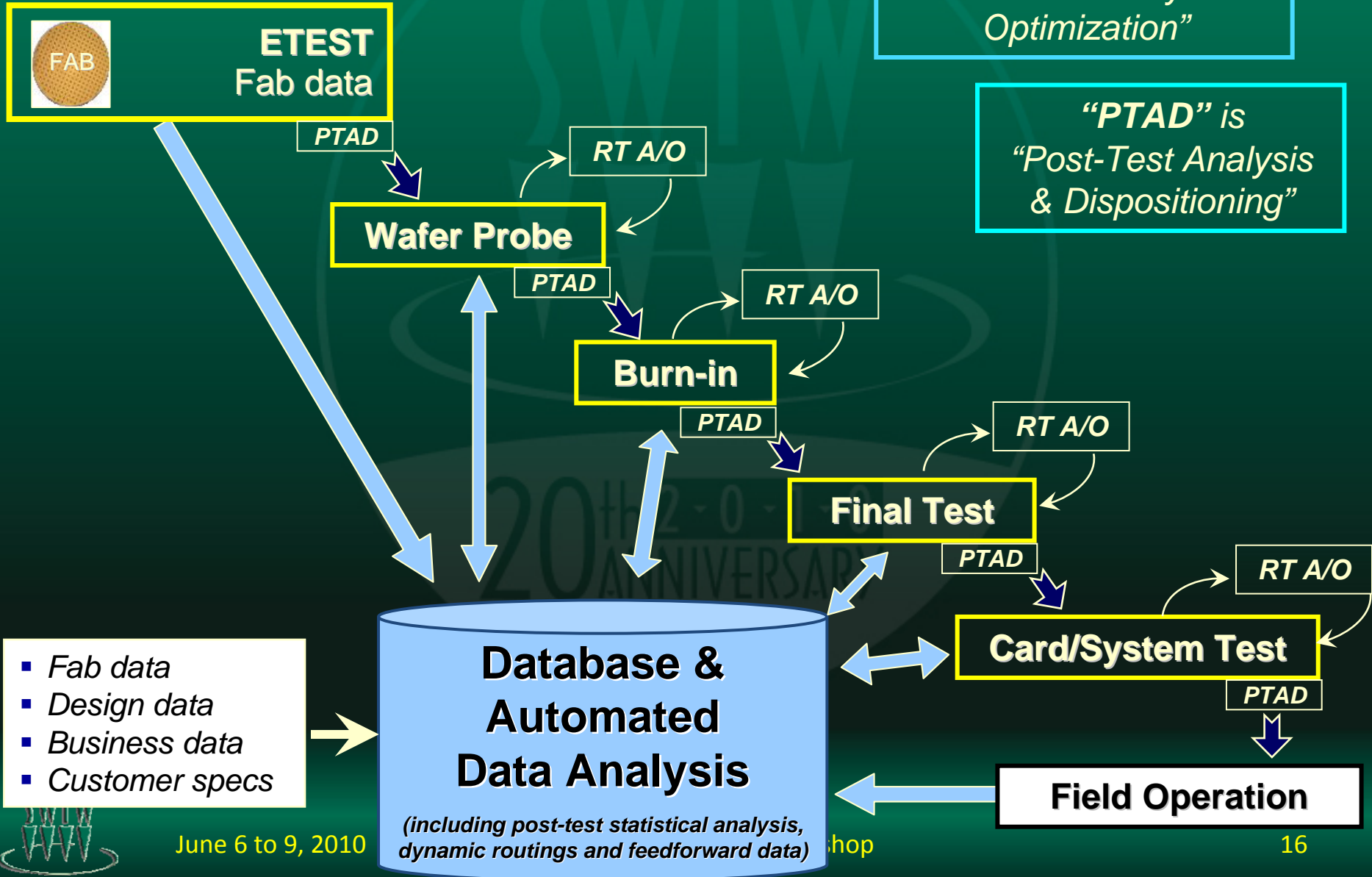
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Adaptive Test Data Flow

“RT A/O” stands for
“Real-Time Analysis & Optimization”

“PTAD” is
“Post-Test Analysis & Dispositioning”



- Fab data
- Design data
- Business data
- Customer specs

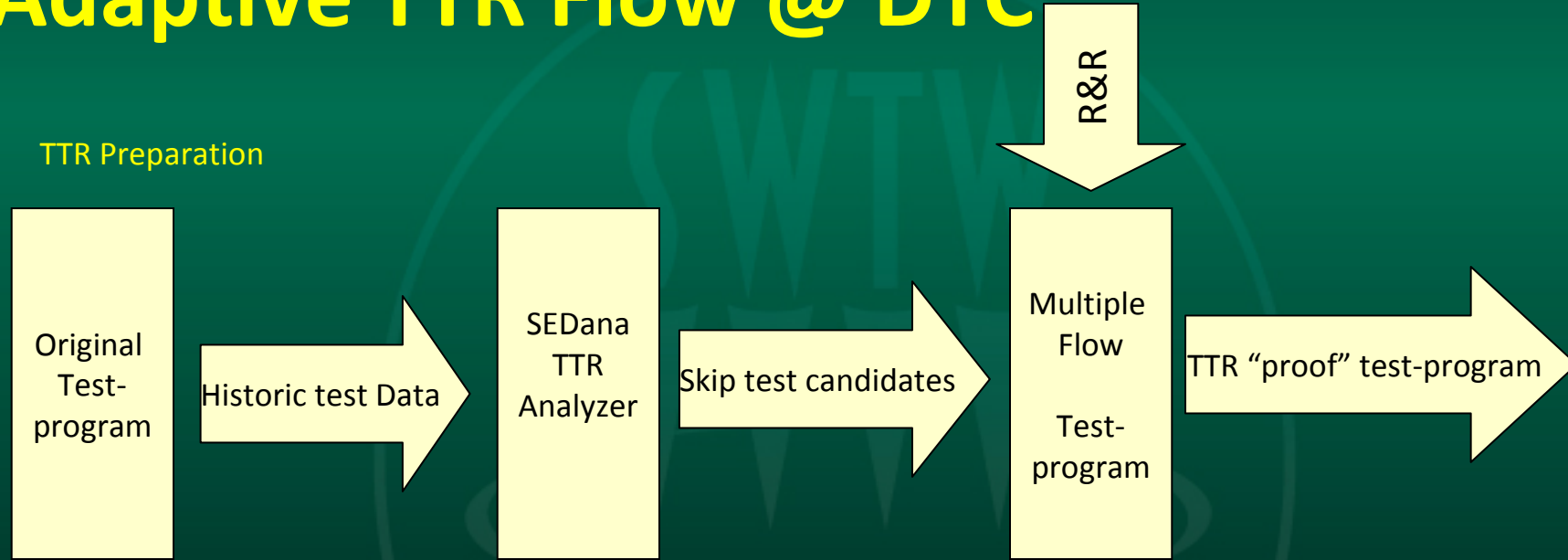
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(including post-test statistical analysis,
dynamic routings and feedforward data)

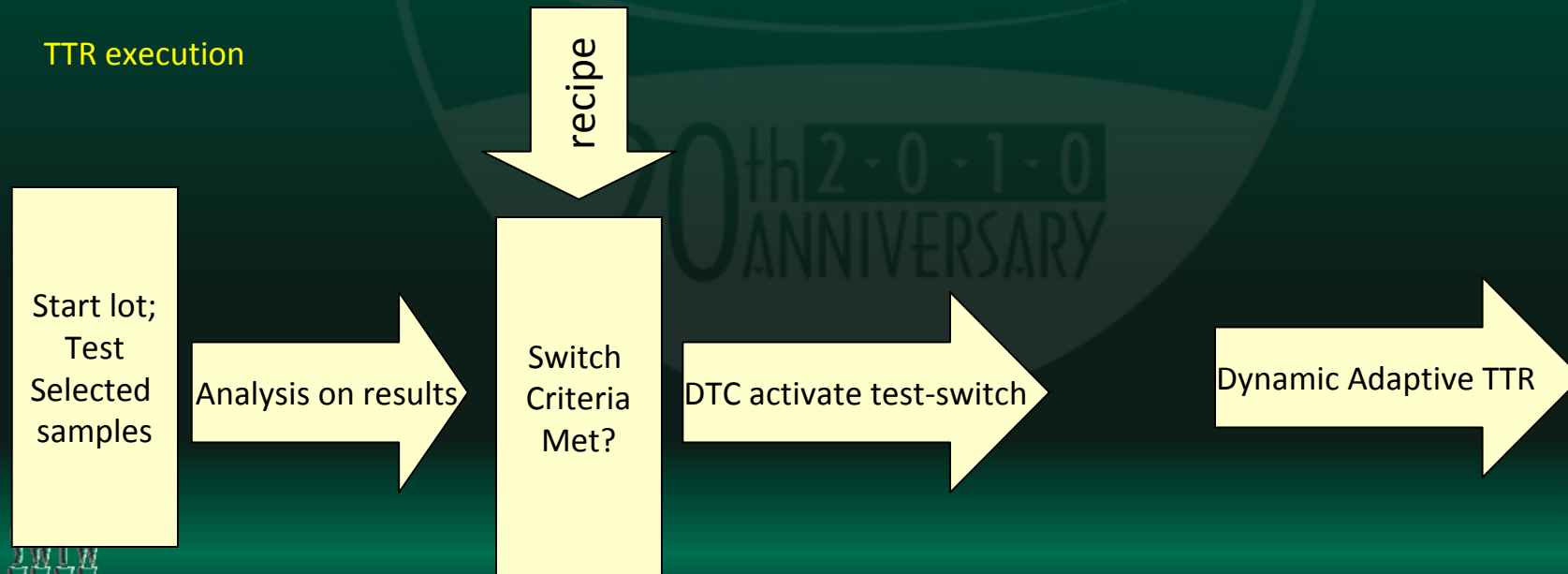
hop

Adaptive TTR Flow @ DTC

TTR Preparation



TTR execution

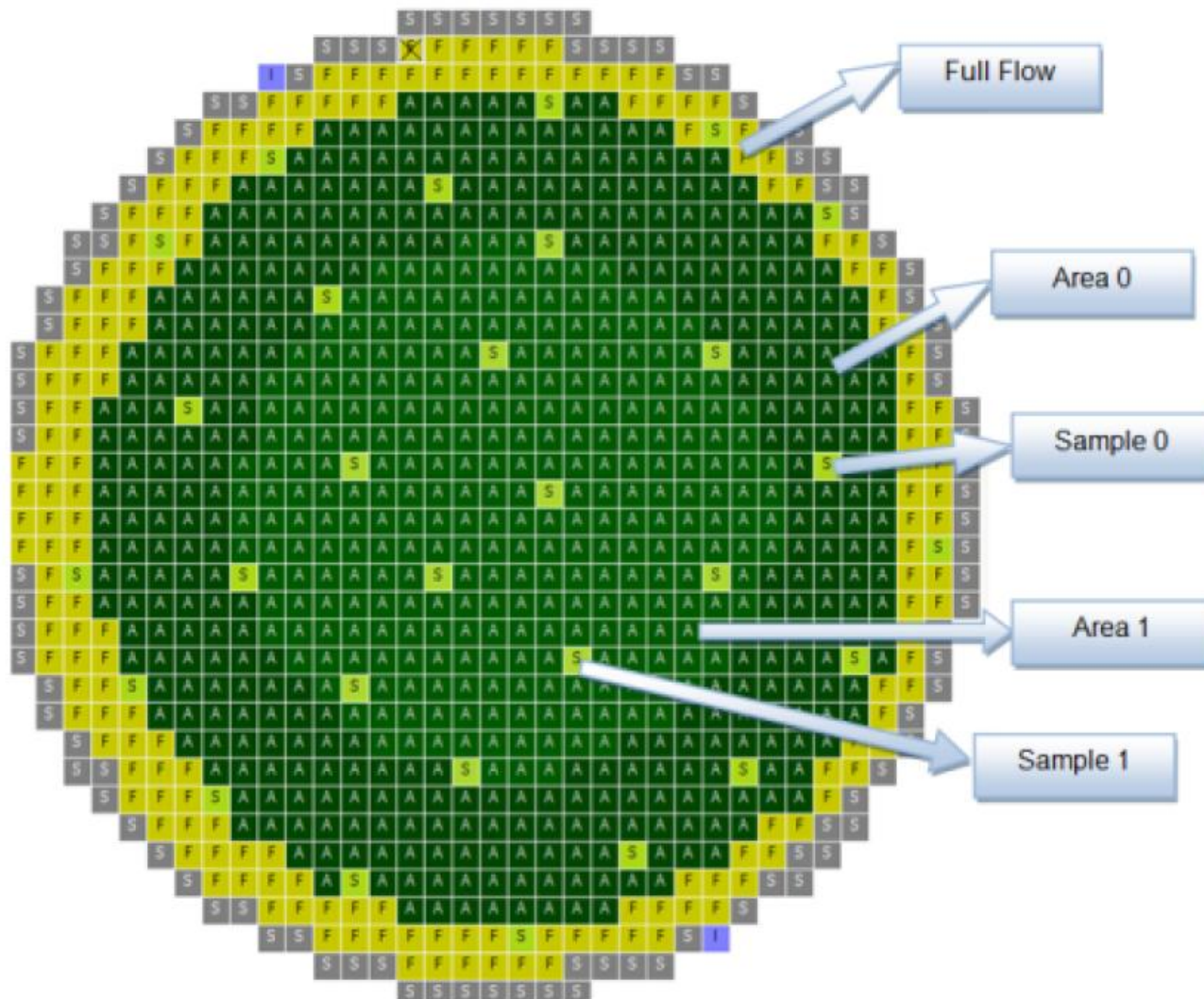


Switch criteria, recipe based

- **Validation towards the lot**
 - Test 1 (or more) wafers to detect if the lot is “good”
 - Run full-flow and monitor:
 - Overall wafer yield
 - Not containing more than X bin-Y
- **Tests to monitor on:**
 - Cpk, Cp, mean/median, sigma on parametric level
 - Yield on bin level
- **Area's on the wafer with corresponding sample die**
- **Watch-dog test**

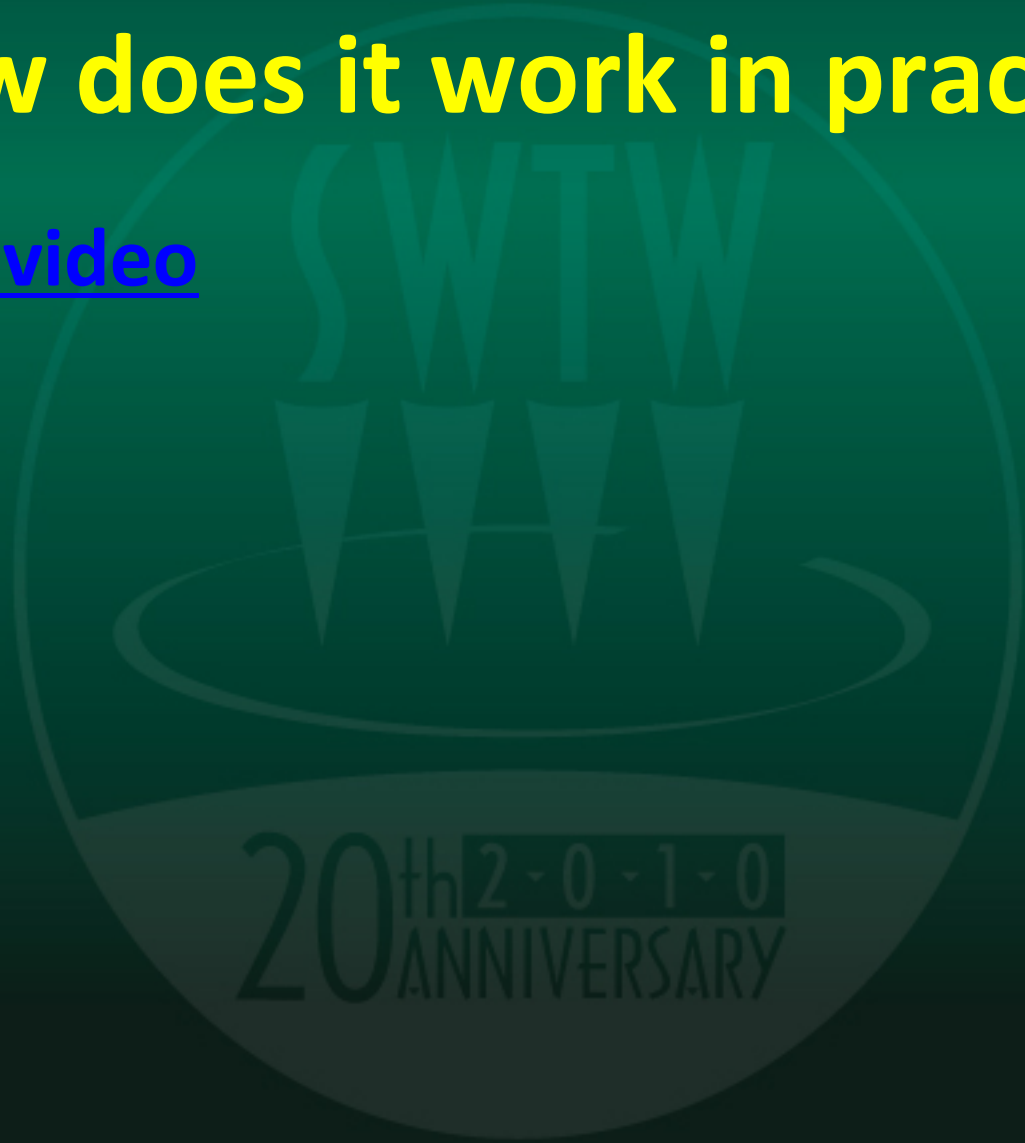


TTR-Control map

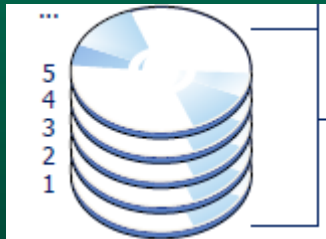


How does it work in practice

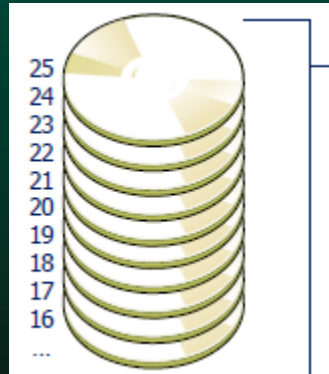
- [Screen video](#)



Results



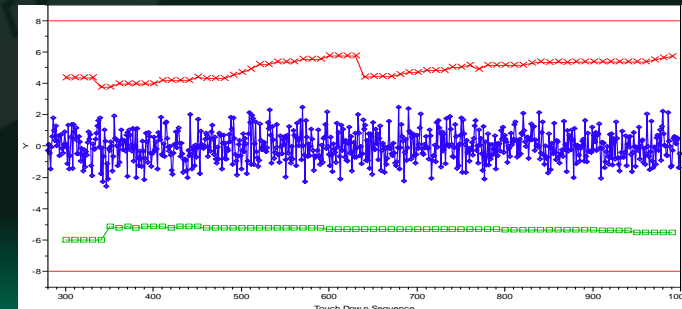
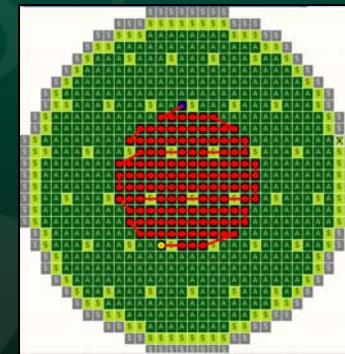
Validation wafers (lot level)

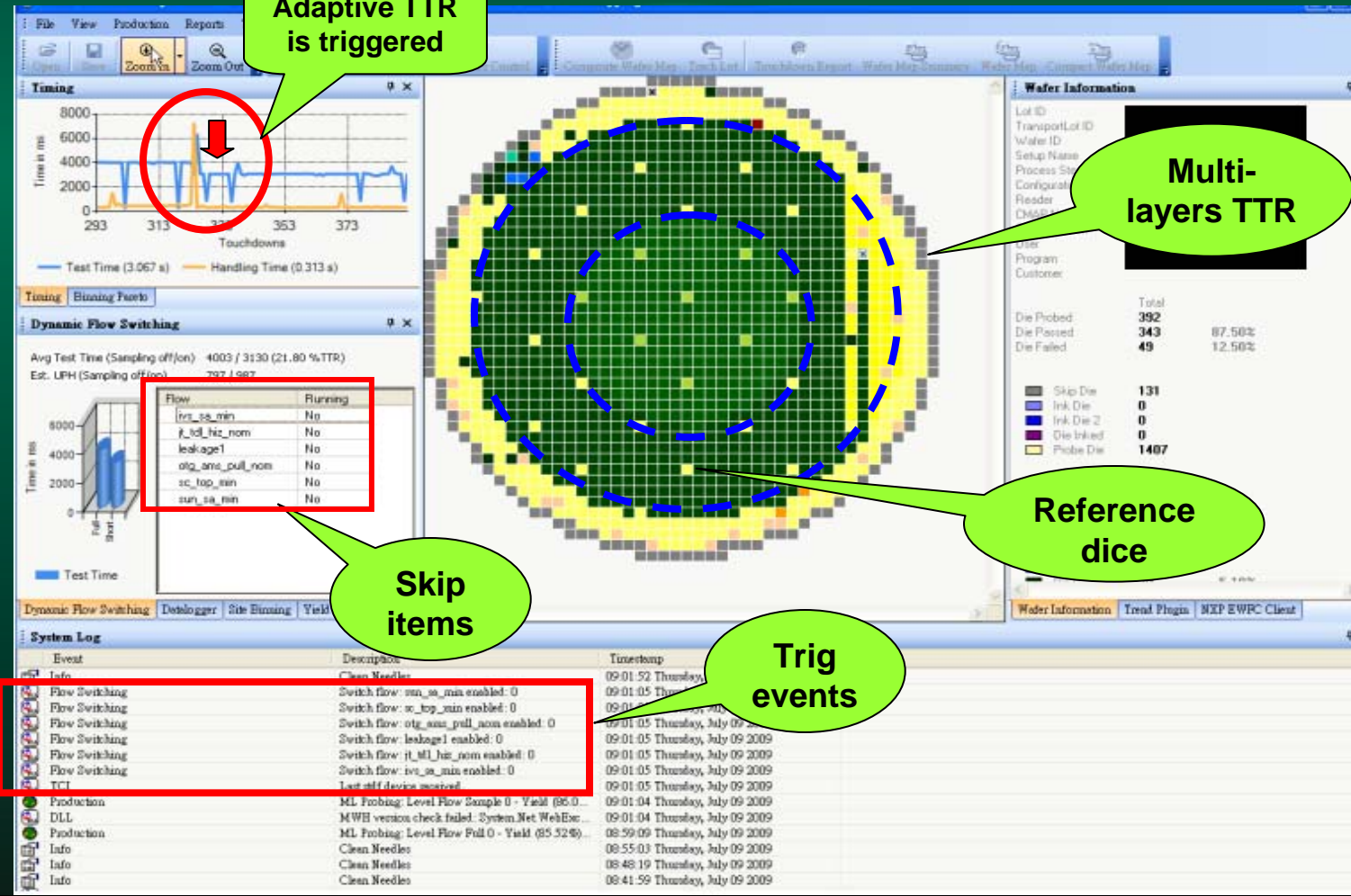


TTR candidate (wafer level)
Multi-layers TTR



Watchdog (die level)
By trend module





Type Name	Test time saving	Remark
Type A	15 %	yield increase ~0.5% at WT with full detected by FT
Type B	16 %	yield increase ~0.6% at WT with full detected by FT
Type C	26 %	yield increase ~0.7% at WT with full detected by FT



Summary / Conclusion

- **Customers targets are not fully reached**
 - Average yield increase 0.6% (compared to 100% testing of same wafer)
 - final-test catches the “Slip-through” parts
 - Average test time reduction 19%
- **Adaptive TTR is definitely a solution to reduce cost of test.**
- **Maturity of the product**
 - More data to be used for analysis
 - Different TTR test-flows over time.
 - The better you understand the “connection” between tests, more reduction can be offered
 - Automatic test program optimization
- **Next to adaptive test time reduction, also additional tests can be activated for higher test coverage.**



Prediction

- **Within the next 2 years; adaptive TTR will be used for at least 30% of all semiconductor test.**



Follow-On Work

- **Improvements**
 - Analysis algorithms
 - Automatic recipe generation tool
 - Extend functionality to PCM-data processing
 - Extend supported platforms
 - Reporting functionality
- **Benefit overview IDM/Fab-less/OSAT**



Special thanks

- ITRS adaptive test committee
- Thijs Haarhuis SE (screen movie)

