IEEE SW Test Workshop
Semiconductor Wafer Test Workshop

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Wafer Level ESD Probe Card Solutions

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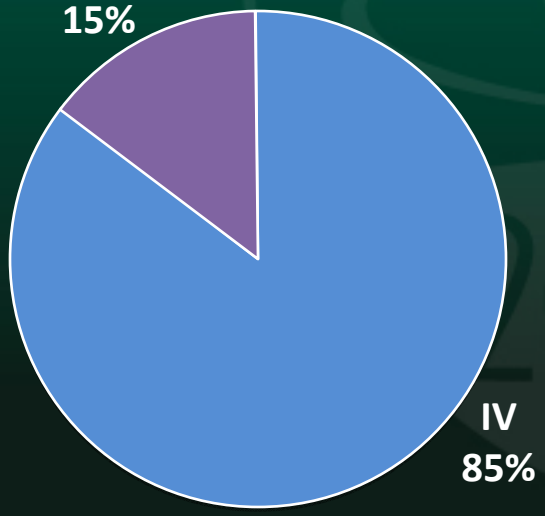
Agenda

- Review of advances in ESD waveforms required for wafer-level scribeline test
- Challenges related to full TEG pattern automation of ESD test structures
- Solutions for combining full DC and ESD parametric testing in a single touchdown
- Conclusions

Evolving Parametric Test Probing

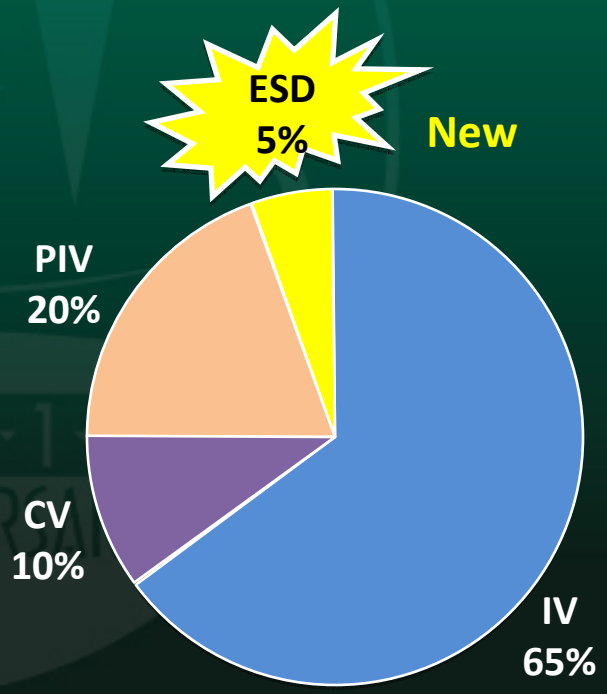
1990's Traditional DC Para

10 MHz Matrix Required



2010's Expanding to HF Para

1 GHz Matrix Required



ESD Scribeline Tests

- **Similar to HF-PIV for power transistor characterization**

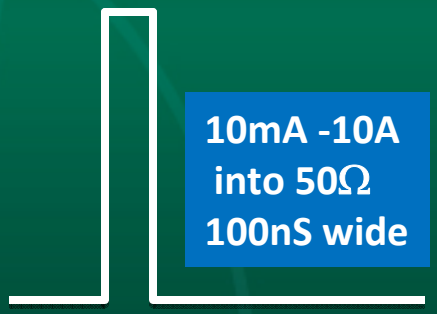
Type	Device	Freq	Matrix	Test Name
IV	Transistor	1 MHz	10 MHz	Vt, Gm, Vsat, BV, IDVD, IDVG, Gate & Drain Leakage, V-ramp, J-ramp, TDDB, HCI, Charge Pump, EM
CV	Transistor Oxide	1 MHz	10 MHz	Thick Gate Tox, Field Tox, Diffusion Profiles, Trapped Charge, Mobile Ion, C-gate, C-drain
HF-CV	Transistor Oxide	100 MHz	1 GHz	Thin Gate Tox, Carrier Life Time, Contamination
HF-PIV	Power Transistor	200 MHz	1 GHz	Vt, Gm, Vsat, IDVD, IDVG, Gate Charge, Trapped Charge, CMOS Latch-up (I/O Structure)
ESD	ESD structure	200 MHz	1 GHz	TLP, HBM, MM, HMM (IEC 61000-4-2), WCDM, TDB(time dependent breakdown) , Leakage curves
Flash R-ram	Transistor Resistor	200 MHz	1 GHz	State 0-State 1 Programming Current/Time, Read Leakage Current

ESD Waveforms

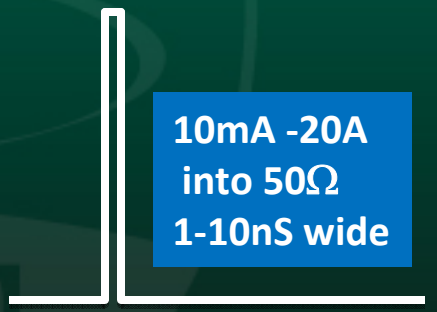
- TLP – Transmission Line Pulse
- HBM – Human Body Model
- CDM – Charge Device Model
- WCDM – Wafer Charged Device Model
- MM – Machine Model
- HMM – Human Metal Model (IEC 61000-4-2)

TLP & VFTLP Waveforms

- **TLP - Transmission Line Pulse**
  - Used for characterization of a ESD structure to a constant voltage pulse
  - Not used for simulating ESD events
  - Pulse delivery can be by a probe card

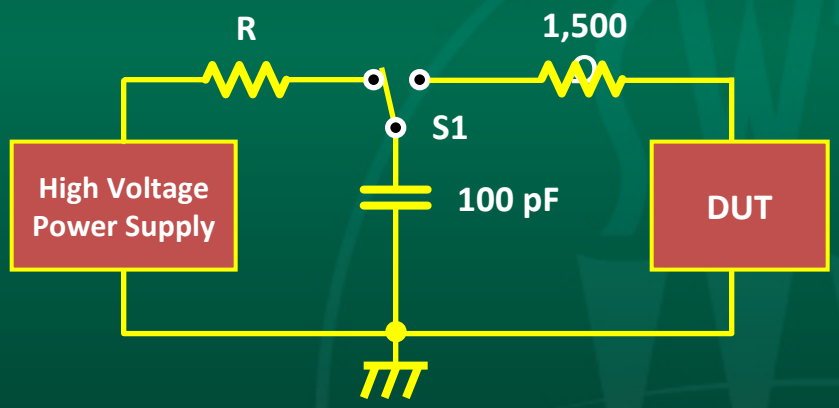


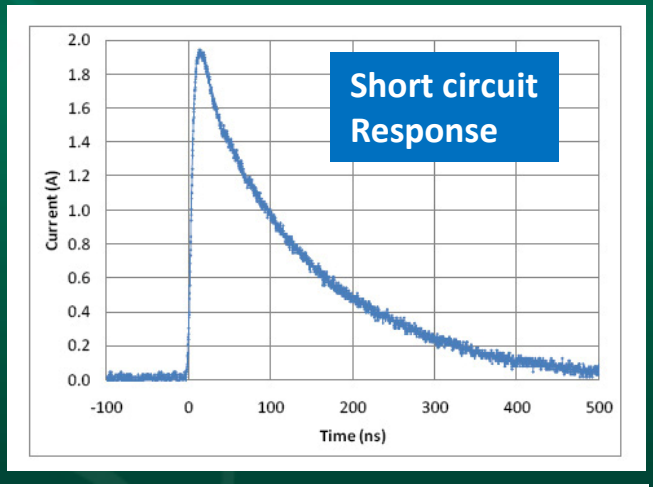
- **VFTLP – Very Fast Transmission Line Pulse**
  - Can characterize ESD structures designed for fastest (CDM) protection
  - Pulse delivery by manual RF probes



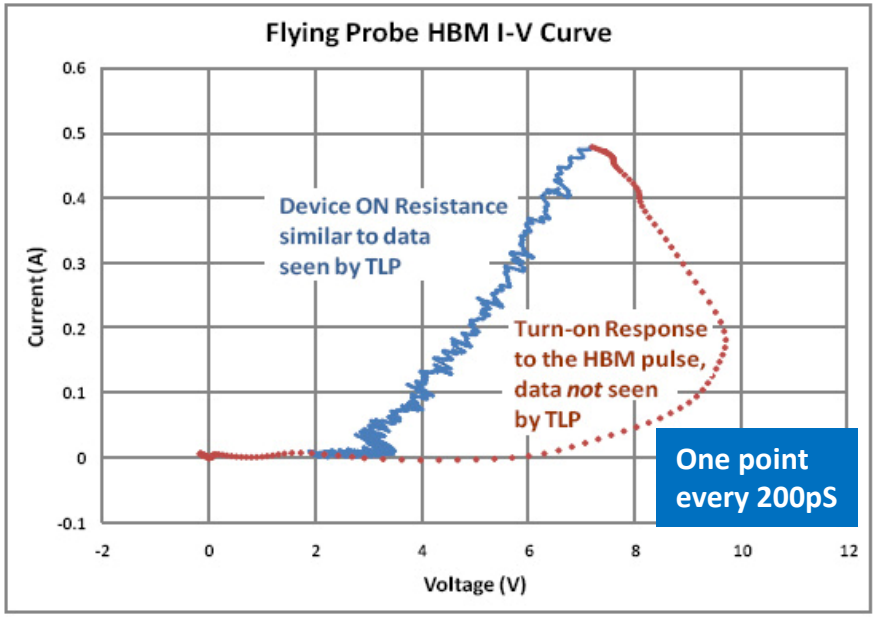
Barth VFTLP System

HBM (Human Body Model)





- **Created by an RC discharge**
- **Clean PIV waveforms showing turn-on response are possible at the wafer level**
  - ***Not*** seen by TLP
  - ***Not*** seen at package level



Example of an I-V Curve from a single HBM pulse

HBM Flying Probe Test System

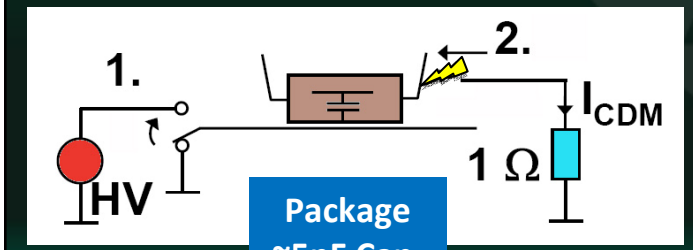
- ESD testing on wafers, bare die, and packaged parts
- Eliminate parasitic distortions in relay-base test systems
- TLP-like measurements of actual DUT pin response

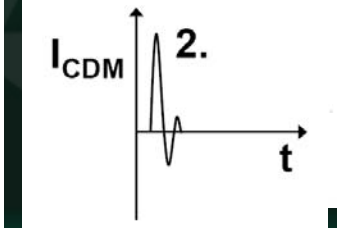
TDR pod for sensing pulse response at the DUT pads

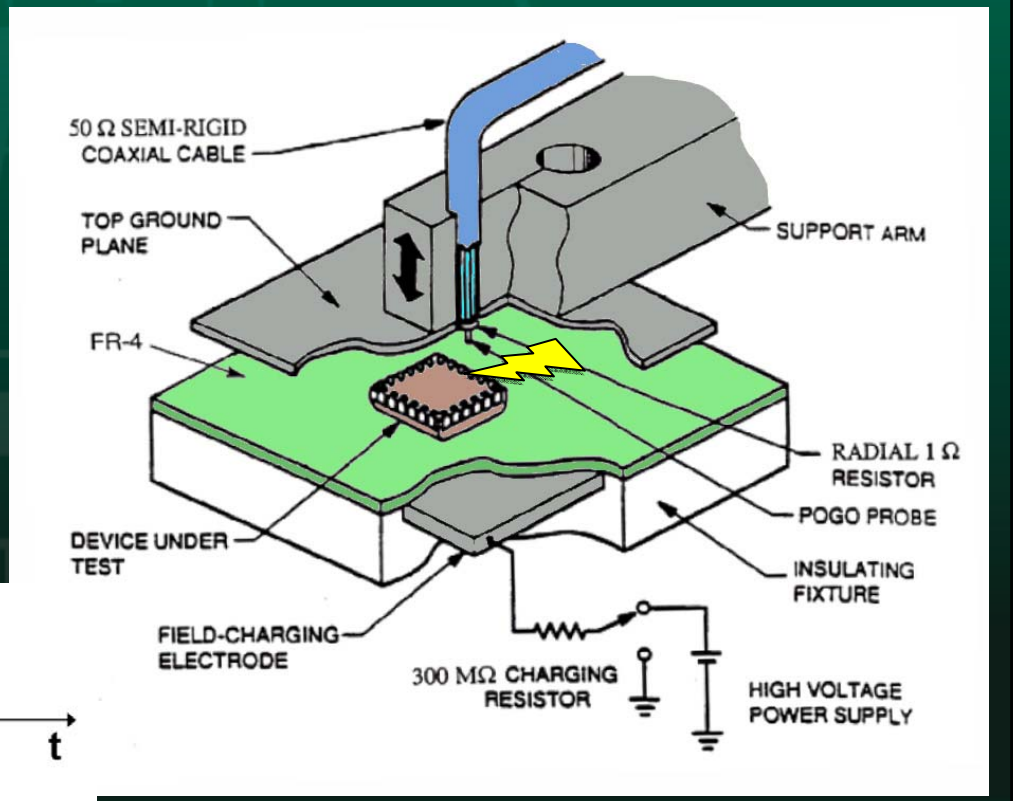
CDM (Charge Device Model)

- Top ground plane is lowered until pogo pin contact DUT pin
- Discharge path is from charged DUT to grounded pogo pin

Hanwa CDM Test System

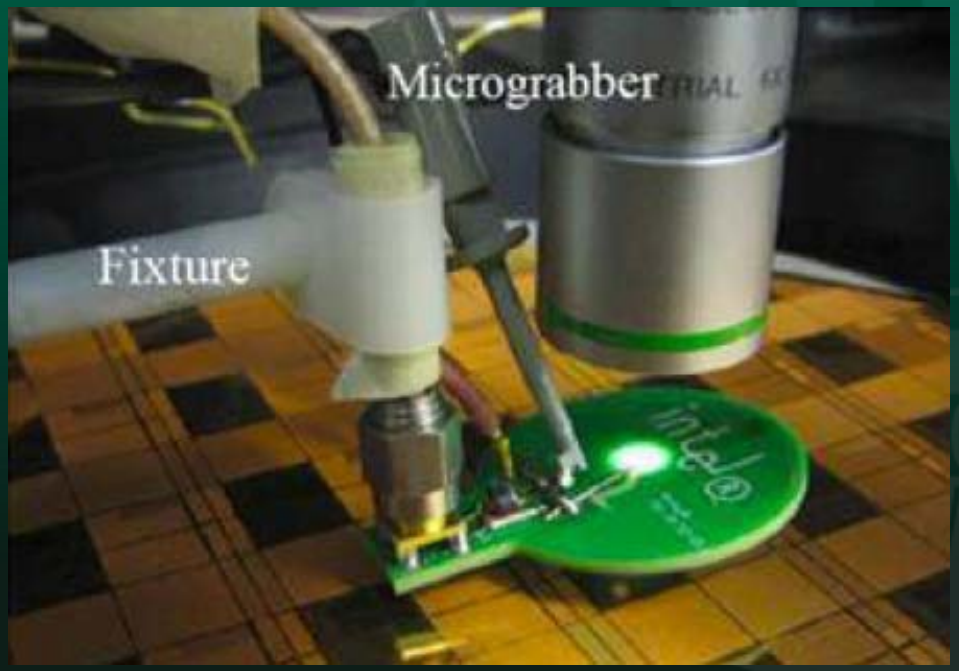




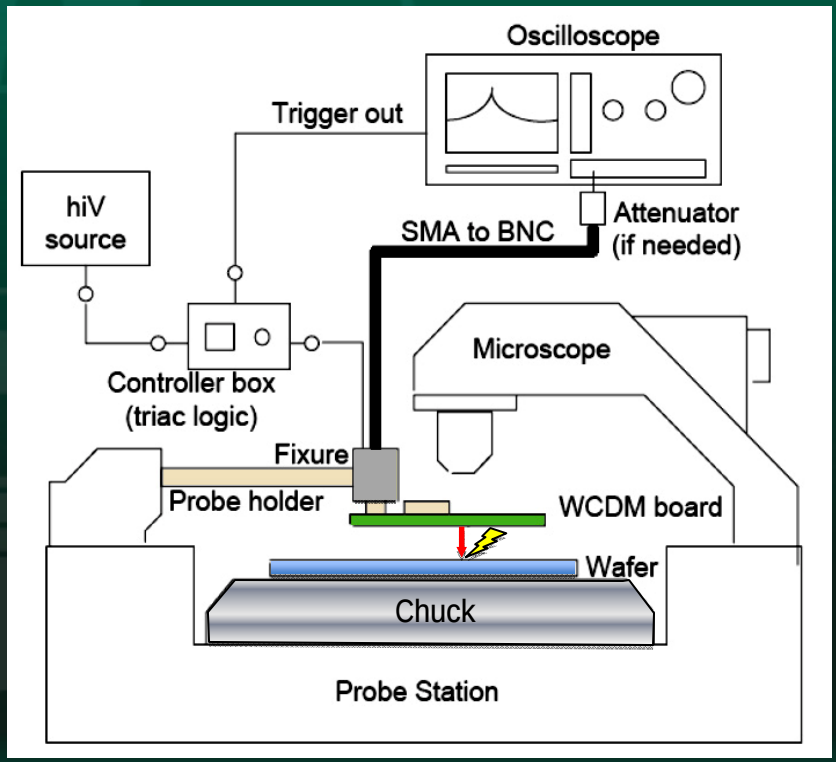


WCDM (Wafer Charge Device Model)

- Discharge path of metal disk is through a single probe (red)
- CDM spark occurs as disk is lowered to make probe contact

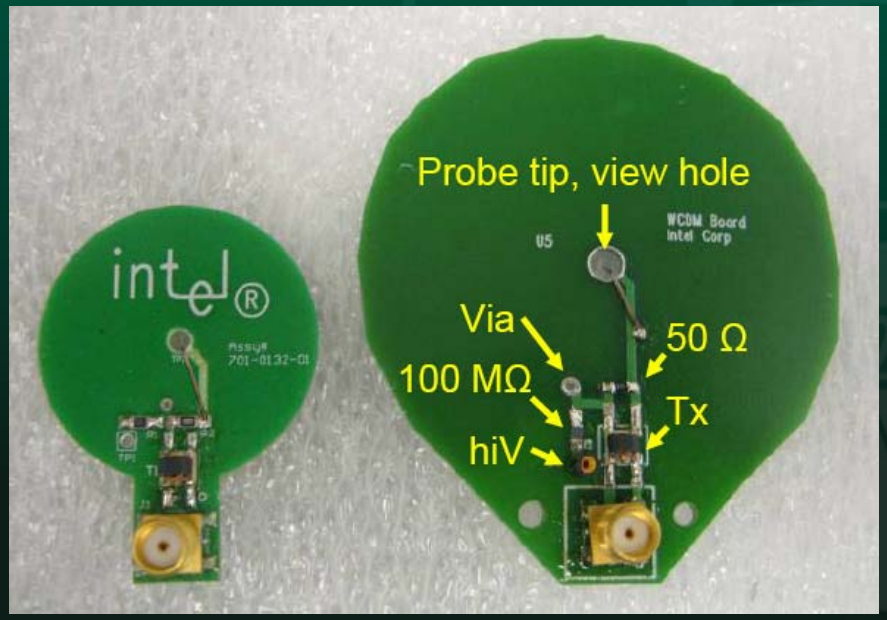


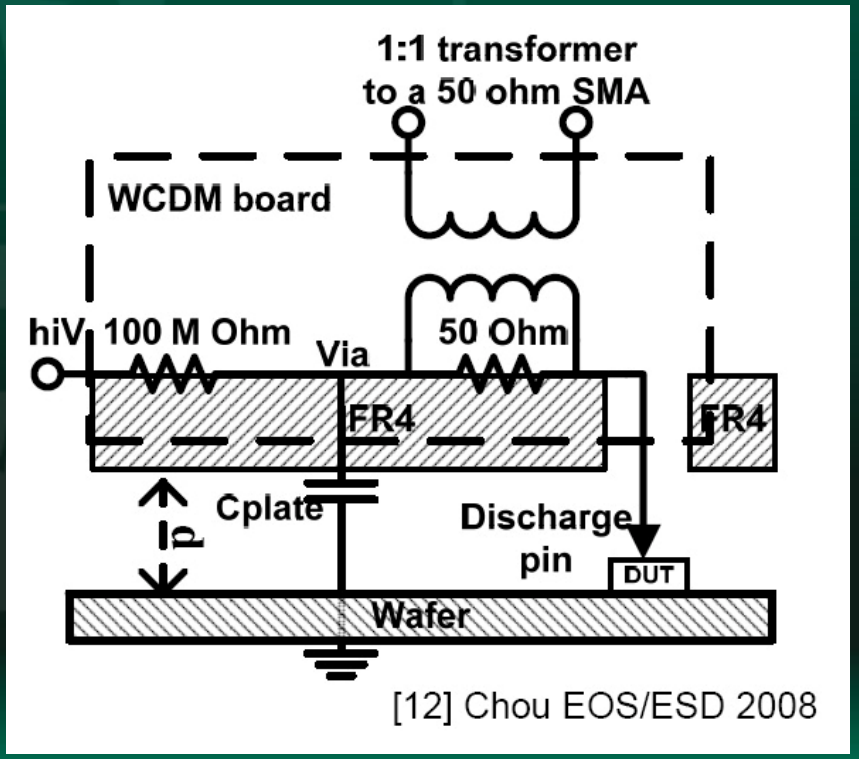
Intel - [12] Chou EOS/ESD 2008



WCDM (Wafer Charge Device Model)

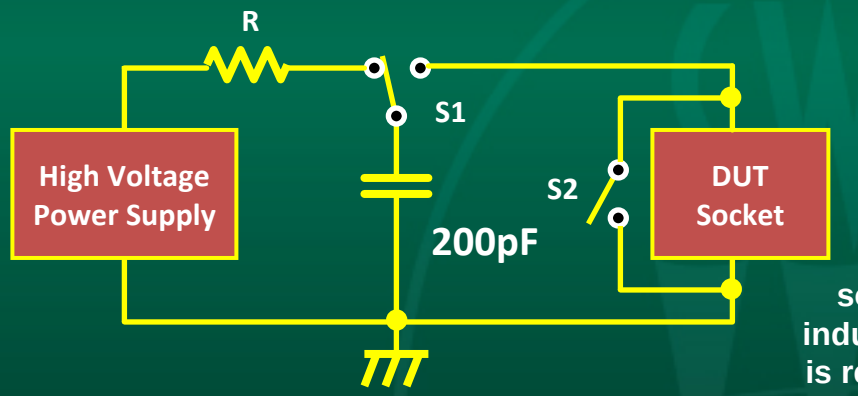
- Two WCDM boards scaled for 5pF and 15pF capacitance
- This simulates small & large package cap. in CDM tests
- Discharge is thru a cantilever tungsten probe tip





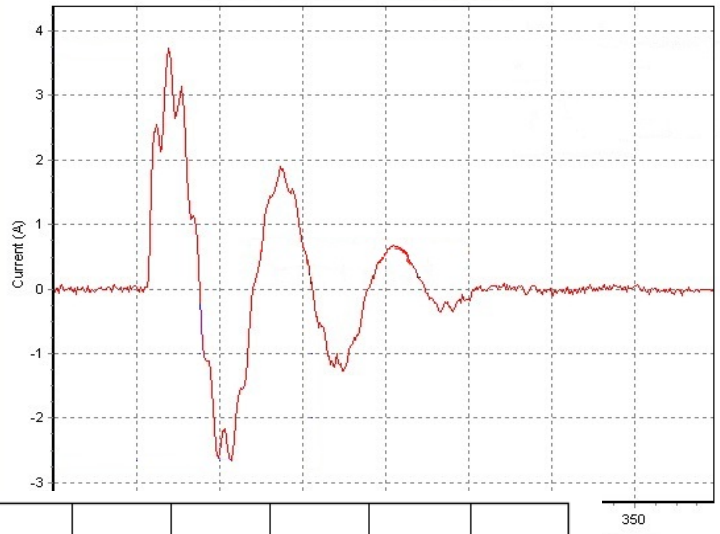
[12] Chou EOS/ESD 2008

MM (Machine Model)

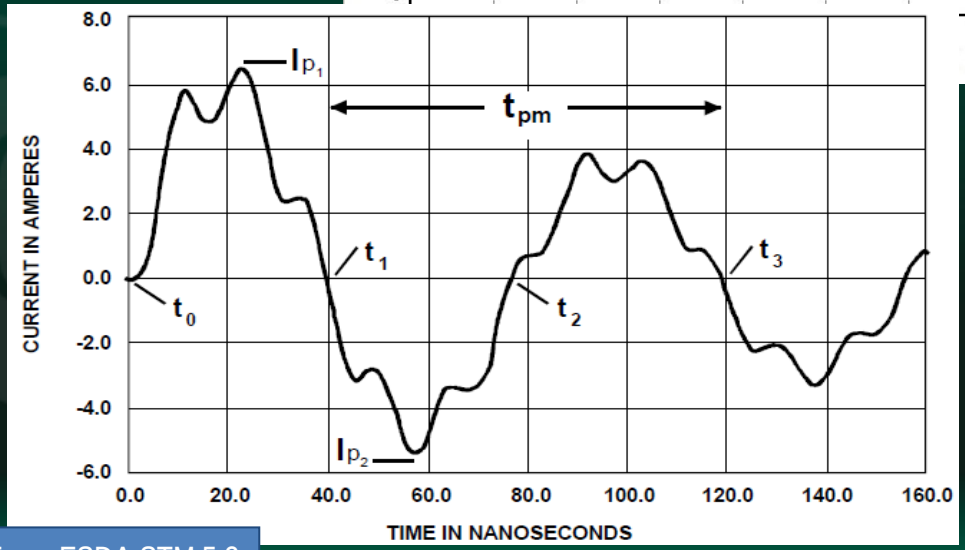


socket inductance is required

MM System Cal. Measurement



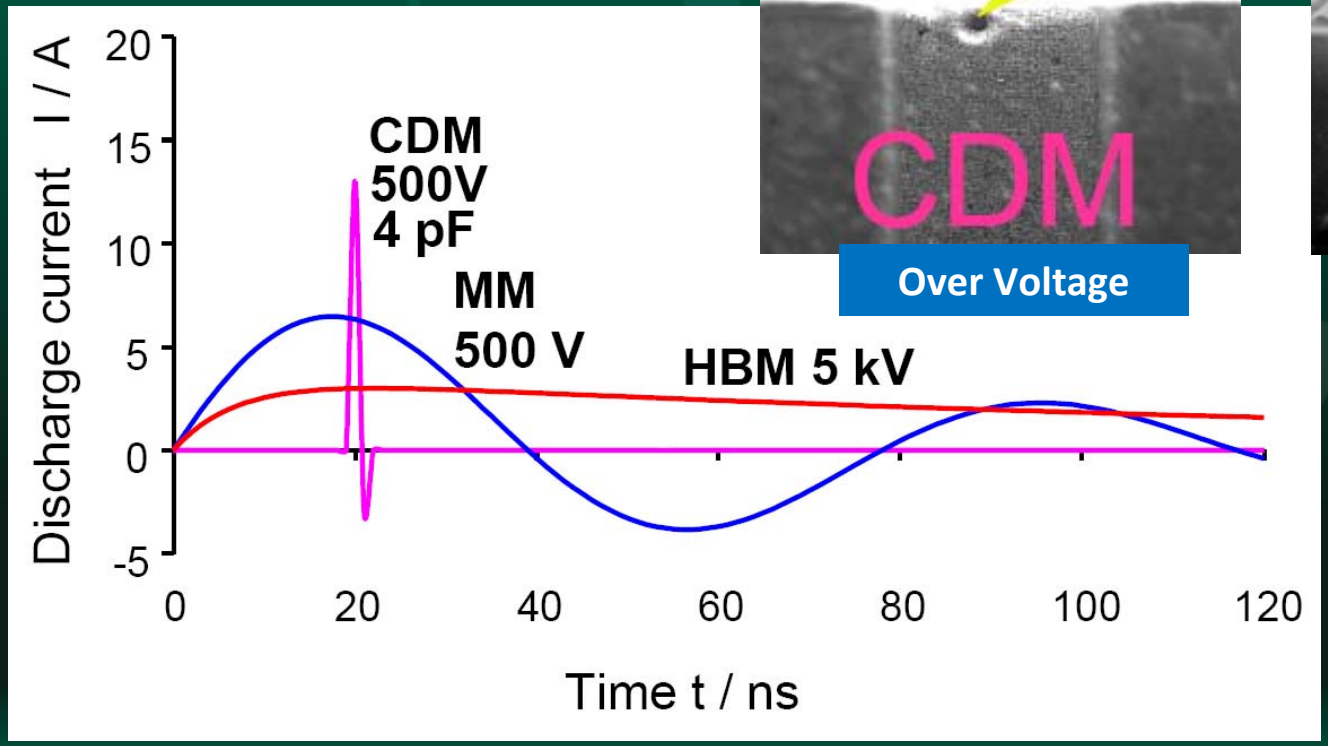
- Under-damped sine wave
- Waveform created by parasitic inductance
- Not the best waveform for wafer-level test !



From ESDA STM 5.2

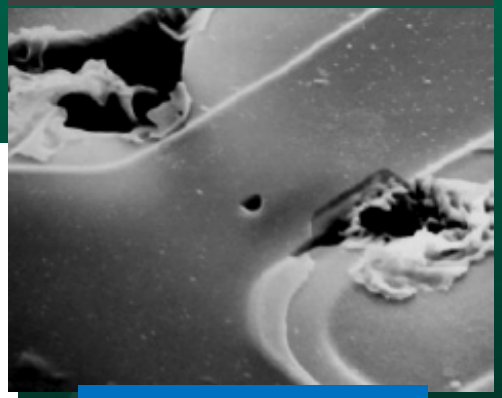
Comparison – CDM, MM, HBM

- **Short pulses produce pin holes and cratering**
- **Longer pulse waveforms cause melting**



Over Voltage

MM, HBM

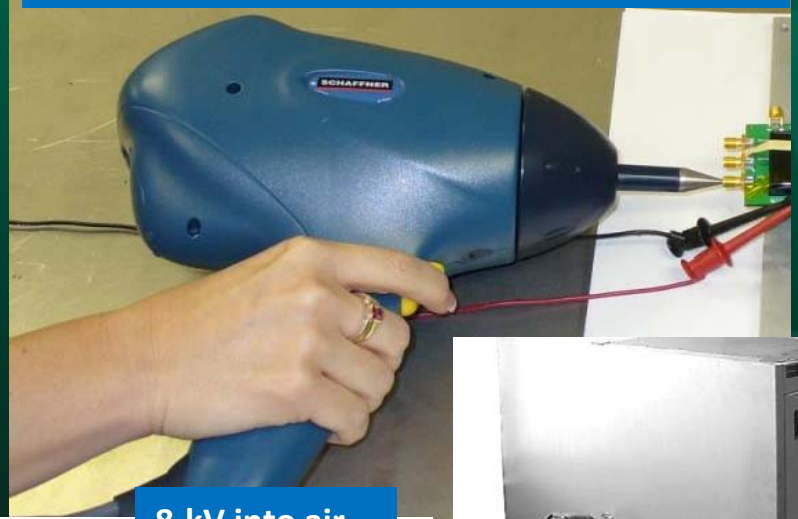


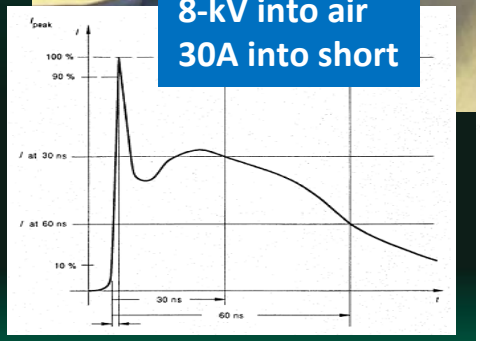
Energy

HMM (Human Metal Model)

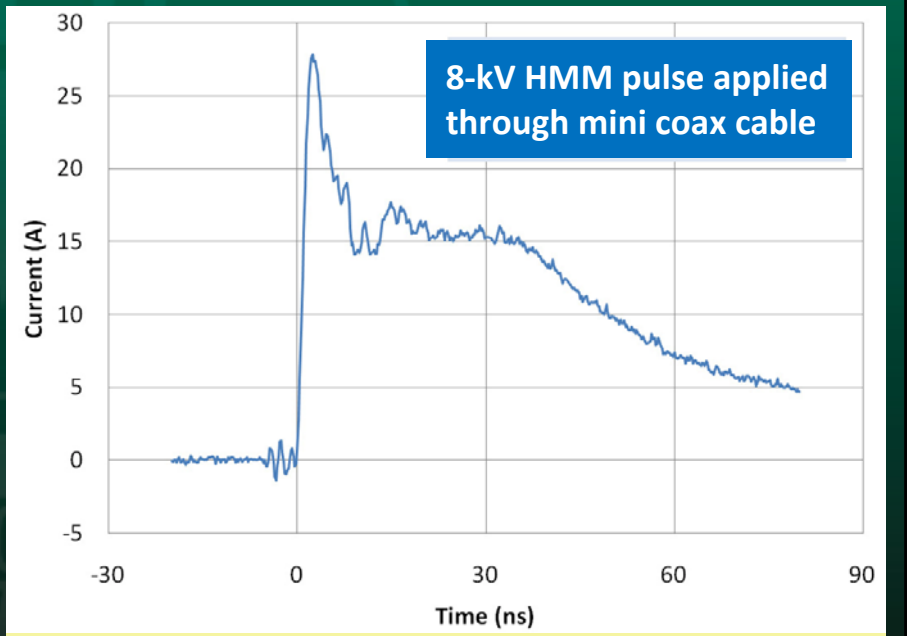
- **Simulates ESD short & long pulse effects; IEC 61000-4-2**
- **Use a 50Ω pulse delivery at wafer-level; *Not* the Gun!**

Schaffner ESD Simulator Gun (not 50Ω output)





8-kV into air
30A into short



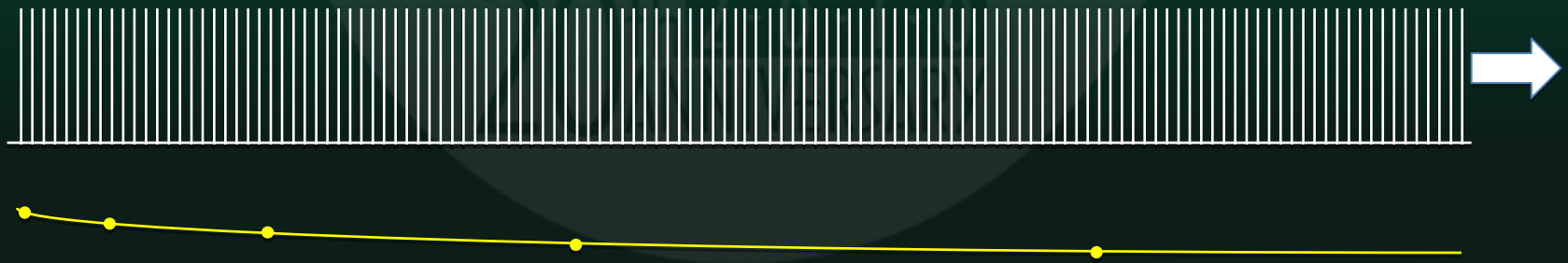
8-kV HMM pulse applied through mini coax cable

8 mil OD 50Ω cable passes CE Mark test using 50Ω delivery of IEC 61000-4-2

ESD-TDB (Time Dependent Breakdown)

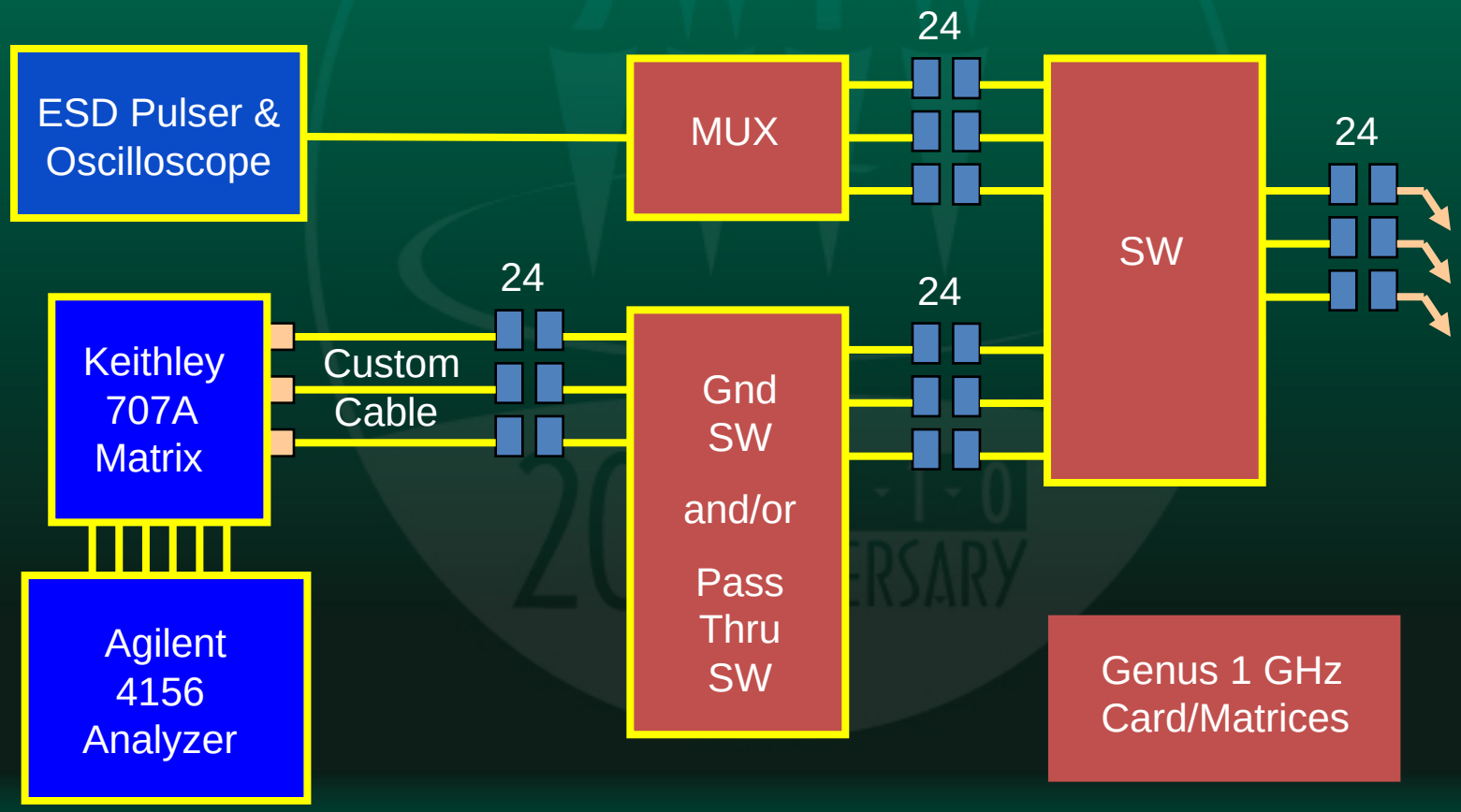
- **Toshiba Example (very similar to TDDB)**
  - Low voltage CDM investigation

    Dec 2008 – Nozomu Kawai, Nobuyuki Wakai
  - < 500V VF-TLP pulse stream on wafer
  - Monitor leakage degradation (wear out)
  - Same test methodology could be applied to standard TLP or HBM pulse streams.

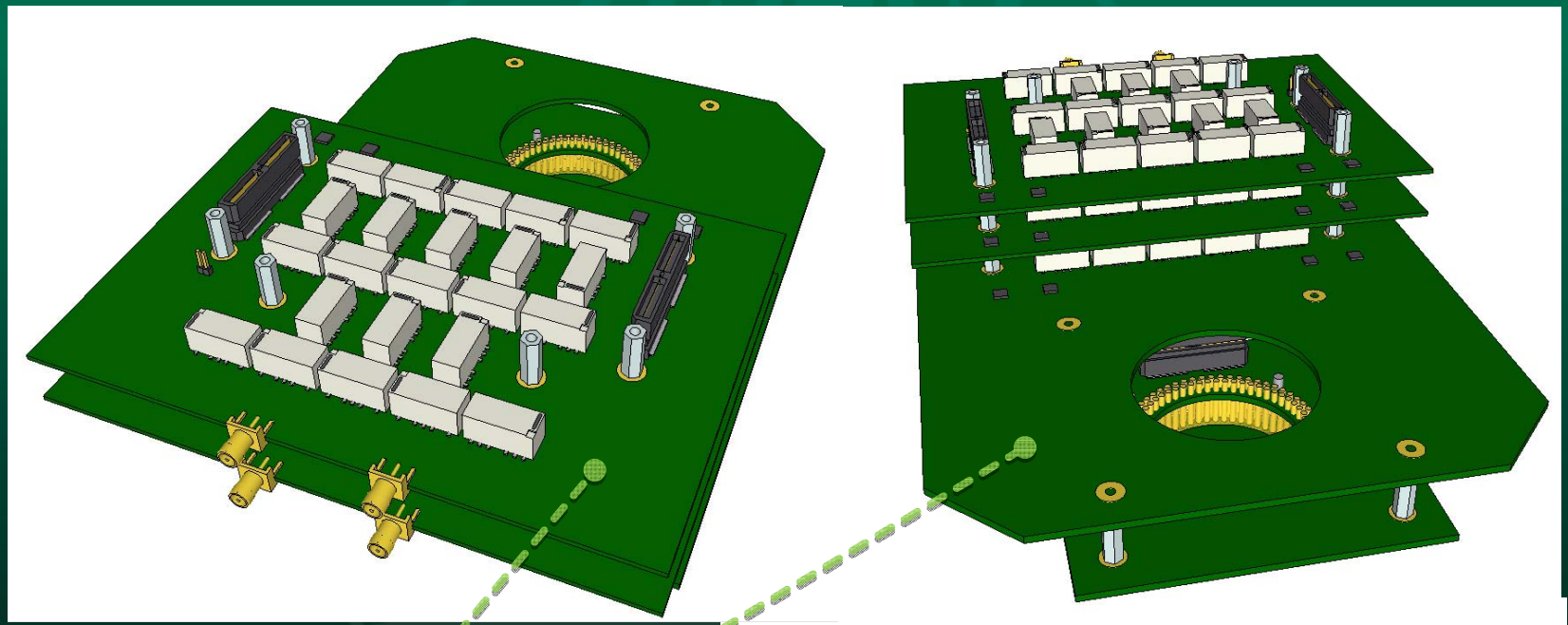


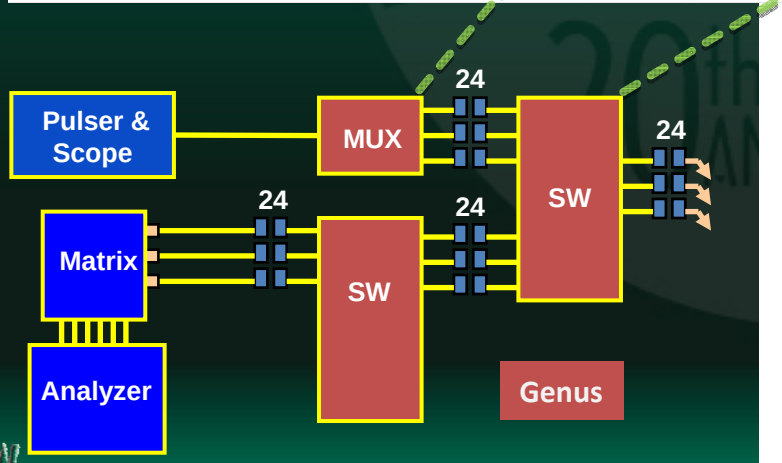
Leakage measured in log time intervals until target %change is reached or device failure

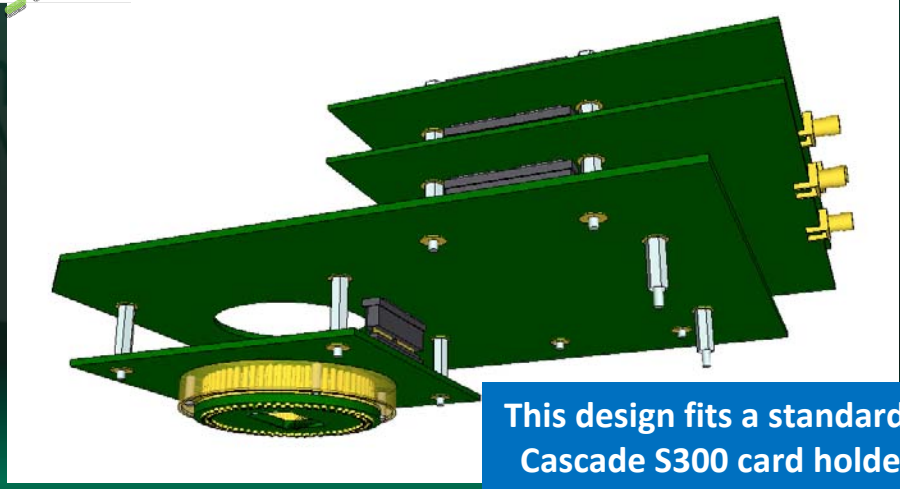
ESD Pulse Delivery With Full DC Parametric Analysis



3-D Views of Genus Probe Card/Matrix





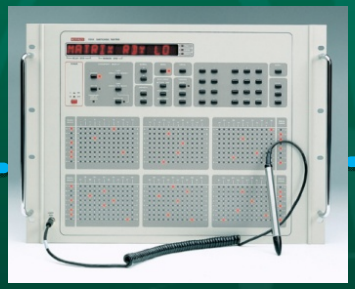


This design fits a standard Cascade S300 card holder

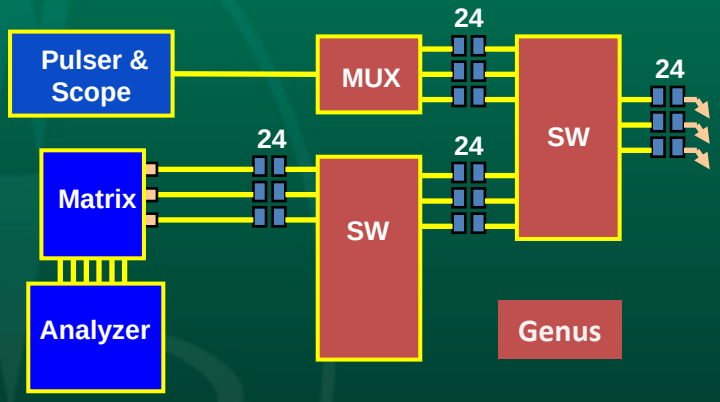
24 Pin DC + HBM Automation

- **Precise PIV characterization – data points every 200ps**

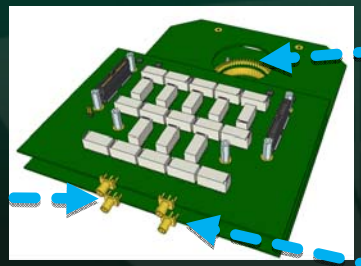
Semiconductor Parameter Analyzer



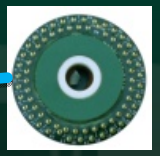
Low Leakage Matrix



Arcus HBM Pulse System

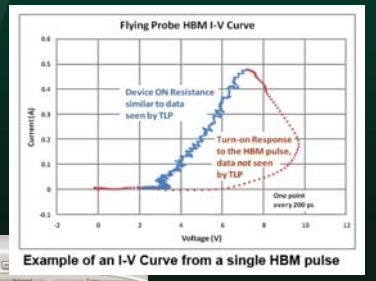


Genus 1 GHz Modular Pin Expander

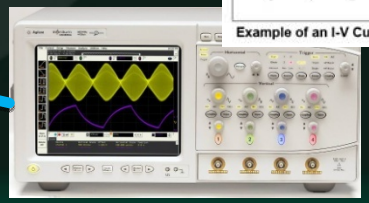


C60 Donut Probe Card

PIV turn-on response to HBM waveform



Example of an I-V Curve from a single HBM pulse



Oscilloscope

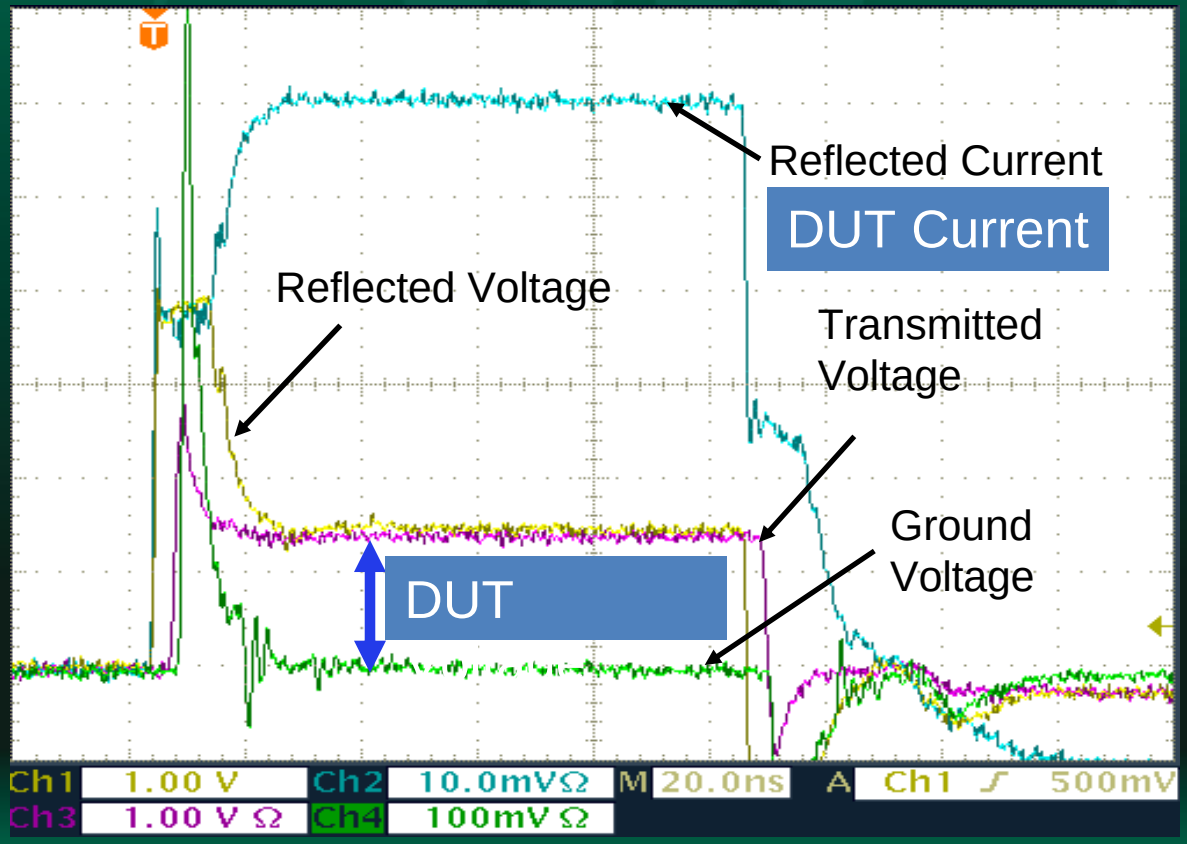
Calibration Is A Big Issue

- **System Corrections**
  - Open & Short calibration required
  - Shorting structure tested at low & high power
  - Oscilloscope gain & offset correction
  - Inductive current sensor linearity correction
  - Multiple pin interaction corrections
  - Non-Kelvin correction for contact resistance
  - Kelvin correction for sense high impedance attenuation

Each raw data point gathered is process by complex vector math equations to account accurately for all correction factors.

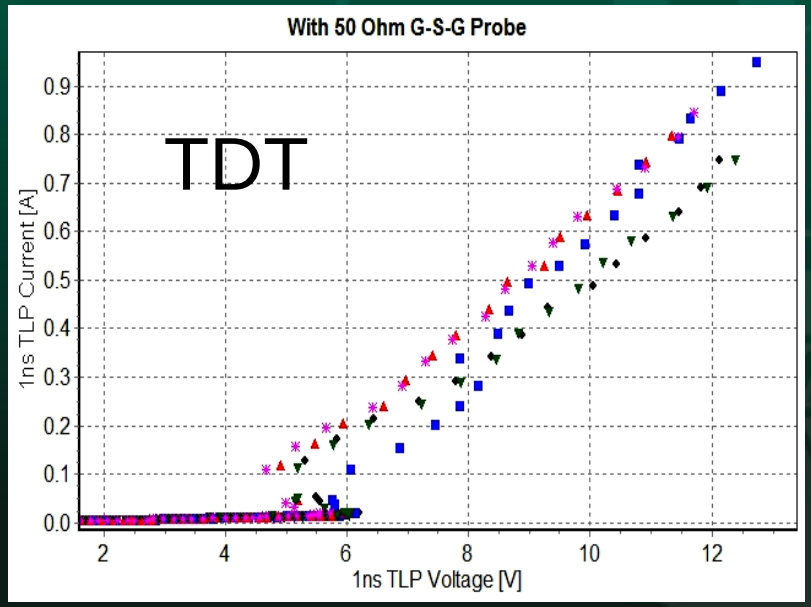
Kelvin TDR Waveforms

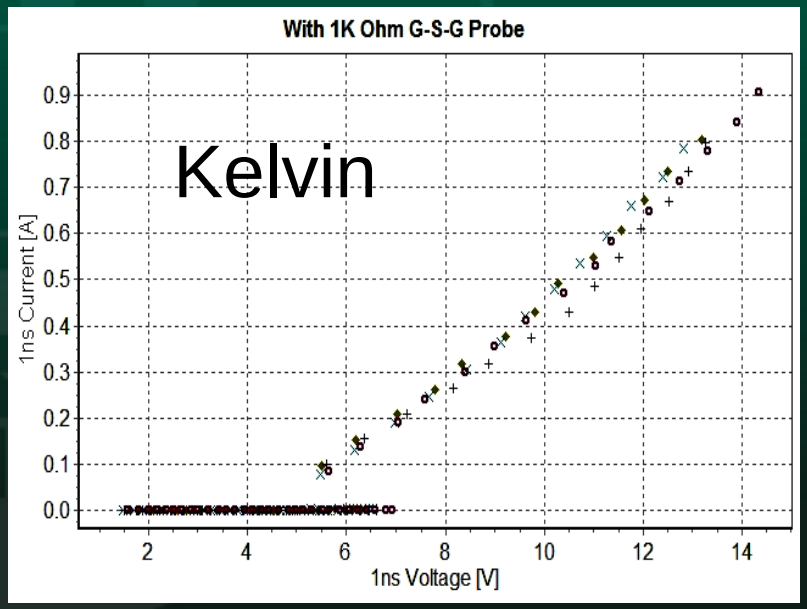
- TLP pulse is delivered with high current force probes
- Separate sense probes measure differential voltage



Performance of TDT and Kelvin

- Measured with 1.2nS pulses
- Kelvin removes the variation of contact resistances





Conclusions

- **Automated ESD scribeline test is now a reality**
  - TLP, HBM, HMM, WCDM, Pulse IV Curve Tracing
  - These tests can be combined with traditional parametric test suites for single touch down characterization
- **Challenges to full TEG automation are solvable**
  - WCDM & VFTLP are constrained to one or two pins
  - Most ESD tests can be automated for full parametric TEG testing using the Genus probe card/switch matrices
  - Sophisticated calibration routines maintain accurate measurements at all probe card needles
  - Modular design of matrices adapt to future test needs