IEEE SW Test Workshop

Semiconductor Wafer Test Workshop

Power Delivery Network Analysis - a case for true 3D simulations

Gert Hohenwarter

GateWave Northern, Inc.

Background

- In many modern integrated circuits the power delivery network must be capable of responding to rapid transient current changes.
- There is a finite (and relatively long) time lag between these transients and the tester's response to such changes.
- Multiple capacitors along the power delivery network or system are used to 'stage' replenishment of energy until the tester response has arrived.

Objectives

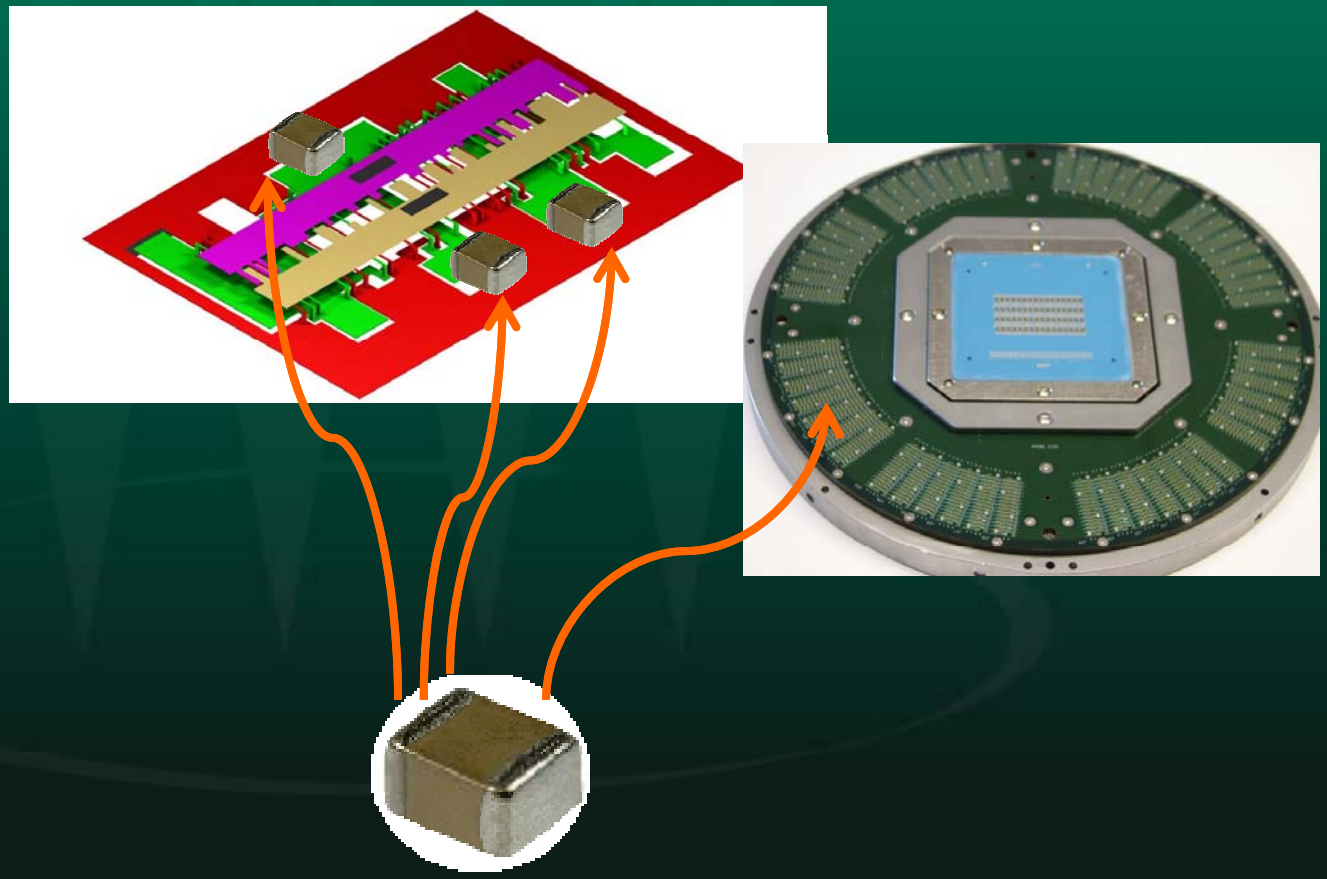
- Examine probe head power delivery performance
- Identify key issues when assessing that performance
- Identify resonance problems
- Offer potential solutions

Approach

- Outline system configuration for probe head and die to be tested
- Present measurement results that are used as input to simulations
- Use simulations with 3D modeler combined with SPICE circuit analysis to highlight problem spots

Probe card PDN architecture

- **Inductors**
  - Contacts
  - Traces
  - Vias
- **Capacitors**
  - Components
  - Planes



Device-under-test (DUT)

- **Circuits on-die**
  - Blocks
  - Ancillary components
  - Structure

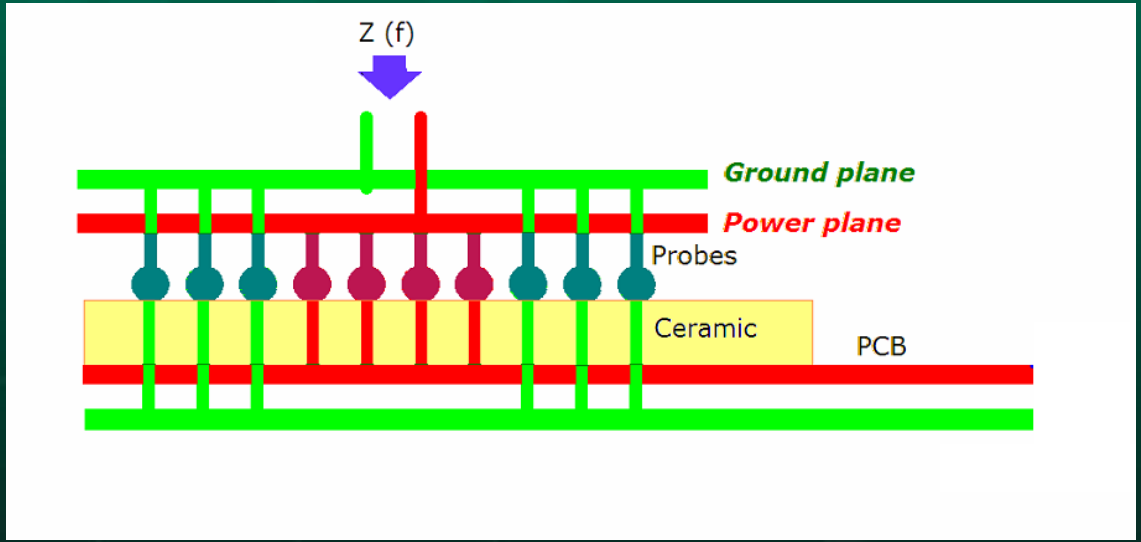
Die circuitry

Packaged DUT

Equivalent circuit ?

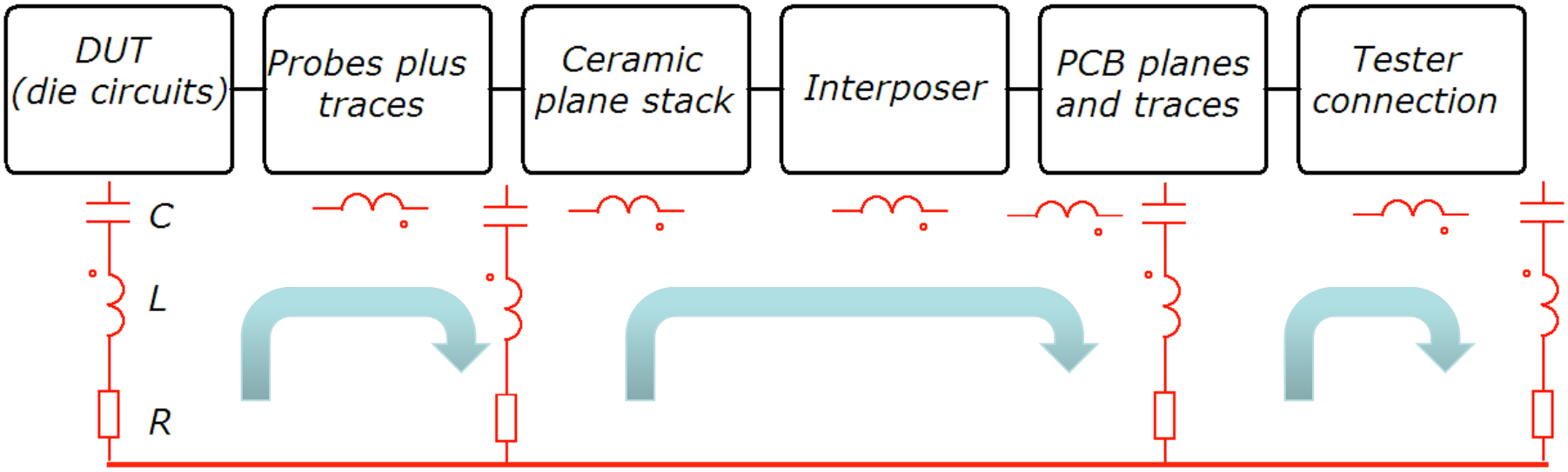
Basic 2D Probe Card PDN Model

- **Simple head**
  - All contacts lumped together
- **Elements**
  - Inductors
  - Capacitors
  - Transmission lines (Planes)

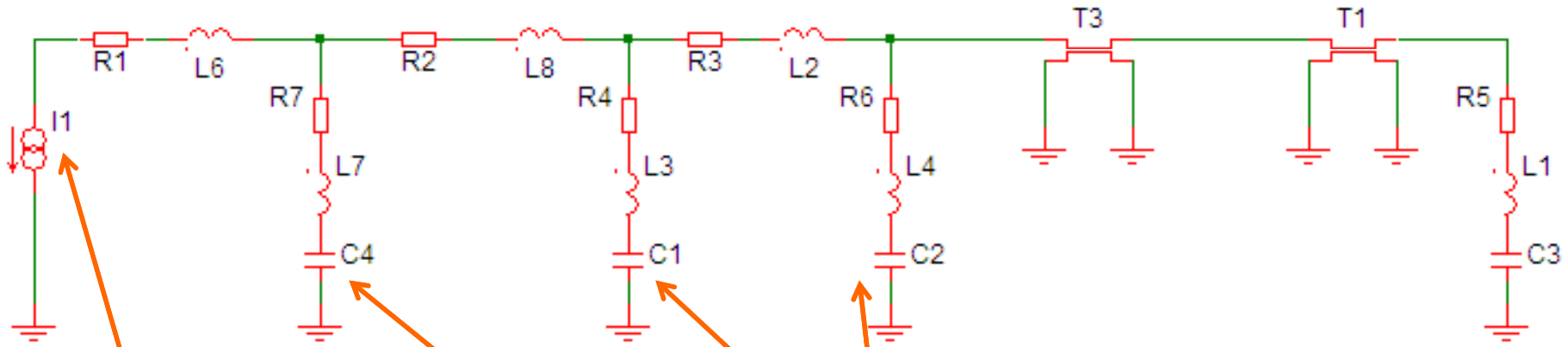


Probe card PDN architecture

- **Multiple paths for currents possible**



Basic Probe card PDN equivalent circuit



Current source (device on-die)

Probe head

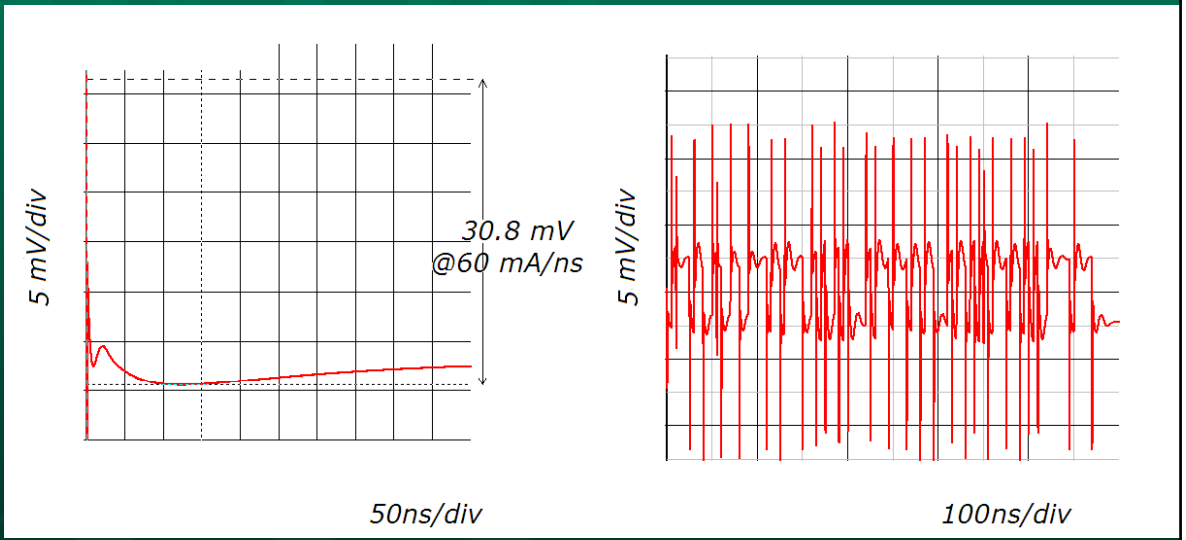
Bypass capacitors

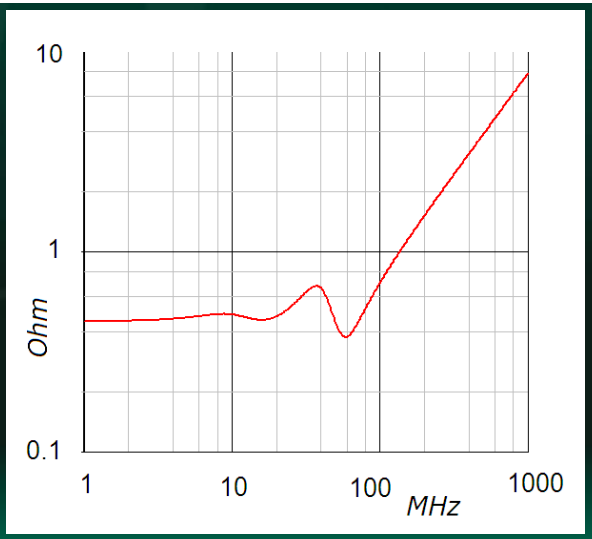
PCB

Connections on PCB and to tester

Performance

- **Time domain**
  - di/dt noise response to step excitation
  - PRBS noise response
- **Frequency domain**
  - Z (f)
    - Resonances apparent due to the multiple current paths

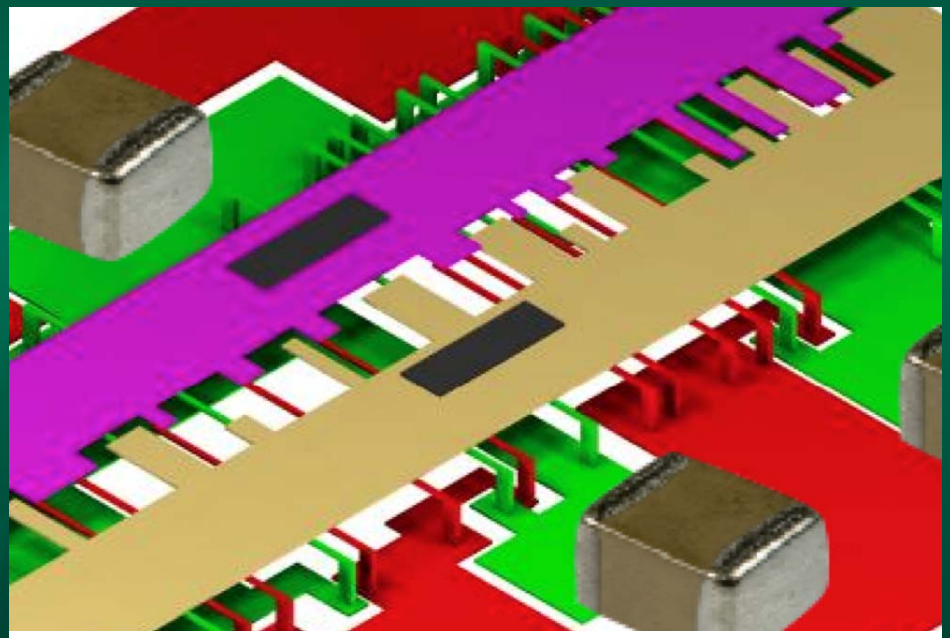


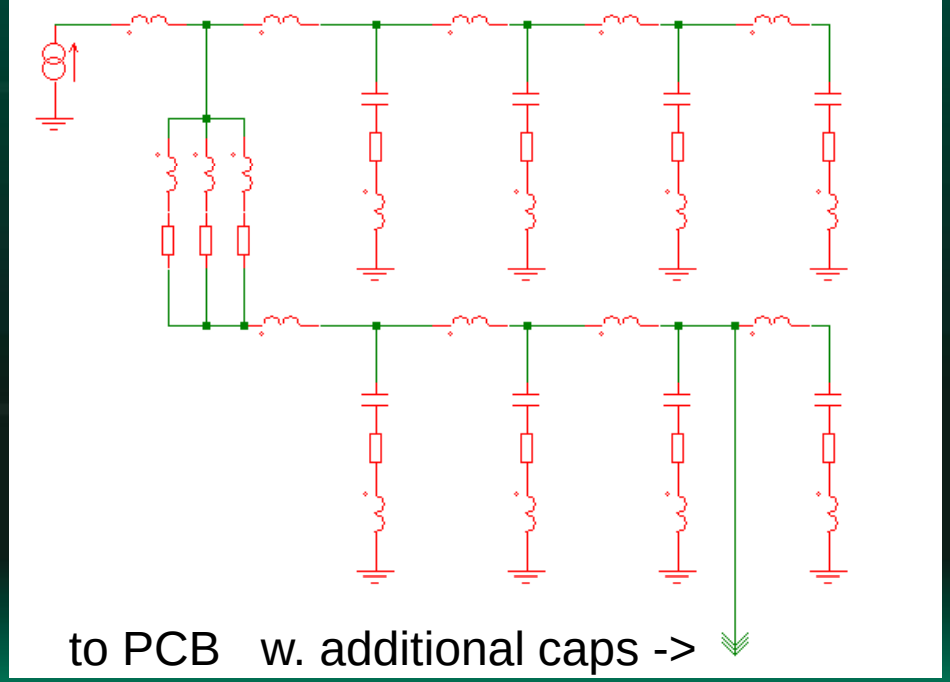


Note: Z (f) measurements must be performed from DUT side

Probe Card PDN 3D Model Detail

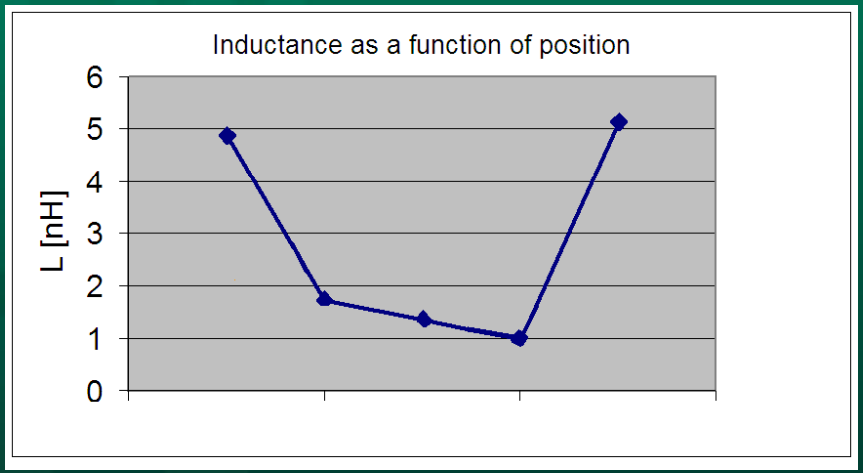
- **Plus….**
  - Multiple paths to capacitors on probe head
  - Multiple paths between planes – PCB caps
- **…..and….**
  - This is not a 2-dimensional problem and thus can not be properly approximated as such

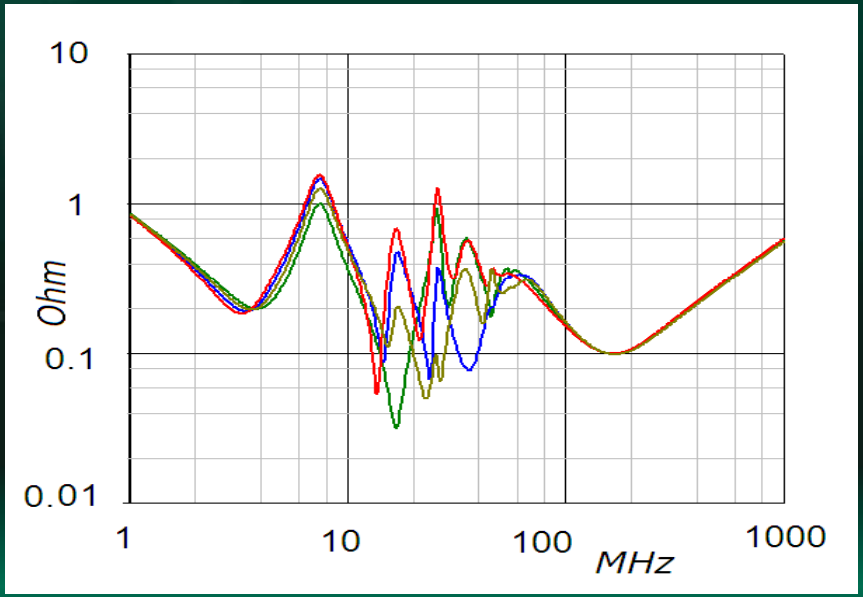




Performance impact of modified model

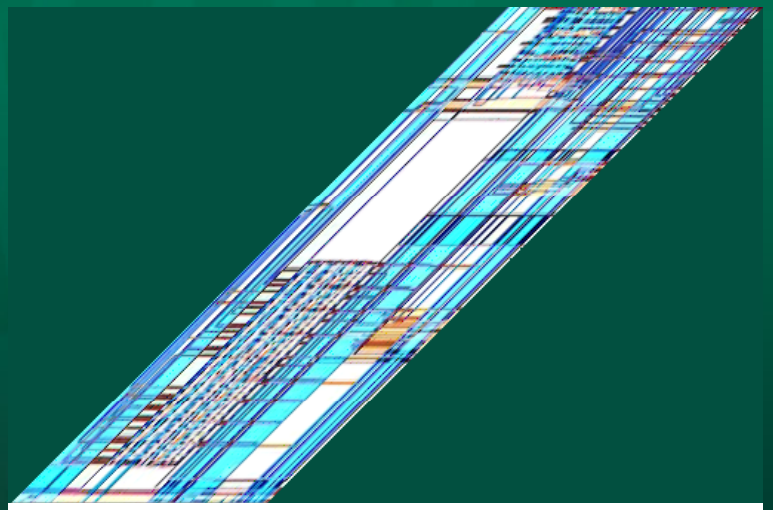
- **Effective inductance becomes a function of position**
  - didt noise also affected depending on die circuit's current draw in specific area
- **Additional resonances appear and change in frequency as a function of position**

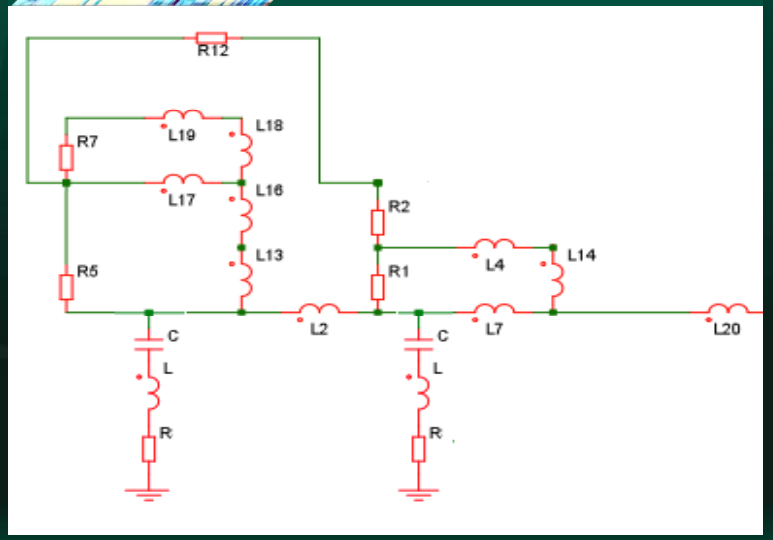




On-die PDN circuits

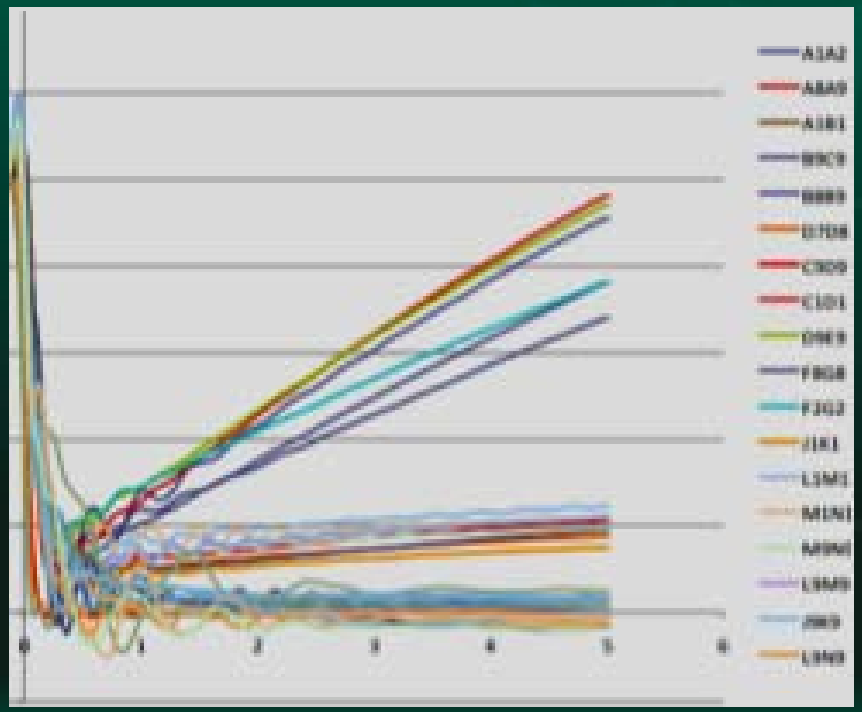
- **….and**
  - Multiple capacitors on-die
  - Multiple paths on die
- **Values determined via**
  - MFR info / IBIS info
  - Reverse engineered data
  - Measurement



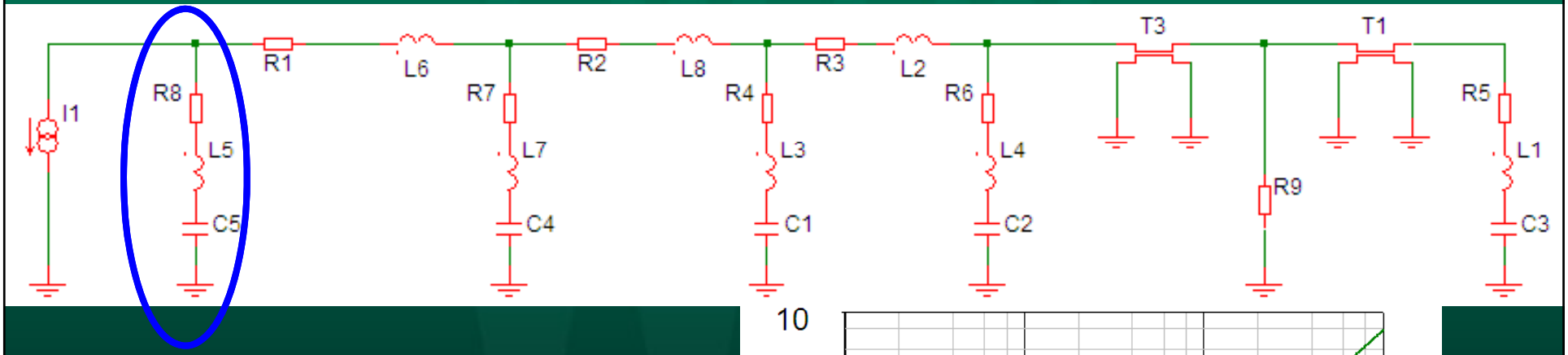


Determining ‘on-die’ circuit values

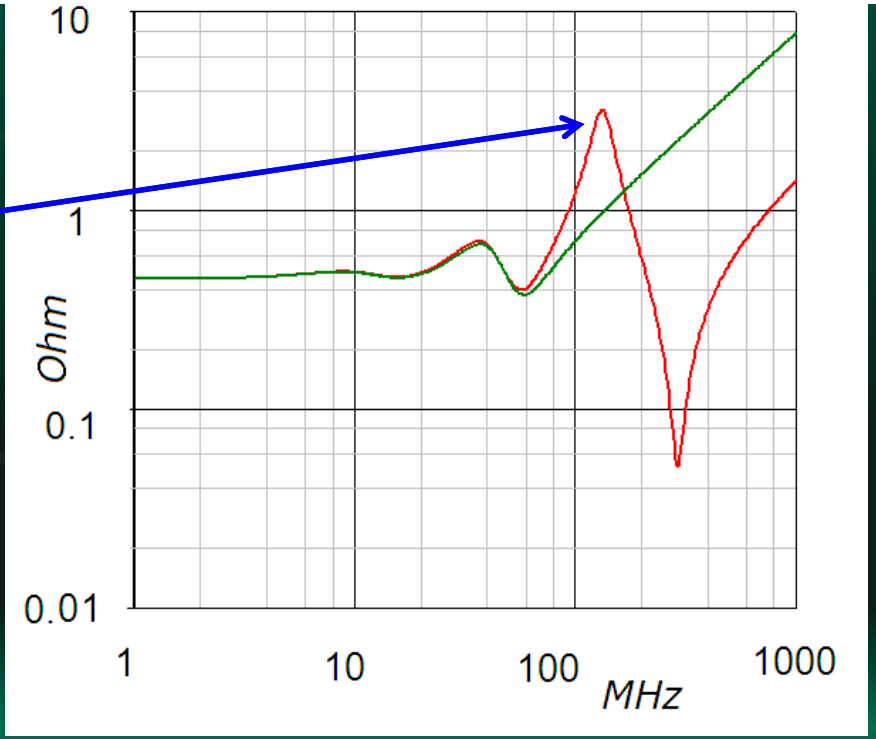
- TDR measurements allow for extraction of capacitance
- VNA measurements allow for extraction of inductance and resistance



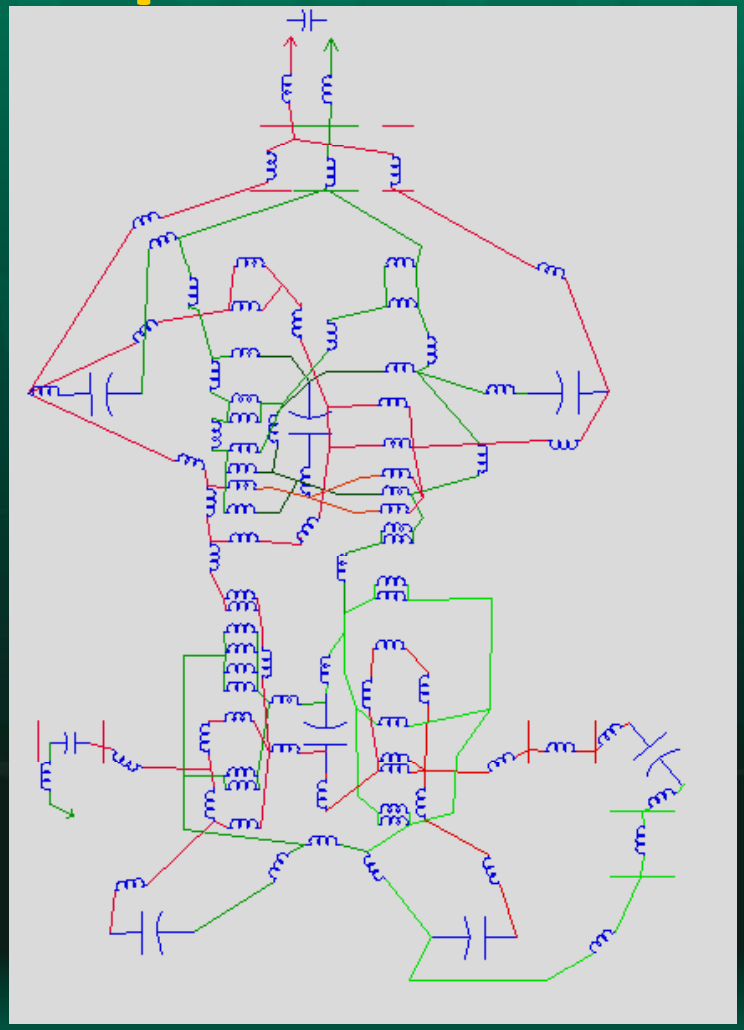
Equivalent circuit model with on-die C



- **Another pole is added to the response, possibly near the clock frequency**



Probe card PDN equivalent circuit: ‘probe head’



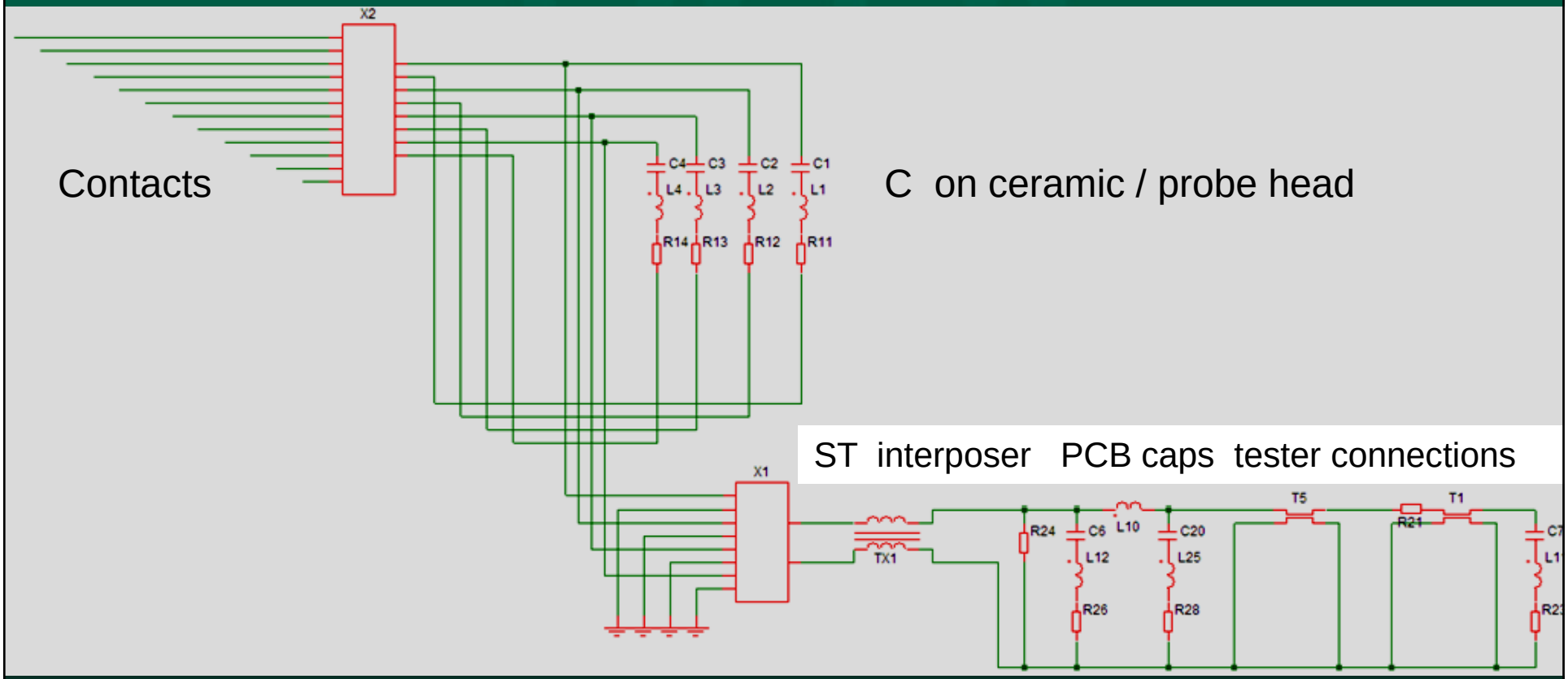
?

How can complexity be reduced and accuracy increased ?

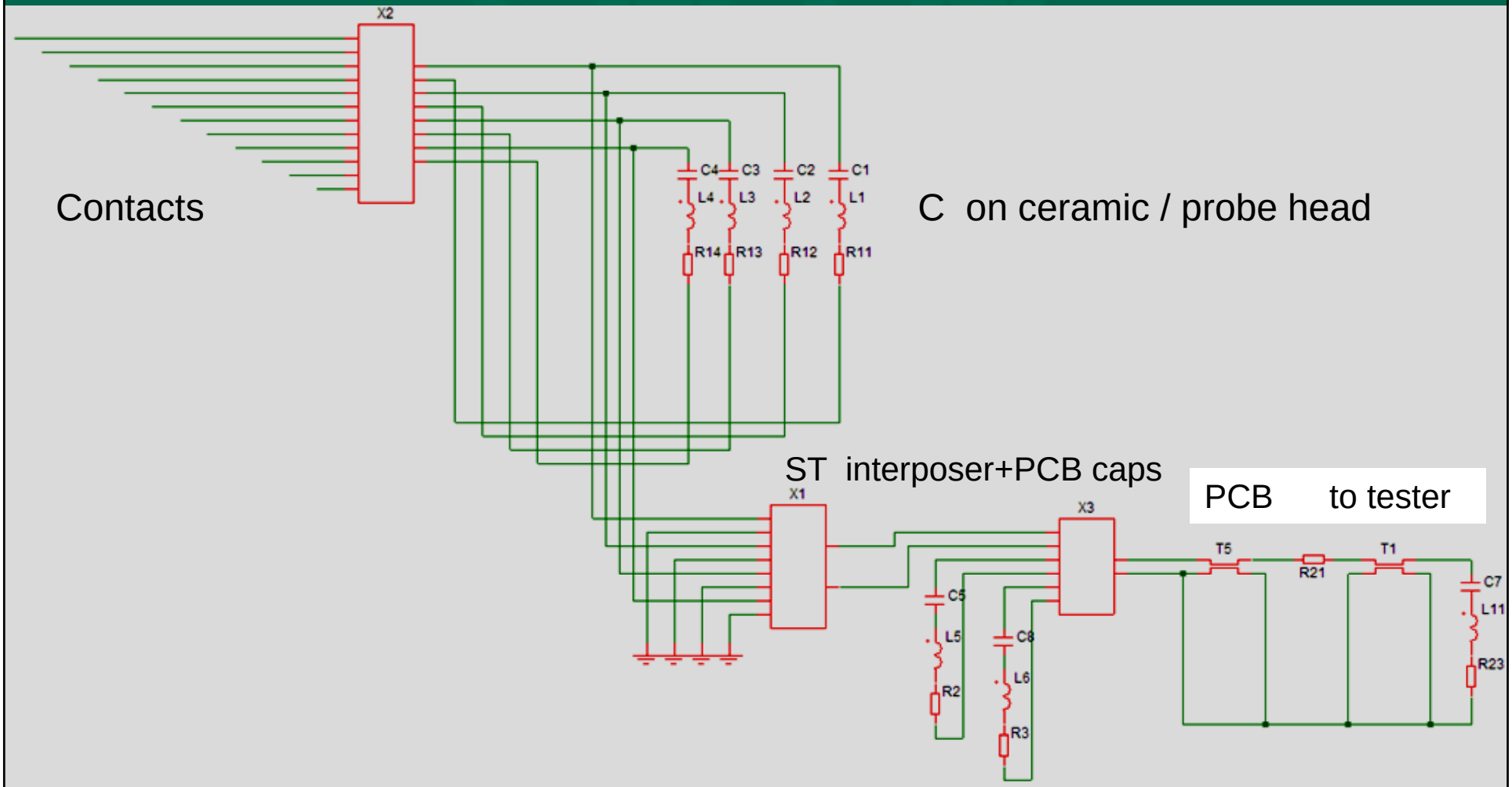
- **Use true 3D modeler**
  - Define finites size regions, e.g. 1 die
  - Subdivide problem (head, ceramic, interposer, PCB)
  - Export S-parameters
- **Combine S-parameter blocks from modeler in SPICE**
  - Z (f)
  - di/dt noise
  - PSRB pulse sequences

Probe card PDN equivalent circuit: ‘simple PCB’

- **Interposer and PCB traces modeled as individual inductors**



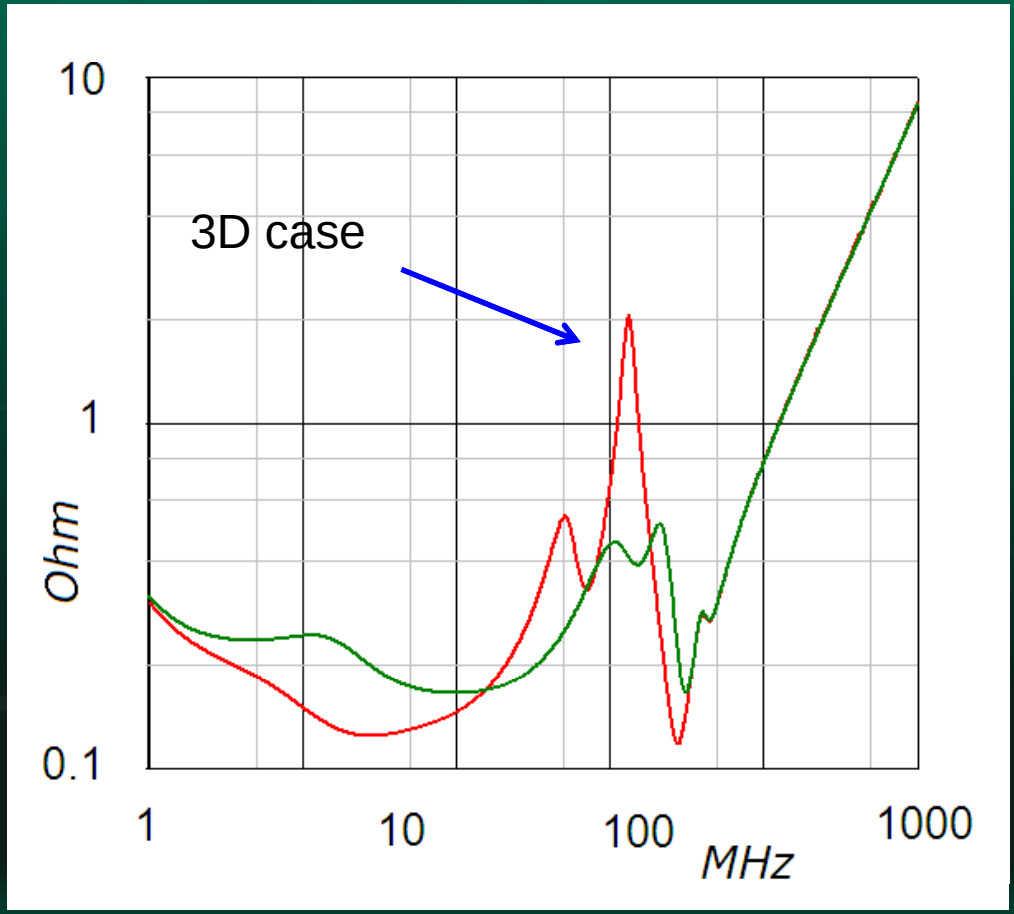
Probe card PDN equivalent circuit: ’3D PCB’



Performance comparison

- **'Simple PCB' vs. '3D PCB':**

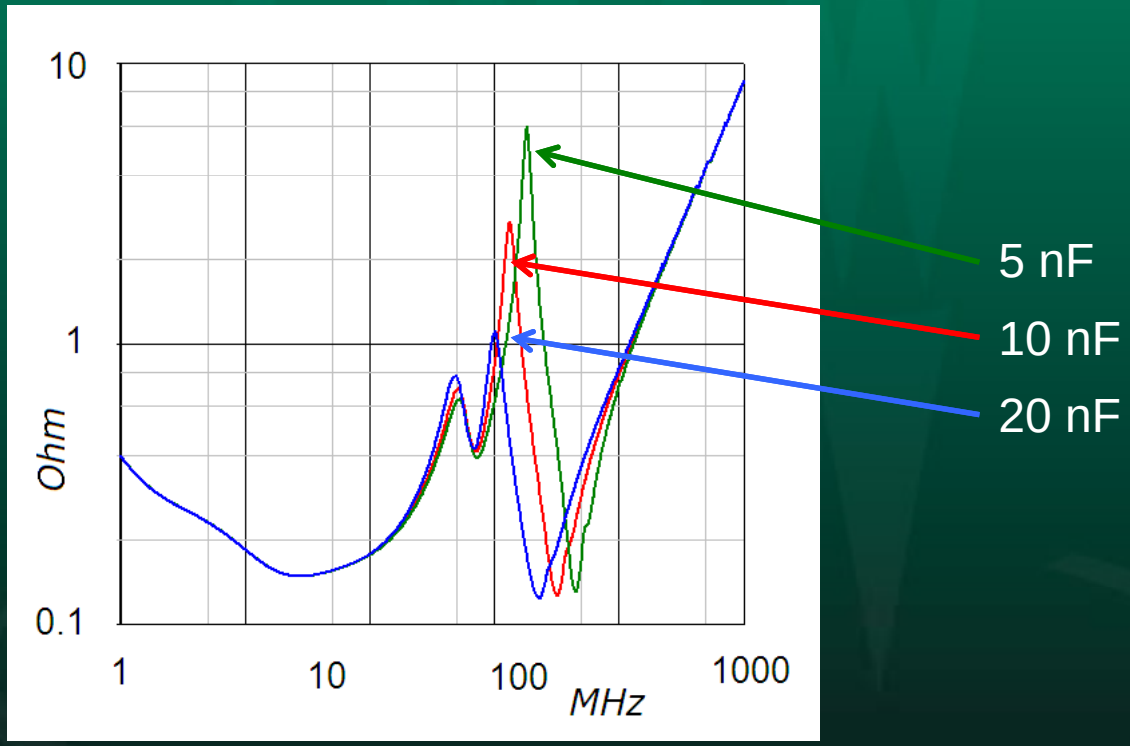
3D model reveals a higher resonance peak than simple (2D) case



Options for improvement

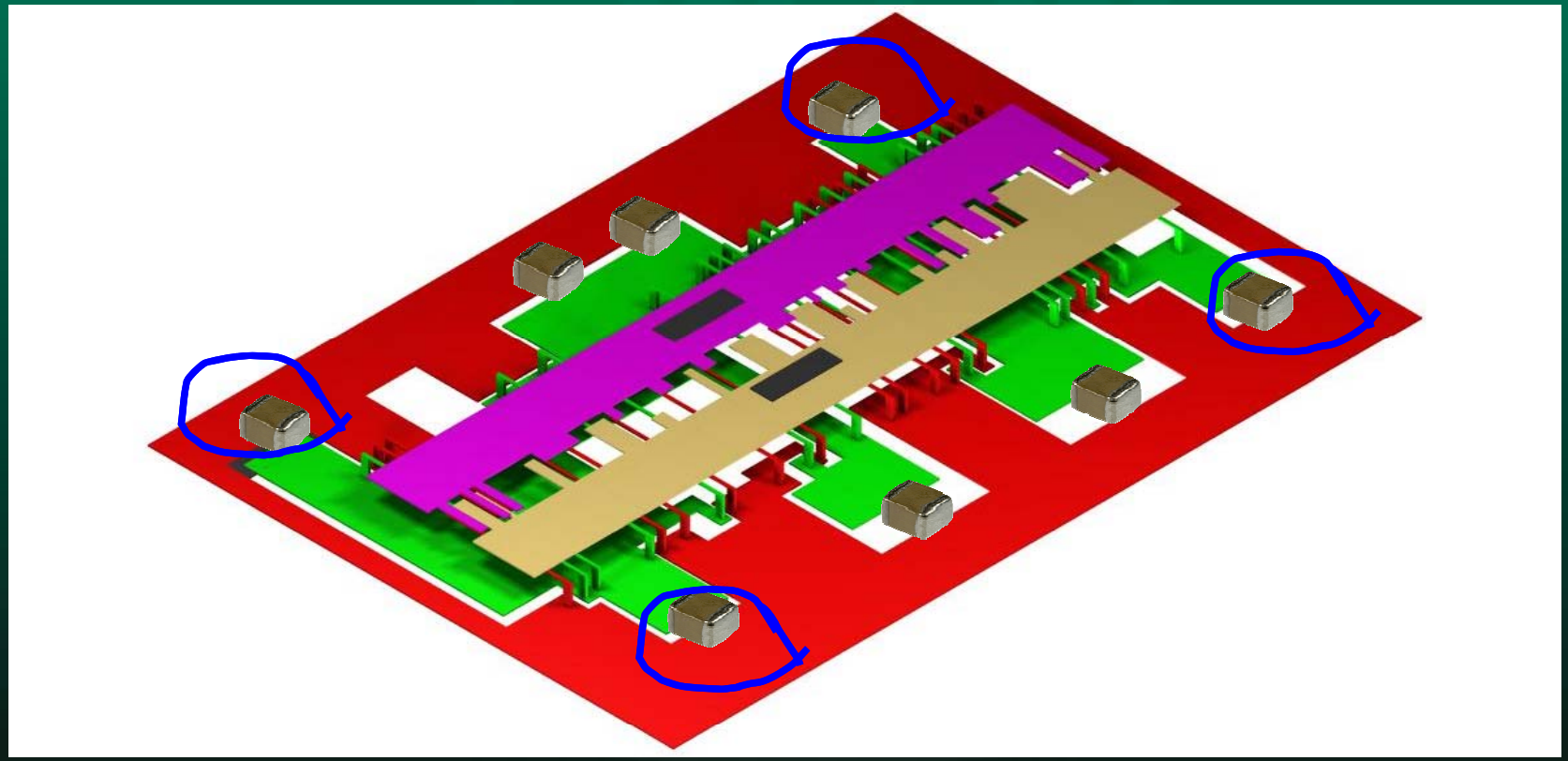
- What variables can we affect and how ?
  - Inductance
    - Layout
    - Trace/plane/via/wire/contact dimensions
  - Capacitance
    - Value
    - Placement
    - Number of capacitors
  - Resistance
    - Value
    - Placement
    - Additional resistors

Z (f) for different capacitor values



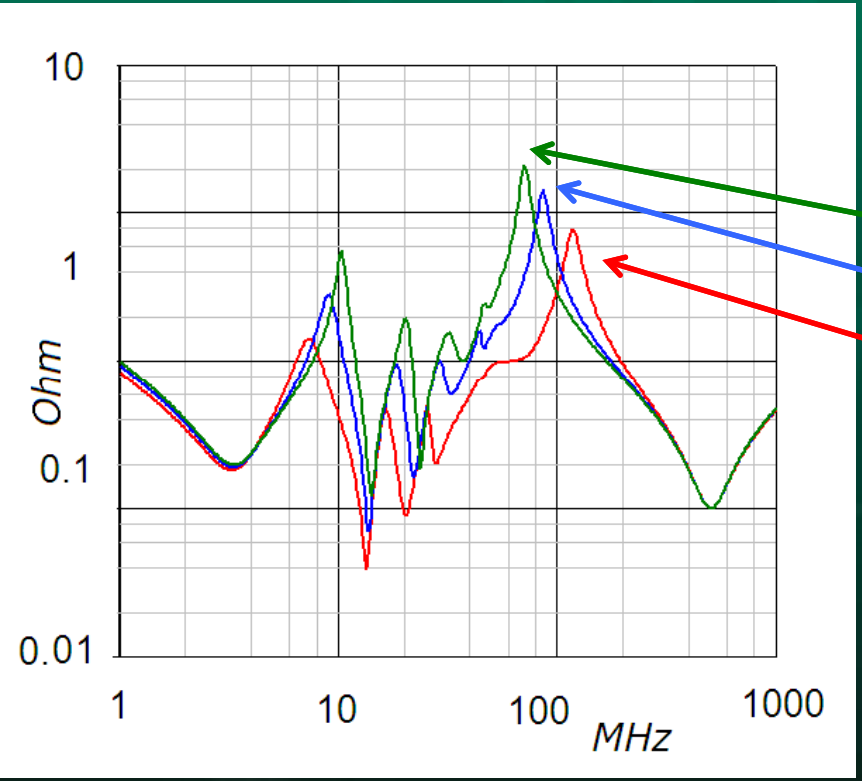
Frequency domain shows shift of worst peak to different frequencies with lower peak height

Other options for improvement



What about adding capacitors?

Z (f) for different capacitor numbers



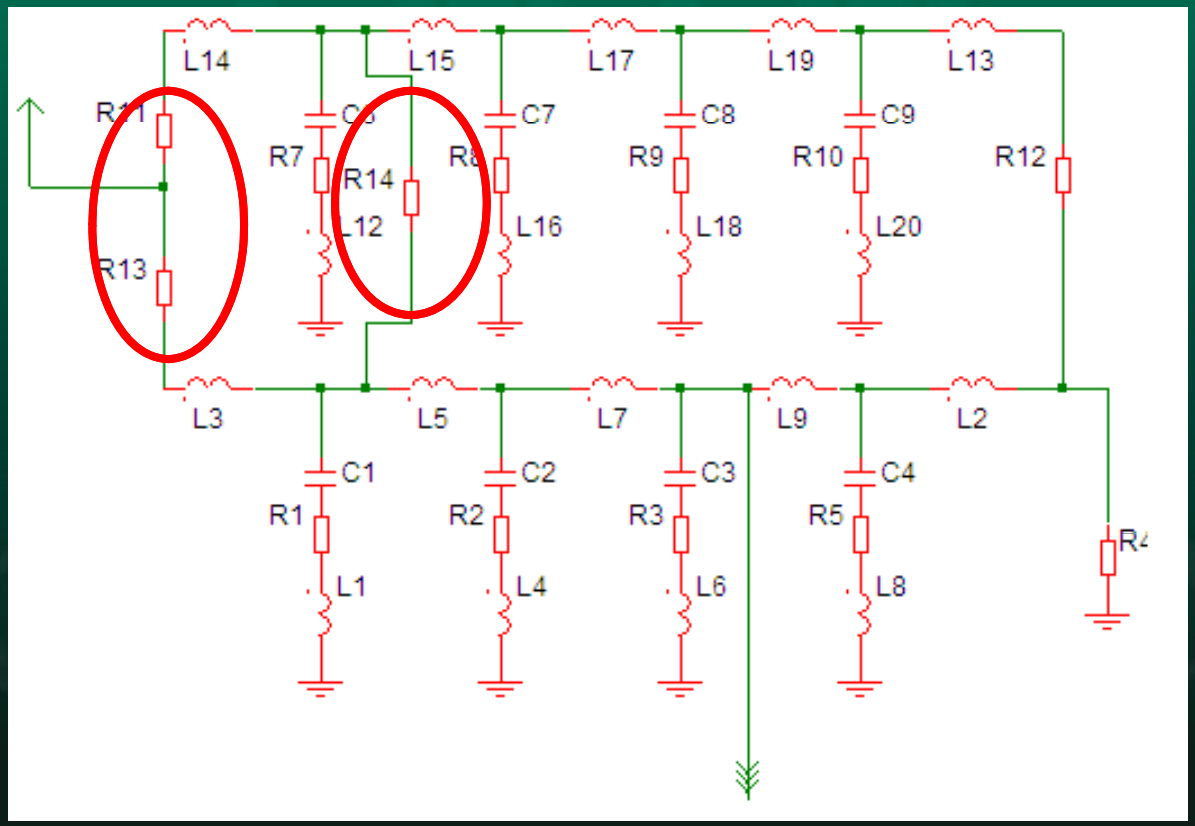
N - 3 capacitors

N - 2 capacitors

N capacitors

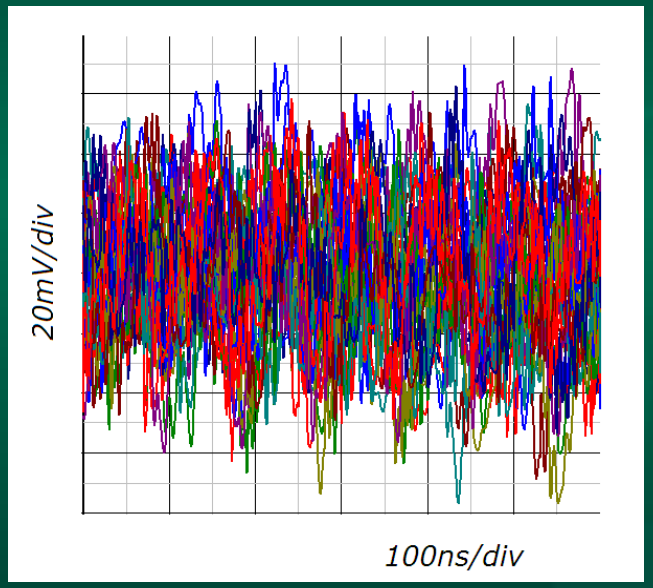
Frequency domain shows shift of peaks to higher values due to effectively lower inductance in resonant circuits

What other effective options are there ? ….



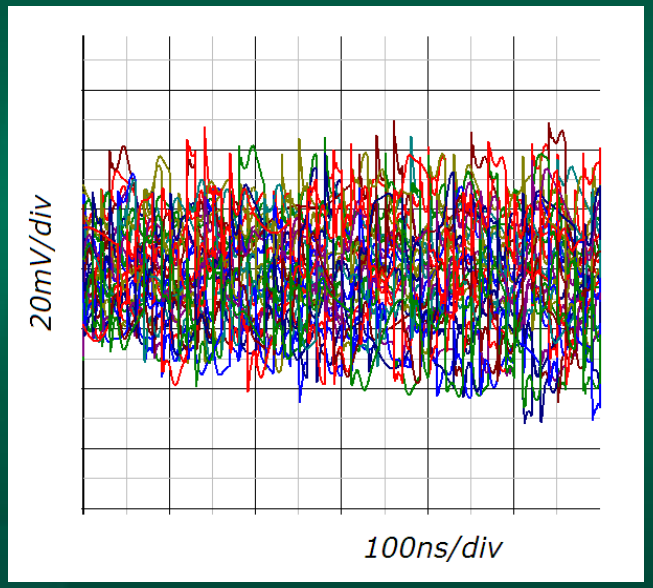
It is possible to add / change resistors

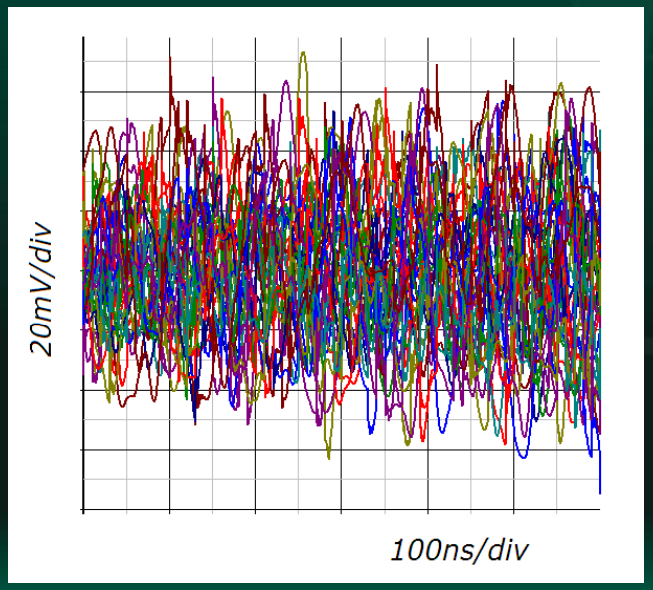
Added R



Original circuit

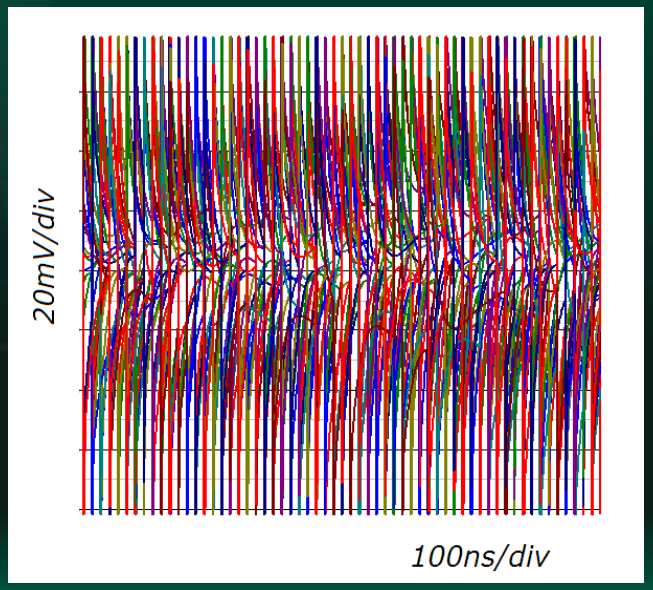
Original circuit + series ‘R’ + shunt ‘R’





Original circuit + series ‘R’

Original circuit +++ series ‘R’ + shunt ‘R’



Conclusion

- Multiple bypass capacitors in probe head, PCB as well as on-die create resonances at multiple frequencies
- Resonances are quite likely within the frequency range of operation
- Noise and crosstalk (into signal paths) performance depend on layout and capacitor placement strategy
- Knowledge of actual performance essential to successful probe card operation in the field
- Improvements possible via capacitance and resistance adjustments and placement. Models must be 3D to predict performance of complex architectures and to accommodate any improvement process.