IEEE SW Test Workshop
Semiconductor Wafer Test Workshop

Testing Probe Cards with Complex Circuits

Bob Davis
Greg Olmstead
Jeff Greenberg

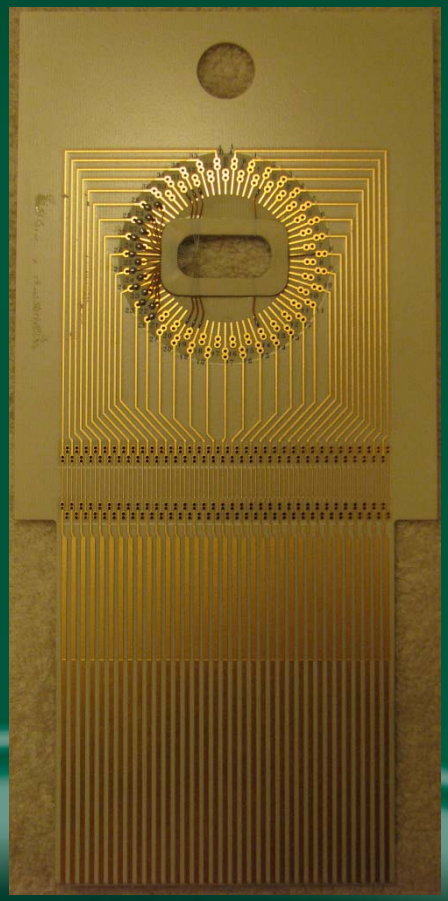
State Based Testing and Design-for-test in a Probe Card Analysis Environment

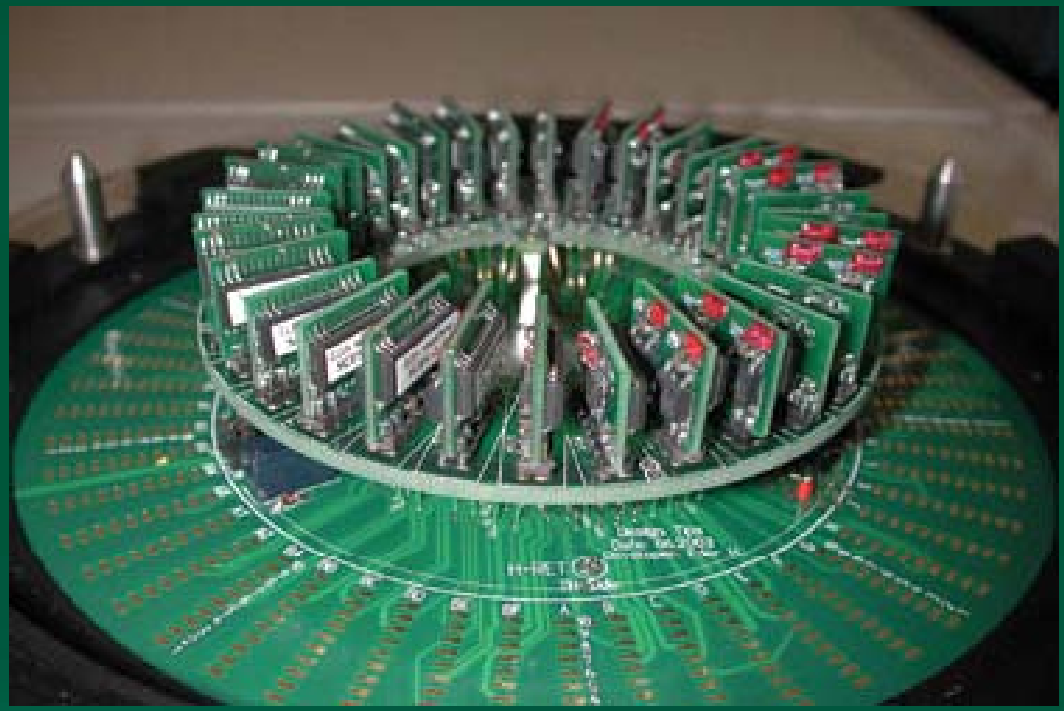
Outline

- **Context** of the Challenge: Circuits on probe cards – designing, producing, validating, and diagnosing
- Extremely abbreviated “History of Complexity Growth”
- **State Based Testing** – a Strategy for Simple Circuit Configuration to enable Probe Card Measurement
- **Tour of Examples:** Probe Card Design For Test(DFT), Configuration and Test Results
- Summary: *State-based PCA capability and PCA-aware DFT maximizes PCA verification of probe cards with increasingly complex circuits, while simplifying the process*

History of Increasing Probe Card Circuit Complexity

Multiple dimensions to these complexity increases…

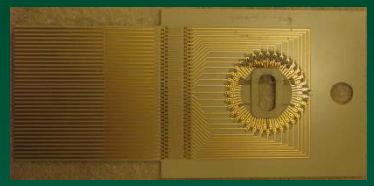




Evaluation Engineering 2006, Courtesy of T.I.P.S.

Probe card circuit complexity increasing

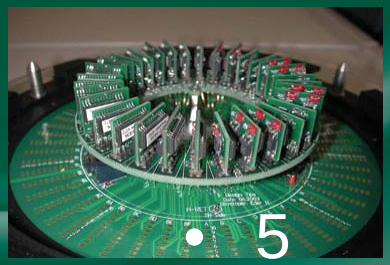
- In the beginning there was the wire…. then
- Basic passive-only circuits
  - Power supply decoupling capacitors



- Relay-switching for passive components
  - In or out of circuit, alternative connection for use in tester or in probe card analyzer
- Relay-switching for probes
  - Extend tester resources, or alternative connections to probes
- Solid-state switching
  - Increased density allows more tester resource extension

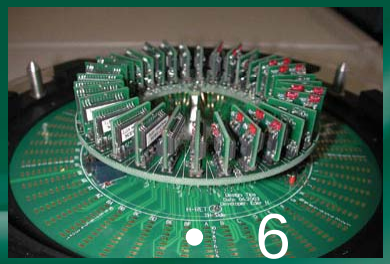
Probe card circuit complexity increasing

- Power distribution, regulation, control, monitoring
  - High speed performance requires local regulation; use few power inputs to probe card with local DC-DC + regulation and bypass capacitance as needed
- Stateful sequential logic to control, monitor, and interact with the design under test and with the tester
  - Local “intelligence” requires less I/O with tester and analyzer in general. Many diverse purposes potentially met via this general approach
- Coincident with huge increases in probe and channel count, probe density, probing forces



Probe Card Test and Analysis

- Measure XYZ positions of probe tips
  - Typically requires DC electrical connection from tester side to probe tip
- Measure electrical properties of probe tips
  - Contact resistance, Leakage current, Capacitance
- Verify wiring
  - From tester side to probe tips
  - From tester side to connections and components
- But …some added PCA functionality and DFT is needed to maintain these capabilities with complex circuits…



Design for Test in Probe Card Analysis

Consider three "phases" of probe card production as verification opportunities:

- **Probe head** – physical probe array without circuit
- **Circuit board** – "classic" electrical test & verification applies, including full electrical test tools.
- **Complete Assembly** – remainder of discussion focuses on this part.

Probe Card Analyzer "State-Based" Testing

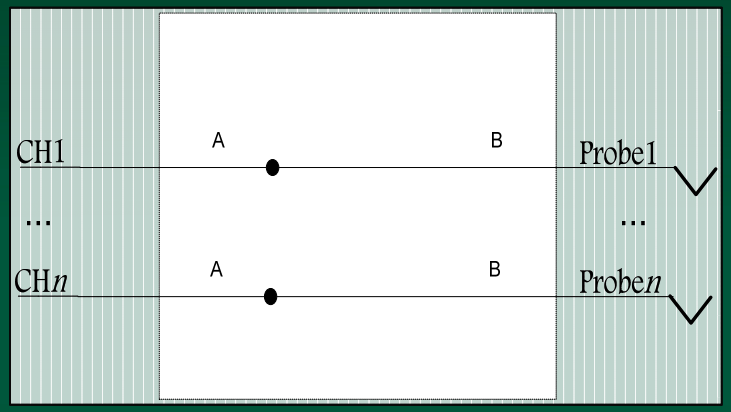
State based testing is simply naming sets of activation details called "States"

These "States" provide connectivity for PCA measurements for particular probes, channels, or components

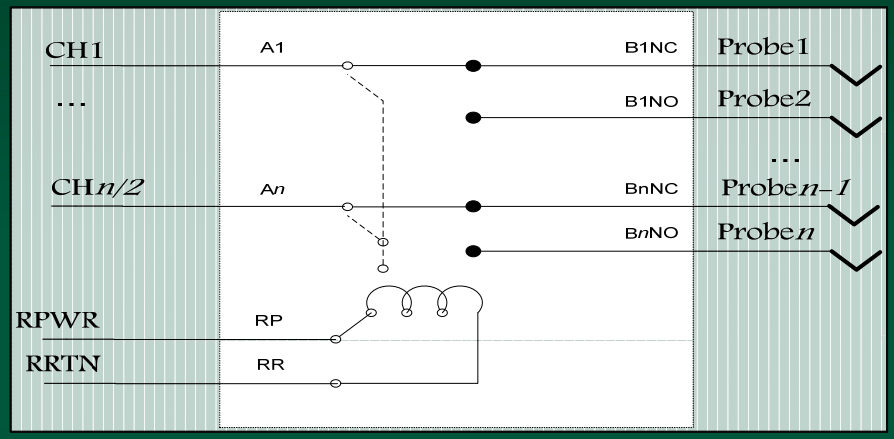
- Designers, their circuits, their users and their testers all understand states of activation
- By naming these in terms of the nodes and details related to them, the PCA can "do what is necessary" while the user gets on with testing the probe card
- States can be as simple or complex as needed; control as little or as much circuitry as indicated by the purposes of the PCA user

Probe Card Analyzer "State-Based" Testing

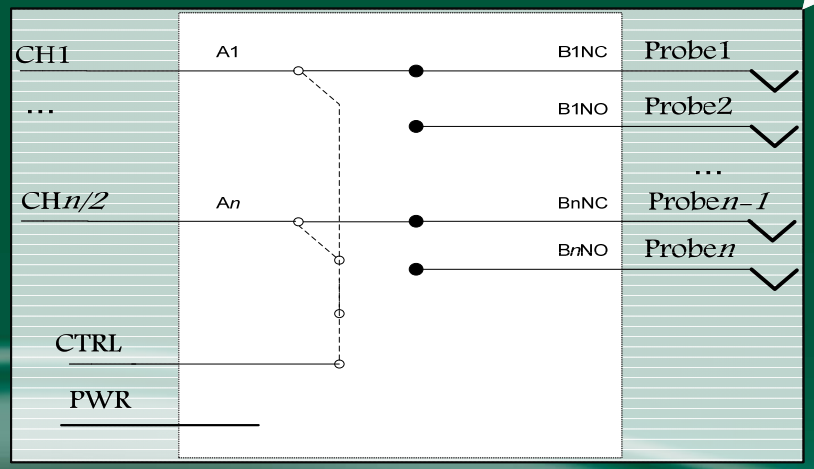
Different *Levels* of Control Complexity



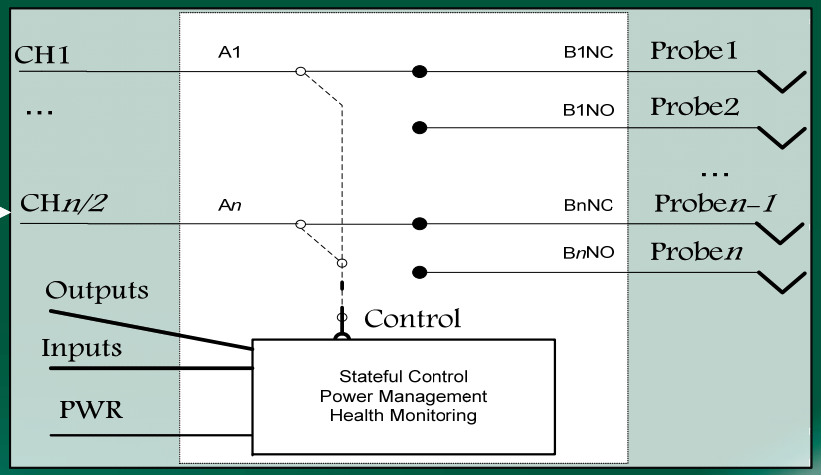
Simple



Relays



(Highly) Configurable

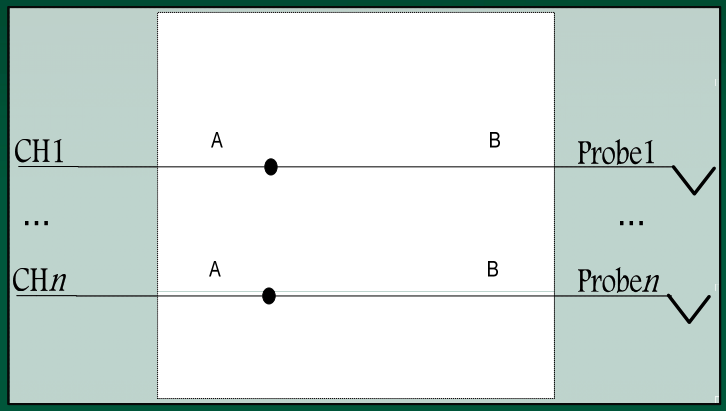


Stateful

Probe Card Analyzer "State-Based" Testing

No control needed

Simple: - no configuration or states required.



Simple

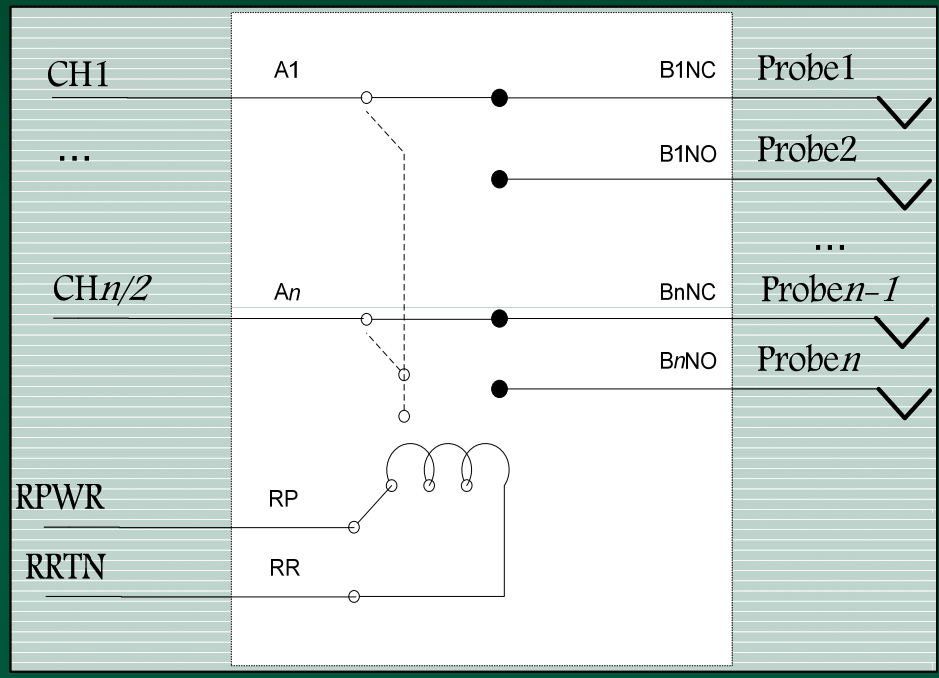
Stays simple; no changes to normal use.

Probe Card Analyzer "State-Based" Testing

Simple Controls

Relays: - state names specify power and control relative to how the relays are connected.

Replaces other, former, means of relay control.

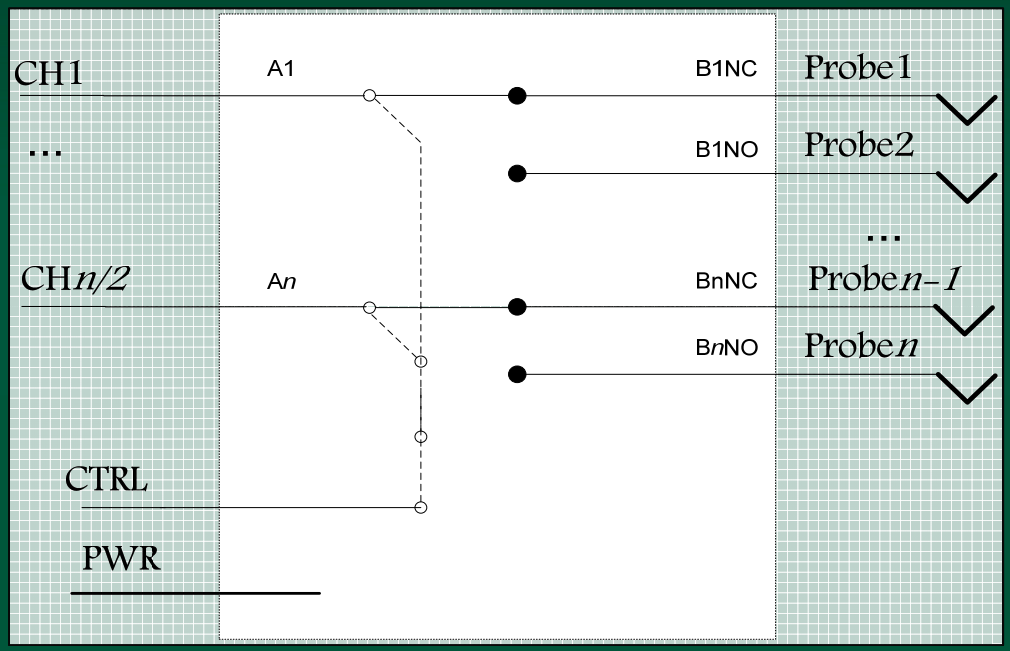


Relays

Probe Card Analyzer "State-Based" Testing

More Complex Controls

Highly Configurable: state names simply define the power, control, and feedback needed for PCA measurements.

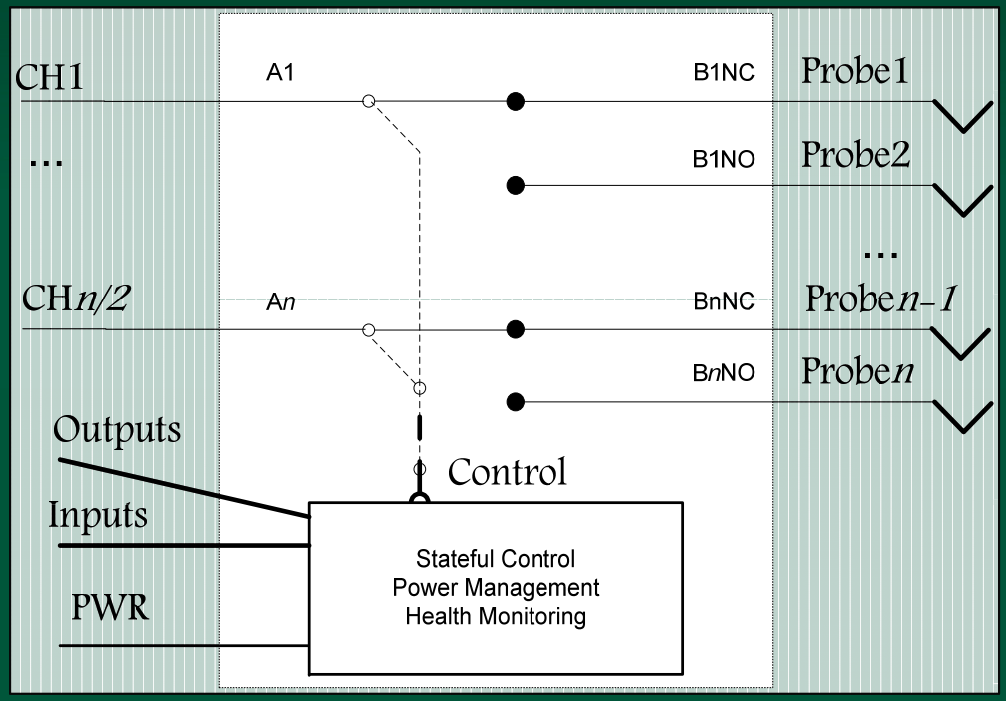


(Highly) Configurable

Probe Card Analyzer "State-Based" Testing

Complex Controls

Stateful: - state names simply define power and control sequences. PCA Interaction with device-under-test implied in control and measurement.



Stateful

Probe Card Analyzer "State-Based" Testing

Defining states in a Probe Card Definition

State Definition | Capacitor | Resistor | Series Capacitor | Series Resistor | Multiple Channel

Total Power/Switch:

	Power: A Channel Label	Power: B Channel Label	Ground Channel Label	Float Channel Label	Delay Time (mSeconds)	State Label
1	5V_UTIL		GND,CTL8,CTL7,CTL6,CTL5,CTL4,CTL3,CTL2,	CTL9,CTL13,CTL12,CTL11,CTL	10	ST_DEFAULT
2	5V_RELAY		CTL11,CTL10	CTL5,CTL1	10	STATE_1
3	5V_RELAY		CTL9,CTL12	CTL7,CTL3	10	STATE_2
4	5V_RELAY		CTL9,CTL13,CTL10		10	STATE_3
5			CTL12,CTL11	CTL6,CTL2,CTL15,CTL14	10	STATE_4
6			CTL13,CTL11	CTL8,CTL4	10	STATE_5
7				CTL9,CTL10	10	STATE_1A

States become just another attribute of the probe card definition of the device under test in the PCA …

Probe Card Analyzer State Based Testing

Using this in the PCA tool…configuration and measurement

Components

State Pre-check | Capacitor | Resistor | Series Capacitor | Series Resistor

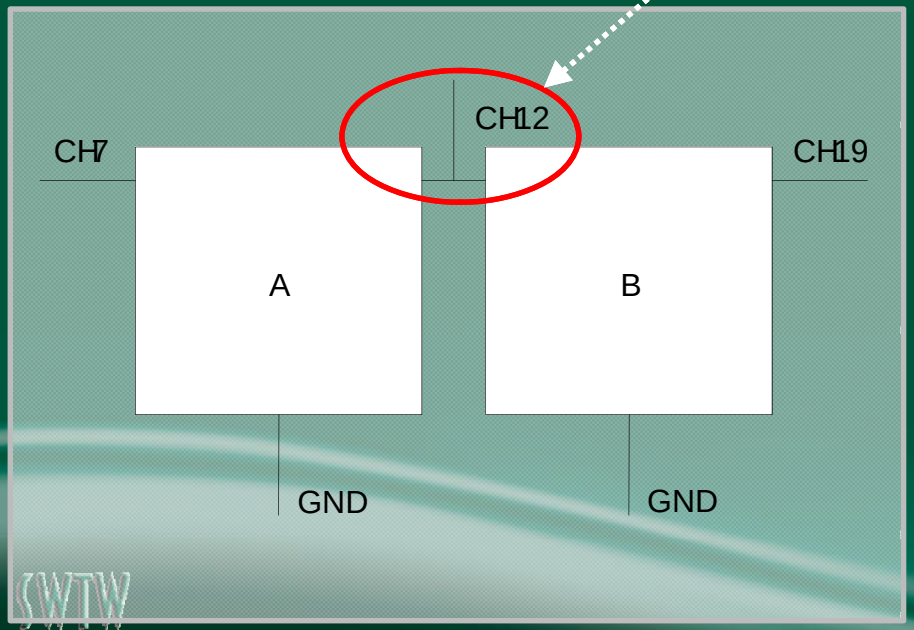
	From : Channel Label	Capacitor (µF)	Measured Capacitor (µF)	Label	To : Channel Label	State Label
14	P126.15	330.000	352.295	C10	GND	
15	P96.2	0.150	0.151	C23*	P96.6	
16	P96.4	0.150	0.150	C24*	P96.6	
17	P96.4	0.150	0.149	C26*	P96.2	
18	PS1	1000.000	1156.960	C28*	GND	
19	PS2	330.000	325.560	C31	GND	
20	PS3	3000.000	3050.960	C21*	GND	
21	PS4	10.000	10.270	C29	GND2	
22	XCH1	0.001	0.001	U2	GND	
23	XCH1	2.200	2.201	U2	GND	STATE_4
24	XCH1	2.200	2.085	U2	GND	STATE_5
25	XCH2	0.001	0.001	U1	GND	
26	XCH2	2.200	2.185	U1	GND	STATE_4
27	XCH2	2.200	2.089	U1	GND	STATE_5
28	XCH6	2.200	2.072	C5	XCH7	
29	XCH6	0.001	0.001	C5	GND	
30	XCH6	2.200	2.153	C5	GND	STATE_4

States shown in results where appropriate.

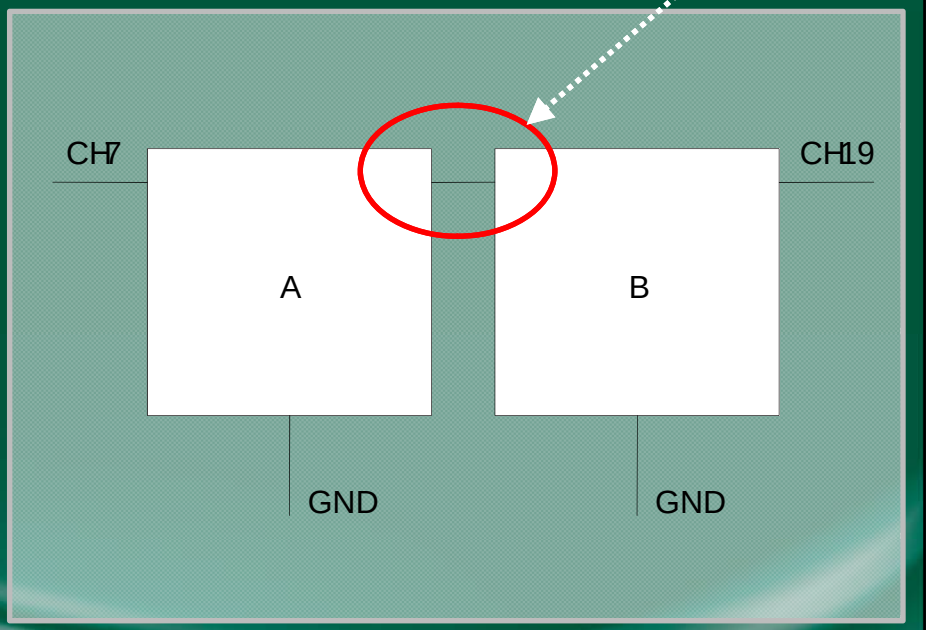
Design for Test in Probe Card Environment

- Expose all essential nodes. Consider adding health feedback for complex cases
- Provide direct DC access to probes in circuit design; OR provide alternate direct access to probes
- Standardize high current traces

Example - Testable



Example – NOT Testable



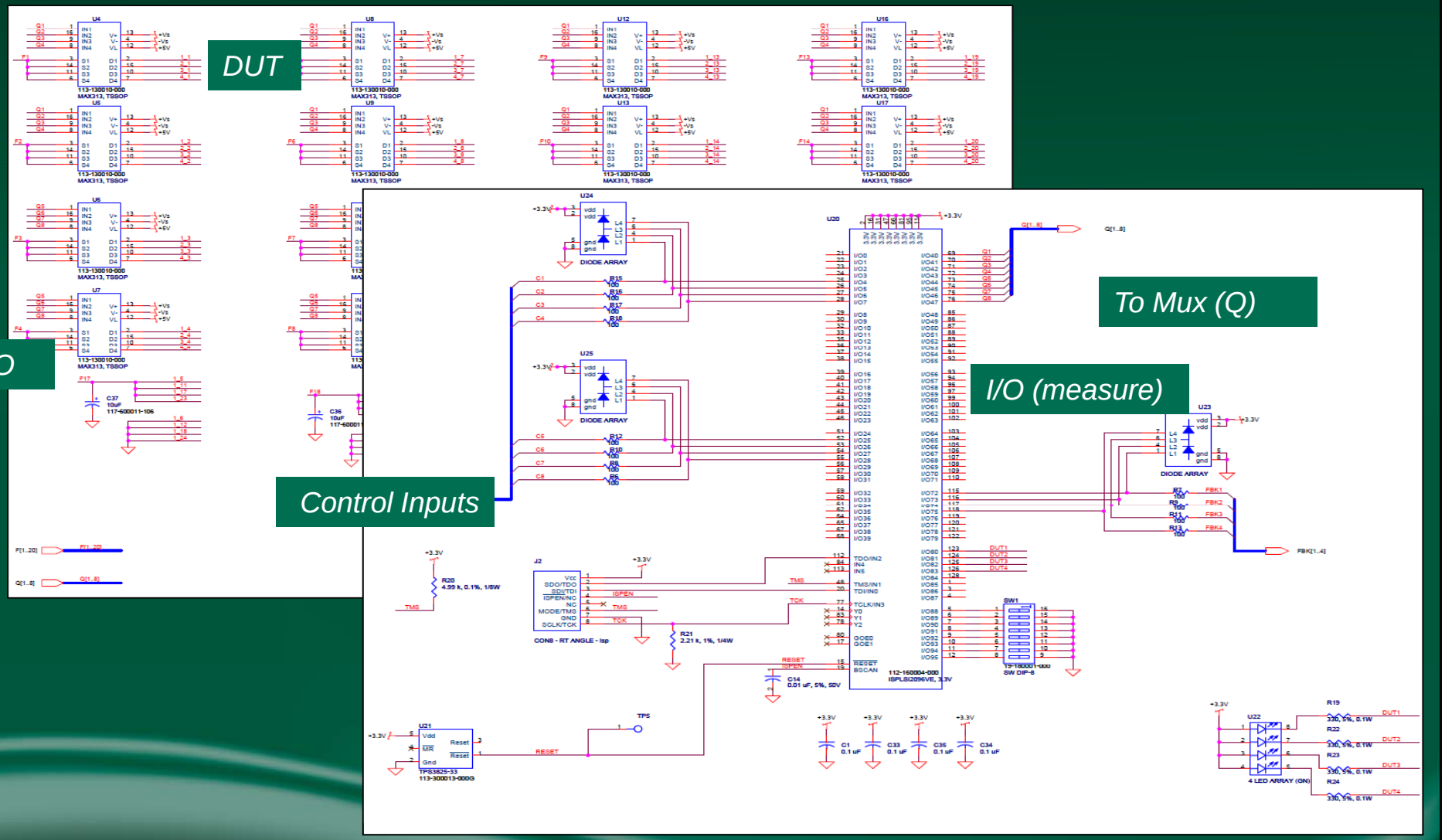
PCA DFT Scenarios and Solutions

For each probe card circuit challenge:

- Challenge and response
- Decompose circuit function
- Identify means of circuit activation in probe-card analyzer (PCA)
- Specify control conditions sufficient to achieve this – activation *states* simplify satisfying the conditions to make the given measurements
- Example PCA measurements and results within this framework

Detailed applications in the following examples.

Test the Probe Card with this Circuit



Don't worry … we'll get there using a sequence of simpler cases.

Challenge: Need more probe connectivity

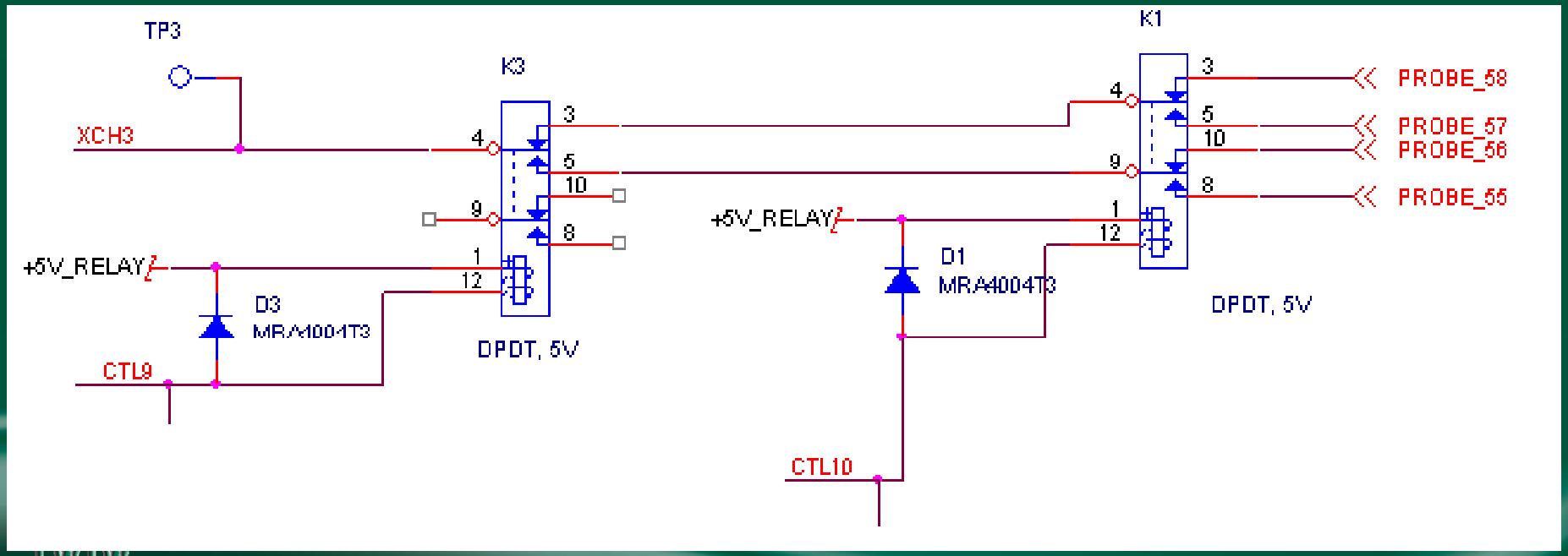
Relay-based probe multiplexing

- Relays control connection to probes, either to increase multiple of probes per channel or to provide alternative connections to probes.
- Low-multiple multiplexing when switching time is not a performance concern, but DC measurement artifacts are a concern.
- Other limitations are density, reliability, and cost.

A familiar case to demonstrate the concepts of state based configuration and measurement.

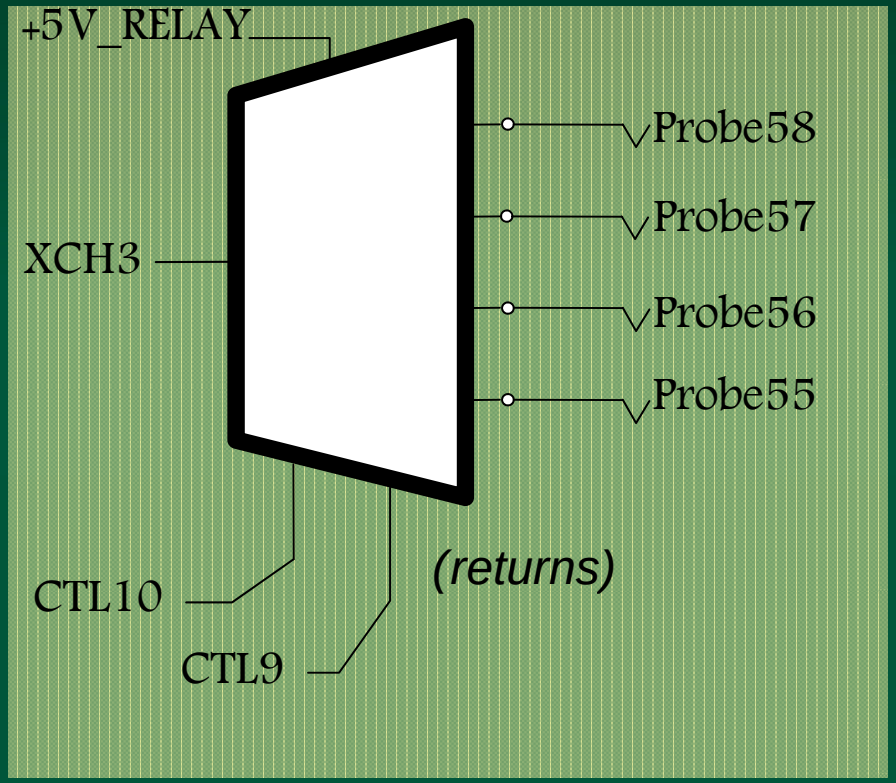
Relay Switching – example circuits

- For this example consider simple probe multiplexer – two levels
- Simple demonstration of means of activation and measurement



Relay Switching – activation and measurement

CTL10	CTL9	connection	state name
open	open	XCH3..Probe58	STATE_P58
return	open	XCH3..Probe57	STATE_P57
open	return	XCH3..Probe56	STATE_P56
return	return	XCH3..Probe55	STATE_P55

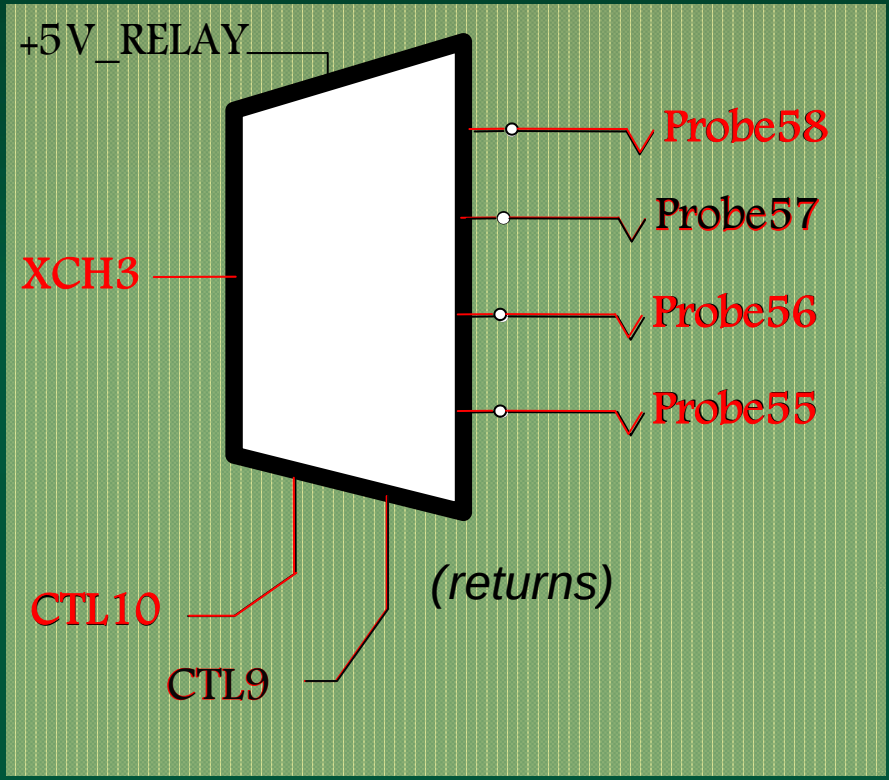


Break down to function and requirements for verification

DFT Note: every edge of controlled connections is reachable or otherwise verifiable

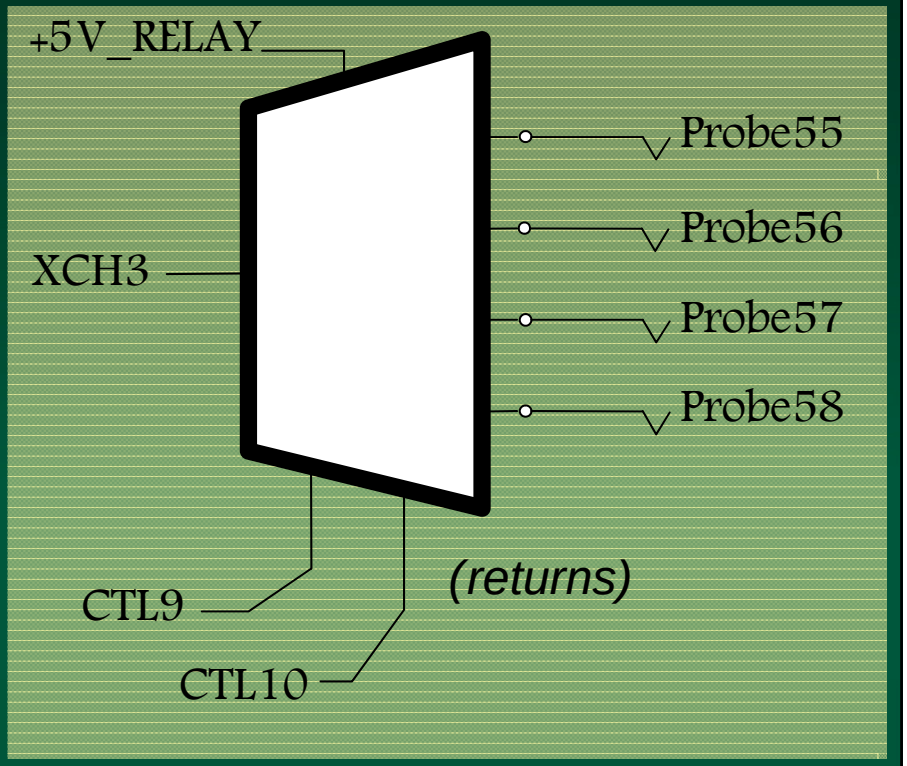
Relay Switching – activation and measurement

CTL10	CTL9	connection	state name
open	open	XCH3..Probe58	STATE_P58
return	open	XCH3..Probe57	STATE_P57
open	return	XCH3..Probe56	STATE_P56
return	**return**	**XCH3..Probe55**	**STATE_P55**



Activating states enables linked controls, desired result

Relay Switching – example results

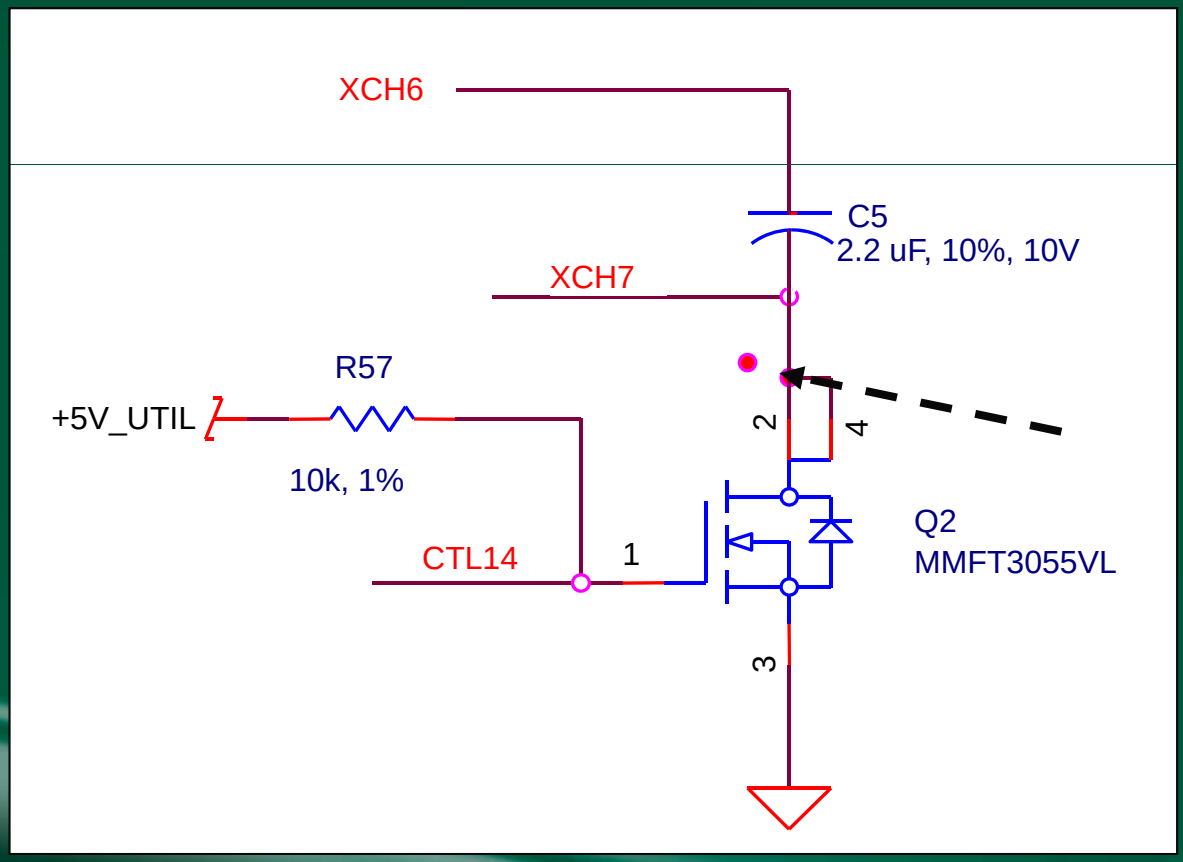


Channel Label	State Label	Probe Label	Primary Channel Res (Ohms)	Primary Channel
XCH3	STATE_P55	Probe55	8.257	Passed
XCH3	STATE_P56	Probe56	8.922	Passed
XCH3	STATE_P57	Probe57	14.061	Passed
XCH3	STATE_P58	Probe58	9.608	Passed

Functional state names make results easily traceable

Challenge: Simple Switching of Components for Validation

Simple circuit to make an important point about testing and diagnosing larger circuits…*exposing nodes to enable verification.*



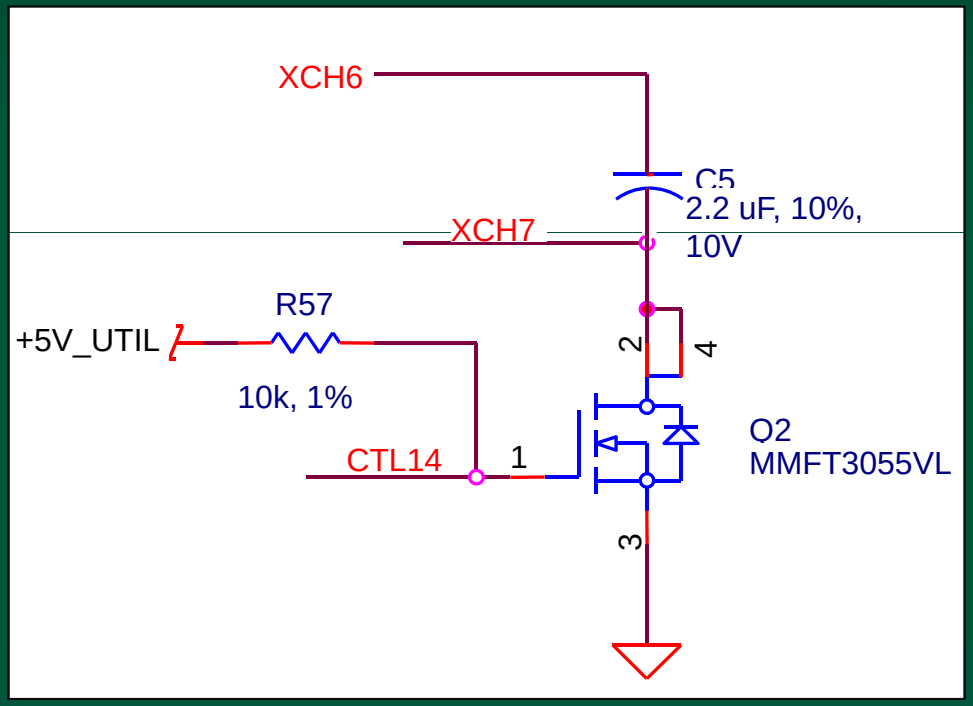
Simple Circuit Switching – example circuit

Simple/minimal component control; *no probes here.*

When CTL14 is logic 1, FET Q2 is closed.

When CTL14 is logic 0, FET Q2 is open.

Cap C5 is removed from the circuit by ST_DEFAULT, but is connected when FET Q2 is on -- State = ST_Q2_ON.



Analysis:

FET switch to control bypass capacitor

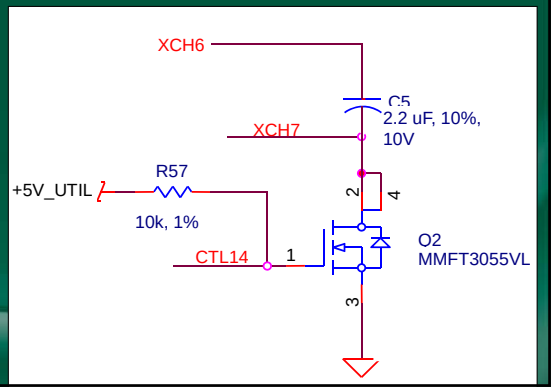
DFT Note: XCH7 allows direct and isolated measurement of C5, and direct and isolated measurement of Q2 drain-source resistance in on and off states.

Simple Circuit Switching – activation and measurement

From : Channel Label	To : Channel Label	State Label	Expected Capacitance (uF)	Measured Capacitance (uF)
XCH6	XCH7	(any)	2.2	2.153
XCH6	GND	ST_Q2_OFF	0.001	0.001
XCH6	GND	ST_Q2_ON	2.2	2.154

From : Channel Label	To : Channel Label	State Label	Expected Resistance (Ohms)	Measured Resistance (Ohms)
XCH7	GND	ST_DEFAULT	open	>40M
XCH7	GND	ST_Q2_ON	1.0	0.231

- **DFT Note:** XCH7 allows direct and isolated measurement of C5, and direct and isolated measurement of Q2 drain-source resistance in on and off states.



Challenge: Arbitrary Configuration of Probes, Components

Configurable - Analog IC Switching

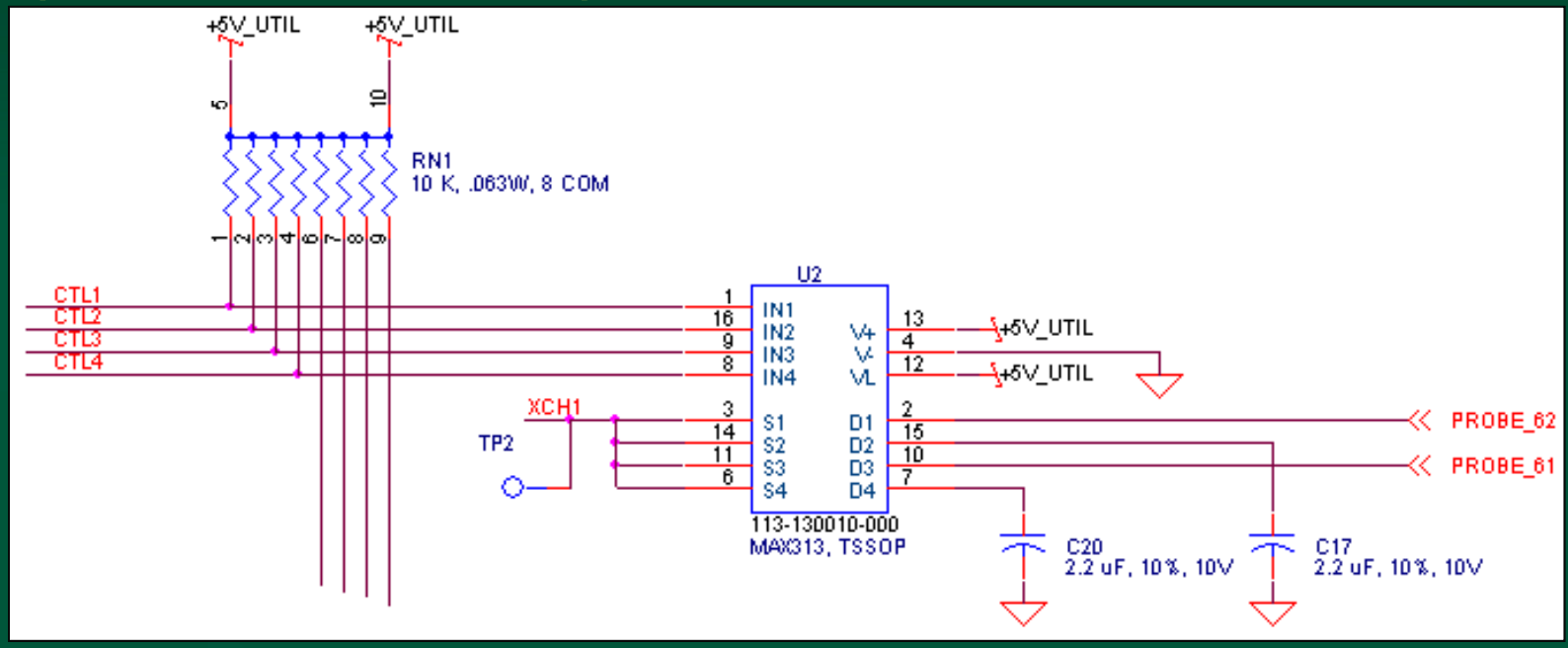
Can be much faster, consume less power, and have greater density than relay-based switching – so in general can be more numerous.

Can present challenges to PCA in terms of shared control returns with other “grounds”, more connections, etc.

Has potential to be configured via on-board logic/state without much “driver overhead” – in that case there are combinations of challenges for the PCA and user.

Analog IC Switching – example circuit

Component control and probe connection control at once.



Analysis:

IC is a quad SPST, normally open, analog switch; pull-ups make on the hardware default.

Switches connect channel XCH1 any of Probe 61, Probe 62, C17, or C20

CTRL lines 1-4 select address these options.

Analog IC Switching – function and states

State Labels

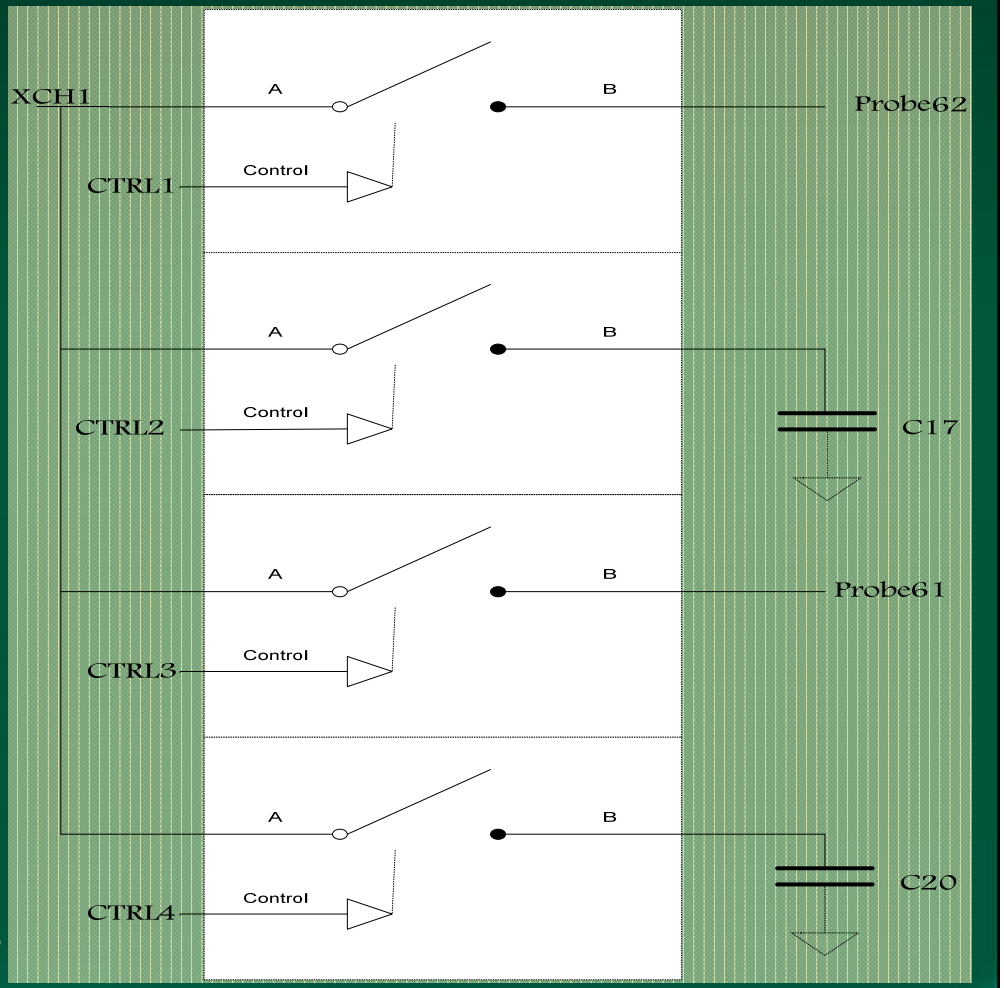
DEFAULT – all switches open (*contrary* to hardware default)

Probe62 – only Probe62 connected

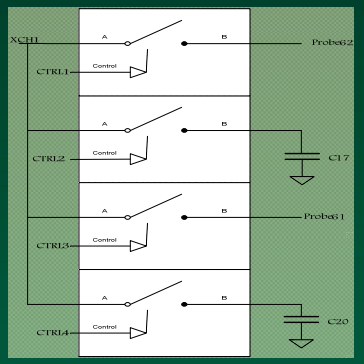
C17 – only capacitor C17 connected

…

Simple mapping provides arbitrary flexibility



Analog IC Switching – activation and measurement



Resistance tests – verify control and proper probe connections

Channel Label	Expected Resistance (Ohms)	Measured Resistor (Ohms)	Probe Label	State Label
XCH1	Open	>40M	PROBE_61	DEFAULT
XCH1	15	22.293	PROBE_61	Probe61
XCH1	Open	>40M	PROBE_62	DEFAULT
XCH1	15	22.641	PROBE_62	Probe62

Capacitance tests – verify control and components functional

From : Channel Label	Expected Capacitance (µF)	Measured Capacitance (µF)	To : Channel Label	State Label
XCH1	0.001	0.001	GND	DEFAULT
XCH1	2.2	2.202	GND	C17
XCH1	2.2	2.082	GND	C20

Validation requirements drive states of control

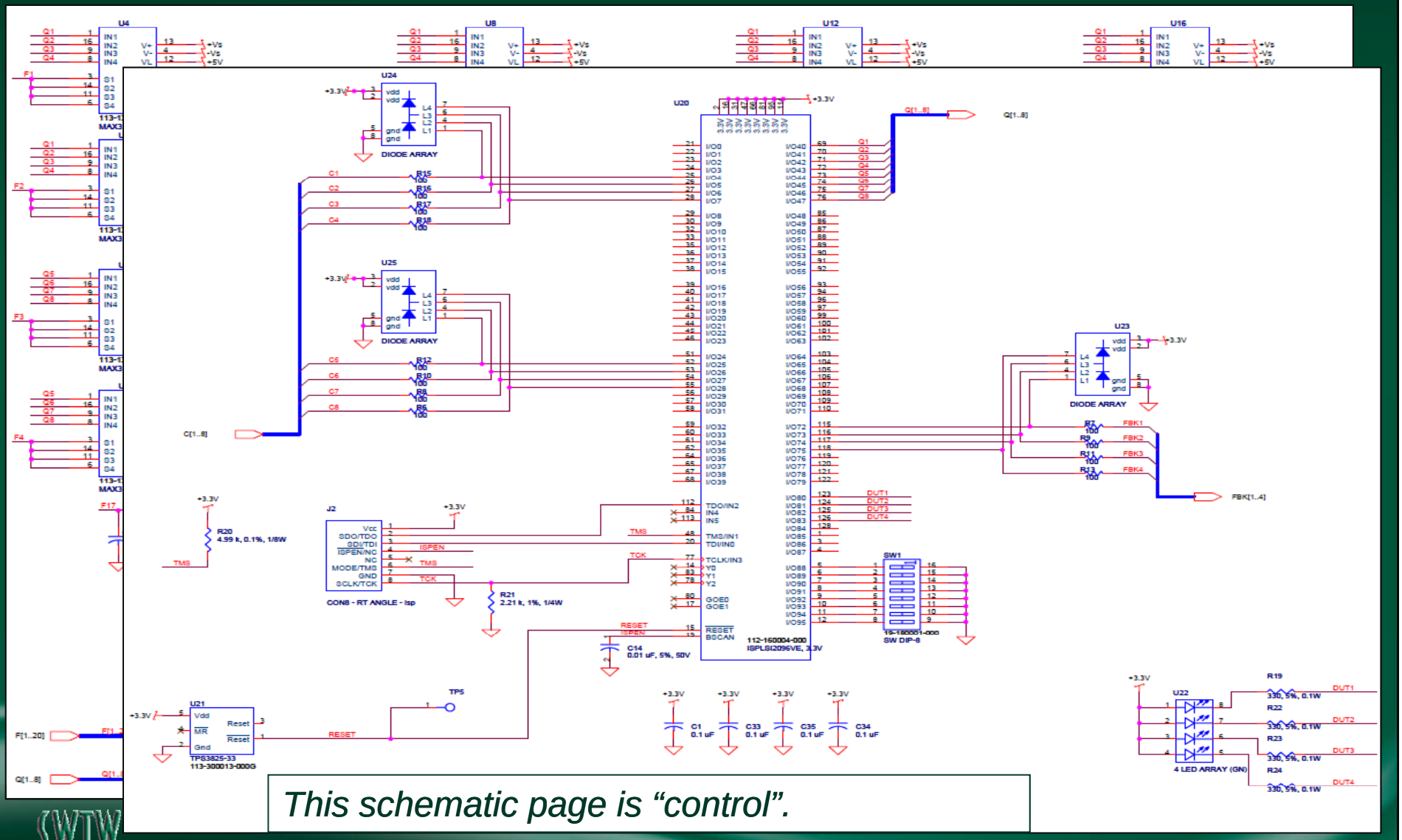
Stateful

(a.k.a. Sequential Logic etc.)

- Satisfies need for “stateful” control or monitoring on the probe card; such as control of switching, power health, identification, verification state
- Activation of this is simplified via a generalization of state-based control – that is, a sequence of control
- Often accompanied by feedback from DUT to PCA (or tester)

Sequential Logic – example circuit

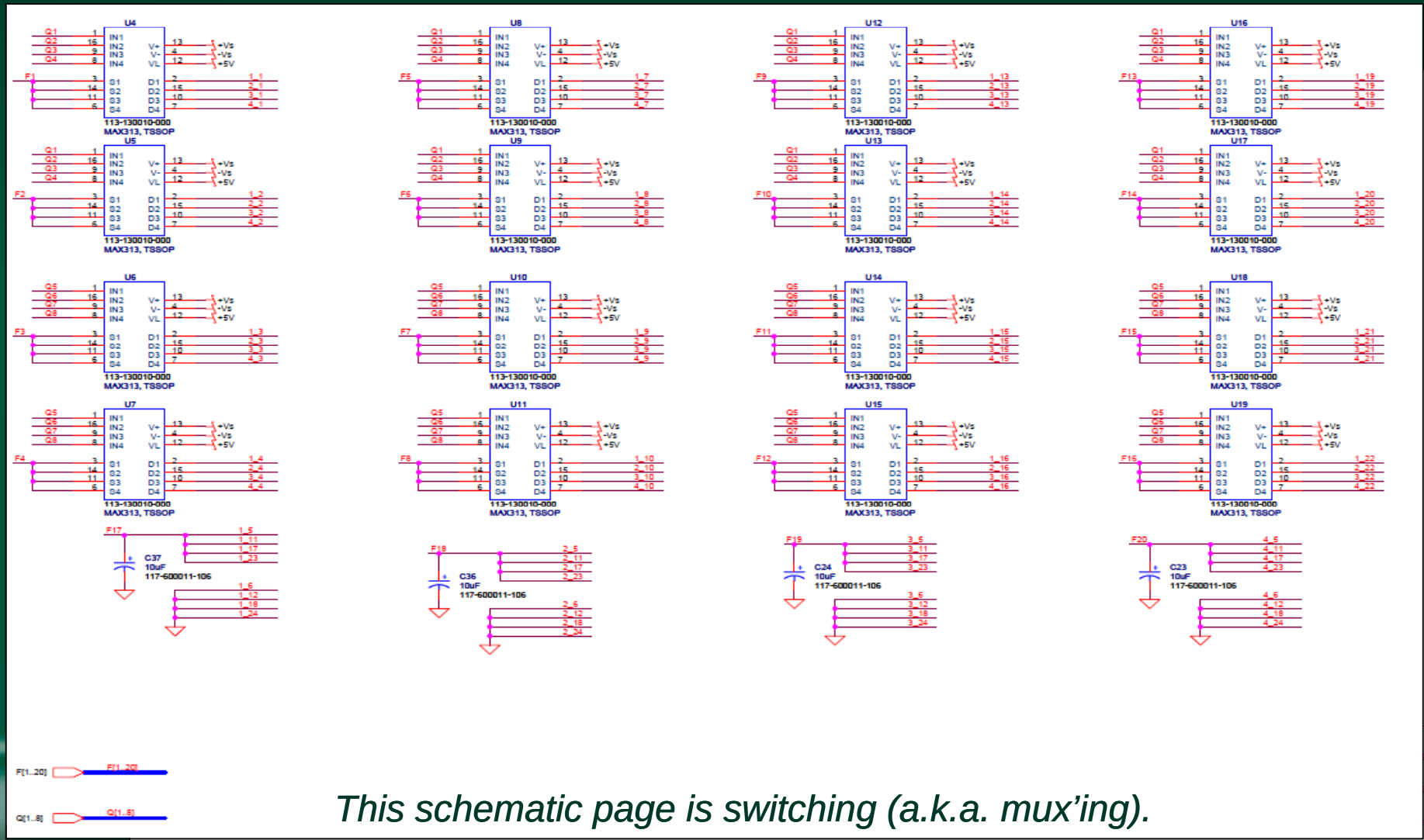
Returning to this “challenge circuit”…



This schematic page is “control”.

Sequential Logic – example circuit

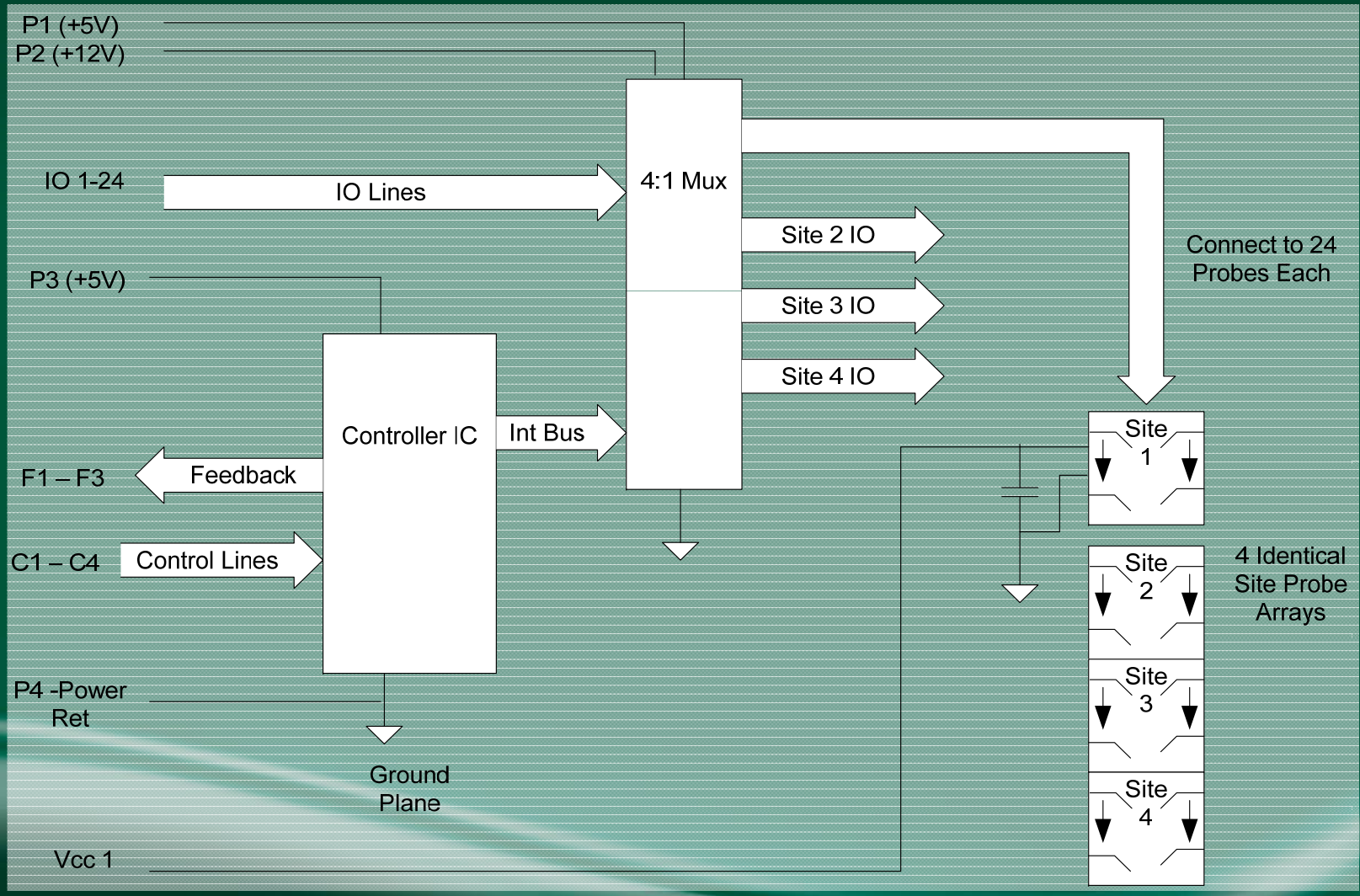
Returning to this “challenge circuit”…



This schematic page is switching (a.k.a. mux’ing).

Sequential Logic – block diagram

Like any other, understanding the functional level…defines test and control needs.

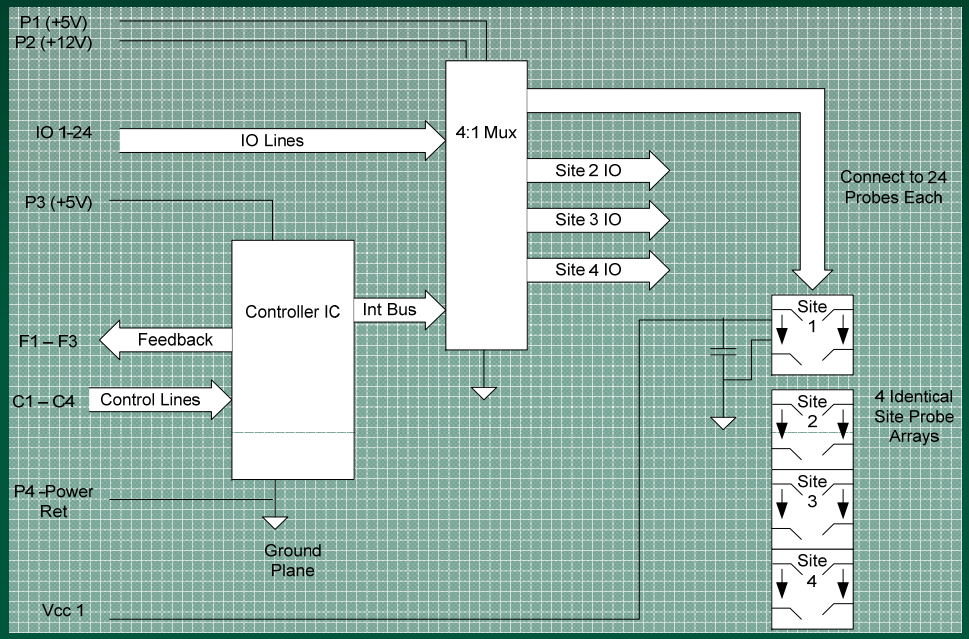


Sequential Logic – notes re test and control

An example of more complex circuits; PCBA will typically have been configured and verified prior to integration into probe card assembly.

Control – more numerous *and may include sequential control schemes*

Feedback – signals returning to tester/PCA give information re health and status.



State definitions allow traditional PCA testing without exposing circuit details.

Provides opportunity to encapsulate intellectual property.

Sequential Logic – Scaling State Based Control

Control States – easily maps to large number of controls

P1	P2	P3	P4	C1	C2	C3	C4	State	Note
5V	12V	5V	GND	GND	GND	GND	GND	Default	IO Not Routed to Any Sites, Only VCC and Gnd
5V	12V	5V	GND	5V	GND	GND	GND	Site 1	24 IO Lines routed to Site 1
5V	12V	5V	GND	GND	5V	GND	GND	Site 2	24 IO Lines routed to Site 2
5V	12V	5V	GND	GND	GND	5V	GND	Site 3	24 IO Lines routed to Site 3
5V	12V	5V	GND	GND	GND	GND	5V	Site 4	24 IO Lines routed to Site 4
5V	12V	5V	GND	5V	5V	5V	5V	Test	Put Controller into Self Test, Look For Feedback

Feedback Sensitivity – PCA *aware* of health and status feedback

F1	F2	F3	Interpretation
0	0	0	No Sites Connected
1	1	1	Self Test Fault
0	0	1	Site 1 Connected
0	1	0	Site 2 Connected
0	1	1	Site 3 Connected
1	0	0	Site 4 Connected

These are used by the PCA to interpret/display feedback results

State Based Testing -- Scalability

Scale easily with probe count, channel count and amount of switching.

Scales easily with amount of control fanout.

Scales to incorporate sequential control.

Scales to incorporate feedback interaction with PCA.

Conclusion

State-based PCA *and* PCA-aware DFT maximizes verification of probe cards with complex circuits, while simplifying the process.

State Based PCA Testing provides a simple, scalable method to enable activation for probe card testing, regardless of complexity.

References

SWTW Papers Having to do with DFT, Complex Probe Cards

Huebner , Michael, "Highest Parallel Test for DRAM Enabled through Advanced TRE", 2009 SWTW.

Huebner ,Michael, "High Speed Control Bus for Advanced TRE", 2010 SWTW.

General Topics Related to DFT & Metrology (much abbreviated)

M. Burns and G. Roberts, ***Introduction to Mixed-Signal IC Test and Measurement,*** New York: Oxford University Press, 2000.

D. Gizopoulos, editor, ***Advances in Electronic Testing Challenges and Methodologies***, Springer, 2006. Chapters 9 and 10.

J. L. Huertas, editor, ***Test and Design-for-Testability in Mixed-Signal Integrated Circuits***, Boston: Springer, 2004.

T. Ozawa, editor***, Analog Methods for Computer-Aided Circuit Analysis and Diagnosis, New York: Marcel Dekker, 1988.***