Testing Probe Cards with Complex Circuits

State Based Testing and Design-for-test in a Probe Card Analysis Environment

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Outline

• **Context** of the Challenge: Circuits on probe cards – designing, producing, validating, and diagnosing

• Extremely abbreviated “History of Complexity Growth”

• **State Based Testing** – a Strategy for Simple Circuit Configuration to enable Probe Card Measurement

• **Tour of Examples:** Probe Card Design For Test(DFT), Configuration and Test Results

• **Summary:** *State-based PCA capability and PCA-aware DFT maximizes PCA verification of probe cards with increasingly complex circuits, while simplifying the process*
History of Increasing Probe Card Circuit Complexity

*Multiple dimensions to these complexity increases...*

Evaluation Engineering 2006, Courtesy of T.I.P.S.
Probe card circuit complexity increasing

- In the beginning there was the wire…. then
- Basic passive-only circuits
  - Power supply decoupling capacitors
- Relay-switching for passive components
  - In or out of circuit, alternative connection for use in tester or in probe card analyzer
- Relay-switching for probes
  - Extend tester resources, or alternative connections to probes
- Solid-state switching
  - Increased density allows more tester resource extension
Probe card circuit complexity increasing

• Power distribution, regulation, control, monitoring
  – High speed performance requires local regulation; use few power inputs to probe card with local DC-DC + regulation and bypass capacitance as needed

• Stateful sequential logic to control, monitor, and interact with the design under test and with the tester
  – Local “intelligence” requires less I/O with tester and analyzer in general. Many diverse purposes potentially met via this general approach

• Coincident with huge increases in probe and channel count, probe density, probing forces
Probe Card Test and Analysis

- Measure XYZ positions of probe tips
  - Typically requires DC electrical connection from tester side to probe tip
- Measure electrical properties of probe tips
  - Contact resistance, Leakage current, Capacitance
- Verify wiring
  - From tester side to probe tips
  - From tester side to connections and components

But ... some added PCA functionality and DFT is needed to maintain these capabilities with complex circuits...
Design for Test in Probe Card Analysis

Consider three “phases” of probe card production as verification opportunities:

• **Probe head** – physical probe array without circuit

• **Circuit board** – “classic” electrical test & verification applies, including full electrical test tools.

• **Complete Assembly** – remainder of discussion focuses on this part.
Probe Card Analyzer “State-Based” Testing

State based testing is simply naming sets of activation details called “States”
These “States” provide connectivity for PCA measurements for particular probes, channels, or components

- Designers, their circuits, their users and their testers all understand states of activation
- By naming these in terms of the nodes and details related to them, the PCA can “do what is necessary” while the user gets on with testing the probe card
- States can be as simple or complex as needed; control as little or as much circuitry as indicated by the purposes of the PCA user
Probe Card Analyzer “State-Based” Testing
Different Levels of Control Complexity

Simple

(Highly) Configurable

Relays

Stateful

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Probe Card Analyzer “State-Based” Testing

No control needed

**Simple**: - no configuration or states required.

Stays simple; no changes to normal use.
Probe Card Analyzer “State-Based” Testing

Simple Controls

Relays: - state names specify power and control relative to how the relays are connected.

Replaces other, former, means of relay control.
Highly Configurable: state names simply define the power, control, and feedback needed for PCA measurements.
Stateful: - state names simply define power and control sequences. PCA Interaction with device-under-test implied in control and measurement.
### Probe Card Analyzer “State-Based” Testing

#### Defining states in a Probe Card Definition

<table>
<thead>
<tr>
<th>State Definition</th>
<th>Capacitor</th>
<th>Resistor</th>
<th>Series Capacitor</th>
<th>Series Resistor</th>
<th>Multiple Channel</th>
</tr>
</thead>
<tbody>
<tr>
<td>Total Power/Switch:</td>
<td>Power: A Channel Label</td>
<td>Power: B Channel Label</td>
<td>Ground Channel Label</td>
<td>Float Channel Label</td>
<td>Delay Time (mSeconds)</td>
</tr>
<tr>
<td>1</td>
<td>5V_UTIL</td>
<td>GND, CTL8, CTL7, CTL6, CTL5, CTL4, CTL3, CTL2,</td>
<td>CTL9, CTL13, CTL12, CTL11, CTL</td>
<td>10</td>
<td>ST_DEFAULT</td>
</tr>
<tr>
<td>2</td>
<td>5V_RELAY</td>
<td>CTL11, CTL10</td>
<td>CTL5, CTL1</td>
<td>10</td>
<td>STATE_1</td>
</tr>
<tr>
<td>3</td>
<td>5V_RELAY</td>
<td>CTL9, CTL12</td>
<td>CTL7, CTL3</td>
<td>10</td>
<td>STATE_2</td>
</tr>
<tr>
<td>4</td>
<td>5V_RELAY</td>
<td>CTL9, CTL13, CTL10</td>
<td>CTL6, CTL2, CTL15, CTL14</td>
<td>10</td>
<td>STATE_3</td>
</tr>
<tr>
<td>5</td>
<td>5V_RELAY</td>
<td>CTL12, CTL11</td>
<td>CTL8, CTL4</td>
<td>10</td>
<td>STATE_4</td>
</tr>
<tr>
<td>6</td>
<td>5V_RELAY</td>
<td>CTL13, CTL11</td>
<td>CTL9, CTL10</td>
<td>10</td>
<td>STATE_5</td>
</tr>
<tr>
<td>7</td>
<td>5V_RELAY</td>
<td>CTL13, CTL11</td>
<td>CTL9, CTL10</td>
<td>10</td>
<td>STATE_1A</td>
</tr>
</tbody>
</table>

States become just another attribute of the probe card definition of the device under test in the PCA …
Probe Card Analyzer State Based Testing

Using this in the PCA tool...configuration and measurement

States shown in results where appropriate.

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Design for Test in Probe Card Environment

- Expose all essential nodes. Consider adding health feedback for complex cases
- Provide direct DC access to probes in circuit design; OR provide alternate direct access to probes
- Standardize high current traces

**Example - Testable**

**Example – NOT Testable**
PCA DFT Scenarios and Solutions

For each probe card circuit challenge:

- Challenge and response
- Decompose circuit function
- Identify means of circuit activation in probe-card analyzer (PCA)
- Specify control conditions sufficient to achieve this – activation states simplify satisfying the conditions to make the given measurements
- Example PCA measurements and results within this framework

*Detailed applications in the following examples.*
Test the Probe Card with this Circuit

Don’t worry … we’ll get there using a sequence of simpler cases.

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Challenge: Need more probe connectivity

Relay-based probe multiplexing

- Relays control connection to probes, either to increase multiple of probes per channel or to provide alternative connections to probes.
- Low-multiple multiplexing when switching time is not a performance concern, but DC measurement artifacts are a concern.
- Other limitations are density, reliability, and cost.

A familiar case to demonstrate the concepts of state based configuration and measurement.
Relay Switching – example circuits

- For this example consider simple probe multiplexer – two levels
- Simple demonstration of means of activation and measurement
### Relay Switching – activation and measurement

<table>
<thead>
<tr>
<th>CTL10</th>
<th>CTL9</th>
<th>connection</th>
<th>state name</th>
</tr>
</thead>
<tbody>
<tr>
<td>open</td>
<td>open</td>
<td>XCH3..Probe58</td>
<td>STATE_P58</td>
</tr>
<tr>
<td>return</td>
<td>open</td>
<td>XCH3..Probe57</td>
<td>STATE_P57</td>
</tr>
<tr>
<td>open</td>
<td>return</td>
<td>XCH3..Probe56</td>
<td>STATE_P56</td>
</tr>
<tr>
<td>return</td>
<td>return</td>
<td>XCH3..Probe55</td>
<td>STATE_P55</td>
</tr>
</tbody>
</table>

#### Break down to function and requirements for verification

**DFT Note:** every edge of controlled connections is reachable or otherwise verifiable.

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Activating states enables linked controls, desired result
## Relay Switching – example results

### Table: Channel Test Results

<table>
<thead>
<tr>
<th>Channel Label</th>
<th>State Label</th>
<th>Probe Label</th>
<th>Primary Channel Res (Ohms)</th>
<th>Primary Channel</th>
</tr>
</thead>
<tbody>
<tr>
<td>XCH3</td>
<td>STATE_P55</td>
<td>Probe55</td>
<td>8.257</td>
<td>Passed</td>
</tr>
<tr>
<td>XCH3</td>
<td>STATE_P56</td>
<td>Probe56</td>
<td>8.922</td>
<td>Passed</td>
</tr>
<tr>
<td>XCH3</td>
<td>STATE_P57</td>
<td>Probe57</td>
<td>14.061</td>
<td>Passed</td>
</tr>
<tr>
<td>XCH3</td>
<td>STATE_P58</td>
<td>Probe58</td>
<td>9.608</td>
<td>Passed</td>
</tr>
</tbody>
</table>

Functional state names make results easily traceable.
Challenge: Simple Switching of Components for Validation

Simple circuit to make an important point about testing and diagnosing larger circuits...exposing nodes to enable verification.

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Simple Circuit Switching – example circuit

Simple/minimal component control; no probes here.

When CTL14 is logic 1, FET Q2 is closed. When CTL14 is logic 0, FET Q2 is open.

Cap C5 is removed from the circuit by ST_DEFAULT, but is connected when FET Q2 is on -- State = ST_Q2_ON.

Analysis:
FET switch to control bypass capacitor

DFT Note: XCH7 allows direct and isolated measurement of C5, and direct and isolated measurement of Q2 drain-source resistance in on and off states.
### Simple Circuit Switching – activation and measurement

<table>
<thead>
<tr>
<th>From : Channel Label</th>
<th>To : Channel Label</th>
<th>State Label</th>
<th>Expected Capacitance (uF)</th>
<th>Measured Capacitance (uF)</th>
</tr>
</thead>
<tbody>
<tr>
<td>XCH6</td>
<td>XCH7</td>
<td>(any)</td>
<td>2.2</td>
<td>2.153</td>
</tr>
<tr>
<td>XCH6</td>
<td>GND</td>
<td>ST_Q2_OFF</td>
<td>0.001</td>
<td>0.001</td>
</tr>
<tr>
<td>XCH6</td>
<td>GND</td>
<td>ST_Q2_ON</td>
<td>2.2</td>
<td>2.154</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>From : Channel Label</th>
<th>To : Channel Label</th>
<th>State Label</th>
<th>Expected Resistance (Ohms)</th>
<th>Measured Resistance (Ohms)</th>
</tr>
</thead>
<tbody>
<tr>
<td>XCH7</td>
<td>GND</td>
<td>ST_DEFAULT</td>
<td>open</td>
<td>&gt;40M</td>
</tr>
<tr>
<td>XCH7</td>
<td>GND</td>
<td>ST_Q2_ON</td>
<td>1.0</td>
<td>0.231</td>
</tr>
</tbody>
</table>

**DFT Note:** XCH7 allows direct and isolated measurement of C5, and direct and isolated measurement of Q2 drain-source resistance in on and off states.

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Challenge: Arbitrary Configuration of Probes, Components

Configurable - Analog IC Switching

Can be much faster, consume less power, and have greater density than relay-based switching – so in general can be more numerous.

Can present challenges to PCA in terms of shared control returns with other “grounds”, more connections, etc.

Has potential to be configured via on-board logic/state without much “driver overhead” – in that case there are combinations of challenges for the PCA and user.
Analog IC Switching – example circuit

Component control and probe connection control at once.

Analysis:
IC is a quad SPST, normally open, analog switch; pull-ups make on the hardware default.

Switches connect channel XCH1 any of Probe 61, Probe 62, C17, or C20

CTRL lines 1-4 select address these options.
Analog IC Switching – function and states

State Labels

**DEFAULT** – all switches open *(contrary to hardware default)*

**Probe62** – only Probe62 connected

**C17** – only capacitor C17 connected

…

Simple mapping provides arbitrary flexibility
Analog IC Switching – activation and measurement

**Resistance** tests – verify control and proper probe connections

<table>
<thead>
<tr>
<th>Channel Label</th>
<th>Expected Resistance (Ohms)</th>
<th>Measured Resistor (Ohms)</th>
<th>Probe Label</th>
<th>State Label</th>
</tr>
</thead>
<tbody>
<tr>
<td>XCH1</td>
<td>Open</td>
<td>&gt;40M</td>
<td>PROBE_61</td>
<td>DEFAULT</td>
</tr>
<tr>
<td>XCH1</td>
<td>15</td>
<td>22.293</td>
<td>PROBE_61</td>
<td>Probe61</td>
</tr>
<tr>
<td>XCH1</td>
<td>Open</td>
<td>&gt;40M</td>
<td>PROBE_62</td>
<td>DEFAULT</td>
</tr>
<tr>
<td>XCH1</td>
<td>15</td>
<td>22.641</td>
<td>PROBE_62</td>
<td>Probe62</td>
</tr>
</tbody>
</table>

**Capacitance** tests – verify control and components functional

<table>
<thead>
<tr>
<th>From : Channel Label</th>
<th>Expected Capacitance (µF)</th>
<th>Measured Capacitance (µF)</th>
<th>To : Channel Label</th>
<th>State Label</th>
</tr>
</thead>
<tbody>
<tr>
<td>XCH1</td>
<td>0.001</td>
<td>0.001</td>
<td>GND</td>
<td>DEFAULT</td>
</tr>
<tr>
<td>XCH1</td>
<td>2.2</td>
<td>2.202</td>
<td>GND</td>
<td>C17</td>
</tr>
<tr>
<td>XCH1</td>
<td>2.2</td>
<td>2.082</td>
<td>GND</td>
<td>C20</td>
</tr>
</tbody>
</table>

Validation requirements drive states of control
Stateful
(a.k.a. Sequential Logic etc.)

• Satisfies need for “stateful” control or monitoring on the probe card; such as control of switching, power health, identification, verification state.

• Activation of this is simplified via a generalization of state-based control – that is, a sequence of control.

• Often accompanied by feedback from DUT to PCA (or tester).
Sequential Logic – example circuit

Returning to this “challenge circuit”…

This schematic page is “control”.

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Sequential Logic – example circuit

Returning to this “challenge circuit”…

This schematic page is switching (a.k.a. mux’ing).
Sequential Logic – block diagram

Like any other, understanding the functional level...defines test and control needs.
Sequential Logic – notes re test and control

An example of more complex circuits; PCBA will typically have been configured and verified prior to integration into probe card assembly.

Control – more numerous and may include sequential control schemes

Feedback – signals returning to tester/PCA give information re health and status.

State definitions allow traditional PCA testing without exposing circuit details.

Provides opportunity to encapsulate intellectual property.

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## Sequential Logic – Scaling State Based Control

**Control States** – easily maps to large number of controls

<table>
<thead>
<tr>
<th>P1</th>
<th>P2</th>
<th>P3</th>
<th>P4</th>
<th>C1</th>
<th>C2</th>
<th>C3</th>
<th>C4</th>
<th>State</th>
<th>Note</th>
</tr>
</thead>
<tbody>
<tr>
<td>5V</td>
<td>12V</td>
<td>5V</td>
<td>GND</td>
<td>GND</td>
<td>GND</td>
<td>GND</td>
<td>GND</td>
<td>Default</td>
<td>IO Not Routed to Any Sites, Only VCC and Gnd</td>
</tr>
<tr>
<td>5V</td>
<td>12V</td>
<td>5V</td>
<td>GND</td>
<td>5V</td>
<td>GND</td>
<td>GND</td>
<td>GND</td>
<td>Site 1</td>
<td>24 IO Lines routed to Site 1</td>
</tr>
<tr>
<td>5V</td>
<td>12V</td>
<td>5V</td>
<td>GND</td>
<td>GND</td>
<td>5V</td>
<td>GND</td>
<td>GND</td>
<td>Site 2</td>
<td>24 IO Lines routed to Site 2</td>
</tr>
<tr>
<td>5V</td>
<td>12V</td>
<td>5V</td>
<td>GND</td>
<td>GND</td>
<td>GND</td>
<td>5V</td>
<td>GND</td>
<td>Site 3</td>
<td>24 IO Lines routed to Site 3</td>
</tr>
<tr>
<td>5V</td>
<td>12V</td>
<td>5V</td>
<td>GND</td>
<td>GND</td>
<td>GND</td>
<td>GND</td>
<td>5V</td>
<td>Site 4</td>
<td>24 IO Lines routed to Site 4</td>
</tr>
<tr>
<td>5V</td>
<td>12V</td>
<td>5V</td>
<td>GND</td>
<td>5V</td>
<td>5V</td>
<td>5V</td>
<td>5V</td>
<td>Test</td>
<td>Put Controller into Self Test, Look For Feedback</td>
</tr>
</tbody>
</table>

**Feedback Sensitivity** – PCA aware of health and status feedback

<table>
<thead>
<tr>
<th>F1</th>
<th>F2</th>
<th>F3</th>
<th>Interpretation</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>No Sites Connected</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>Self Test Fault</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>Site 1 Connected</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>Site 2 Connected</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>Site 3 Connected</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>Site 4 Connected</td>
</tr>
</tbody>
</table>

*These are used by the PCA to interpret/display feedback results*

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State Based Testing -- Scalability

Scale easily with probe count, channel count and amount of switching.

Scales easily with amount of control fanout.

Scales to incorporate sequential control.

Scales to incorporate feedback interaction with PCA.
Conclusion

State-based PCA and PCA-aware DFT maximizes verification of probe cards with complex circuits, while simplifying the process.

State Based PCA Testing provides a simple, scalable method to enable activation for probe card testing, regardless of complexity.
SWTW Papers Having to do with DFT, Complex Probe Cards

Huebner, Michael, "Highest Parallel Test for DRAM Enabled through Advanced TRE", 2009 SWTW.

Huebner, Michael, "High Speed Control Bus for Advanced TRE", 2010 SWTW.

General Topics Related to DFT & Metrology (much abbreviated)


