Wafer Probing on Fine-Pitch Micro-Bumps for 2.5D- and 3D-SICs

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Presentation Outline

1. Introduction to TSV-Based 2.5D- and 3D-SICs
2. Test Challenges
3. Probing on Fine-Pitch Micro-Bumps
4. Experimental Results
5. Conclusion
1. Introduction to TSV-Based 2.5D- and 3D-SICs

**TSVs: Through-Silicon Vias**

- **TSV**
  - Conducting nail; typically Cu or W
  - Electrical path from front-side to back-side of thinned-down silicon wafer
  - Interconnection of vertically stacked dies

- **Typical TSV Dimensions**
  - Diameter : 5µm
  - Height : 50µm
  - Min. pitch : 10µm
  
  Aspect Ratio 1:10

- **Benefits over Wire-Bonds**
  - High density
  - Low capacitance
  - Result: improved bandwidth, performance, power dissipation
1. Introduction to TSV-Based 2.5D- and 3D-SICs

TSV Manufacturing

1. TSV Fabrication

- deep silicon etching
- via oxide deposition
- Cu seed deposition
- Cu plating
- CMP

2. Wafer Thinning and Bonding

- temporary carrier bonding
- back-side thinning
- expose Cu nails
- permanent bonding
- temporary carrier de-bonding
1. Introduction to TSV-Based 2.5D- and 3D-SICs

Die Stacking

Endless Stacking Opportunities
“Whatever your children can make using Lego bricks”

• 3D-SIC

• 2½D-SIC

• 2½D + 3D = 5½D-SIC
1. Introduction to TSV-Based 2.5D- and 3D-SICs

**Micro-Bump Bonding**

**Electroplated Micro-Bumps**
- Cylindrical bumps
  - Side1: Cu (5μm)
  - Side2: CuSn (5μm + 3.5μm)
- Size (scaling down!)
  - Diameter: 25μm
  - Pitch: 40μm

**Bonding**
- Transient-Liquid Phase (250 °C)
- Diffusion bonding (150 °C)
- Bump planarization
1. Introduction to TSV-Based 2.5D- and 3D-SICs

Micro-Bump Bonding
Demonstration of high yield collective CuSn bonding
2. Test Challenges

Test Challenges – Overview

1. 3D Test Flows
   What to test when?

2. 3D Test Contents
   New test patterns to cover new defects
   2A. Due to 3D processing steps
   2B. Due to TSV-based interconnects

3. 3D Test Access
   Pumping stimuli in/responses out of the DUT
   3A. External: Wafer probing
   3B. Internal : Design-for-Test

[Marinissen – APCCAS’10]
2. Test Challenges

**Challenge 1: 3D Test Flows**

Potential Test Moments:

- **Pre-Bond Test**
  - Content: die (+ TSVs)
  - Access: wafer probe

- **Mid- and Post-Bond Test**
  - Content: interconnects (+ dies)
  - Access: wafer probe + DfT

- **Final Test**
  - Content: dies + interconnects
  - Access: socket + DfT

- Many more natural wafer test moments
- Pre-Bond and Post-Bond tests are distinctly different in test access
- Disintegrated production flow more likely: KGD / KGS testing
- Integrated flow: test benefits need to exceed costs $\Rightarrow$ cost modeling

[Taouil et al. - ATS’10]
2. Test Challenges

Challenge 2: 3D Test Contents

- All manufacturing defects that can occur in conventional 2D chips, can also occur in 3D-SICs
  - Logic: stuck-at, transition, delay, VLV, ...
  - Memory: array, decoder, control, data-lines, ...
  - Analog: INL, THD, ...

- New defects due to new 3D processing steps
  - Wafer thinning: shifts in device performance
    [Ikeda et al. – ICMTS’04] [Perry et al. – DATE’09 3D Workshop]
  - Thermal dissipation and thermo-mechanical stress
  - Yield loss

- Defects in TSV-based interconnects
  - TSV fabrication: liner, barrier, plating
  - Interconnect bonding: height, align
2. Test Challenges

Challenge 3: Test Access

Wafer Probing

- Pre-Bond Test
  - Large arrays of fine-pitched micro-bumps
  - New metallurgies
  - Front-side and/or back-side probing

- Mid- and Post-Bond Test
  - Non-planar topologies

Design-for-Test

- Die-level test wrapper [Marinissen et al. – VTS’10, 3DIC’10]
  - Modular die/interconnect tests
  - Supports pre-, mid-, and post-bond tests
  - TestTurns: from and to ext. I/O in bottom die
  - TestElevators in each (non-top) die

- Supported by Cadence tools
- Proposed to IEEE P1838 Working Group
3. Probing on Fine-Pitch Micro-Bumps

Today’s State-of-the-Art

- **Probe cards do not meet pitch requirements**
  - Micro-bump pitch: 40μm (and scaling down!)
  - Probe card pitch: ≥50μm
  - Some cantilever cards go smaller, but they do not handle arbitrary probe arrays

- **Solution today: additional pre-bond probe pads**
  - Dedicated: only for pre-bond test
  - Extra
    - Design effort
    - Silicon area
    - Processing steps
  - Trade-off area vs. test time
  - Not the ‘real’ entry/exit point for functional data

Source: Samsung, ISSCC'11
Source: ST-Ericsson, CDNLive EMEA'11

IEEE South-West Test Workshop – San Diego, California, June 2011
3. Probing on Fine-Pitch Micro-Bumps

Pyramid Membrane Probe Cards

- **Probe core** with two litho-defined membrane layers span over a plunger:
  1. Routing layer to probe card
  2. Replaceable contact layer with probe tips

- **Probe card** adapts to probe station

- Application focus on
  - RF filters, switches
  - Process monitors (incl. M1 copper)
  - RF-SOC Multi-DUT
3. Probing on Fine-Pitch Micro-Bumps

New RBI Probe Technology

- **Conventional Pyramid tips**
  ~100µm pitch, ~10g/contact

- **Rocking Beam Interposer technology**
  ~35µm pitch, ~1g/contact
  - Same materials
  - Decrease xyz dimensions by factor $k$
  - Decrease z motions by factor $k$
  - Decrease force/tip by $k^2$ for constant tip pressure
3. Probing on Fine-Pitch Micro-Bumps

Requirements on Probe Station

- Probing on small targets
  → Accurate XY positioning
- Future bondability on micro-bumps
  → Reducing probe force with accurate Z control
- Accurate contact stability
  → High-performance vibration isolation
- TSV thermal stress measurements
  → Fast thermal transition time
- TSV thermal issues due to increased power densities
  → Thermal chuck dissipation and resistance
- Probing with high-pin count vertical probe cards
  → Safe operation inside shielded environment
4. Experimental Results

Contact on Blanket Wafers

- IMEC blanket wafers with micro-bump metallurgy: Cu 5µm
- Single RBI probe tip with precise tip force measurement
- Iterating over 0.25, 0.50, 0.75, and 1.00 gram probe tip force
- \(4 \times 12 + 4 \times 50 + 4 \times 50\) touch-downs without cleaning

Contact resistance: \(0.3 \leq R_c \leq 1.6\) Ohm

Dependent on:
- Probe surface: metallurgy, roughness, oxidation, cleanliness (Cu vs. CuSn)
- Probe tip: material, shape, area, cleaning recipe
- Probe force
4. Experimental Results

Contact on Blanket Wafers

Probe damage: raised berm
- Length 3-4μm
- Height 200nm

Cu wafer
4. Experimental Results

New RBI Probe Cards at IMEC

• Several cores
  – 100µm pitch, 24 tips
  – 50µm area array, 184 tips
  – 40µm area array, 480 tips

• Probe cards for
  – Cascade Microtech PA300-3D semi-auto prober
  – TEL P12XLm auto-prober
4. Experimental Results

Target: WideIO 3D-DRAM Interface

- JEDEC standardized interface for low-power 3D-DRAMs
- 4 independent channels
  - 128-bit data/channel
  - 6×50 micro-bumps/channel
  - 40µm pitch x, 50µm pitch y

- RBI-technology probe card
  - One WideIO-channel version
  - 300 probe tips, all routed independently
  - Initially focused on engineering and failure analysis applications
5. Conclusion

Summary

- 3D-SICs based on TSV is fast-emerging technology
- 3D-SICs have several test challenges: flow, contents, access

- Probing on fine-pitch micro-bumps is one of those challenges
  - In order to avoid additional dedicated probe pads
  - Requirements:
    - Micro-bumps at 40µm pitch
    - Array size: 4 × (6×50) micro-bumps (JEDEC WideIO)
    - Probe damage not to inhibit downstream bonding

- Tough requirements on probe cards and probe stations, but first experimental results point towards feasibility
  - Contact resistance ~ 1 Ohm: probe-able
  - Berm of only 200nm: bond-able

Work in Progress!
5. Conclusion

3D-TEST Workshop

- First edition with ITC’10 very successful

- Second edition with ITC’11
  - September 22+23, 2011
  - Disneyland Hotel, Anaheim, CA

- Call for Submissions available
  - Papers
  - Posters
  - Panel session ideas

- More information:
  http://3dtest.tttc-events.org