Wafer Probing on Fine-Pitch Micro-Bumps for 2.5D- and 3D-SICs

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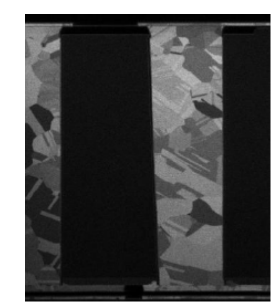
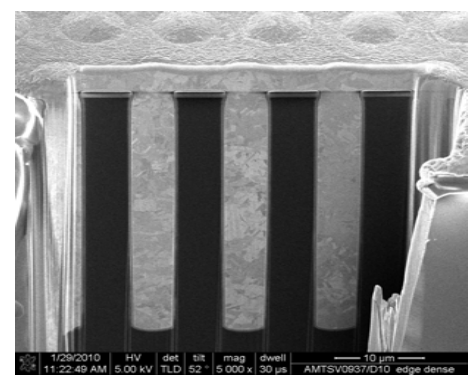
Presentation Outline

1. Introduction to TSV-Based 2.5D- and 3D-SICs
2. Test Challenges
3. Probing on Fine-Pitch Micro-Bumps
4. Experimental Results
5. Conclusion

TSVs: Through-Silicon Vias



- **TSV**
  - Conducting nail; typically Cu or W
  - Electrical path from front-side to back-side of thinned-down silicon wafer
  - Interconnection of vertically stacked dies



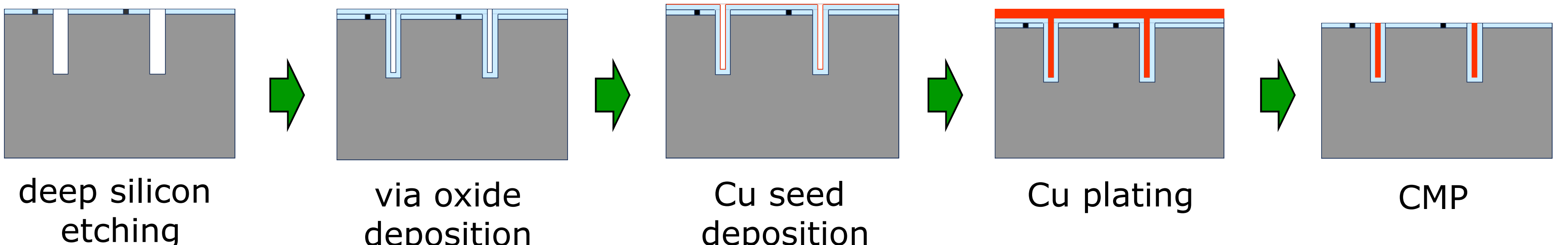
- **Typical TSV Dimensions**
  - Diameter : 5µm
  - Height : 50µm
  - Min. pitch : 10µm

  (Diameter and Height: Aspect Ratio 1:10)

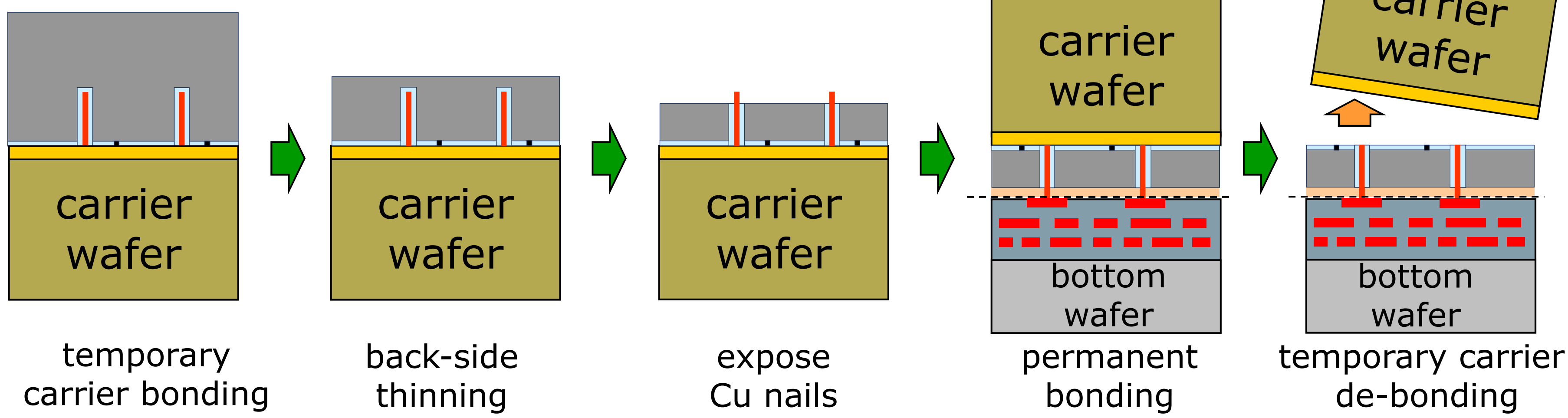
- **Benefits over Wire-Bonds**
  - High density
  - Low capacitance
  - Result: improved bandwidth, performance, power dissipation

TSV Manufacturing

1. TSV Fabrication



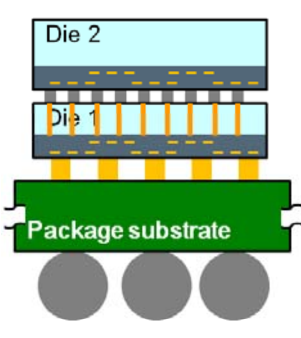
2. Wafer Thinning and Bonding

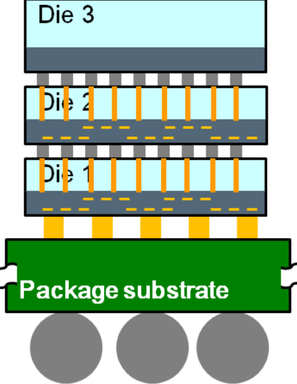


Die Stacking

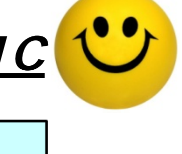
Endless Stacking Opportunities
"Whatever your children can make using Lego bricks"

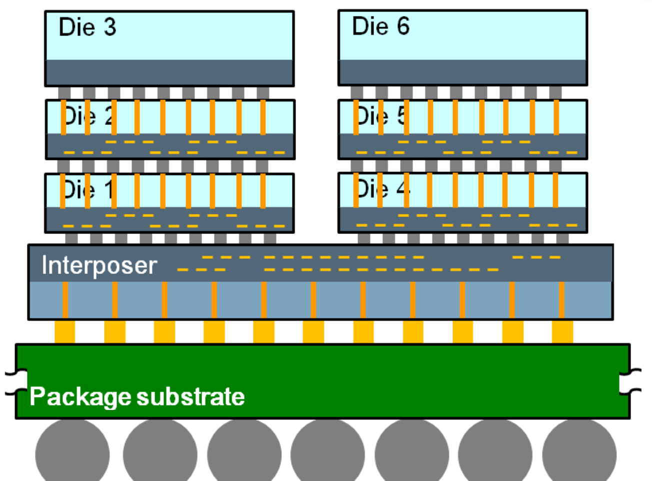
- **3D-SIC**



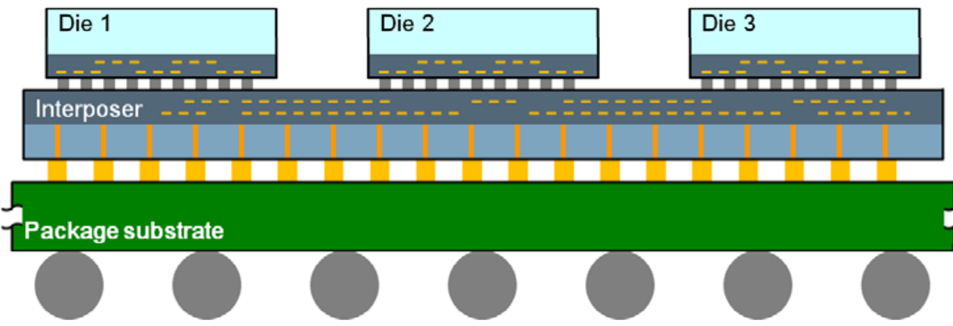


- **2½D + 3D = *5½D-SIC***





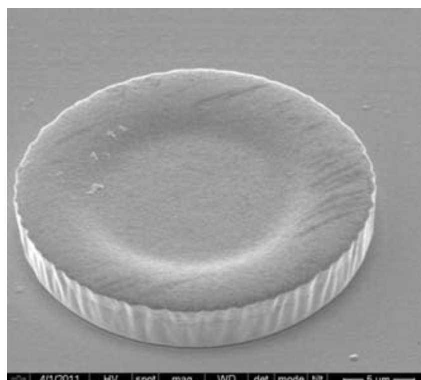
- **2½D-SIC**

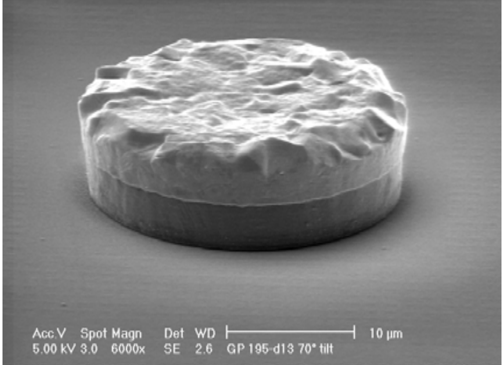


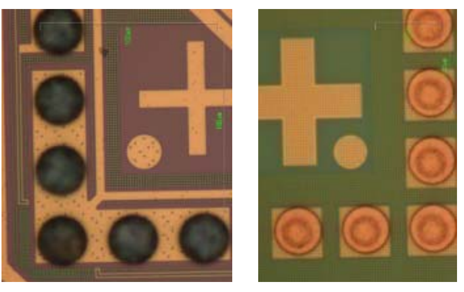
Micro-Bump Bonding

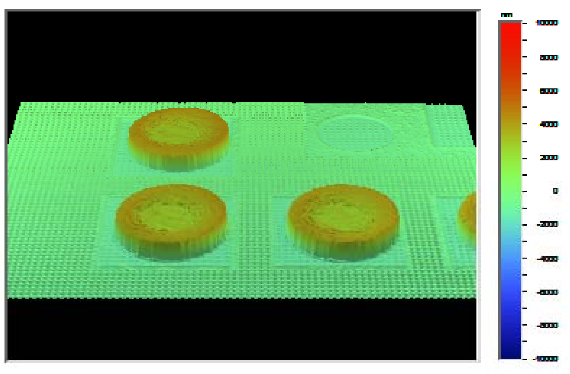
Electroplated Micro-Bumps

- Cylindrical bumps
  - Side1: Cu (5µm)
  - Side2: CuSn (5µm + 3.5µm)
- Size (scaling down!)
  - Diameter : 25µm
  - Pitch : 40µm









Bonding

- Transient-Liquid Phase (250 °C)
- Diffusion bonding (150 °C)
- Bump planarization

Micro-Bump Bonding

LOGIC

TSV

Backside RDL and Cu µbump

Backside Polymer isolation

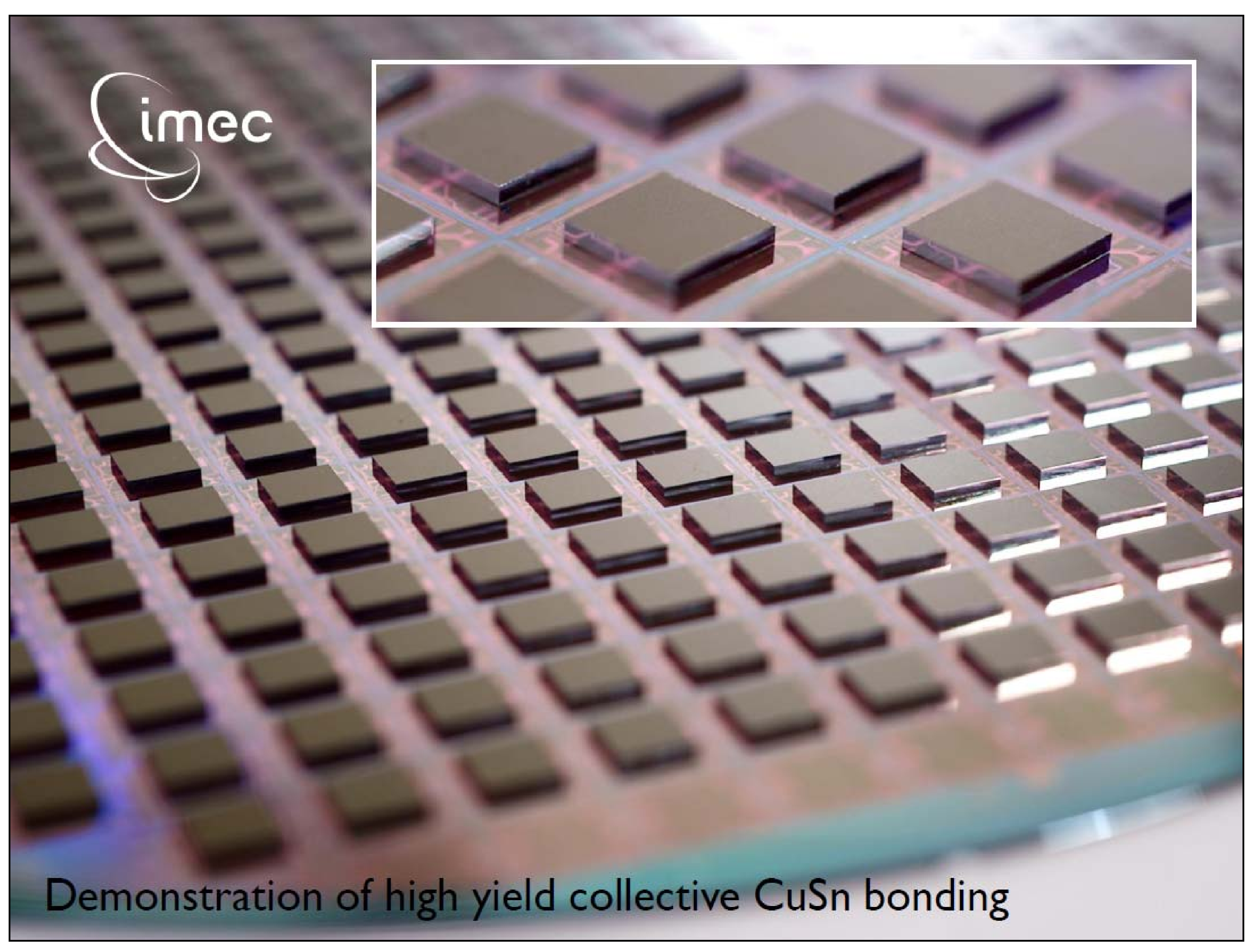
Cu µbump

SnAg

Cu µbump

DRAM

10/8/2010 4:17:48 PM | HV 30.00 kV | tilt 0 ° | mag 5 000 x | det ETD | curr 9.7 pA | 20 µm | sample 8 fib 2


imec
Demonstration of high yield collective CuSn bonding

Test Challenges – Overview

1. **3D Test Flows**
   What to test when?

2. **3D Test Contents**
   New test patterns to cover new defects
   2A. Due to 3D processing steps
   2B. Due to TSV-based interconnects

3. **3D Test Access**
   Pumping stimuli in/responses out of the DUT
   3A. External : Wafer probing
   3B. Internal : Design-for-Test

Embedded Tutorial at
IEEE Asia Pacific Conference on Circuits and Systems (APCCAS'10)
Kuala Lumpur, Malaysia – December 2010

Challenges in Testing TSV-Based 3D Stacked ICs: Test Flows, Test Contents, and Test Access

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Abstract

Three-dimensional stacked ICs (3D-SICs) based on Through-Silicon Vias (TSVs) have many attractive benefits and hence are quickly gaining ground. Testing such products for manufacturing defects is still fraught with many challenges. This paper provides an overview of those challenges and their emerging solutions, categorized in the areas of (1) test flows, (2) test contents, and (3) test access.

1 Introduction

Vertical stacking of multiple integrated circuits offers dense integration of possibly heterogeneous technologies with a small area footprint. The semiconductor industry is preparing itself now for vertical interconnection of multiple stacked tiers by means of TSVs [1–3]. In comparison to conventional wire-bonded interconnects, TSVs promise to increase the interconnect bandwidth and performance while lowering power dissipation and overall manufacturing cost. Consequently, TSV-based 3D technologies enable the creation of a new generation of 'super chips' by opening up new architectural opportunities [4, 5] and hence might help the semiconductor industry to extend the momentum of Moore's Law into the next decade.

A lot of research and development work has been done, is being done, and still needs to be done to enable TSV-based 3D integration. One of the first challenges to be addressed was the development of processing recipes to be able to manufacture TSVs. Typical TSV dimensions are 5 μm diameter and 50 μm height (see Figure 1). Etching and properly filling TSVs with such a large aspect ratio is not an easy task [6, 7]. A normal wafer is much thicker than the TSV height, and hence the wafer needs to be thinned down to make the TSV extend out of the wafer's back-side to connect to the next tier. Wafer thinning and thin-wafer handling [8], back-side processing, bonding [9, 10], and packaging of die stacks are also on the list of technology challenges. To be able to monitor the processing, in-line inspection [11], metrology [12], and failure analysis tools need to be upgraded to cope with this new type of circuits.

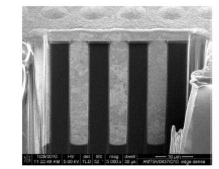


Figure 1: Cross-section photo of Through-Silicon Vias with aspect ratio 10:1.

Research and development work on 3D integration also addresses design issues. The impact of 3D processing on the operation of the circuit needs to be assessed and compensated for [13, 14]. This includes the effects of TSV proximity on transistors and metal interconnect, mechanical stress and warpage (especially of thinned wafers), thermal stress (as the vertical stack might block heat dissipation) [15], etc. New design methods and software tools need to be developed that handle 3D designs [16, 17], from high-level architectural trade-offs including hardware-software co-design, down to three-dimensional transistor netlist and layout [18].

Like all ICs, these new TSV-based 3D-SICs also need to be tested for manufacturing defects, in order to guarantee sufficient outgoing product quality to the customer. Whereas 3D-SICs require most of today's advanced test and Design-for-Test (DfT) approaches, simply because they are composed of advanced IC designs in advanced technology nodes, they also have some unique test challenges of their own [19, 20]. These challenges pertain to (1) test flows, (2) test contents, and (3) test access. This paper provides an overview of these challenges and their solutions, to the extent that they already exist.

2 3D Test Flows

Most conventional single-die chips have a test flow consisting of two tests: a *wafer test* and a final *packaged test*. The test flow for 3D-SICs is potentially a lot more complex; their manufacturing process consists of many more steps and hence has many more potential natural test moments. As shown in Figure 2, we distinguish between (1) *pre-bond die tests*, (2) *post-bond stack tests*, and (3) *packaged tests*. Pre-bond and post-bond tests are both wafer probe tests; we distinguish between them, as they are distinctly different in their purpose, test contents, and test access.

In a dis-integrated production flow, intermediate products which are building blocks for one company, are final products for another company. For example, DRAM dies to be stacked on top of logic dies are intermediate products in view of the overall stack, but are final products for the DRAM maker. In such a setting, the supply contract typically requires that the intermediate products (DRAMs, in our example) are tested with final-test quality, including at-speed and burn-in tests. The delivered products are termed *Known-Good Dies* (KGD) [21], or, in case of die stacks, *Known-Good Stacks* (KGS) [20].

In an integrated production flow, where absolute KGD/KGS quality is not required, the test coverage and quality for intermediate products becomes

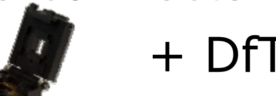
1

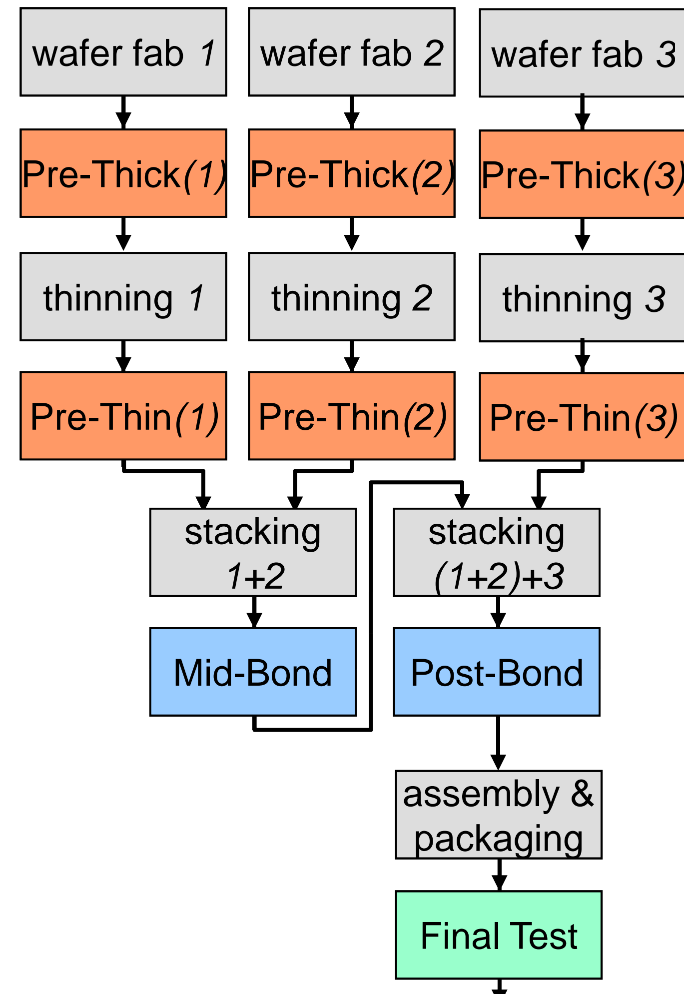
[Marinissen – APCCAS'10]

2. Test Challenges

Challenge 1: 3D Test Flows

Potential Test Moments:

- **Pre-Bond Test**
  - Content : die (+ TSVs)
  - Access : wafer probe
- **Mid- and Post-Bond Test**
  - Content : interconnects (+ dies)
  - Access : wafer probe + DfT
- **Final Test**
  - Content : dies + interconnects
  - Access : socket  + DfT



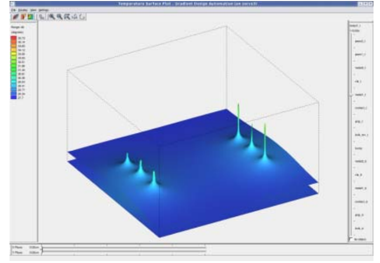
- Many more natural wafer test moments
- Pre-Bond and Post-Bond tests are distinctly different in test access
- Disintegrated production flow more likely: KGD / KGS testing
- Integrated flow: test benefits need to exceed costs ⇒ cost modeling

[Taouil et al. - ATS'10]

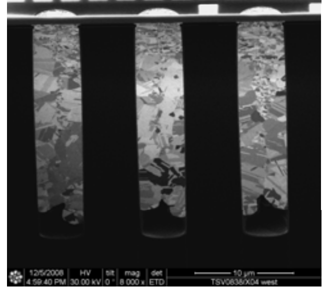
Challenge 2: 3D Test Contents

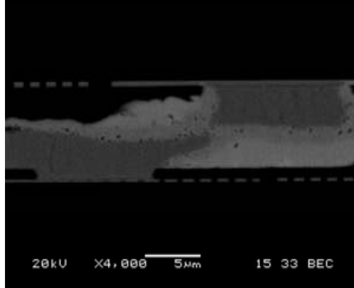
- All manufacturing defects that can occur in conventional 2D chips, can also occur in 3D-SICs
  - Logic : stuck-at, transition, delay, VLV, …
  - Memory : array, decoder, control, data-lines, …
  - Analog : INL, THD, …

- New defects due to new 3D processing steps
  - Wafer thinning: shifts in device performance [Ikeda et al. – ICMTS'04] [Perry et al. – DATE'09 3D Workshop]
  - Thermal dissipation and thermo-mechanical stress
  - Yield loss



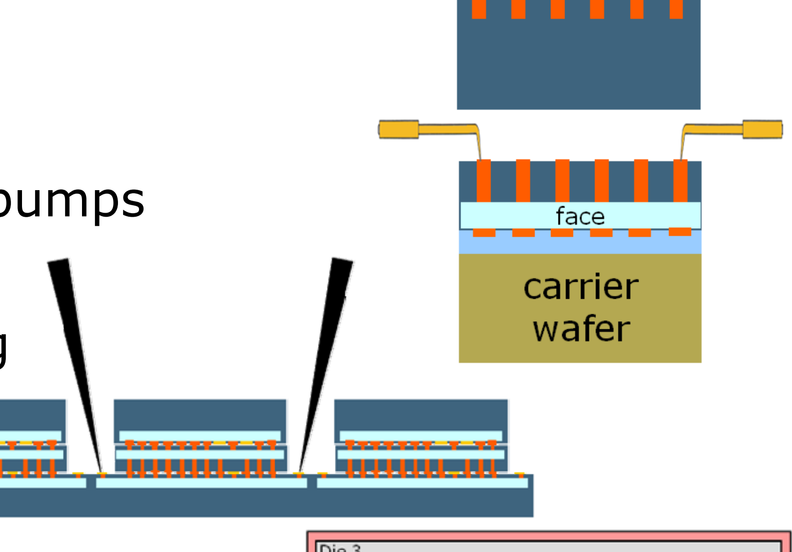
- Defects in TSV-based interconnects
  - TSV fabrication: liner, barrier, plating
  - Interconnect bonding: height, align





2. Test Challenges

Challenge 3: Test Access



Wafer Probing

- Pre-Bond Test
  - Large arrays of fine-pitched micro-bumps
  - New metallurgies
  - Front-side and/or back-side probing
- Mid- and Post-Bond Test
  - Non-planar topologies

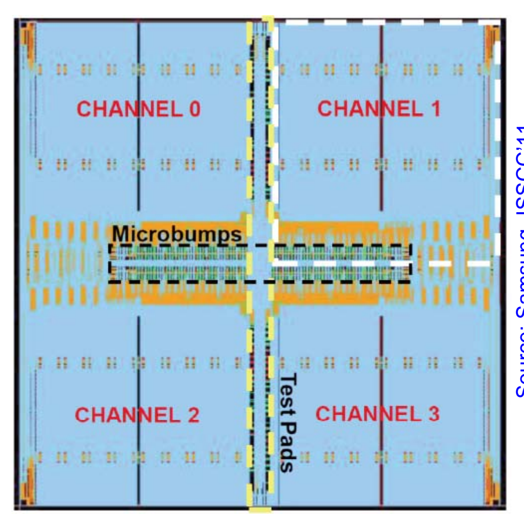
Design-for-Test

- Die-level test wrapper [Marinissen et al. – VTS'10, 3DIC'10]
  - Modular die/interconnect tests
  - Supports pre-, mid-, and post-bond tests
  - TestTurns: from and to ext. I/O in bottom die
  - TestElevators in each (non-top) die
- Supported by Cadence tools
- Proposed to IEEE P1838 Working Group

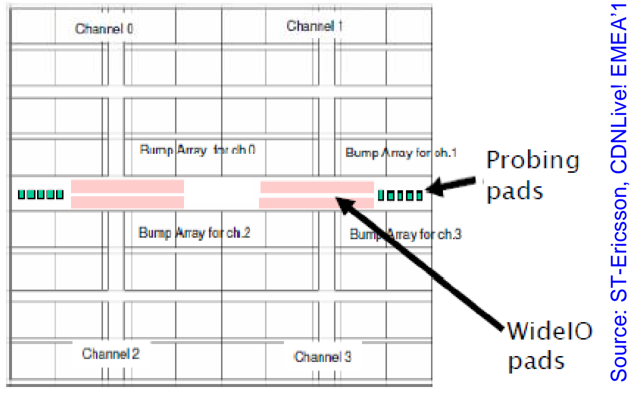
3. Probing on Fine-Pitch Micro-Bumps

Today's State-of-the-Art

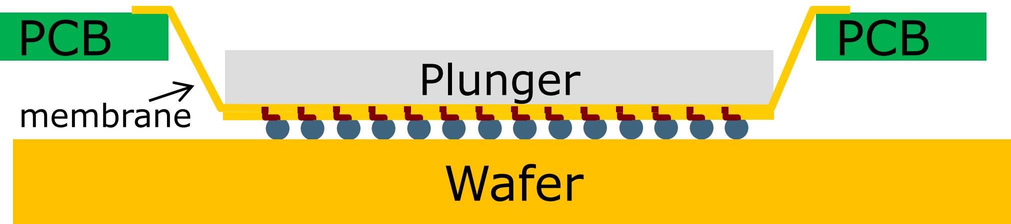
- **Probe cards do not meet pitch requirements**
  - Micro-bump pitch : 40μm (and scaling down!)
  - Probe card pitch : ≥50μm
  - Some cantilever cards go smaller, but they do not handle arbitrary probe arrays

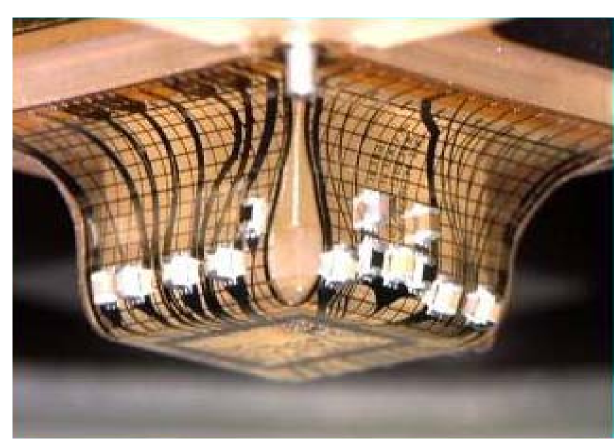


- **Solution today: additional pre-bond probe pads**
  - Dedicated: only for pre-bond test
  - Extra
    - Design effort
    - Silicon area
    - Processing steps
  - Trade-off area vs. test time
  - Not the 'real' entry/exit point for functional data

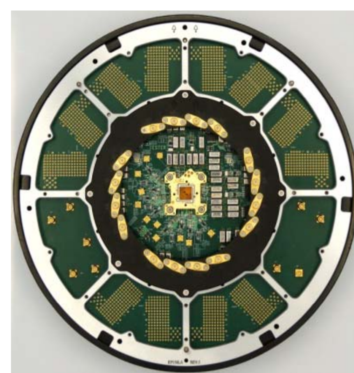


Pyramid Membrane Probe Cards





- **Probe core** with two litho-defined membrane layers span over a plunger:
  1. Routing layer to probe card
  2. Replaceable contact layer with probe tips
- **Probe card** adapts to probe station
- Application focus on
  - RF filters, switches
  - Process monitors (incl. M1 copper)
  - RF-SOC Multi-DUT

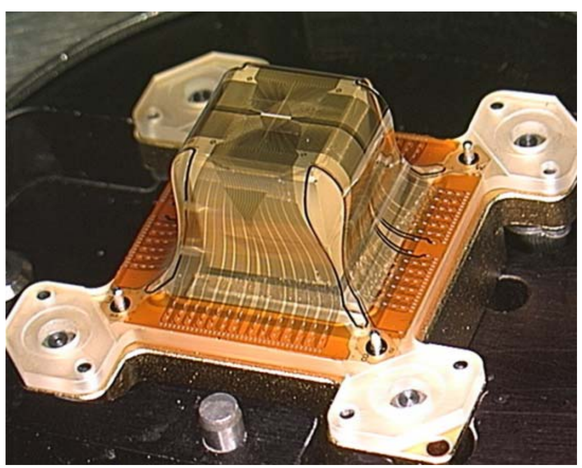


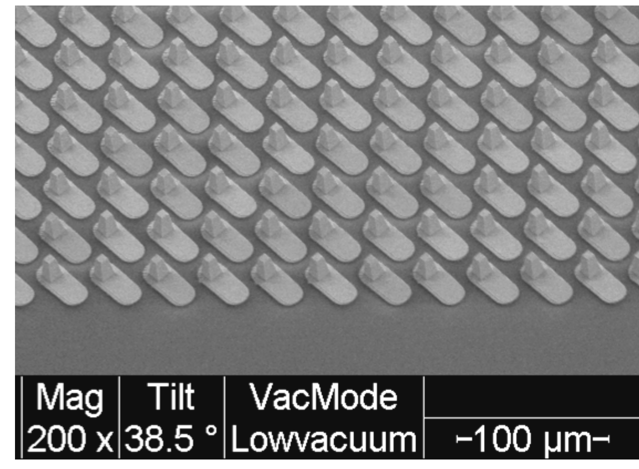
3. Probing on Fine-Pitch Micro-Bumps

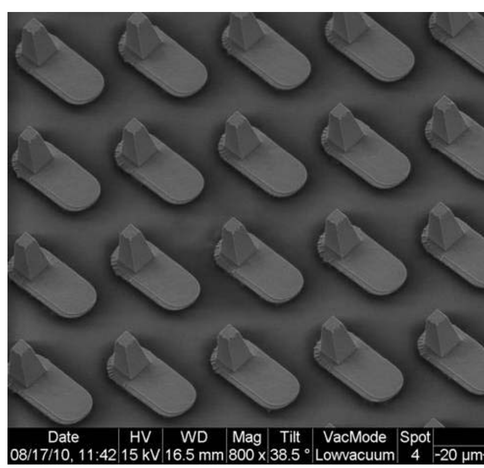
New RBI Probe Technology

- **Conventional Pyramid tips**
  ~100µm pitch, ~10g/contact

- **Rocking Beam Interposer technology**
  ~35µm pitch, ~1g/contact
  - Same materials
  - Decrease *xyz* dimensions by factor *k*
  - Decrease *z* motions by factor *k*
  - Decrease force/tip by k^2 for constant tip pressure







Requirements on Probe Station

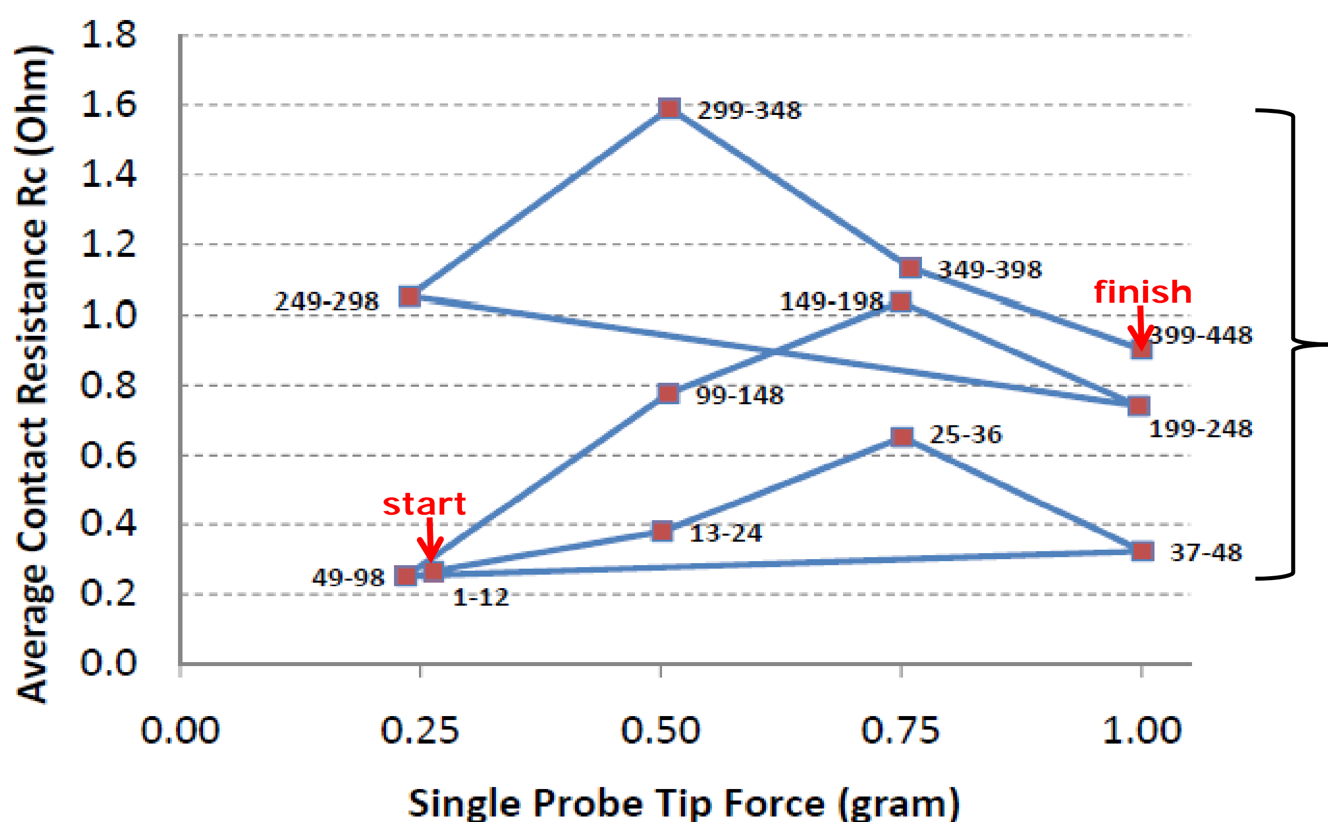
- Probing on small targets
  → Accurate XY positioning
- Future bondability on micro-bumps
  → Reducing probe force with accurate Z control
- Accurate contact stability
  → High-performance vibration isolation
- TSV thermal stress measurements
  → Fast thermal transition time
- TSV thermal issues due to increased power densities
  → Thermal chuck dissipation and resistance
- Probing with high-pin count vertical probe cards
  → Safe operation inside shielded environment

Cascade Microtech
PA300 ProbeShield 3D

4. Experimental Results

Contact on Blanket Wafers

- IMEC blanket wafers with micro-bump metallurgy: Cu 5μm
- Single RBI probe tip with precise tip force measurement
- Iterating over 0.25, 0.50, 0.75, and 1.00 gram probe tip force
- 4×12 + 4×50 + 4×50 touch-downs *without cleaning*



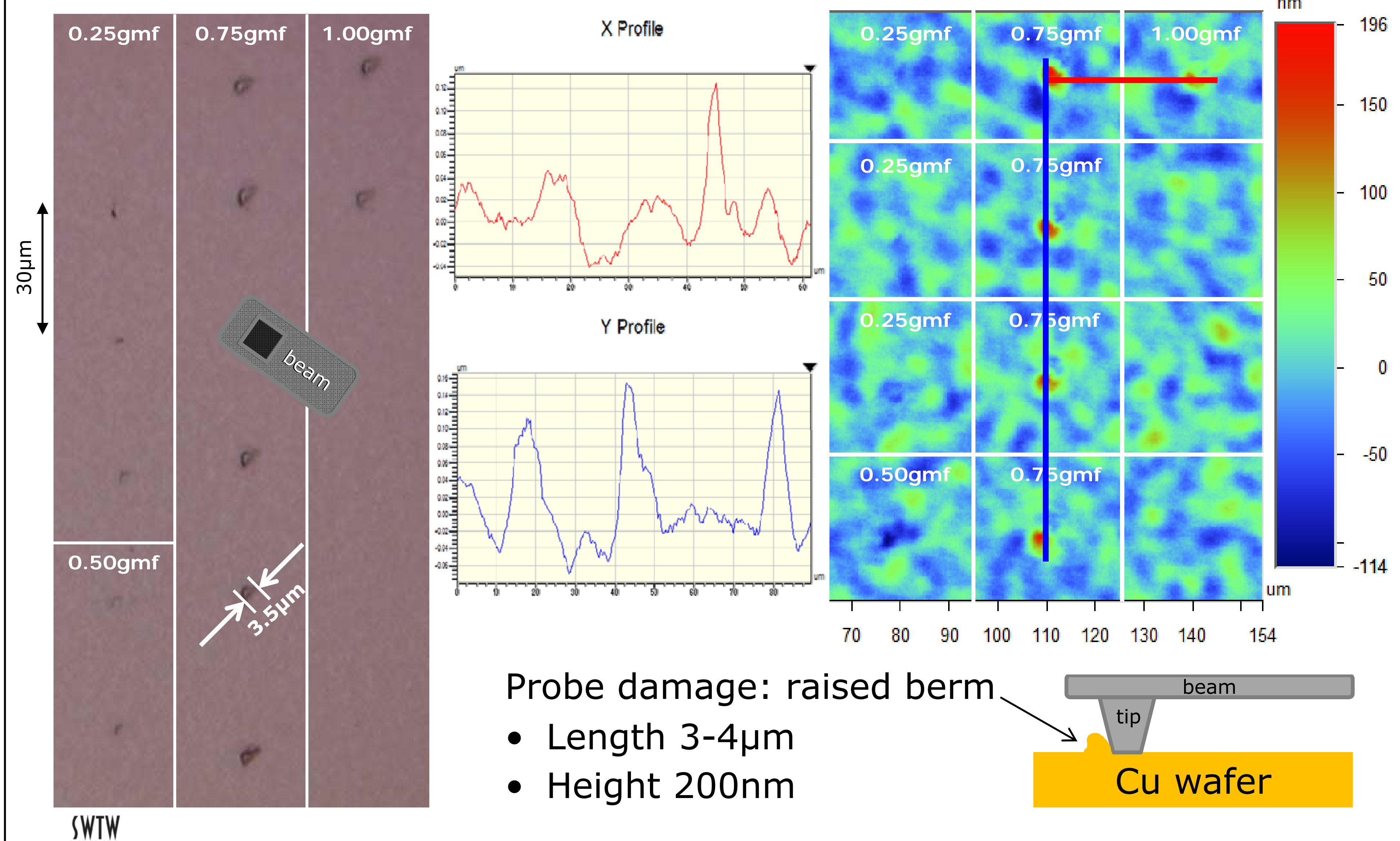
Contact resistance:
$0.3 \leq R_c \leq 1.6$ Ohm

Dependent on:

- Probe surface: metallurgy, roughness, oxidation, cleanliness (Cu vs. CuSn)
- Probe tip: material, shape, area, cleaning recipe
- Probe force

4. Experimental Results

Contact on Blanket Wafers

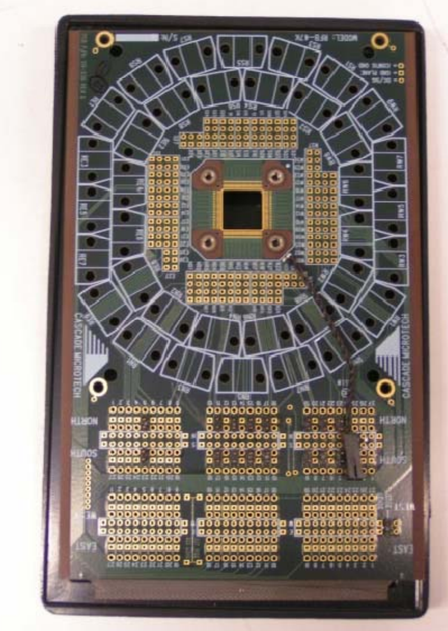


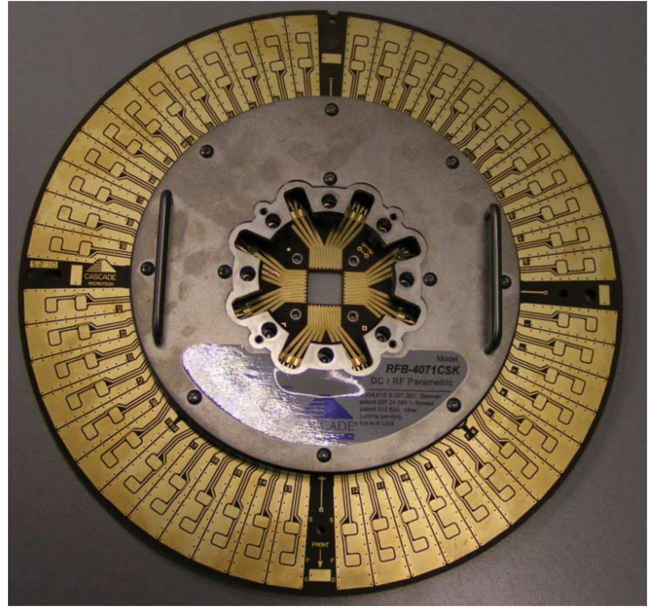
4. Experimental Results

New RBI Probe Cards at IMEC

- Several cores
  - 100µm pitch, 24 tips
  - 50µm area array, 184 tips
  - 40µm area array, 480 tips

- Probe cards for
  - Cascade Microtech PA300-3D semi-auto prober
  - TEL P12XLm auto-prober

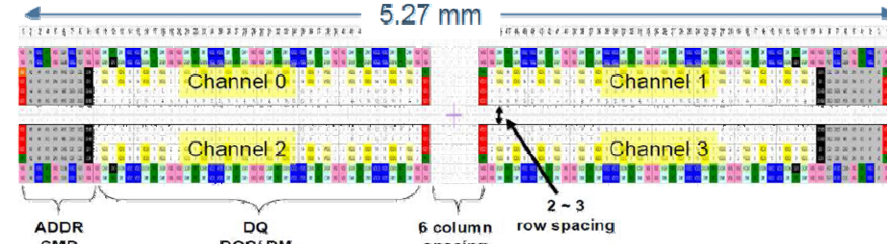




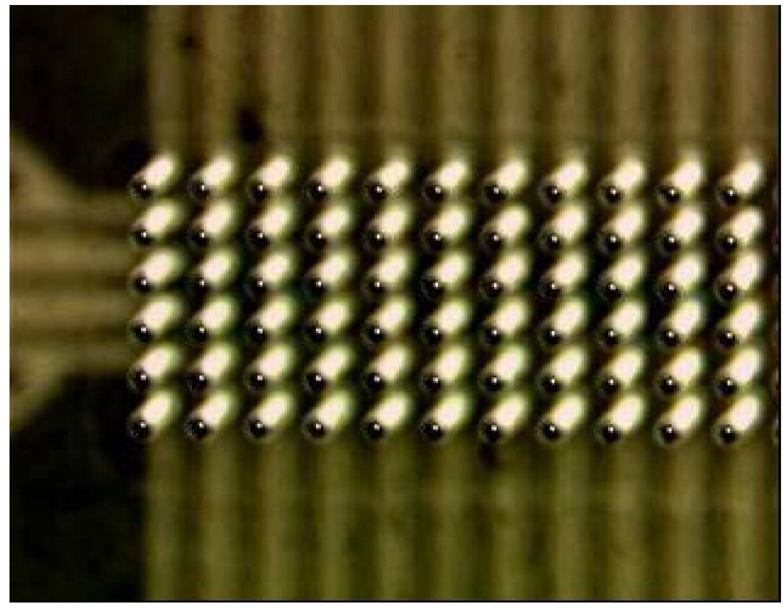
4. Experimental Results

Target: WideIO 3D-DRAM Interface

- JEDEC standardized interface for low-power 3D-DRAMs
- 4 independent channels
  - 128-bit data/channel
  - 6×50 micro-bumps/channel
  - 40µm pitch *x*, 50µm pitch *y*



- RBI-technology probe card
  - One WideIO-channel version
  - 300 probe tips, all routed independently
  - Initially focused on engineering and failure analysis applications



5. Conclusion

Summary

- 3D-SICs based on TSV is fast-emerging technology
- 3D-SICs have several test challenges: flow, contents, access

- Probing on fine-pitch micro-bumps is one of those challenges
  - In order to avoid additional dedicated probe pads
  - Requirements:
    - Micro-bumps at 40μm pitch
    - Array size: 4 × (6×50) micro-bumps (JEDEC WideIO)
    - Probe damage not to inhibit downstream bonding

- Tough requirements on probe cards and probe stations,
  but first experimental results point towards feasibility
  - Contact resistance ~ 1 Ohm : probe-able
  - Berm of only 200nm : bond-able

  Work in Progress!

5. Conclusion

3D-TEST Workshop

- First edition with ITC'10 very successful
- Second edition with ITC'11
  - September 22+23, 2011
  - Disneyland Hotel, Anaheim, CA
- Call for Submissions available
  - Papers
  - Posters
  - Panel session ideas
- More information: http://3dtest.tttc-events.org

Second IEEE International Workshop on Testing Three-Dimensional Stacked Integrated Circuits

3D-TEST

in conjunction with ITC / Test Week 2011
Disneyland Hotel – Anaheim, California, USA
September 22+23, 2011
http://3dtest.tttc-events.org

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B. Patti – Tezzaron Semiconductor (US)
F. Pöhl – Intel (D)
M. Ricchetti – AMD (US)
D. Rishavy – TEL Test Systems (US)
T. Thärigen – Cascade Microtech (D)
E. Volkerink – Verigy (US)
Y. Xie – Penn. State Univ. (US)
Q. Xu – Chinese Univ. Hong Kong (HK)
M. Zhang – Samsung Electronics (US)

Call for Submissions

The 3D-TEST Workshop focuses exclusively on test of and design-for-test for three-dimensional stacked ICs (3D-SICs), including Systems-in-Package (SiP), Package-on-Package (PoP), and especially 3D-SICs based on Through-Silicon Vias (TSVs). While 3D-SICs offer many attractive advantages with respect to heterogeneous integration, smaller form-factor, higher bandwidth and performance, and lower power dissipation, there are many open issues with respect to testing such products. The 3D-TEST Workshop offers a forum to present and discuss these challenges and (emerging) solutions among researchers and practitioners alike.

3D-TEST will take place in conjunction with the IEEE International Test Conference (ITC) and is sponsored by the Test Technology Technical Council (TTTC) of the IEEE Computer Society.

Topic Areas – You are invited to participate and submit your contributions to the 3D-TEST Workshop. The workshop's areas of interest include (but are not limited to) the following topics:

- *Defects due to Wafer Thinning*
- *Defects in Intra-Stack Interconnects*
- *DfT Architectures for 3D-SICs*
- *EDA Design-to-Test Flow for 3D-SICs*
- *Failure Analysis for 3D-SICs*
- *Known-Good Die / Stack Testing*
- *Pre-Bond, Mid-Bond and Post-Bond Test*
- *Reliability of 3D-SICs*
- *Standardization for 3D Testing*
- *System/Board Test Issues for 3D-SICs*
- *Test Cost Modeling for 3D-SICs*
- *Test Flow Optimization for 3D-SICs*
- *Tester Architecture incl. ATE and BIST*
- *Thermal/Mechanical Stress in 3D-SICs*
- *TSV Test, Redundancy, and Repair*
- *Wafer Probing and Probe Damage of 3D-SICs*

Submission Instructions – Submissions must be sent in as PDF file. The Workshop prefers Full Paper submissions (of up to six pages), but also allows Extended Abstract submissions (of at least two pages). Detailed submission instructions can be found at the Workshop's website: http://3dtest.tttc-events.org. All submissions will be evaluated for selection with respect to their suitability for the workshop, originality, technical soundness, and presented results. Selected submissions can be accepted for regular or poster presentation at the Workshop.

Publications – The workshop will make available to all participants an Electronic Workshop Digest, which includes all material that authors are willing to provide: abstract, paper, slides, poster, etc. Authors of a selected subset of submissions will be invited to submit an extended and re-worked version of their manuscript to be considered for publication in IEEE 'Design & Test of Computers'.

Key Dates

- Submission deadline : August 1, 2011
- Notification of acceptance : August 20, 2011
- Camera-ready material : September 3, 2011

Further Information

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