IEEE SW Test Workshop
Semiconductor Wafer Test Workshop

June 12 to 15, 2011
San Diego, CA

WSP-Wafer Socket Probe for Flip Chip Applications

Brandon Mair
bmair@ti.com
Norman Armendariz
norm@ti.com
TTC – Test Technology Center

Agenda

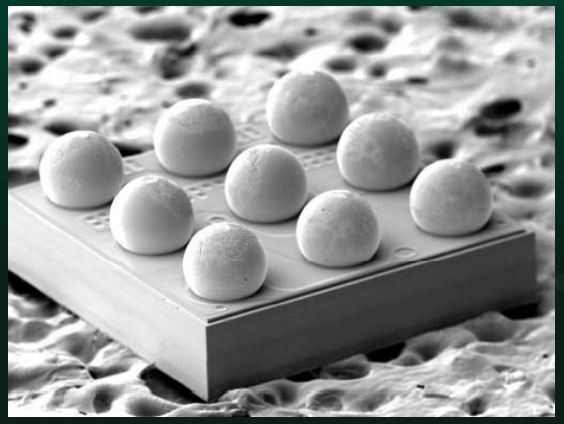
- Introduction
- Probe Tip Effect On Bump
- WSP-FC Probe Attributes
- Approach
- Test Plan
- Data
  - Technology Qualification
  - Production Qualification
- Key Observations
- Summary
- Acknowledgments

Introduction:

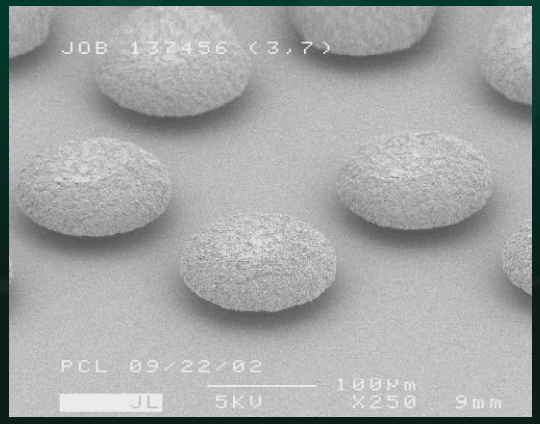
- WSP- Wafer Socket Probe technology has demonstrated better physical, electrical performance and COO compared to CVPC- conventional vertical probe cards on WLCSP devices as observed on 400 um pitch (250um bump dia.) solder balls.

- Currently, Canti-bump and CVPC technologies are used on the smaller bumped FC-Flip-Chip devices.

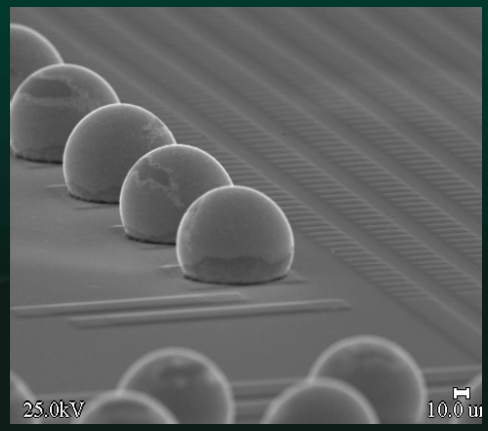
- Objective was to determine if the WSP could be scaled down to Flip-Chip geometries (~150um) and validate if similar WSP-FC attributes would also result on both un-reflowed or reflowed spherical bumps.



WLCSP
Spherical Ball

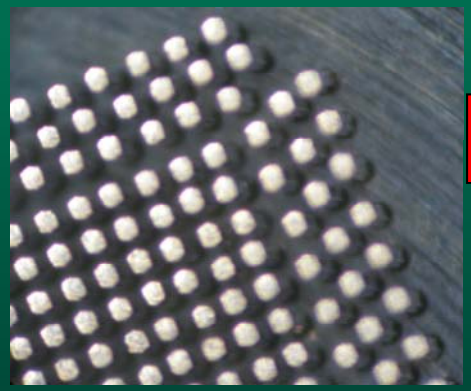


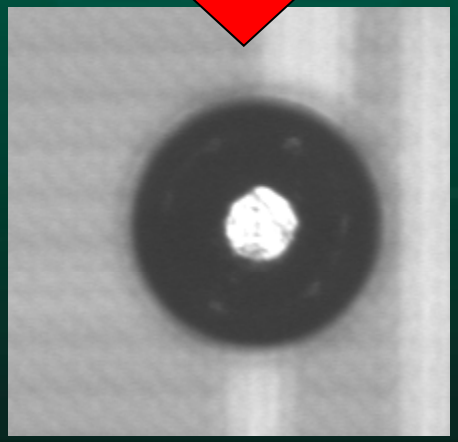
FLIP CHIP
Un-reflowed Bump

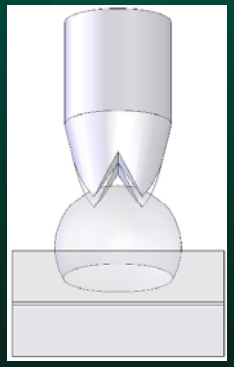


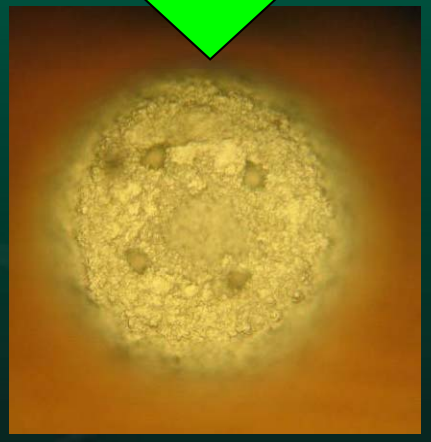
FLIP CHIP
Spherical Bump

CVPC vs WSP FC Probe Tip Effect on Bump









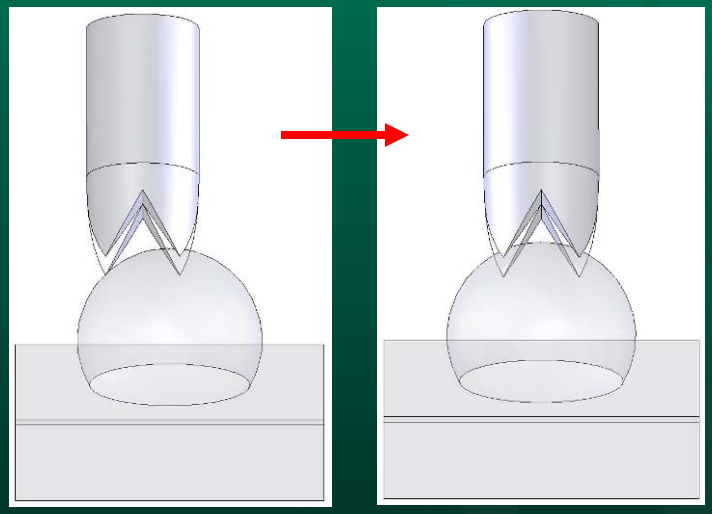
CVPC Flat tips “impact” the top side of the ball (POR). Ball height <1/3 affects SMT process. CRes not as stable, requiring more force and more cleaning to remove compacted debris and reflow.

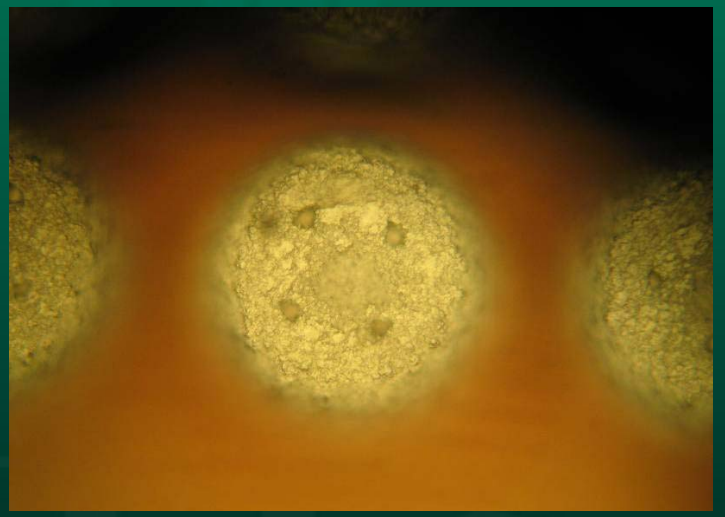
Four WSP-FC Crown tips self-align and “pierce” the sides with min. damage and no effect on ball ht. with min. CRes. Valleys between tips allow debris to channel away during probing.

WSP-FC PROBE ATTRIBUTES:

- Self-Aligning 4-8 pts
- Bump Damage < CVPC
- No reflow req'd.
- Lifetime estm ~ 3 M TDs
- Planarization not req'd.
- Single-pin repairable
- CRes < CVPC
- Cost ~ CVPC
- Deflection > CVPC
- Force / pin < CVPC
- Heads Interchangeable
- Cleaning < CVPC

Probe Attributes: Alignment / Probe Mark

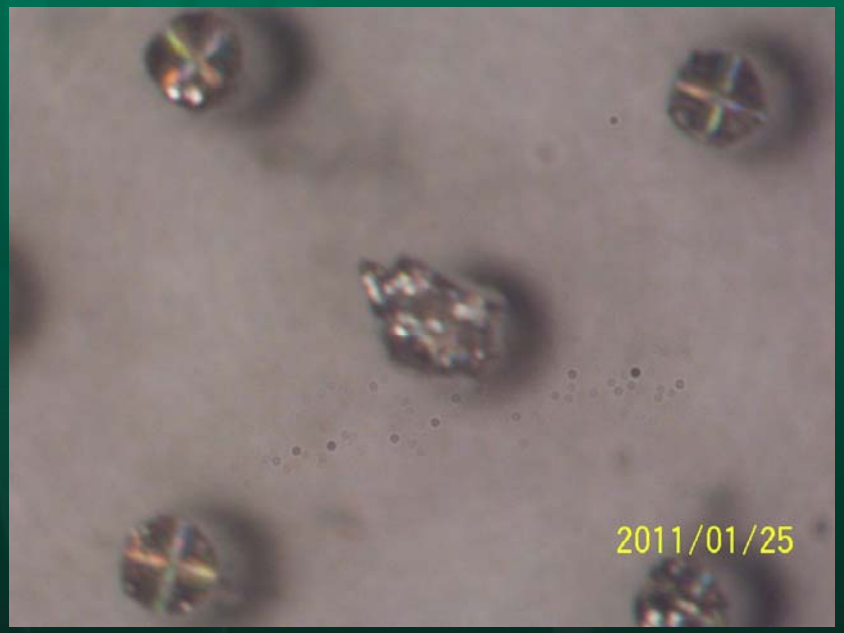




- WSP-FC pogo-pins tend to self-align and center on solder bump because of 4-pt fulcrum design.
- No bump damage is observed at the apex, only four small indents on the sides of the bump.

Probe Attributes: Reparability

- In terms of reparability, WSP technology relatively easy to repair because individual pins can be replaced ON-SITE, similar to typical BGA sockets.
- While probing, one pogo-pin was replaced because melted solder stuck to its tip.
- The process took less than 15 minutes, and subsequent planarization was not required.

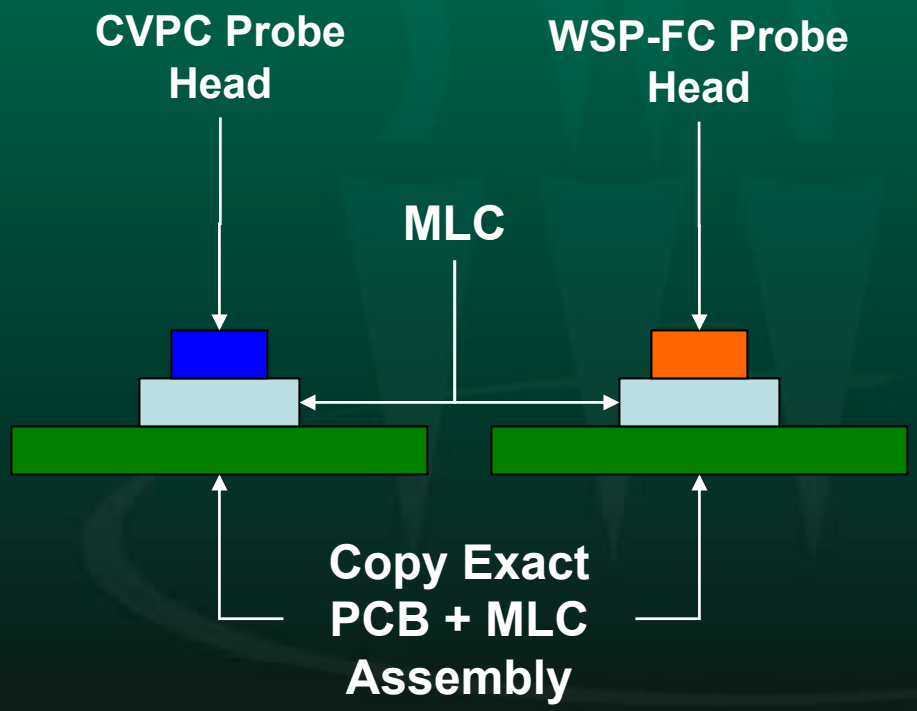


Melted solder stuck to tip, Single pin quickly replaced ON-SITE.

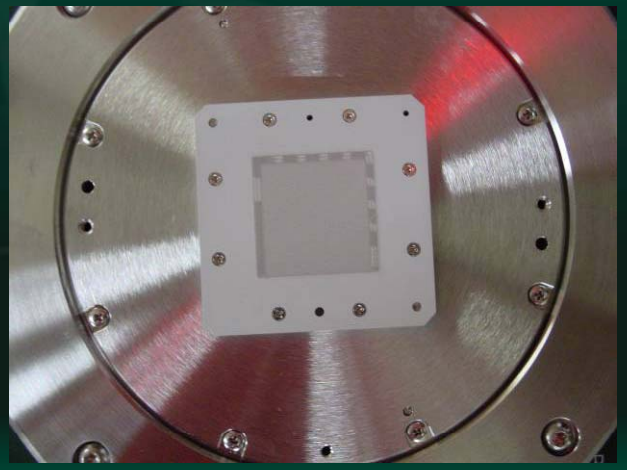
Comparative Evaluation Approach

- A production device was selected as the test vehicle to perform a head-to-head evaluation between a WSP-FC and CVPC probe head based on a “copy exact” test platform.
- The device chosen was a high performance device with ~6,000 “un-reflowed” solder bumps ~120um in diameter and on ~190um pitch centers.
- The qualification process used to qualify and integrate probe card technologies is structured into 2 phases:
  1. Technology Qualification
  2. Production Qualification

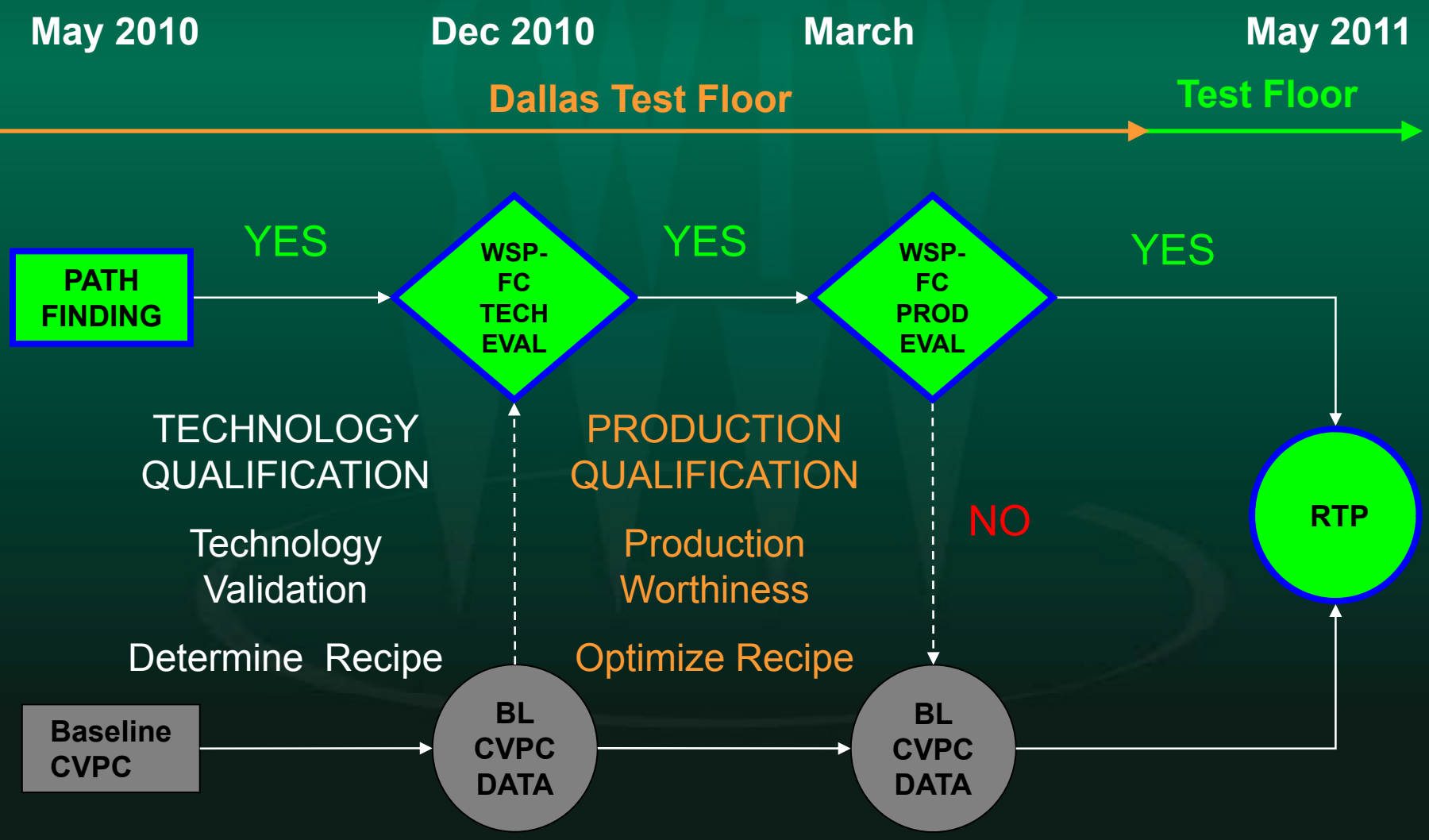
Comparative Evaluation Approach



CVPC vs. WSP- FC



TEST PLAN: WSP-FC vs CVPC



Baseline CVPC was also built to ensure a contingent probe solution available.

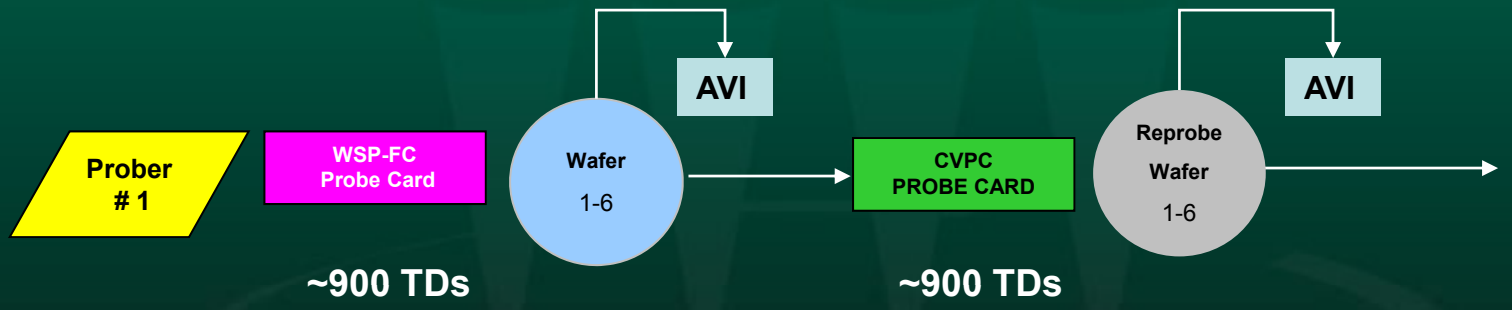
Technology Qualification: Test Flow

152TD TDs / Wafer

TOTAL TDs = ~900-1000 TDs/ Card

6 Wafers
6 Wafers Reprobed
Total: 48hrs

TQ performed to determine a stable probe process recipe in order to run a production qualification to obtain sufficient volume data to characterize.



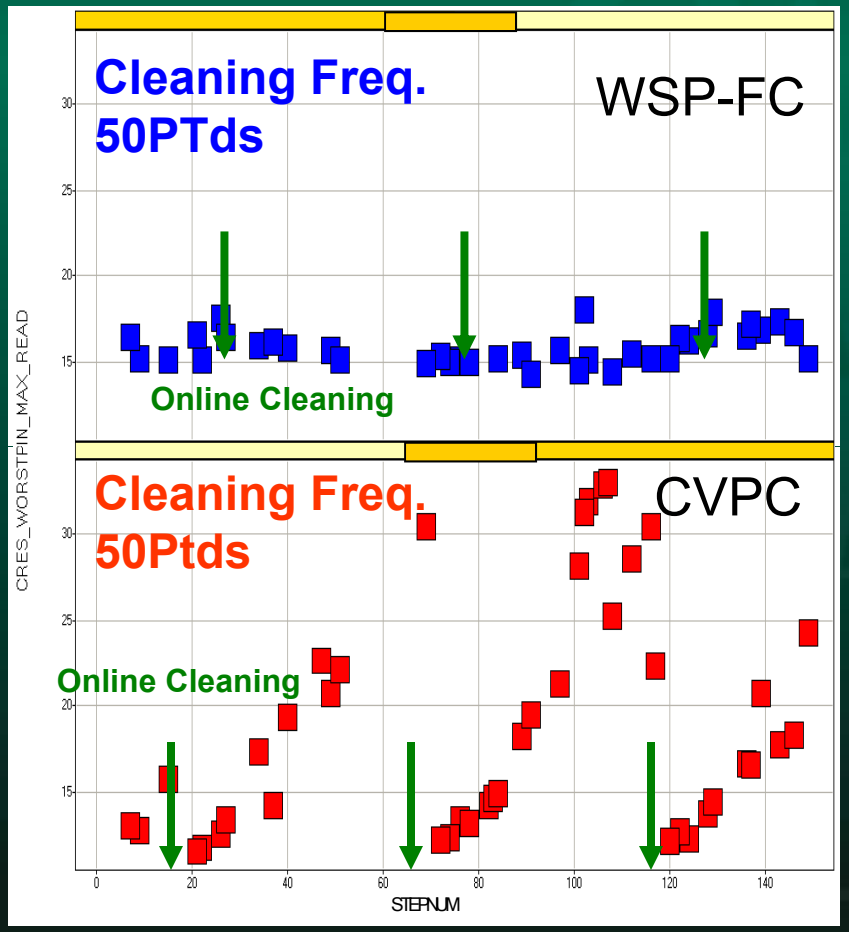
Input Variables:

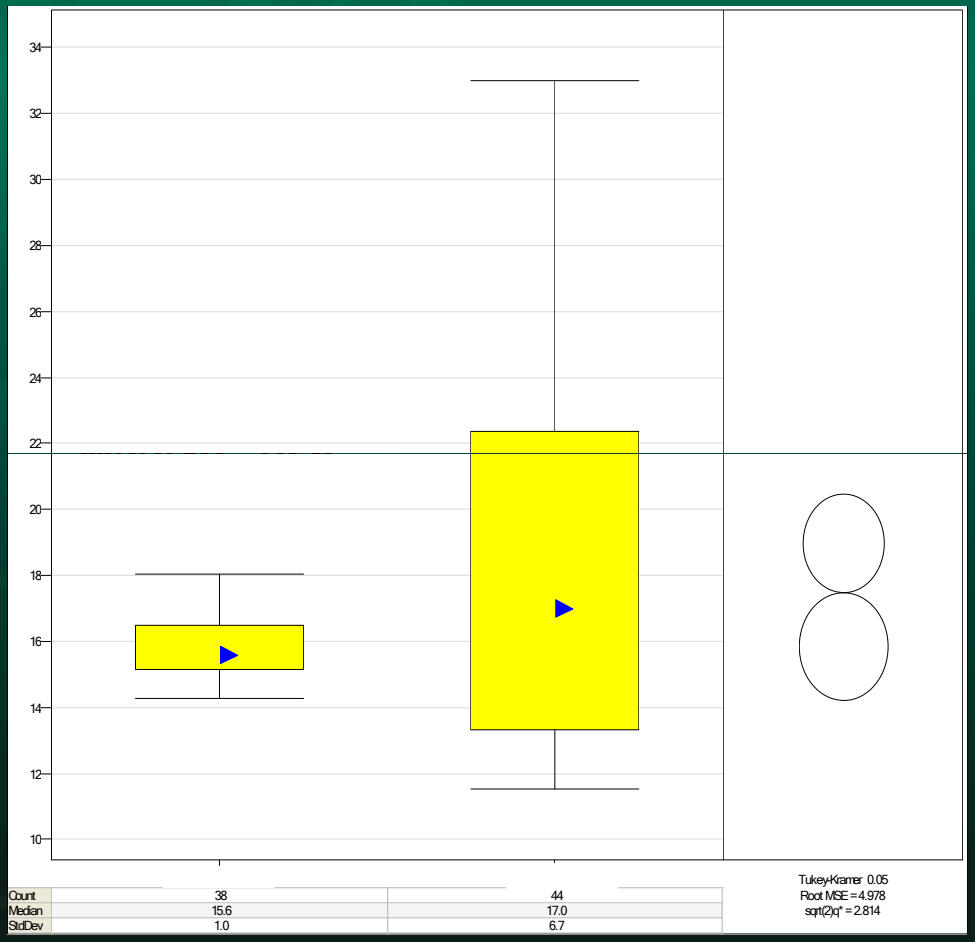
- CVPC Probe Head
- WSP-FC Probe Head
- PH INTERCHANGEABILITY
- Wafer to Wafer

Output Variables:

- CRes
- Yield
- Planarity
- Alignment
- Reprobe Rate
- Tip Length
- Test / Wafer Time
- Bump Damage (AVI)

Technical Qualification: Cleaning Characterization

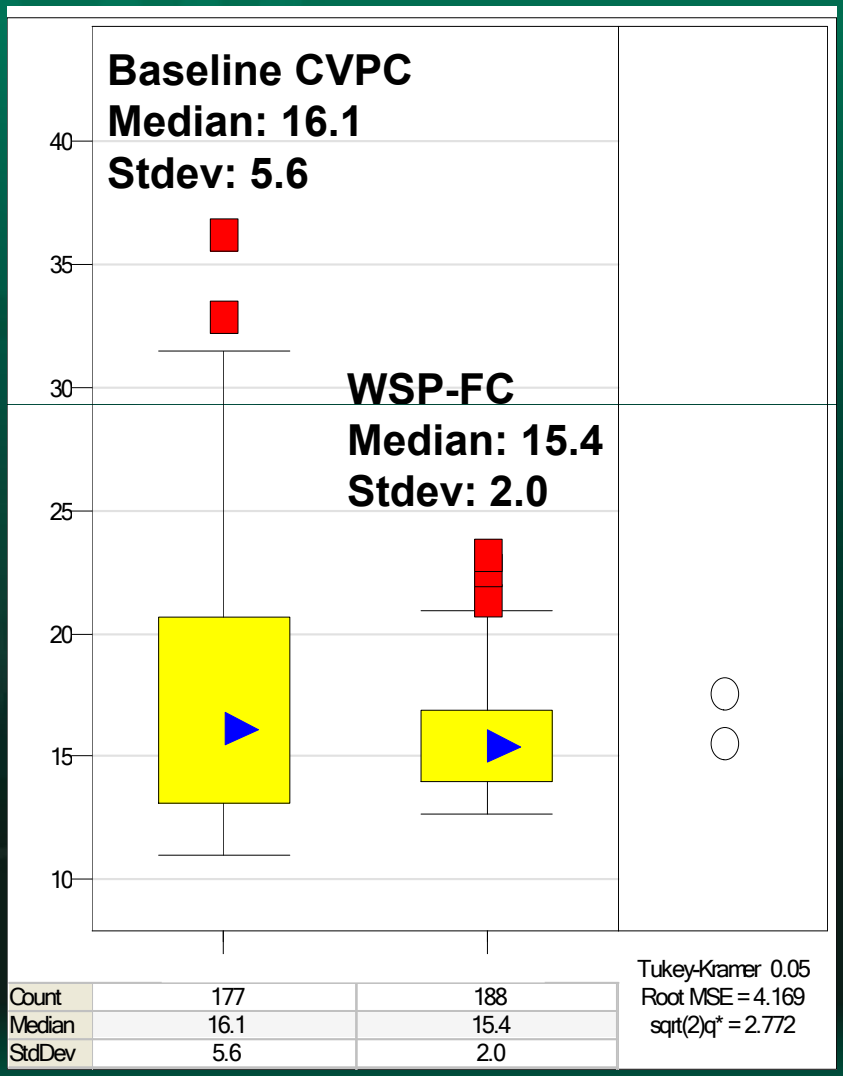




On initial wafer probed at start of evaluation, WSP CRes statistical lower than CVPC. Cleaning "sawtooth" pattern is observed on CVPC every 50 TDs.

Technical Qualification: CRes Characterization

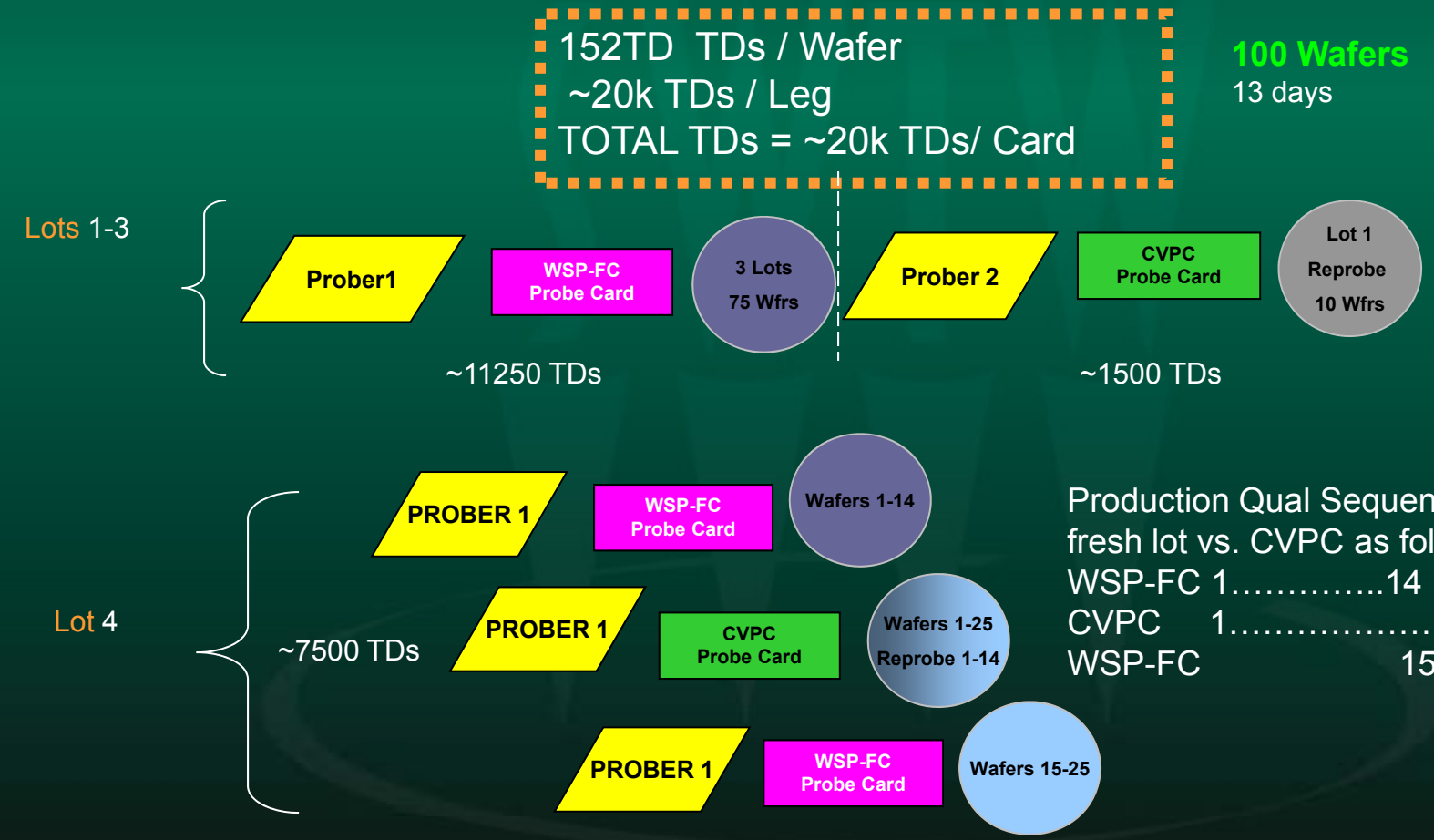
- 6 wafers were probed with CVPC, then reprobed with WSP-FC.
- WSP-FC CRes STD data is statistical significantly lower than CVPC.
- WSP-FC showed better performance than CVPC in many of the major CTF probe attributes.
- As a result TQ was passed with a stable probe/clean process to then proceed to the Production Qualification Phase.



Production Qualification

- Production Qualification consisted of 4 lots under EWR- Engineering Work Request.
- A 1 : 1 comparison of CVPC vs WSP-FC technology was performed on one lot. Probing each wafer in that lot with both technologies.
- Cleaning interval for WSP-FC was optimized to every 50Tds.

Production Qualification: Test Flow



Production Qual Sequence run on 1 fresh lot vs. CVPC as follows:

WSP-FC 1……..14

CVPC 1……..25

WSP-FC 15……..25

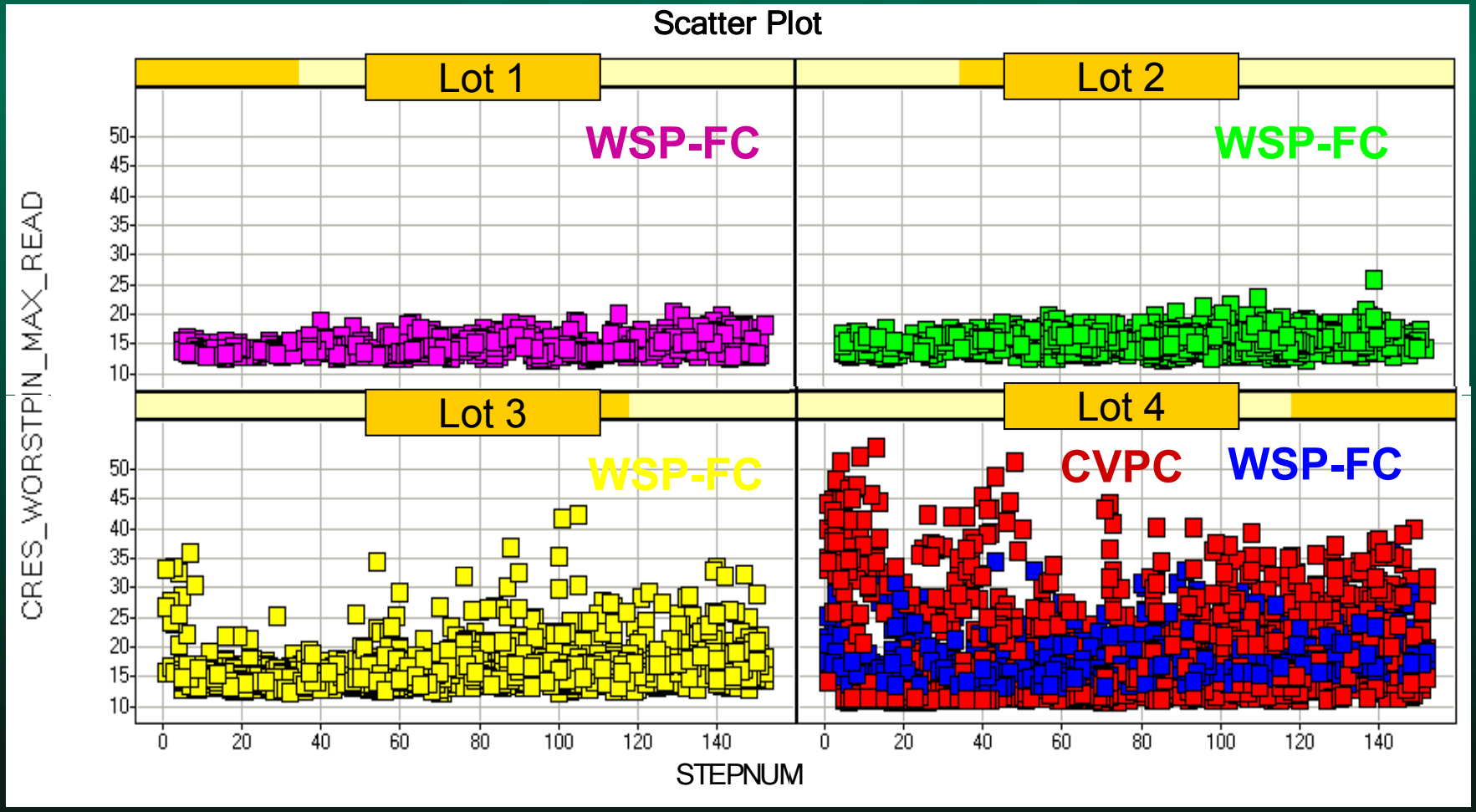
Input Variables:

- CVPC Probe Head
- WSP-FC Probe Head
- Prober to Prober
- Wafer to Wafer

Output Variables:

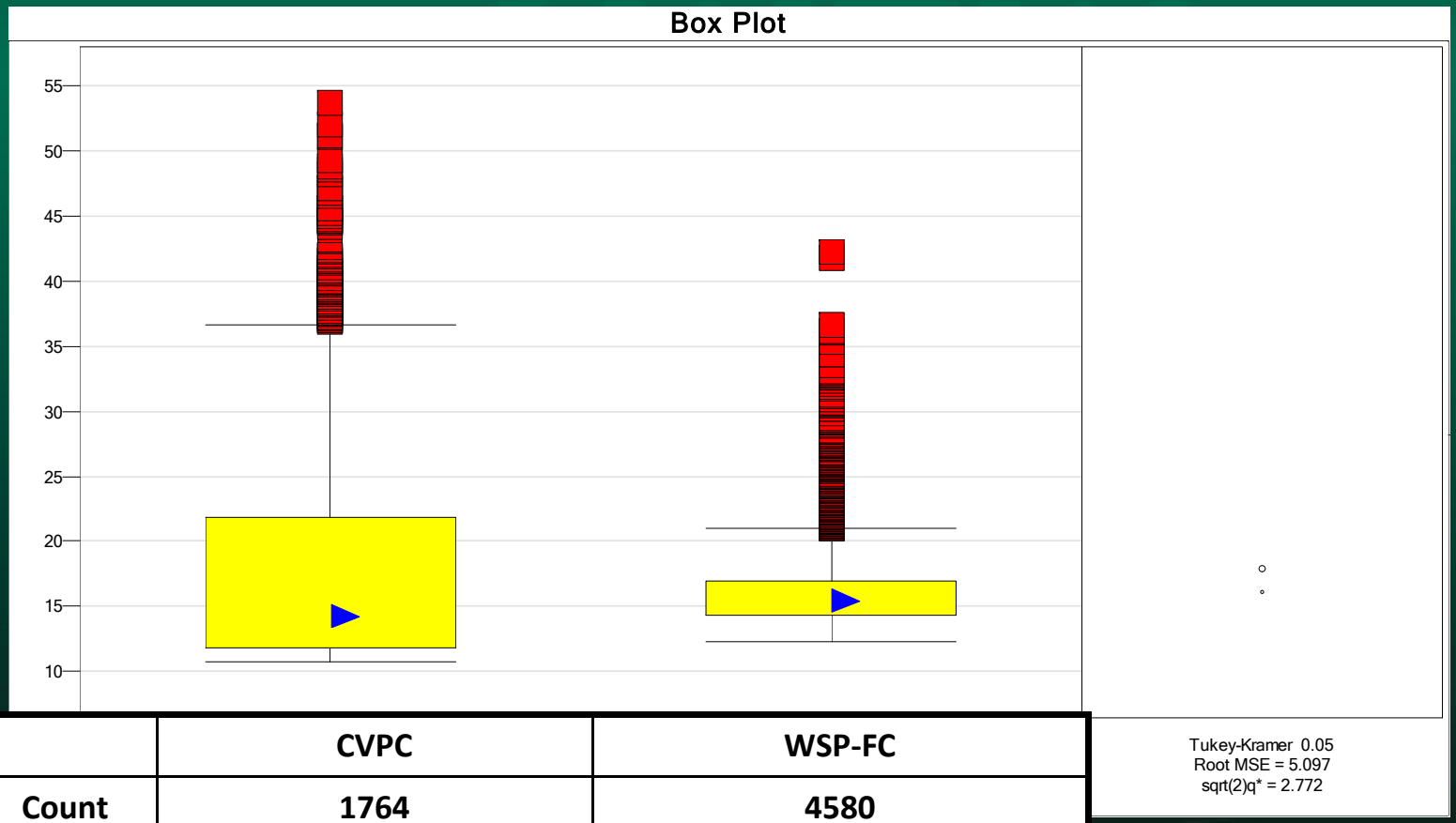
- CRes
- Yield
- Planarity
- Alignment
- Reprobe Rate
- Tip Length (Lifetime)
- Test / Wafer Time
- Bump Damage (AVI)
- Reliability

Production Qualification: CRes Characterization



In Production Qualification, WSP-FC CRes data is more stable except in yellow lot where increased cleaning interval was explored. The red / blue lot does have overall higher CRes than other lots, but WSP-FC CRes is still lower.

Production Qualification: CRes Characterization



	CVPC	WSP-FC
Count	1764	4580
Median	14.2	15.4
StdDev	8.4	3.0

CRes StdDev of WSP-FC is statistically significantly lower than CRes of Baseline CVPC over the span of Production Qualification.

Production Qualification: CVPC vs WSP-FC Comparison

	CVPC	WSP-FC
Pin Count	~6,000	~6,000
Pitch (um)	~190	~190
POT (um)	LT+60	LT+60
Clean Freq.	50 PTds	50 PTds
Alignment (um)	15um	30um (Self-Aligns)
Yield %	BASELINE	↑5.30%
Cres Mean Ω	BASELINE	↑ 1.2Ω
Cres STD Ω	BASELINE	↓5.42Ω
Force/pin @OT (gm)	19.2g	5.5g
Repairability	Depends on damage	Single-pin replaceable
Bump Damage	Flattens top of bump	4 small dimples on side
CCC (A)	1.2A	1.4A
Min. Pitch (um)	100um	150um
Max OT	220um	250um
Planarization	Required	Not Required

WSP-FC Production Qualification: PASS

WSP-FC shows better performance than CVPC in many of the major CTF probe attributes. Production Qualification of WSP-FC was passed and WSP-FC recommended to RTP – Release to production.

Key Observations:

- The “probe physics” of the WSP-FC or interaction of the crown tips with DUT solder bump better addressed the min CRes required and lower force requirements for high-bump count devices w/ higher CCC required.

- PCO-probe card operations were simplified:
  - Ease of repair
  - Planarization not required
  - Head exchangeability

- Improved Yield $$$

Summary:

- WSP-FC technology is a viable alternative to conventional probe solution for flip-chip bumped devices with enhanced performance overall, i.e., Lower force and CRes variability.

- As a result, TI will begin releasing this technology on production test floors and begin the transition from canti-bump and CVPC to WSP-FC as production and test configurations warrant.

ACKNOWLEDGEMENTS

Dallas Test Floor
Joey Perry
Dana Nichols
Alysa Rickman
Nayef Saleh
James Tong

Akira Okuma
Makoto Yumino
Satoshi Shoji
Masahiro Takahashi
Osamu Ito
Kondo-San