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Semiconductor Wafer Test Workshop

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Novel Vertical MEMS Probe Card for High Speed Devices

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Agenda

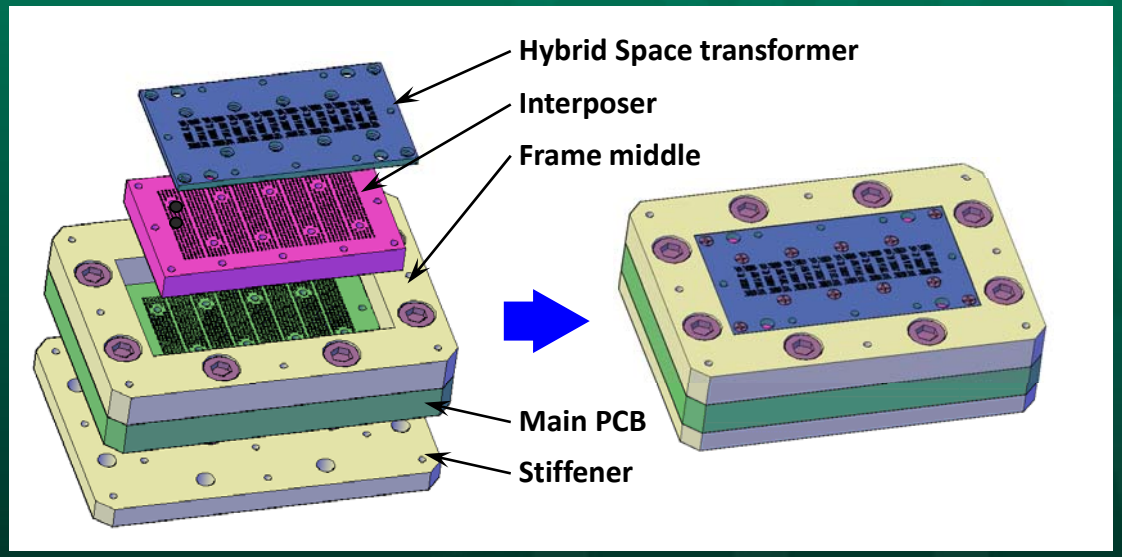
- **Outline**
- **Structure of "G-probe" Probe Card**
  - MEMS Guide Probe block
  - Hybrid Space Transformer
- **"G-probe" Probe Card Example**
  - 1Para Wide I/O Memory
  - 16 Para Media SOC
  - Concept of block array for the multi-parallel test
- **Summary**

Challenges and Remedies

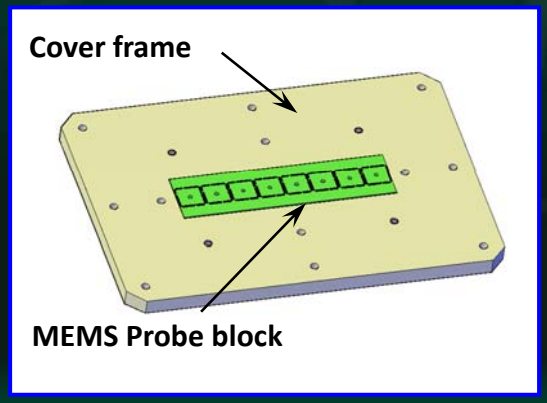
- Covering different pad arrays (LOC, Peripheral, Area) & fine pitch.
- Having the best and high accuracy of probe positioning.
- Having solution to make easy multi parallel testing.
- Making the low cost probe card.

- Small & thin probe tip
- Using Si wafer instead of ceramic guide
- Hybrid space transformer without MLC

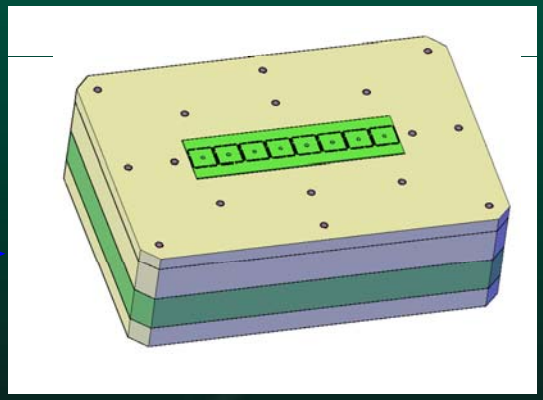
“G-probe” Probe Card Structure



Main PCB + Interposer + Space transformer assembly



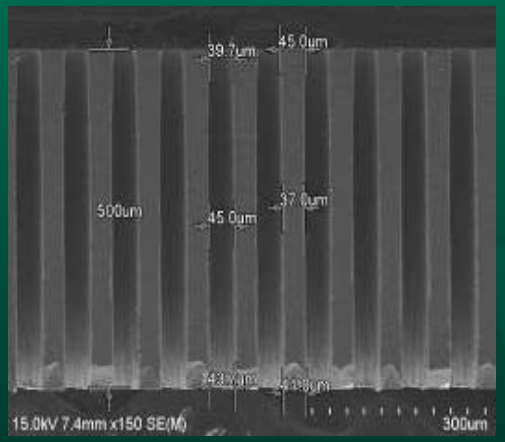
Probe block + Cover assembly



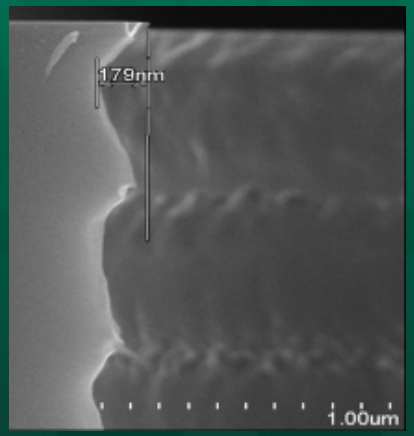
“G-probe” Probe Card

MEMS Probe Guide

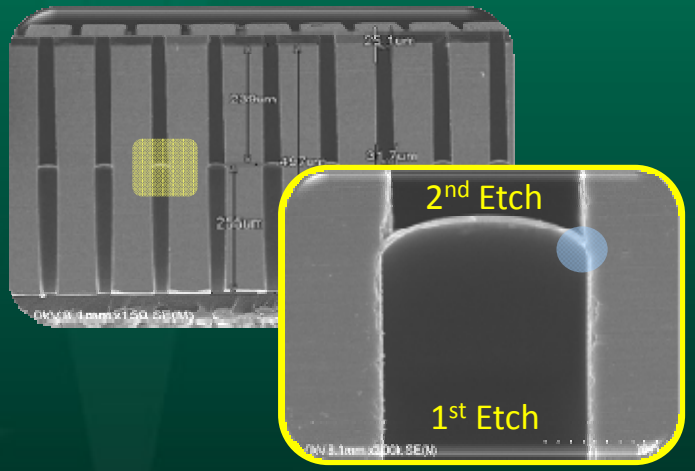
❖ 8” wafer etching (Deep RIE, Reactive Ion Etching)

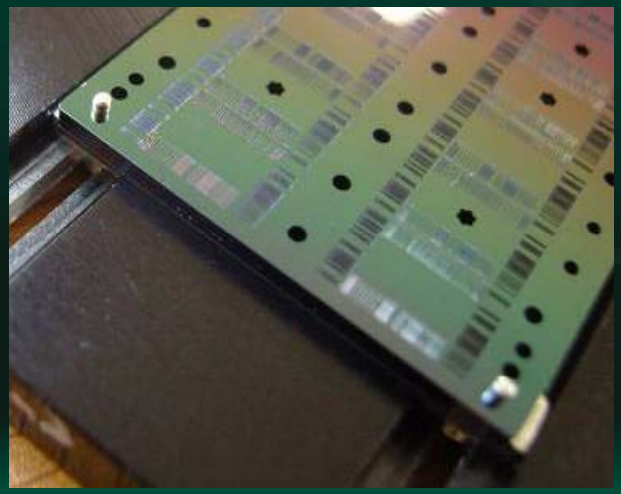


Cross section of etched hole



Scallop pattern

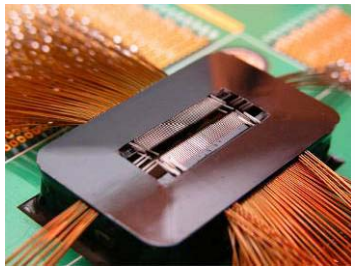




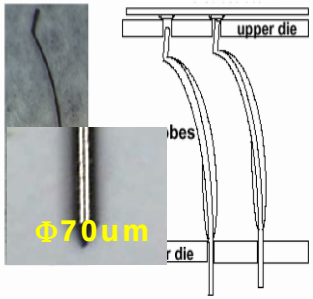
MEMS probe guide after bonding

- 500um thickness wafer thru hole etching
- Guide hole dimension accuracy : ±0.5um
- Guide hole position accuracy : ±0.5um
- Guide position accuracy after bonding : ±1.5um
- Scallop pattern of submicron
- Possible to etch the hole on both top and bottom side
- CTE matching with device by using Si wafer guide

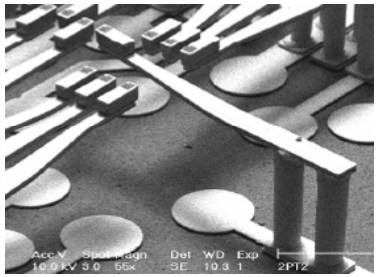
Probe Tip



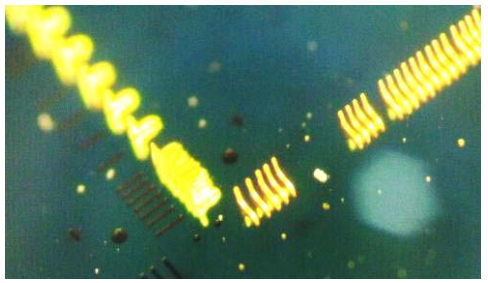
Cantilever



Vertical



MEMS



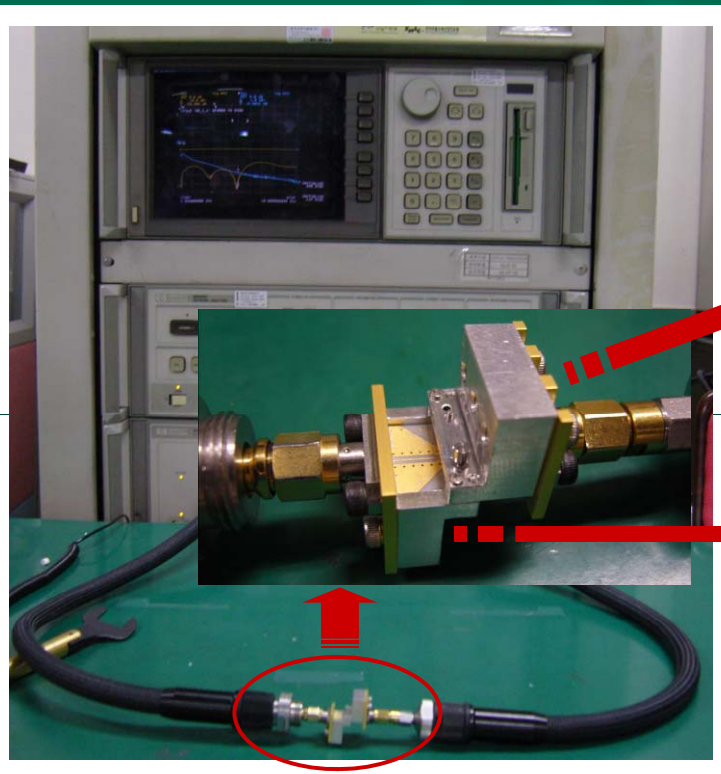
G-probe

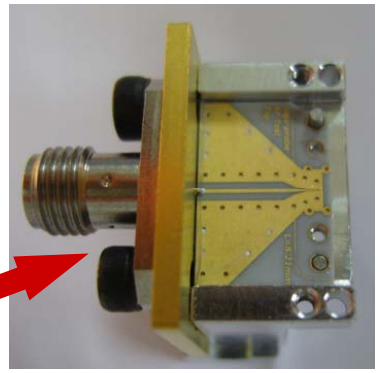
- G-Probe is a vertical probe, made by electroforming
- Planar 2D, Covers fine pitch
  - 20um pin thickness
  - Pitch, Inline : 40um, staggered : 20um, WLCSP : 130um
- Force
  - Cobra type : 5gf @ 70um travel
  - Spring type : 1gf @ 50um travel
- Good pointing accuracy by limited guide
- Covers LOC, peripheral, area pad arrays
- Small scrub limited by MEMS guide

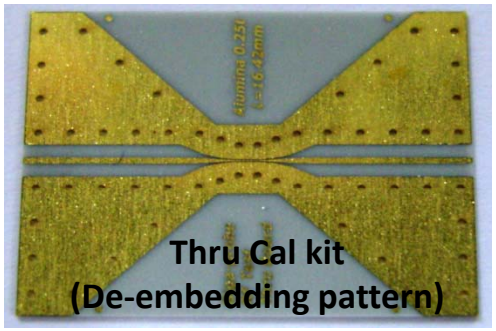
Cobra

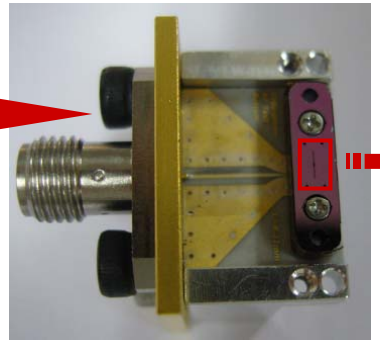
Spring

Test Equipment



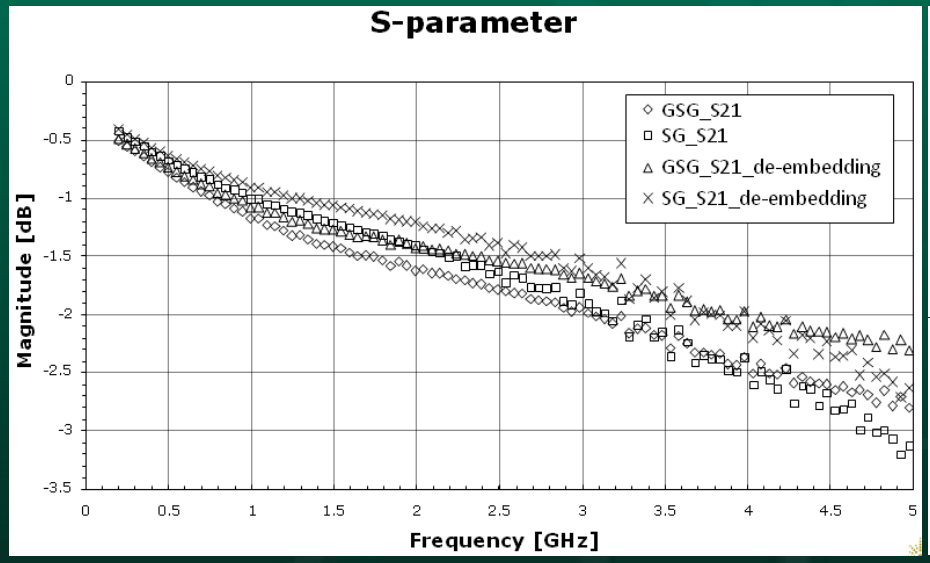


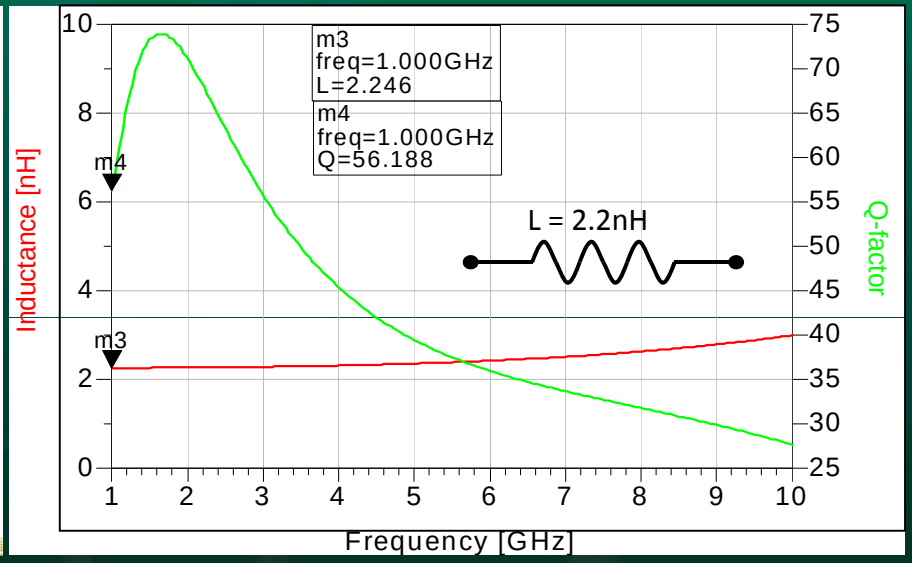




- Tester : HP 8510C Vector Network Analyzer
- Test Jig : UTF (Universal Test Fixture)
- Test pin : G-probe Cobra type , 80um pitch
- Pin array : GND-Signal-GND, GND-Signal

Test Data

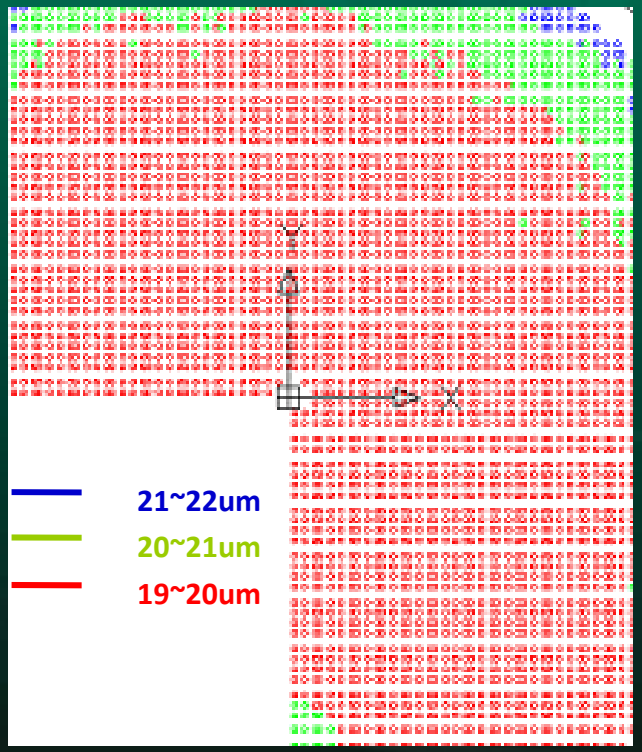




- Tip insertion loss (80um pitch, Probe Height: 2.93mm)
  - GSG type : 1.1dB @1GHz
  - GS type : 0.9dB @1GHz
- G-probe Model : 2.2nH High-Q inductor
- Good performance compare to cantilever type (GHz VS. MHz)

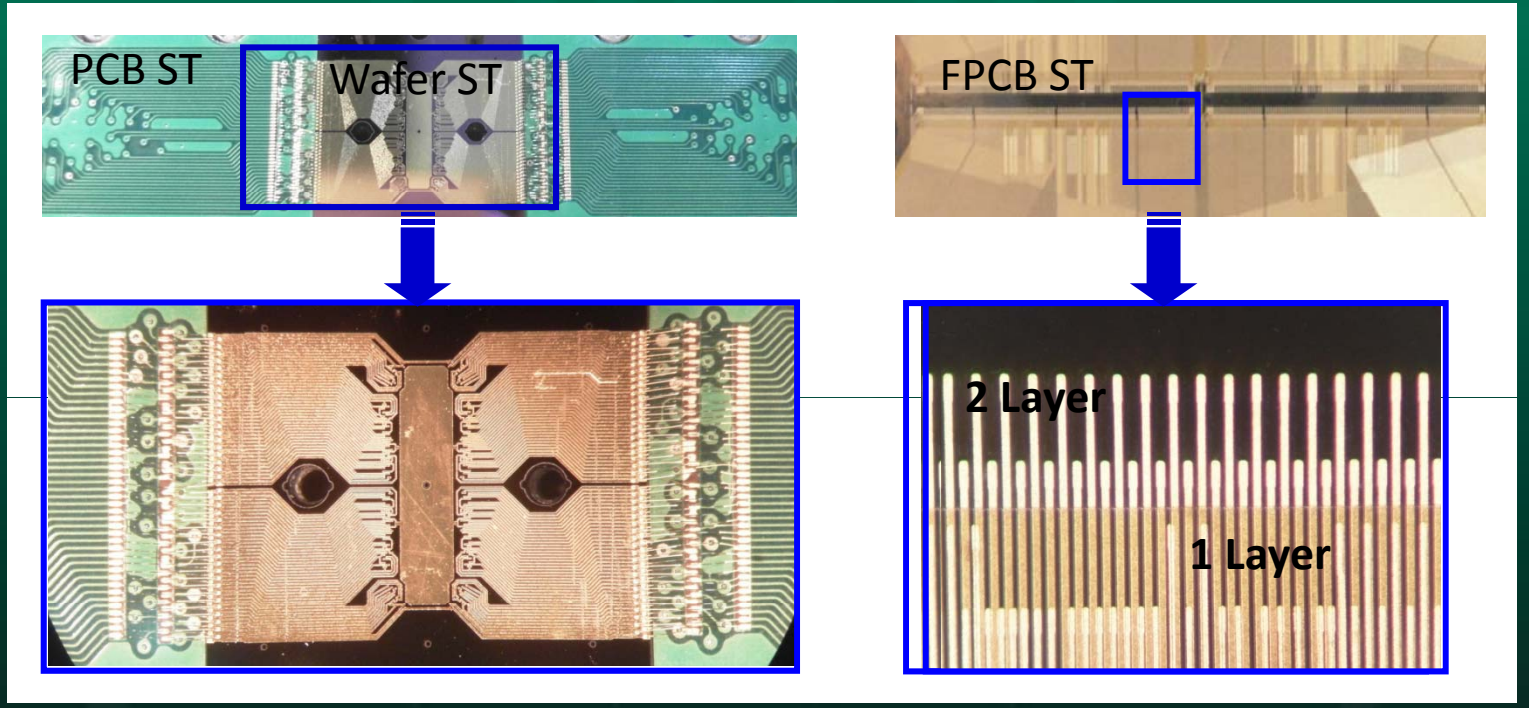
Probe Specification

❖ Thickness scatter



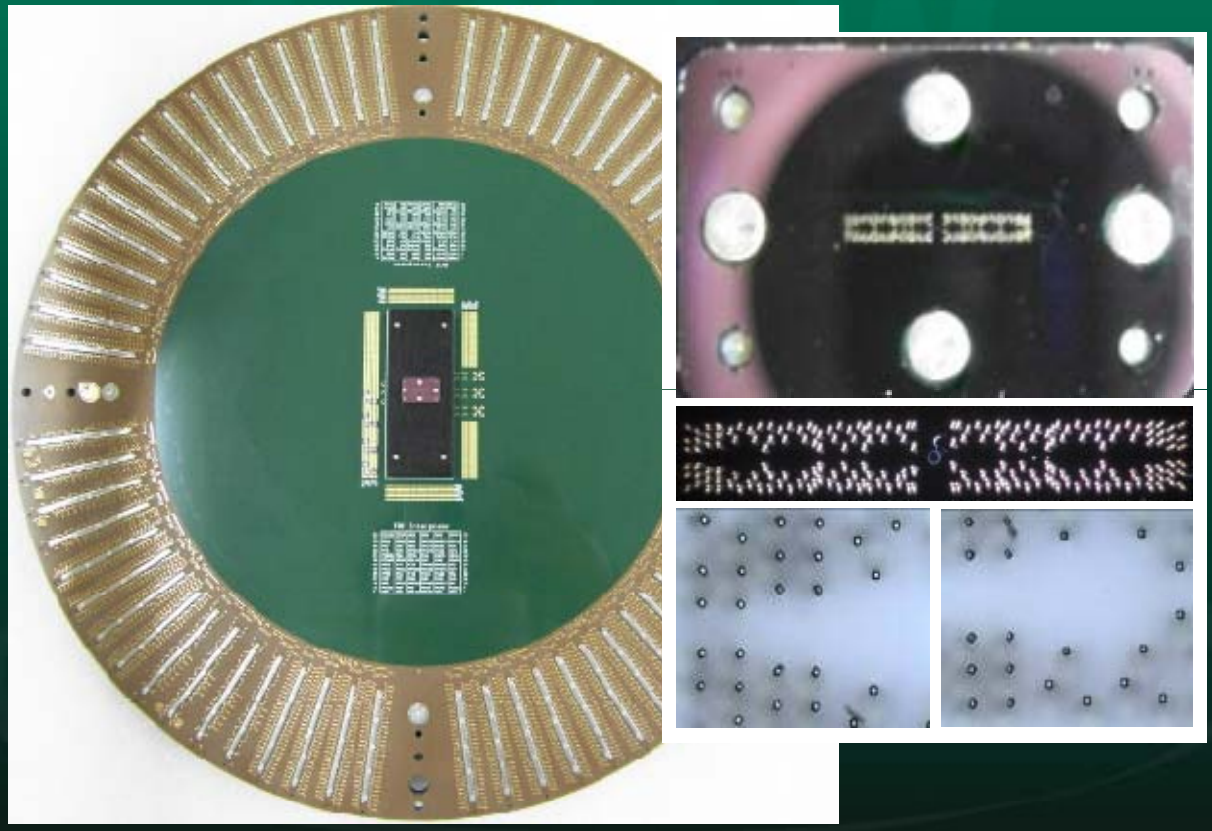
- Probe tip pointing accuracy : ±0.5um
- Probe thickness : 20um ±1.0um (>90% within 8” area)
- More than 20K probe tip within 8” area using electroplating process
- Low cost and easy fabrication process

Space Transformer



- Hybrid space transformer construction
  - Si Wafer, rigid PCB, FPCB
- Fine-pattern process (width 10um, space 10um)
- Multilayer, ∅10um small via process
- CTE matching with device because of using Si wafer
- Low cost and fast delivery

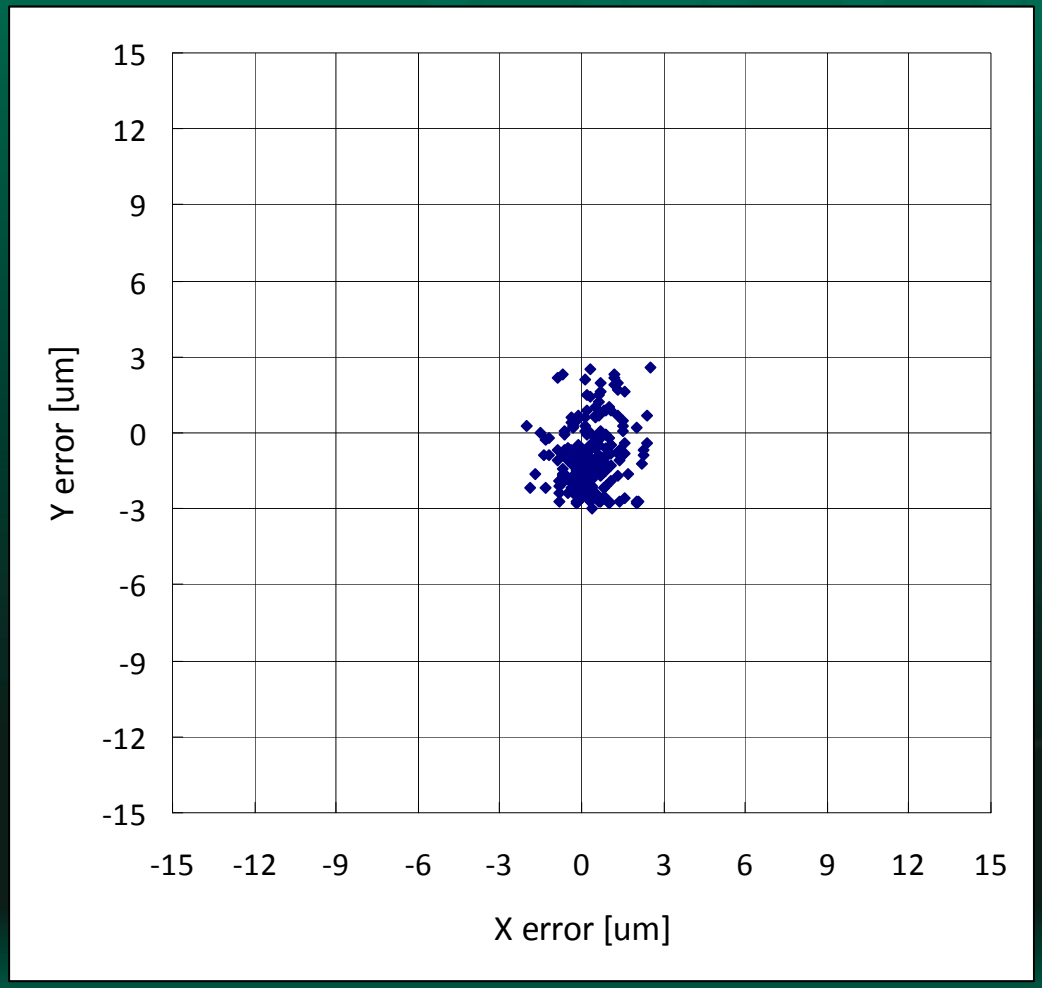
G-probe Example 1

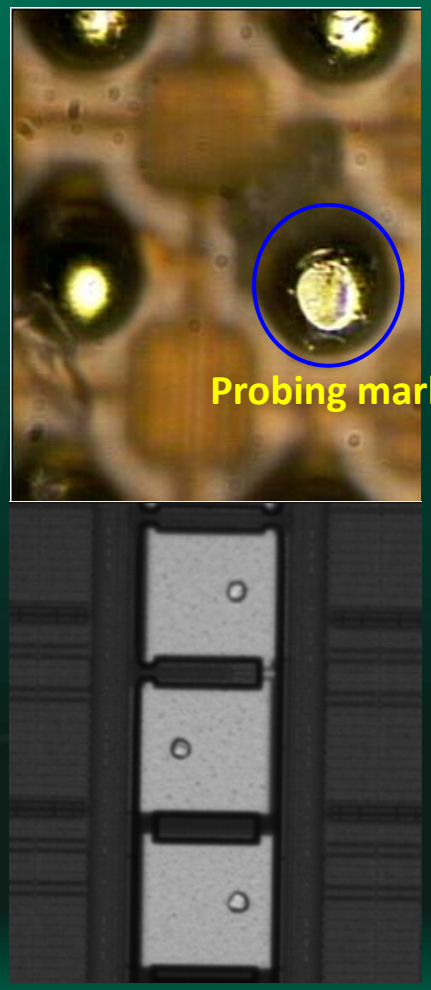


- Application: Wide I/O Memory Bump
- Device pitch, X:50um, Y:40um
- Ball Bump Size : Φ 20um
- 1-PARA / 200 Probes
- Probing pitch, X: 50um, Y:120um
- Pointing accuracy: ± 3um, Planarity : ±2um

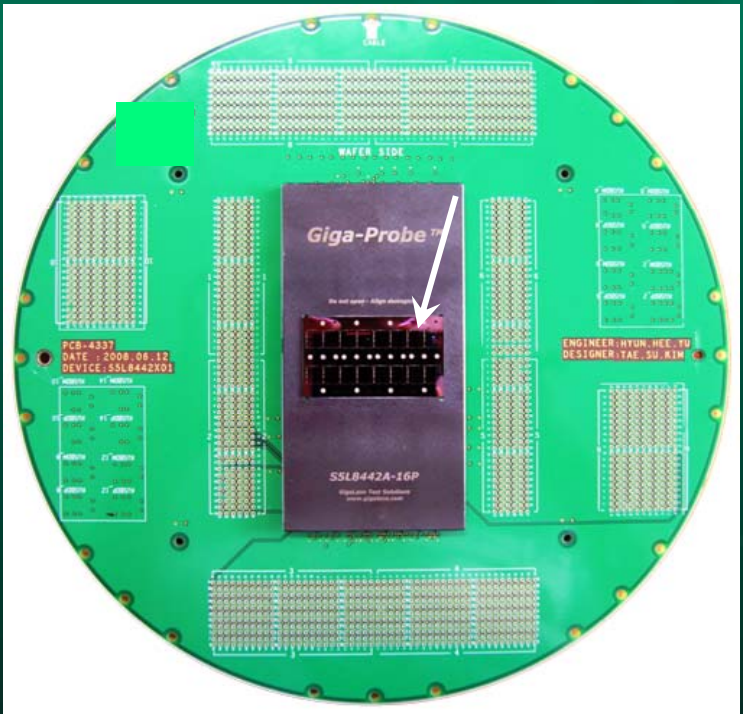
G-probe Example 1

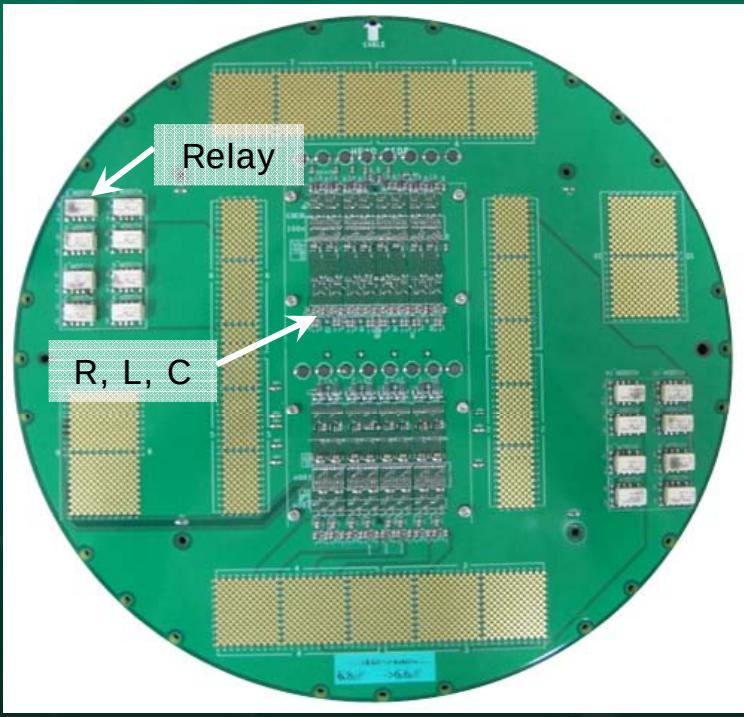
- *G-probe Position Scatter & probing mark*





G-probe Example 2

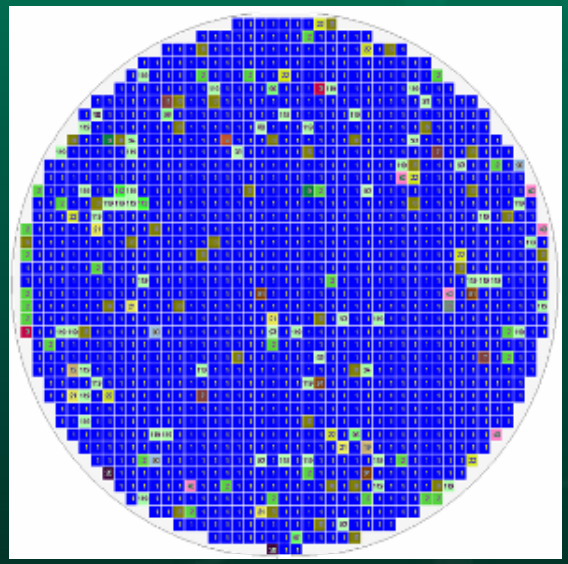




- **Device : Media SOC**
- **I/O Pad configuration : Peripheral in-line**
- **Pad pitch : 50um**
- **Probe block area : 50.72*20.57=1043.3mm²**
- **Pin count : 213x16=3408 probes**
- **Probe card interface : *Teradyne UltraFlex™***
- **Array :**

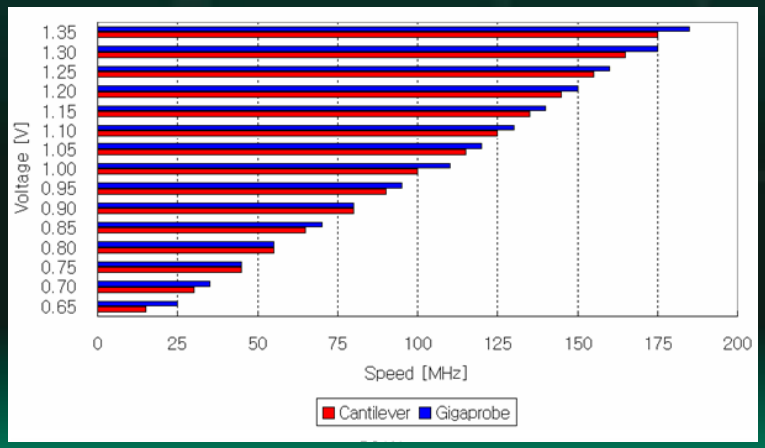
G-probe Example 2

❖ G-probe wafer test Map



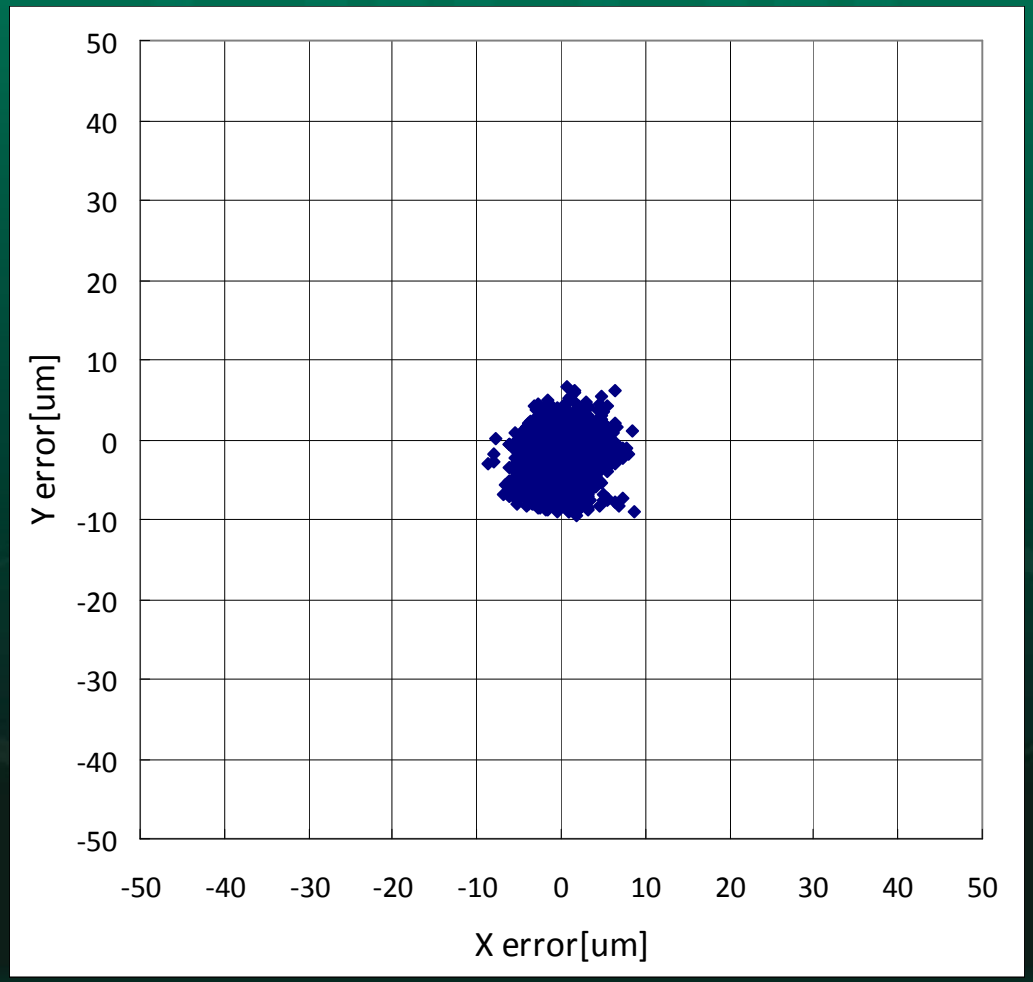
	4Para Cantilever	16Para G-probe
Test yield	79.9 %	80.0 %
Open fail	0.1%	0.1%
Logic	3.1%	3.2%
BIRA	2.2%	2.1%
Etc.	14.7%	14.6%

❖ Shmoo for the BIST



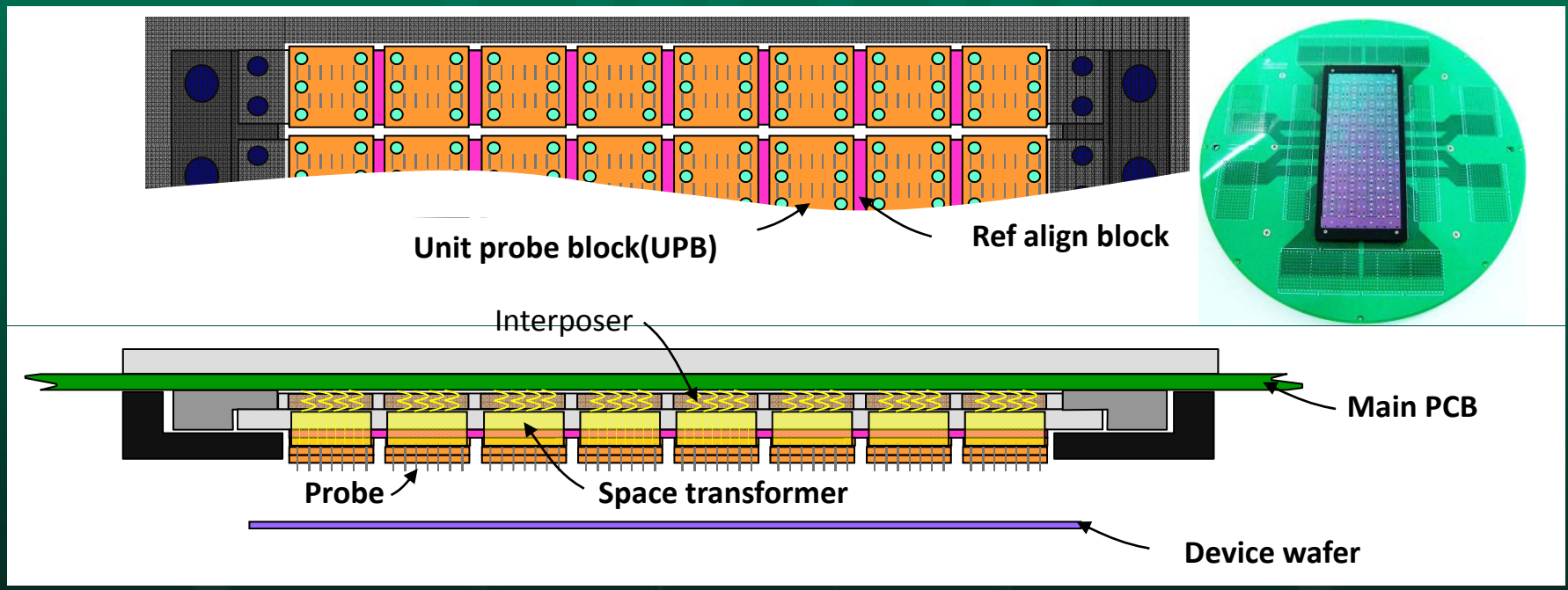
- Probe Card
  - 4Para Cantilever
  - 16Para G-probe
- Measure yield & shmoo with same wafer
- Better shmoo performance than cantilever
- Same Test Yield

G-probe Example 2



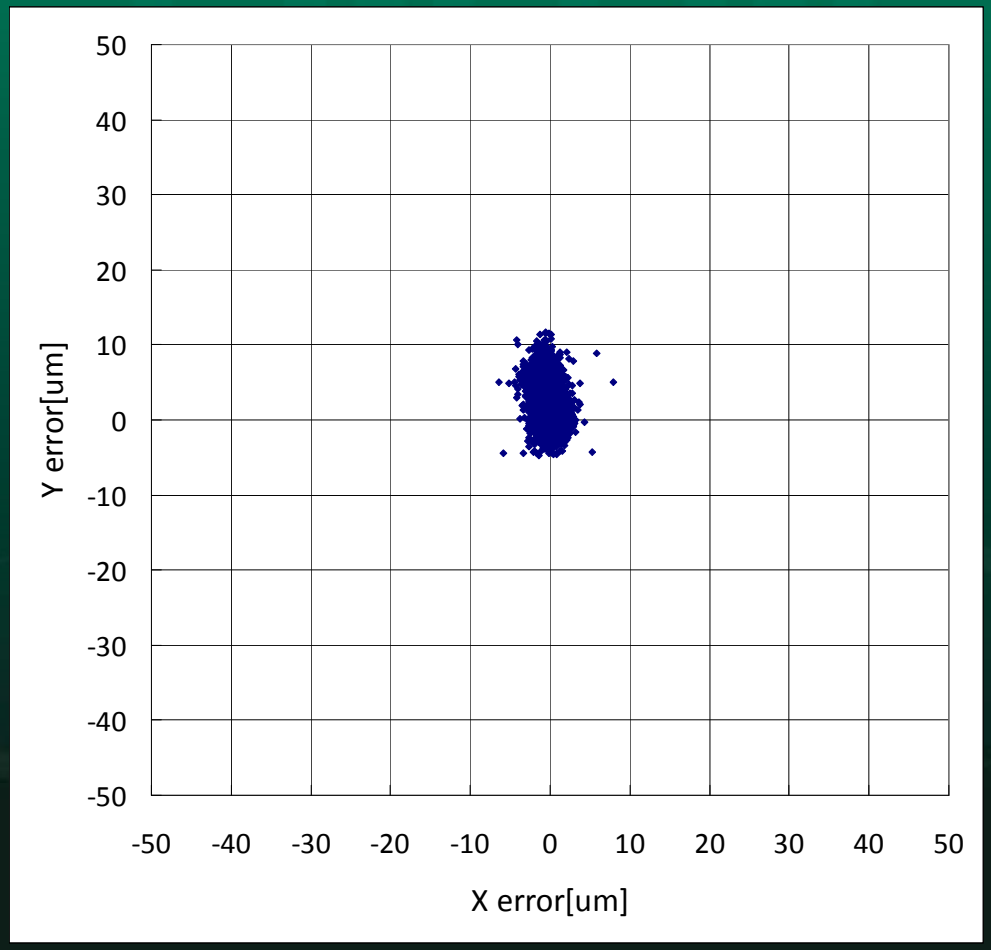
- **3408 probes positioning error < ±10um**

G-probe Example 3



- ❖ Advantage of block array "G-probe" probe card
  - Easy repair & assembly
  - Easy block array for the multi parallel test
  - Good CTE matching by using Si wafer for making UPB & reference align block

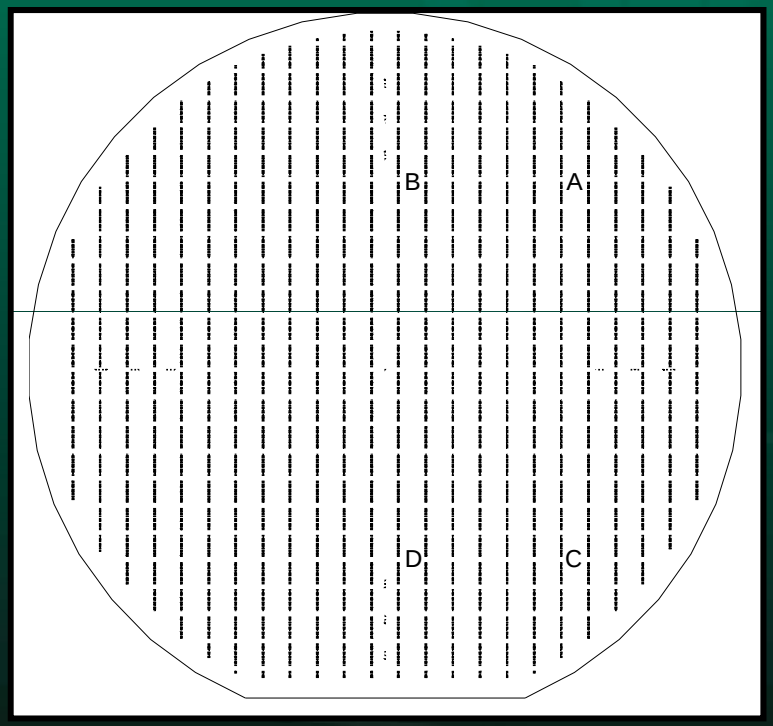
G-probe Example 3

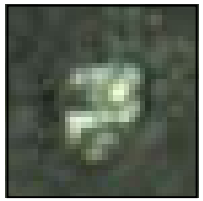
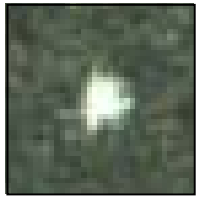
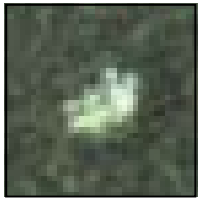


- **9600 probes positioning error < ±10um**

G-probe Example 3

❖ *Temperature test at 90°C*



B	A
	
D	**C**
	

- **Probing area : 60,700um*121,400um**
- **Probe tip size : 15~18 um**
- **Pad size : 70um*70um**
- **6 times touch down for 1hr at 90°C after initial probing (at room temp.)**
- **Good CTE matching**

Summary

- **Novel vertical MEMS probe card**
  - Overcomes constraint of traditional vertical probe card
    - Fine pitch : Inline 40um, Staggered 20um, Area 130um
    - Pad array : LOC, Peripheral, Area (WLCSP)
  - MEMS guide
    - Good position accuracy
    - CTE matching with device wafer
  - Hybrid space transformer
    - Low cost & fast delivery
    - CTE matching with MEMS probe block
  - Great multi parallelism solution

Thank You!