IEEE SW Test Workshop
Semiconductor Wafer Test Workshop

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Electromagnetic Analysis and Verification of Probe Card Performance for First Pass System Success

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Introduction

- **Today in Multi-Probe wafer level, test is increasing with highly needed frequency capability demands:**
    - RF ICs Wafer sort (WLAN, Bluetooth, GPS, WiMax etc.)
    - Final Test capabilities at EWS (multi Gigabit x second channel)
    - Known-Good-Dice (KGD)
- **New high-speed ATE platform are already in the market**
- **This creates new and exciting challenges for Probe Card development**

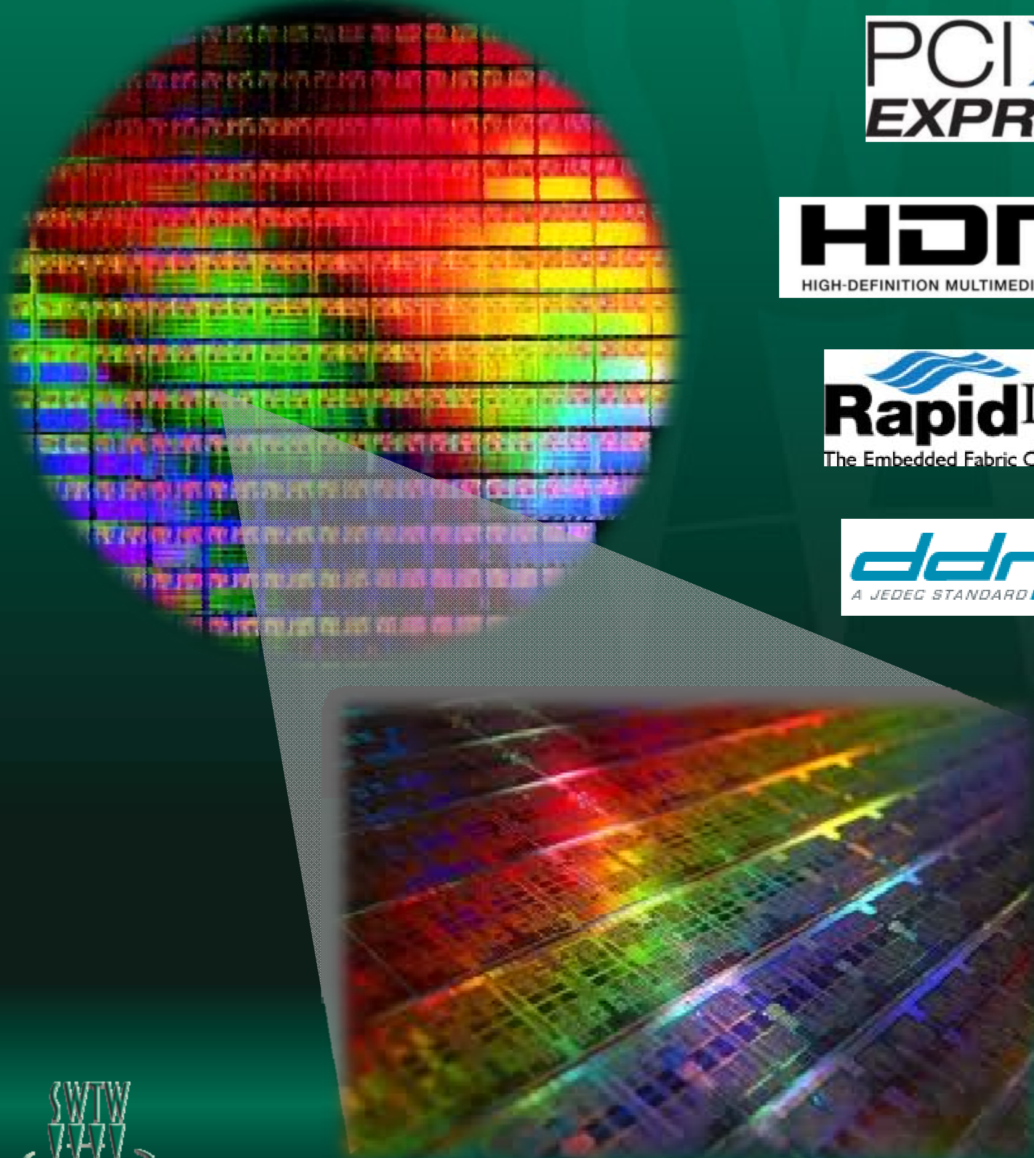
Objective

- **Probe Card lead time becomes the main challenges for high frequency design:**
  - An example could be 5 - 6 working weeks for vertical PC
  - This means a very short time window for Probe Card design (usually no more than 2 weeks)
- **There is not enough time for prototyping and lab test/debug:**
  - Directly deliver *good* and *full functional* PC to customer
- **The goal of this presentation is to show the usage of *HF Simulation Methodology* for addressing all design issues prior to manufacture Probe Card**

Agenda

- Probe Card Design Flow for high speed performance
- Step by step Signal Integrity Analysis and simulation examples on Probe Card system
- Step by step Power Integrity Analysis and simulation examples on Probe Card system
- High Frequency Probe Card example

Wafer DIE: Many HF Standard



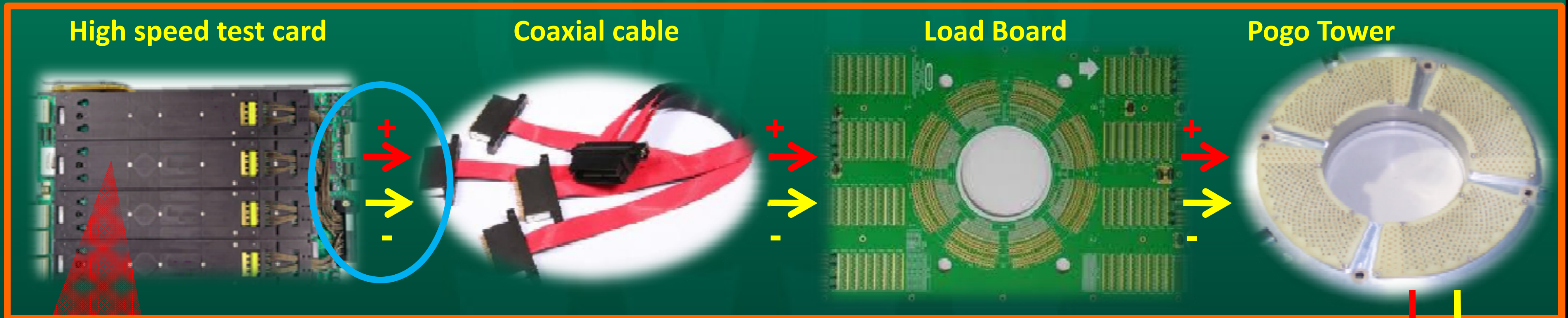
SWTW

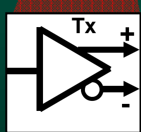
Standard High Speed Data Rate

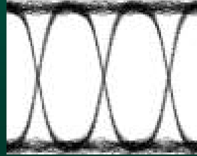
Standard	Data Rate (GT/s)
PCI Express	2.5 / 5 / 8
USB 3.0	5
RapidIO	1.25 / 2.5 / 3.125 / 5 / 6.25
DDR3	0.800 / 2133
HDMI	10.2
DisplayPort	1.62 / 2.7 / 5.4
InfiniBand	2.5 / 5 / 10 / 14.0625 / 25.78125
Serial ATA	1.5 / 3 / 6
Serial Attached SCSI	1.5 / 3 / 6
Fibre Channel	1.0625 / 2.125 / 4.25 / 8.5 / 10.53 / 14.025

GT/s – Giga Transfer per Second – raw bit rate (i.e. including balance bits due to 8B/10B encoding)

EWS System: Many Interconnections

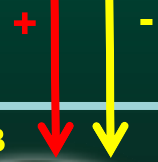


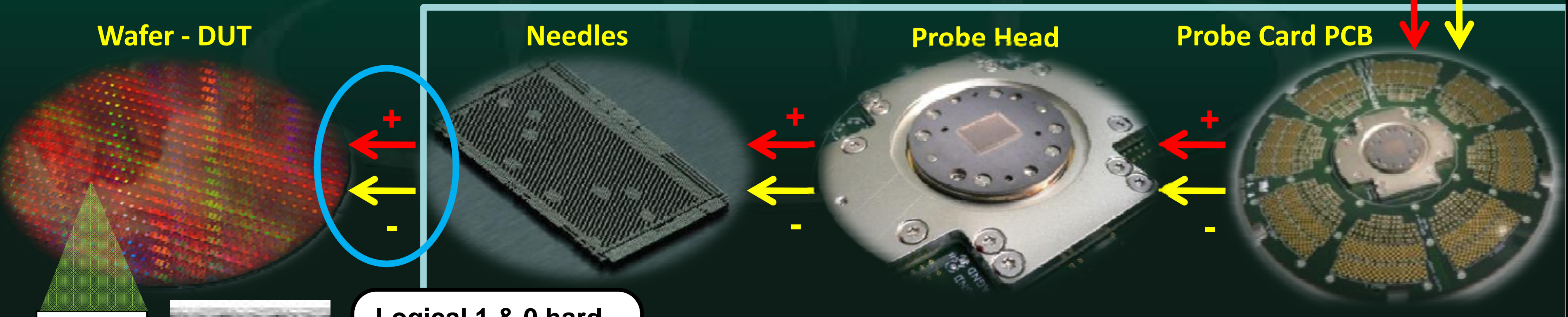


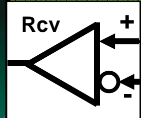


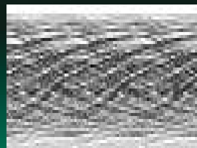
Clean, open, logical 1 & 0 at launch from transmitter

ATE SYSTEM









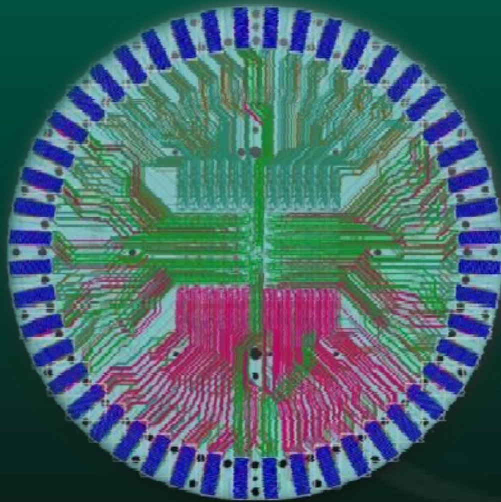
Logical 1 & 0 hard to distinguish at end interconnects; CLOSED EYE

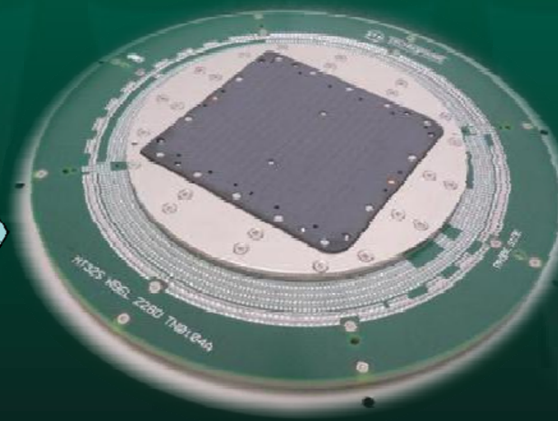
PROBE CARD SYSTEM

Traditional PC Design Flow

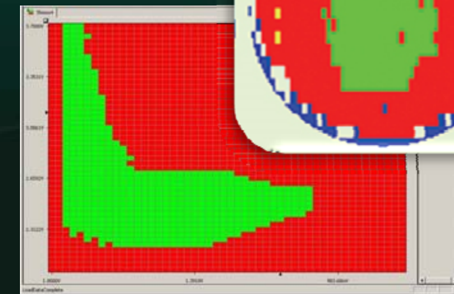
Layout Tool:
Cadence, Mentor, Zuken, Altium…

PC manufacturing





EWS pass test?

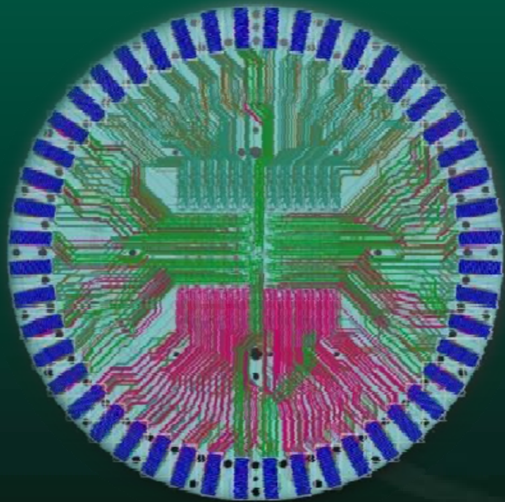


Start again…

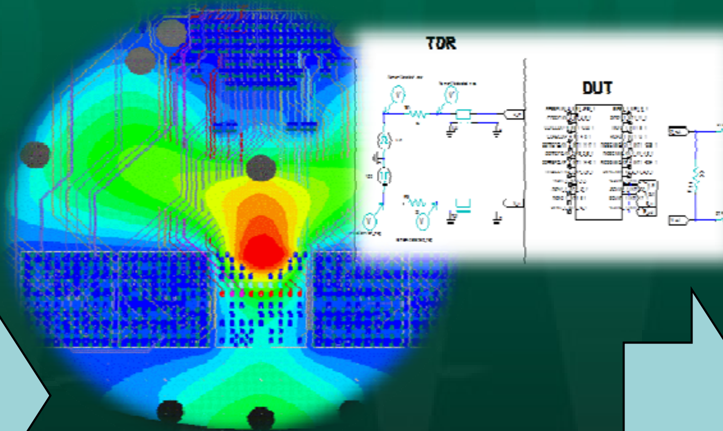
Drawbacks
Money for PC re-build
Time for building them
CUSTOMER CLAIMS

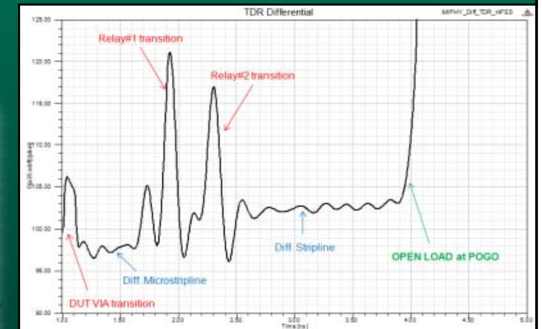
High Frequency PC Design Flow

Layout Tool:
Cadence, Mentor, Zuken, Altium…

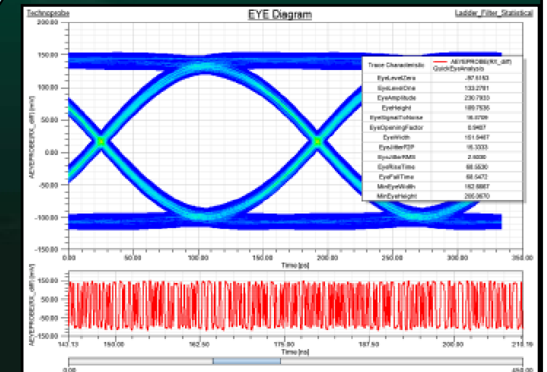


Virtual Prototype:
Field Solver + Circuit Simulator





Simulation:
Fit Specs?

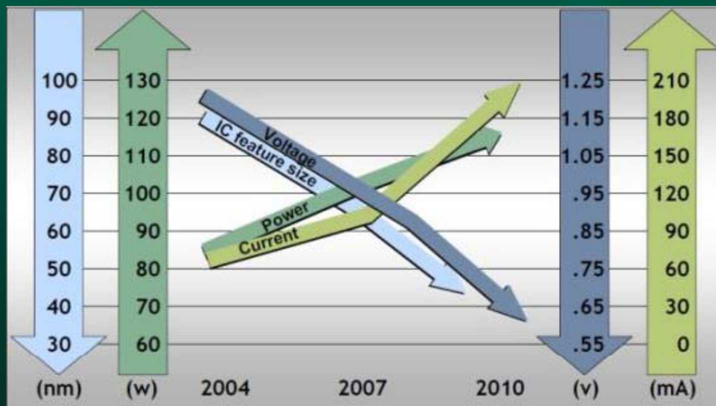


Benefits
No prototypes
Save time and money

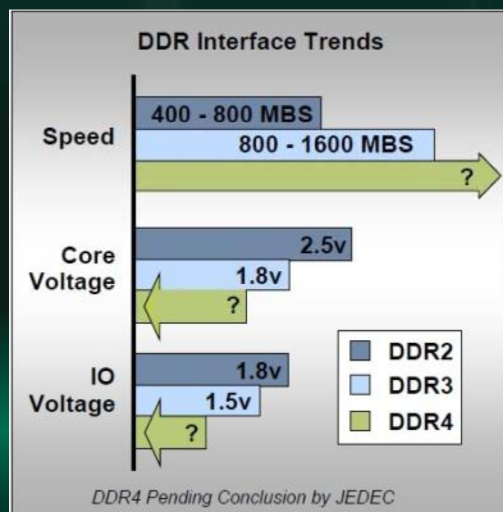
Choose your strategy and verify it by simulation

HF PC Design Flow Requirements

- **Design challenges to take into account during Probe Card development:**



  - Low voltage, high current Power Delivery System (PDS):
  - Need to accurately control **Power Integrity**



  - High frequency, high speed analog and digital signals:
  - Need to accurately control **Signal Integrity**

Signal Integrity Check-List

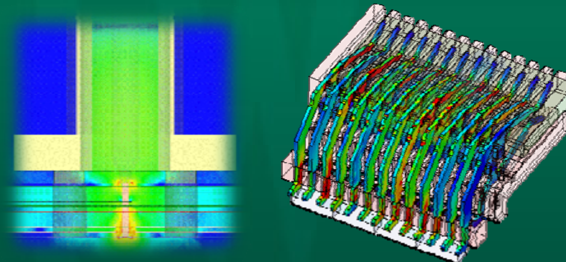
- **Stackup analysis and Impedance control**
- **Frequency Domain analysis (Linear-Network-Analysis):**
  - Insertion Loss (IL), Return loss (RL), Coupling (X-talk), Bandwidth performance (-1dB; -3dB)
- **Time Domain analysis (Transient analysis):**
  - TDR/TDT, rise/fall time, overshoot/undershoot, VIL/VOH margin, ringing etc.
- **Cross Talk analysis:**
  - Near-End-Xtalk (NEXT), Far-End-Xtalk (FEXT), noise from multiple aggressor
- **SSNO analysis (Simultaneous Switching Noise Output)**
- **EYE diagrams, BER, Jitter, Skew etc.**

Power Integrity Check-List

- **Verify noise margin:**
  - IR Drop (DC)
  - Power Plane impedance profile vs frequency (AC)
- **Current distribution:**
  - High density current, bottleneck → hot/heat source
- **Decoupling capacitor solutions, tuning and optimization:**
  - Decoupling capacitor configuration, number of components, placement location, mounting effect, parasitic effect (ESR,ESL)
- **Resonance modes:**
  - Identify location and frequency of natural cavity resonances that exist between planes (power and ground bouncing)

Which ElectroMagnetic Simulator?

- **3D Electromagnetic Field Solver**
  - Need to accurately characterize and optimize 3D interconnections (needles, connectors, VIAs etc.)
  - Solve the full Maxwell's Equations on each mesh element (FEM)
  - Rigorous and accurate approach, but cannot be used for PDS characterization

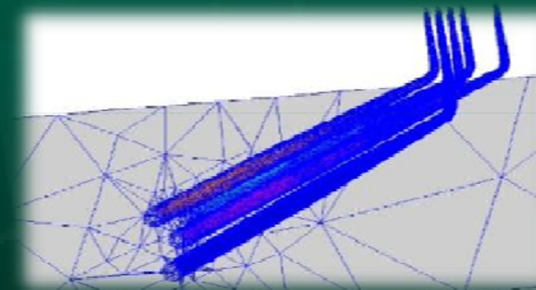


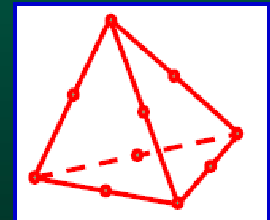
$$\nabla \times E = -\frac{\partial B}{\partial t}$$

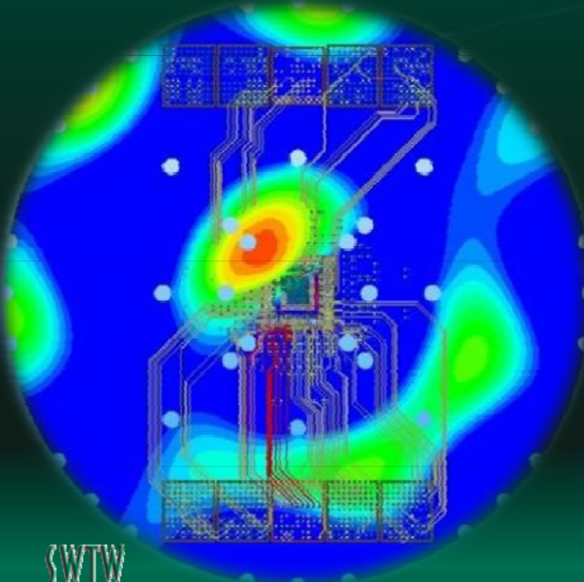
$$\nabla \times H = J + \frac{\partial D}{\partial t}$$

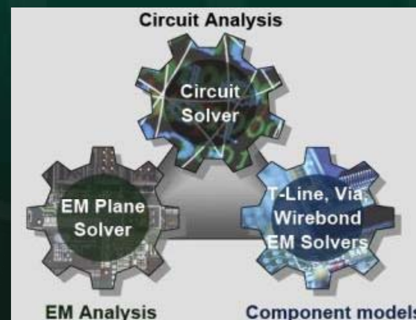
$$\nabla \cdot D = \rho$$

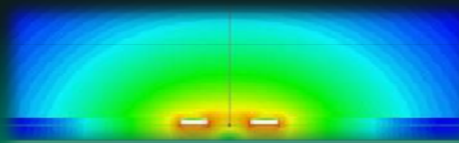
$$\nabla \cdot B = 0$$





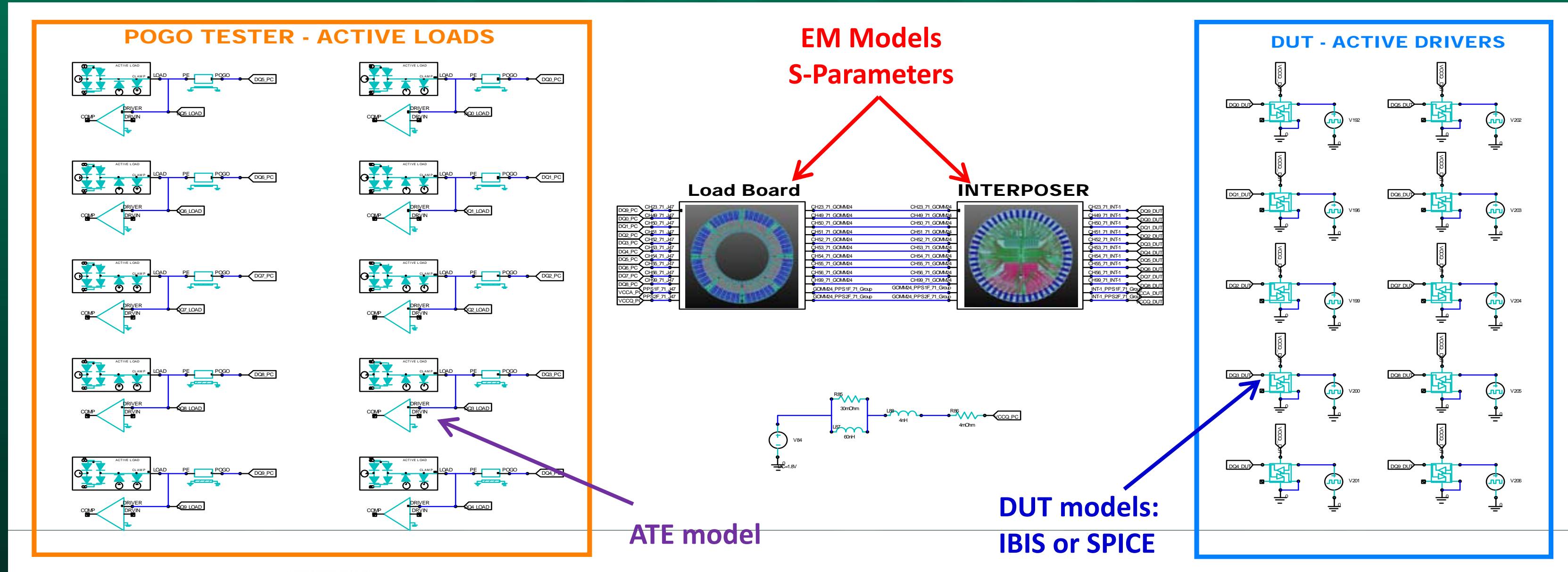


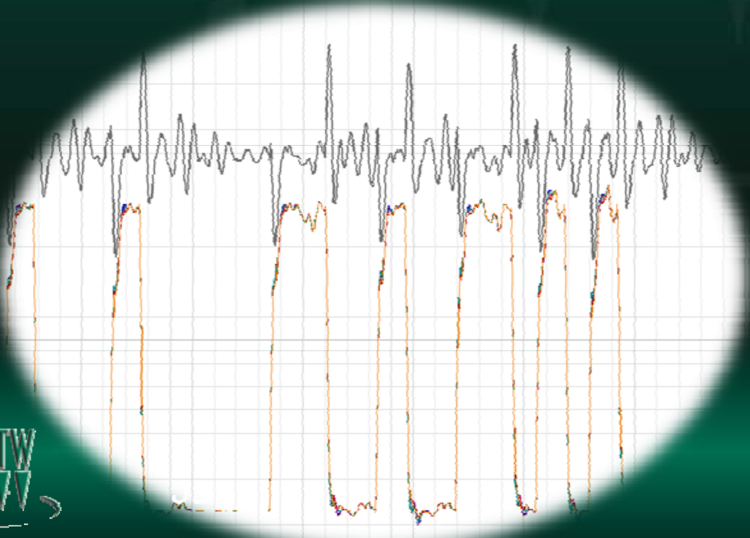


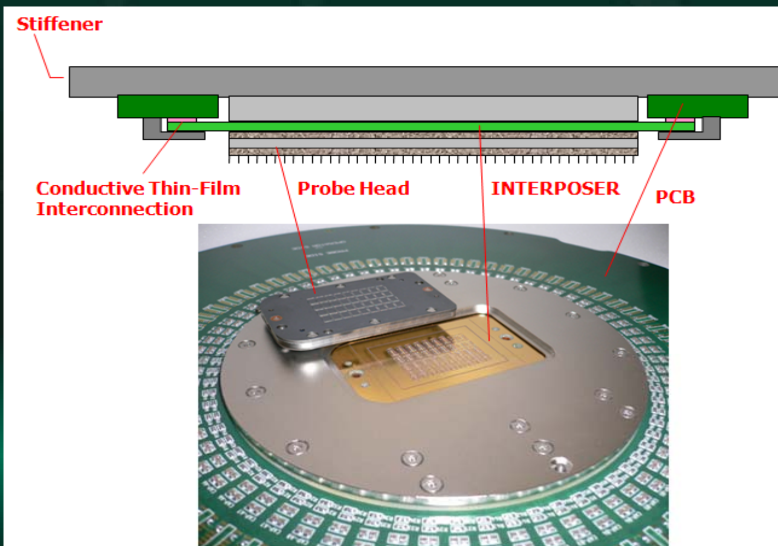


- **2.5D Electromagnetic Field Solver**
  - Need to accurately characterize and optimize PCB power delivery system (impedance/inductance, decoupling capacitors etc.)
  - Hybrid solver technologies is used for speed up simulation and characterize full PCB

Circuit Environment: Simulate Entire EWS System







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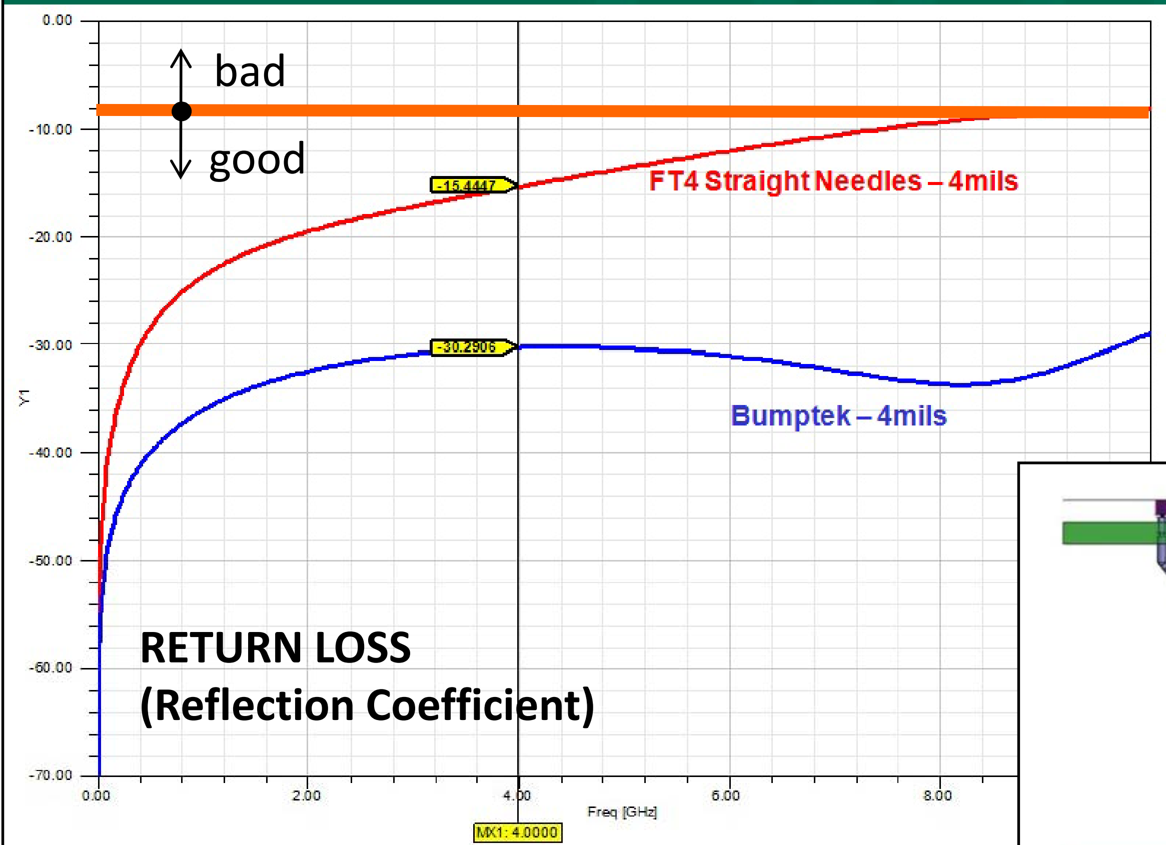
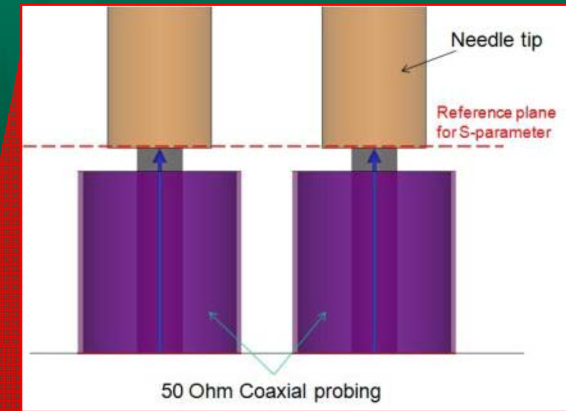
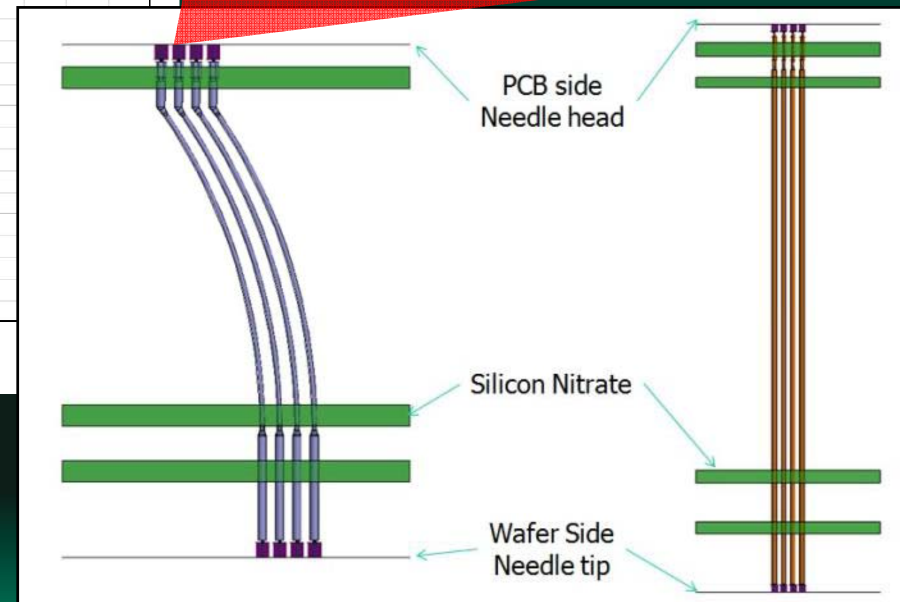
Signal Integrity: STEP #1

Needle Characterization

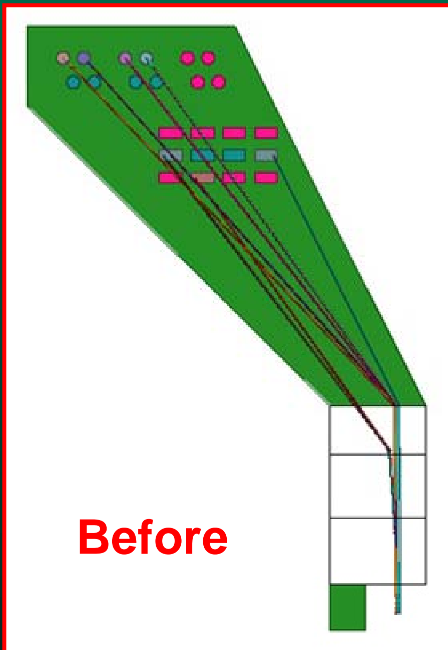


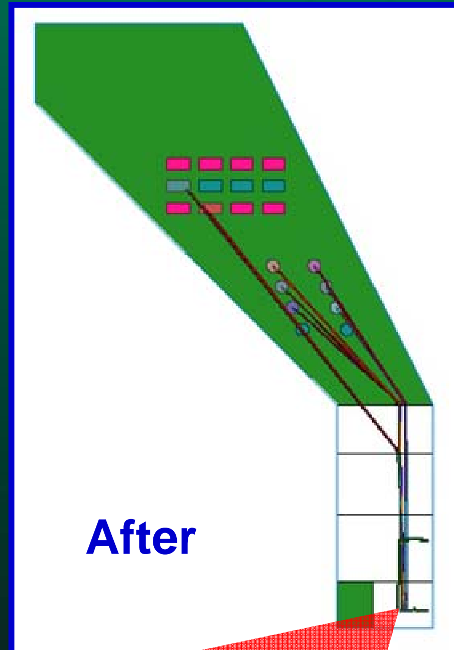


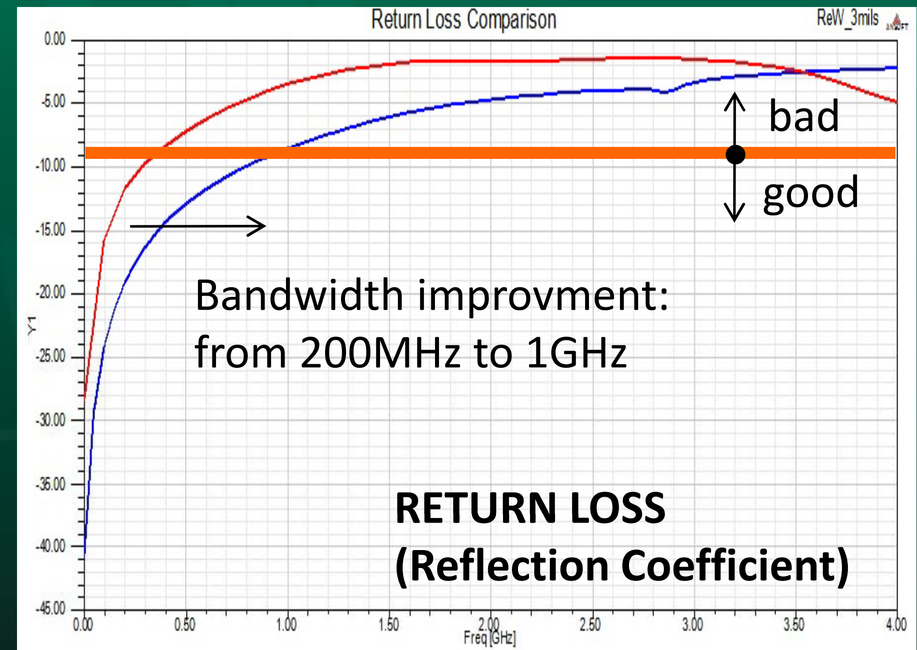


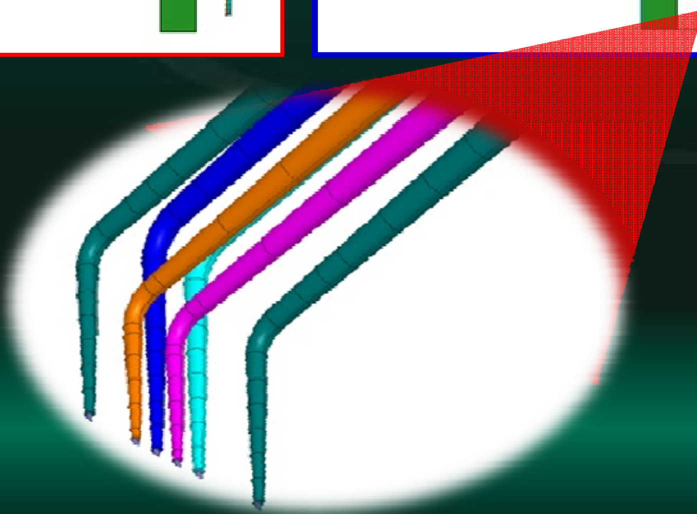
Signal Integrity: STEP #2

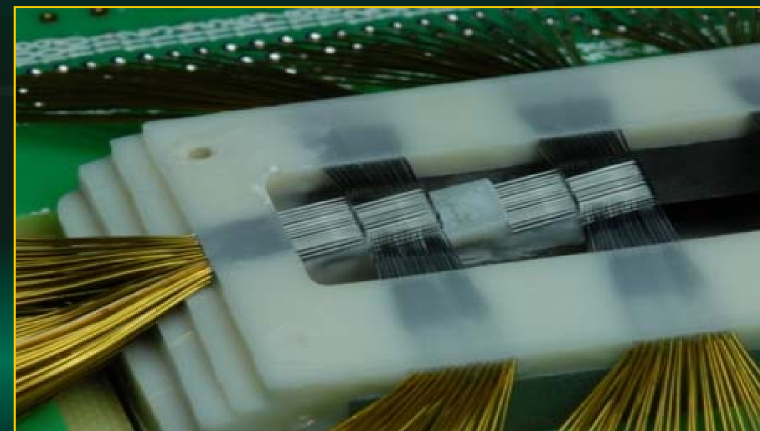
Needle Performance Optimization







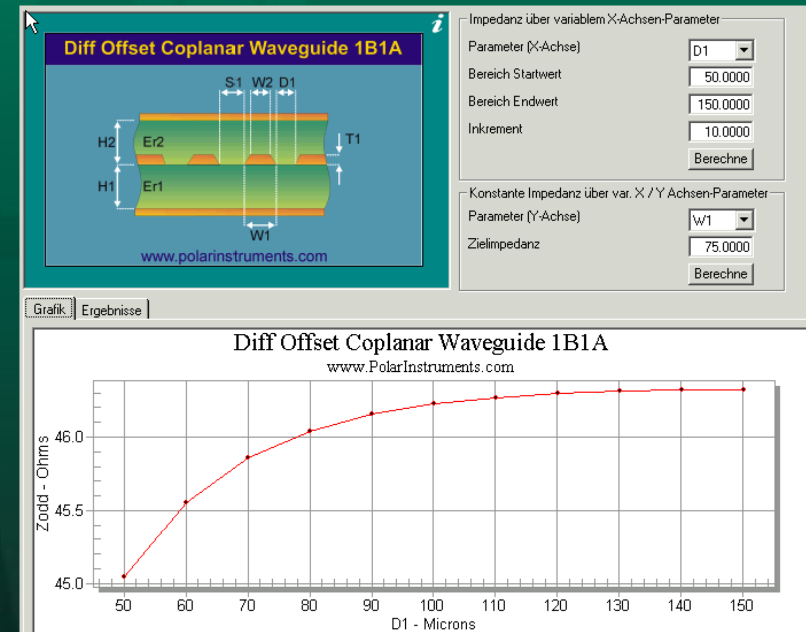




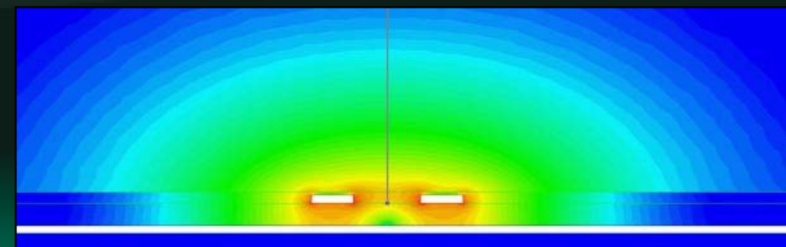
Signal Integrity: STEP #3

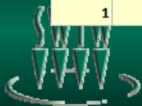
PCB Stackup Analysis and Controlled Impedance

Number		Layer	Thickness (um)	VIA Structure
	1	TOP	25	
		Pre-peg IS410	60	
	2	GND	17	
		Pre-peg IS410	60	
	3	SIG (Differential)	17	
		Pre-peg IS410	60	
	4	GND + SENSE	17	
		Pre-peg IS410	60	
	5	SIG	17	
		Pre-peg IS410	60	
	6	PWR (PWR VDD 1V2)	17	
		Core IS410	75	
	7	PWR (AVCC)	17	
		Pre-peg IS410	120	
	8	GND	35	
		Core IS410	100	
	9	PWR (VDD)	35	
		Pre-peg IS410	120	
9	10	PWR (VDD)	35	
		Core IS410	100	
8	11	GND	35	
		Pre-peg IS410	120	
7	12	SIG	17	
		Core IS410	75	
6	13	PWR (VDD_split)	17	
		Pre-peg IS410	60	
5	14	GND	17	
		Pre-peg IS410	60	
4	15	SIG	17	
		Pre-peg IS410	60	
3	16	SIG	17	
		Pre-peg IS410	60	
2	17	GND + Fanout	17	
		Pre-peg IS410	60	
1	18	BOT	25	



Differential Pair – Target Zo=100Ohm

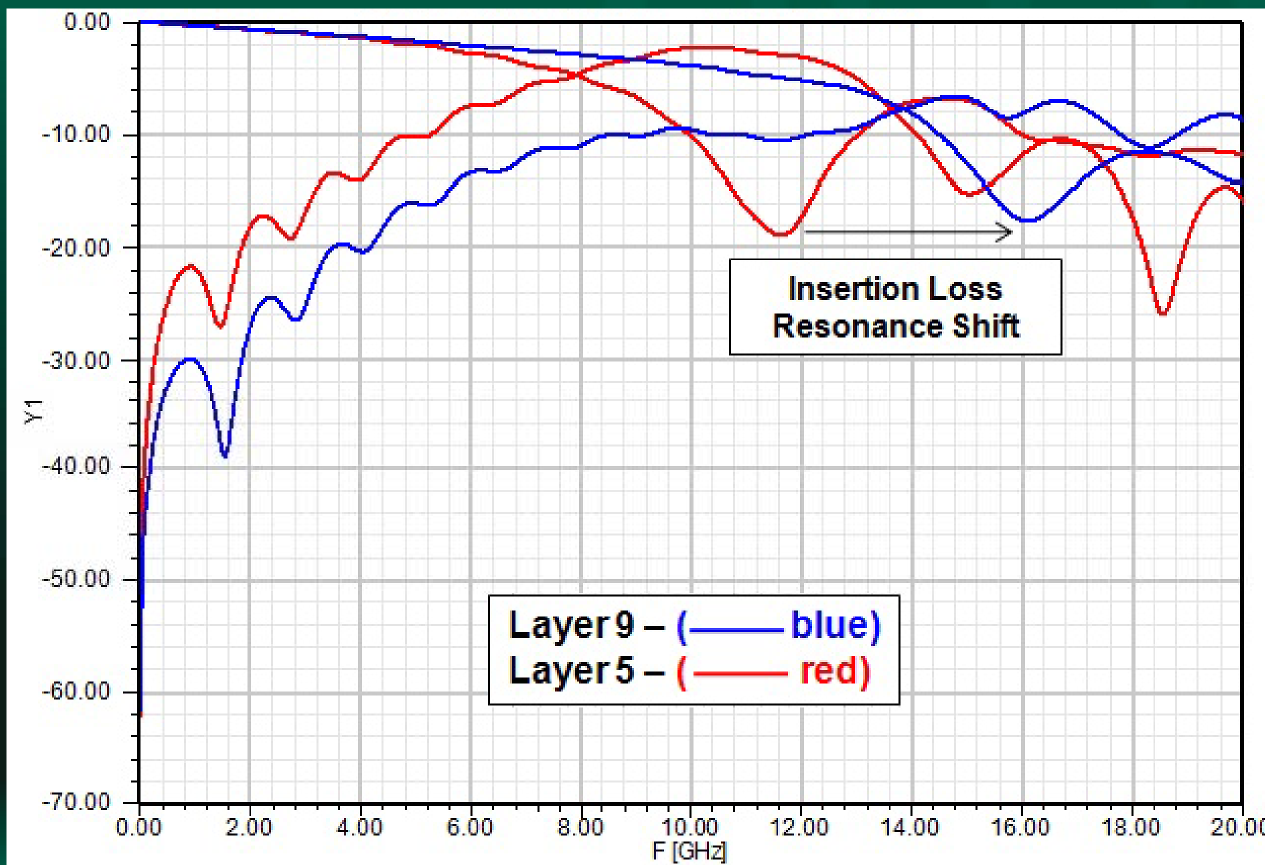


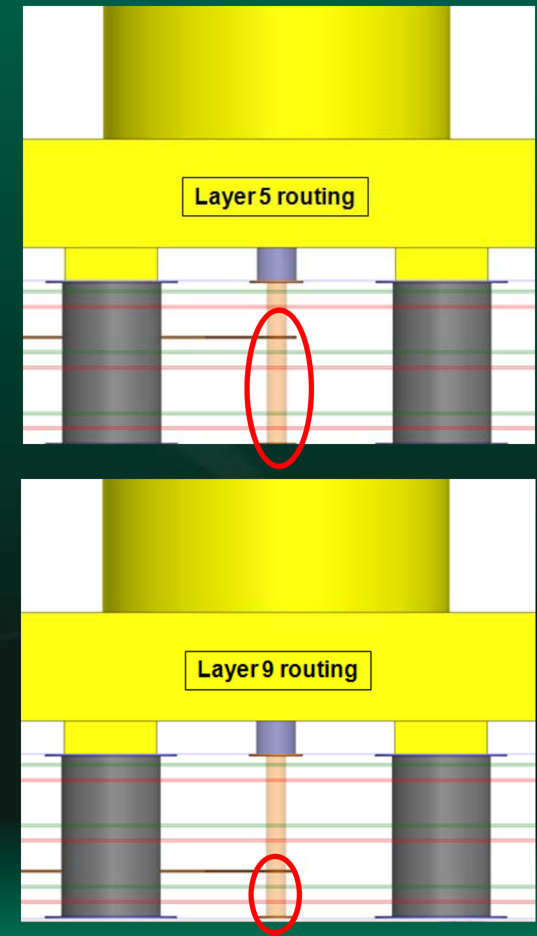


Signal Integrity: STEP #4

PCB Interconnection Optimization

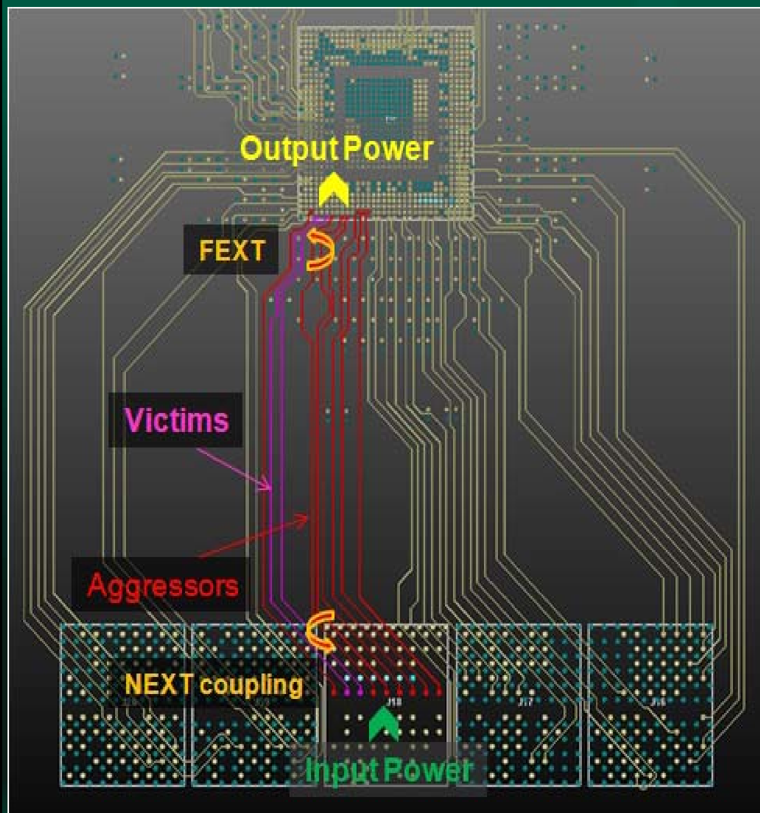
- **VIA stub impact: Routing Analysis – Layer #5 vs Layer #9**

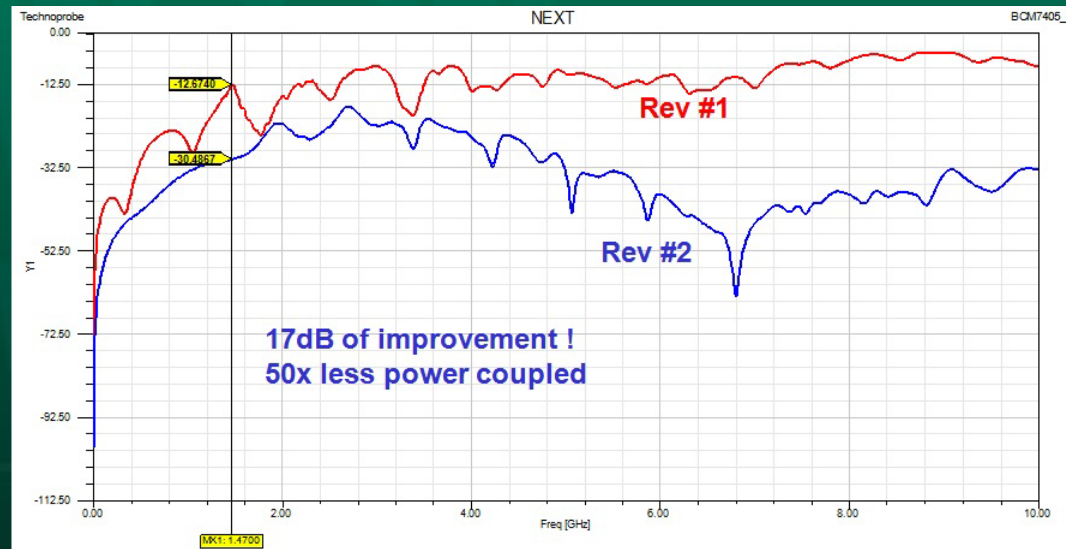


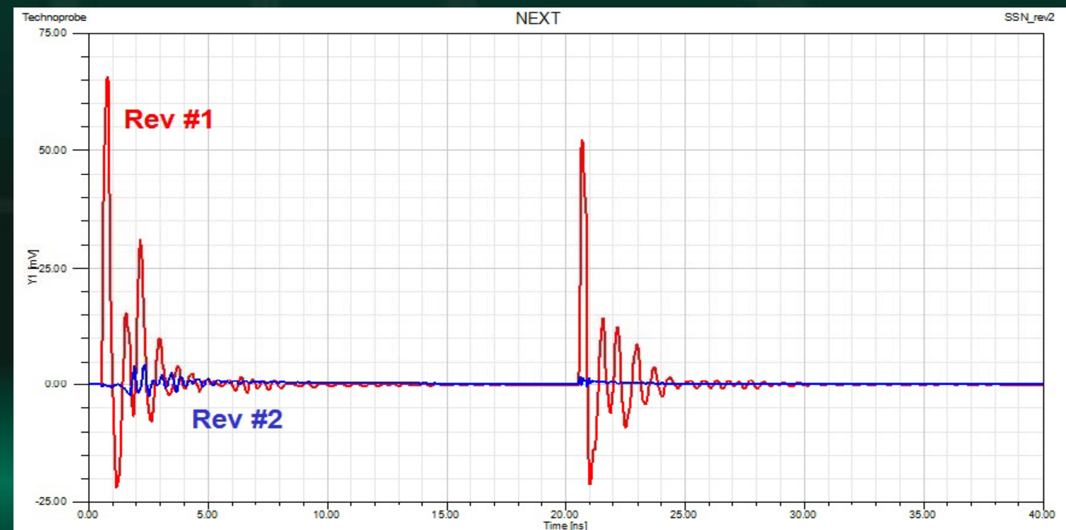


Signal Integrity: STEP #5

Cross Talk Analysis

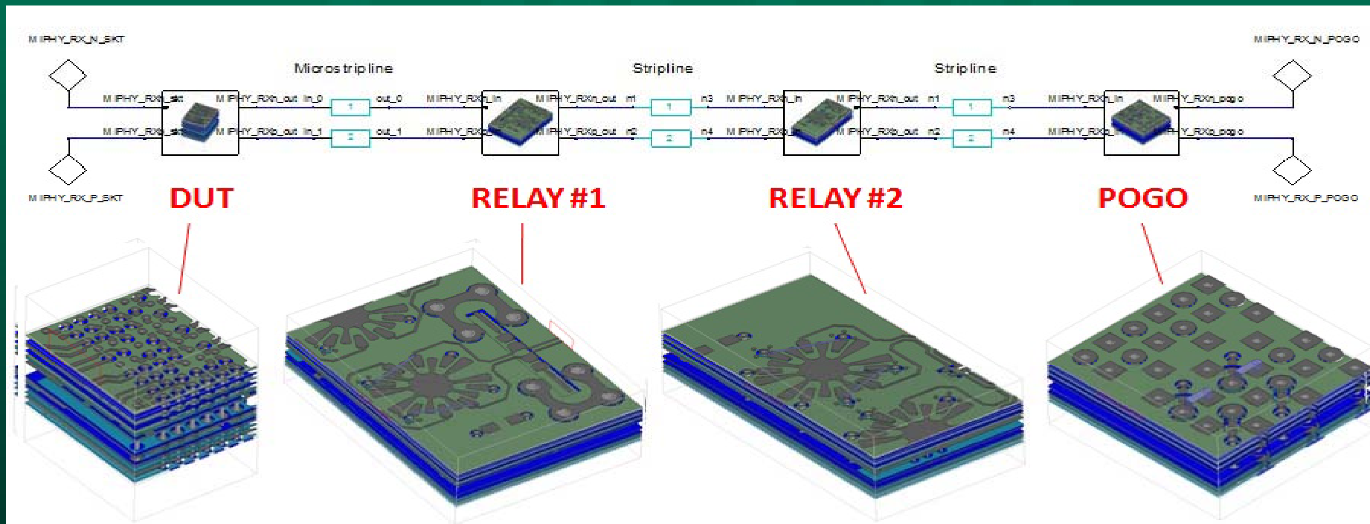


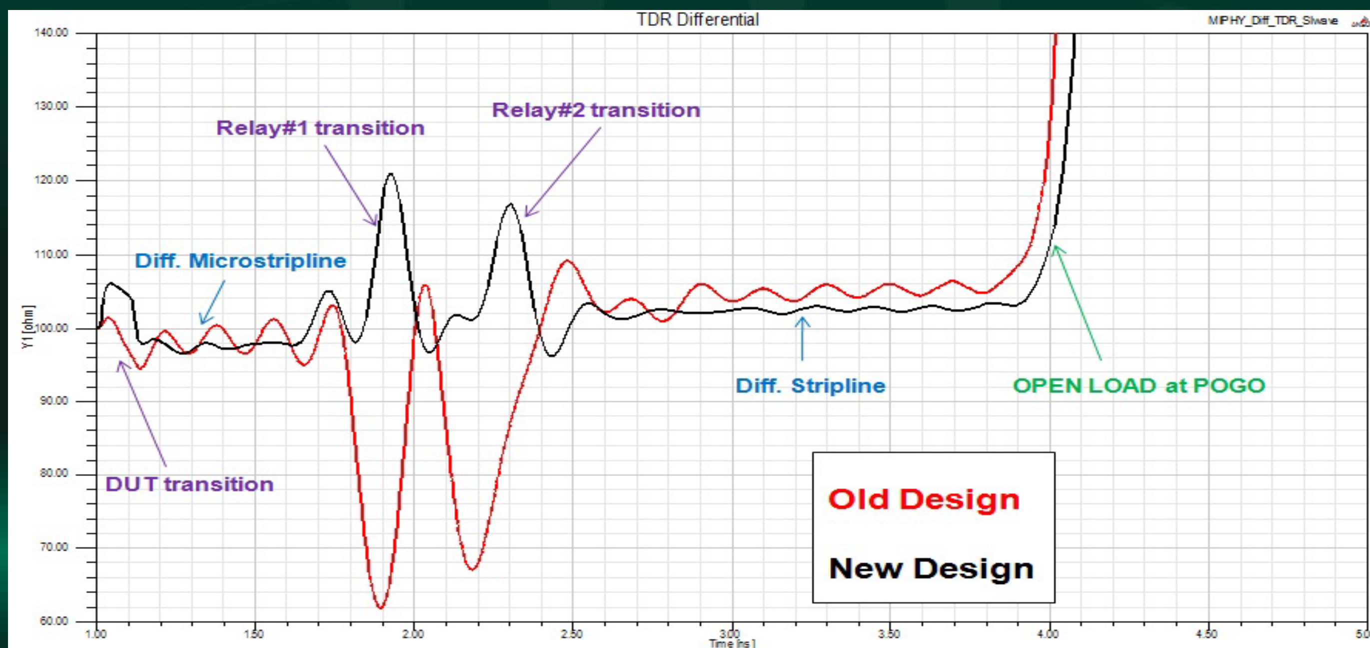




Signal Integrity: STEP #6

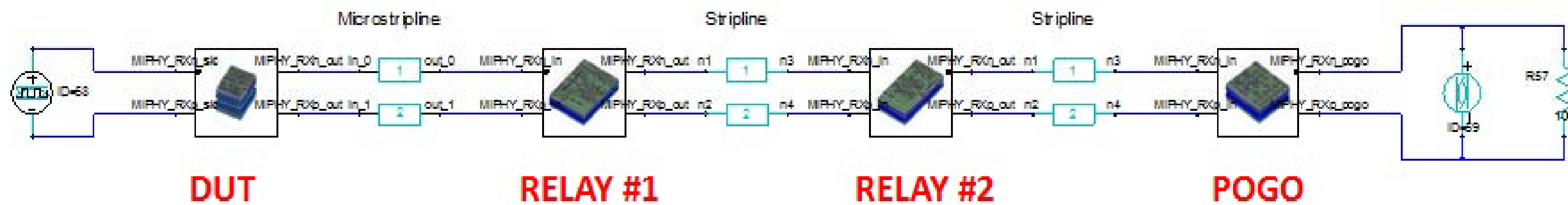
TDR Analysis – Impedance Improvement



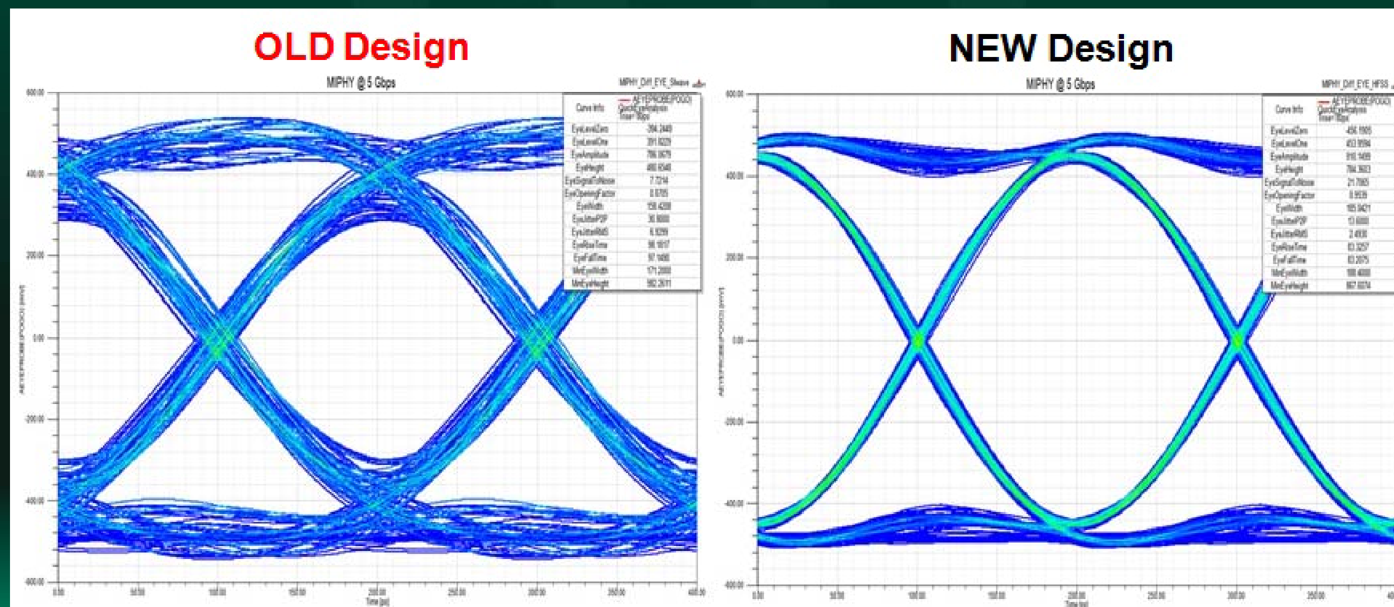


Signal Integrity: STEP #6

EYE Analysis – Gigabit Channel Improvement



- **Eye source pattern PRBS15 with 8b10b Encoding, 80ps rise/fall time, 5 Gbps of Datarate, 2 Vpp and 100 Ohm differential load at Pogo pads**



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- **Step by step Power Integrity Analysis and simulation examples on Probe Card system**
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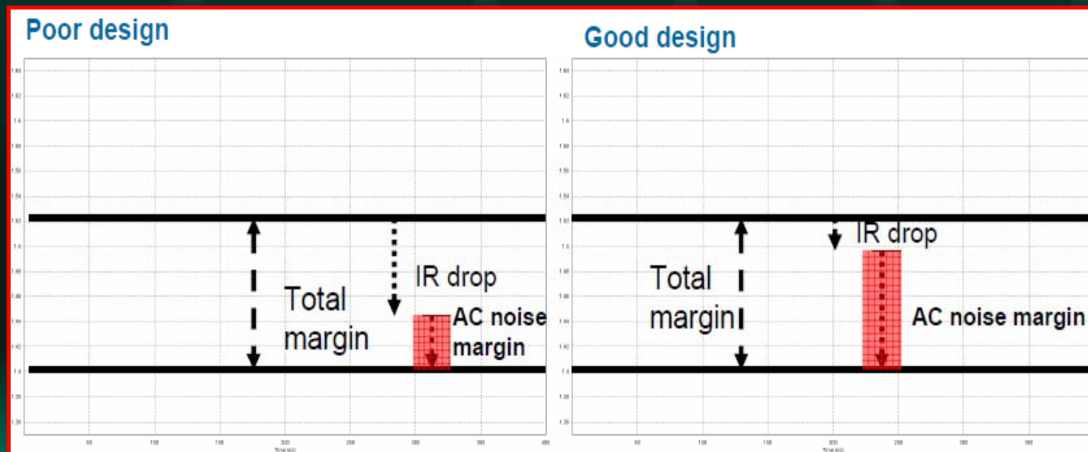
Power Integrity: STEP #1

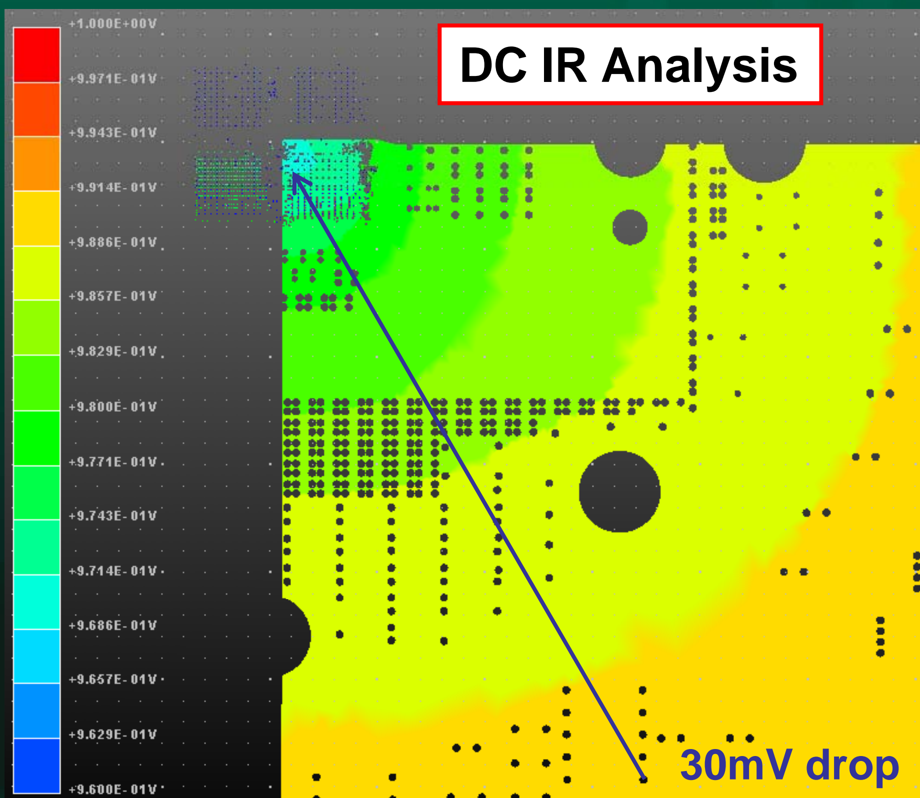
Check DC PDS Specification

- **What is the best DC PDS performance?**
  - Devices see voltage closet to nominal voltage
    - *Low IR drop*
    - *Well balanced DC voltages among devices on the same rail*
  - Low Temperature Rise on Metal
    - *Low Current Density*

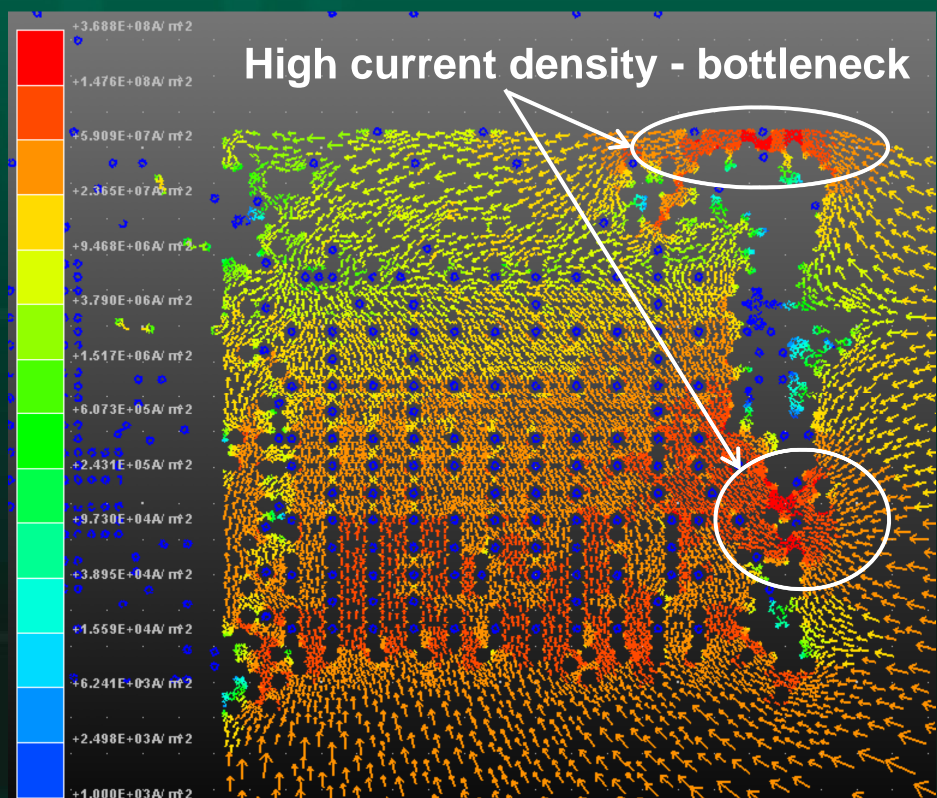


DC Power Delivery System Simulation

VDD Core Voltage Drop



VDD Core Current Distribution

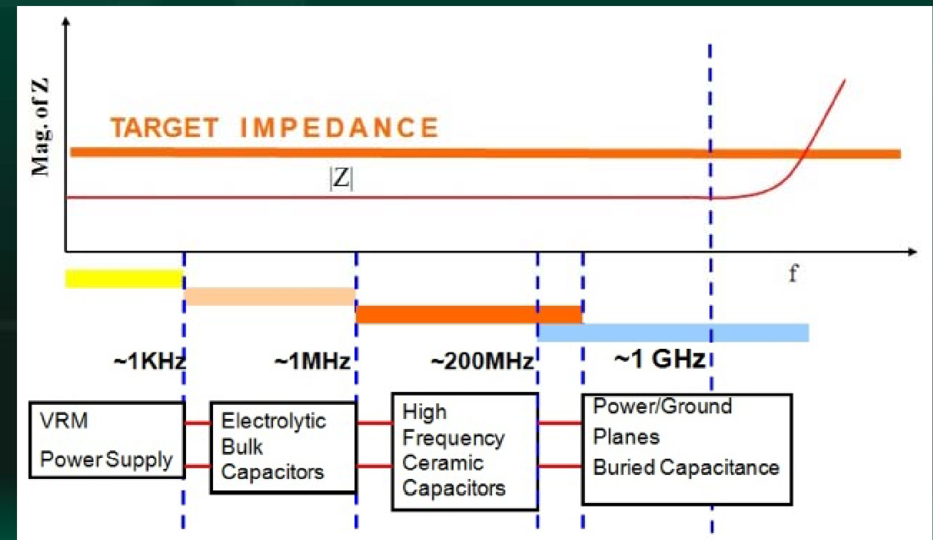


Power Integrity: STEP #2

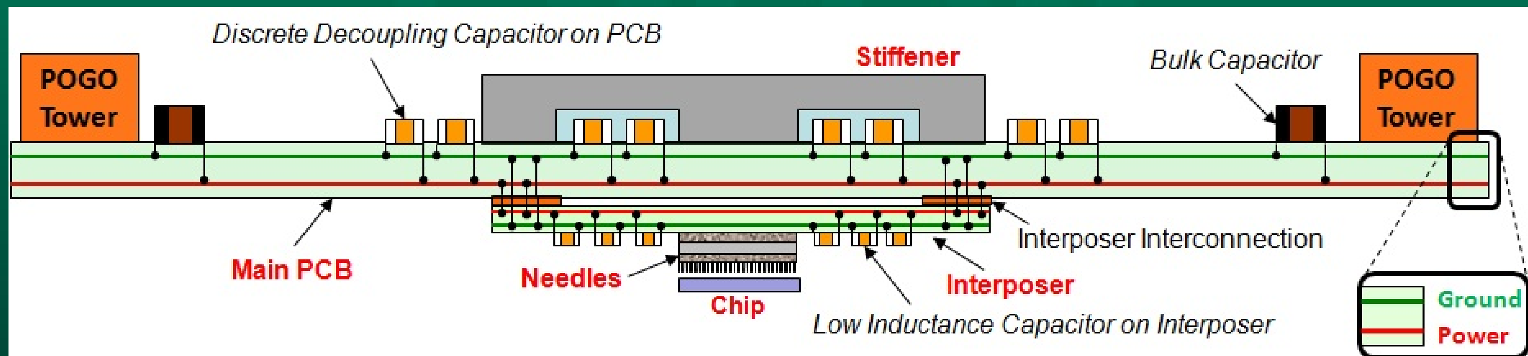
Check AC PDS Specification

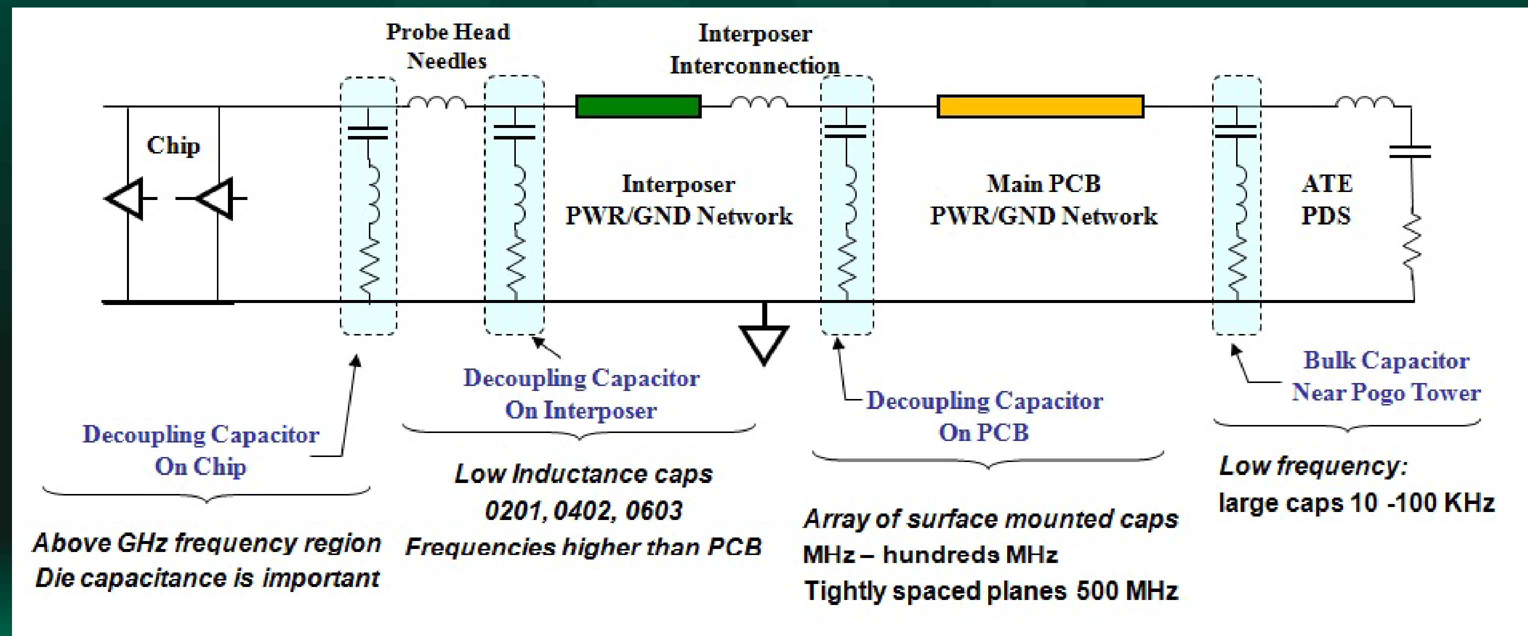
- **What is the best AC PDS performance?**
  - Low noise
    - *Low loop inductance*
    - *Low and Flat impedance*
- **What are the PDS design issues?**
  - Number of Caps, location/placement
  - Number of Vias, signals routing issue
  - Component mounting effect
  - PCB plane location/stack-up
  - Interposer effect

$$Z_{\text{Target}} = \frac{(V_{PWR}) \times (\%\,Noise)}{Current}$$



Power Delivery System Topology

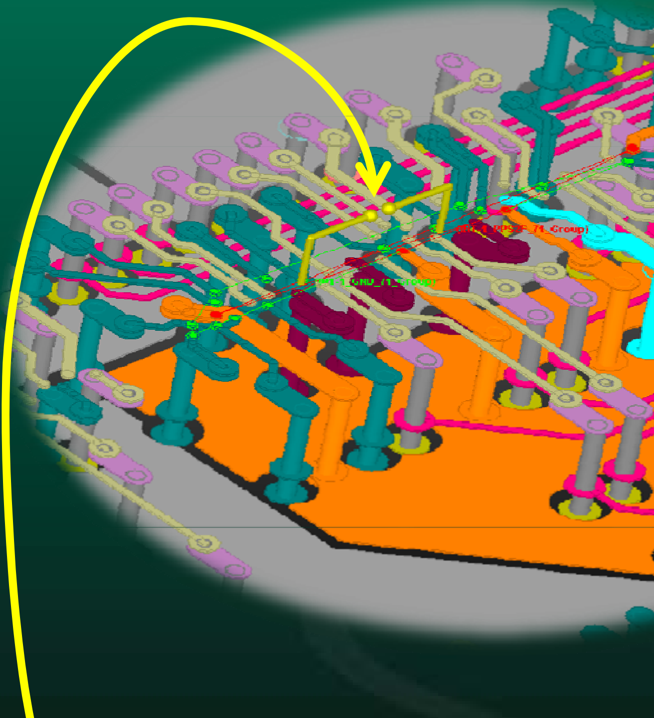




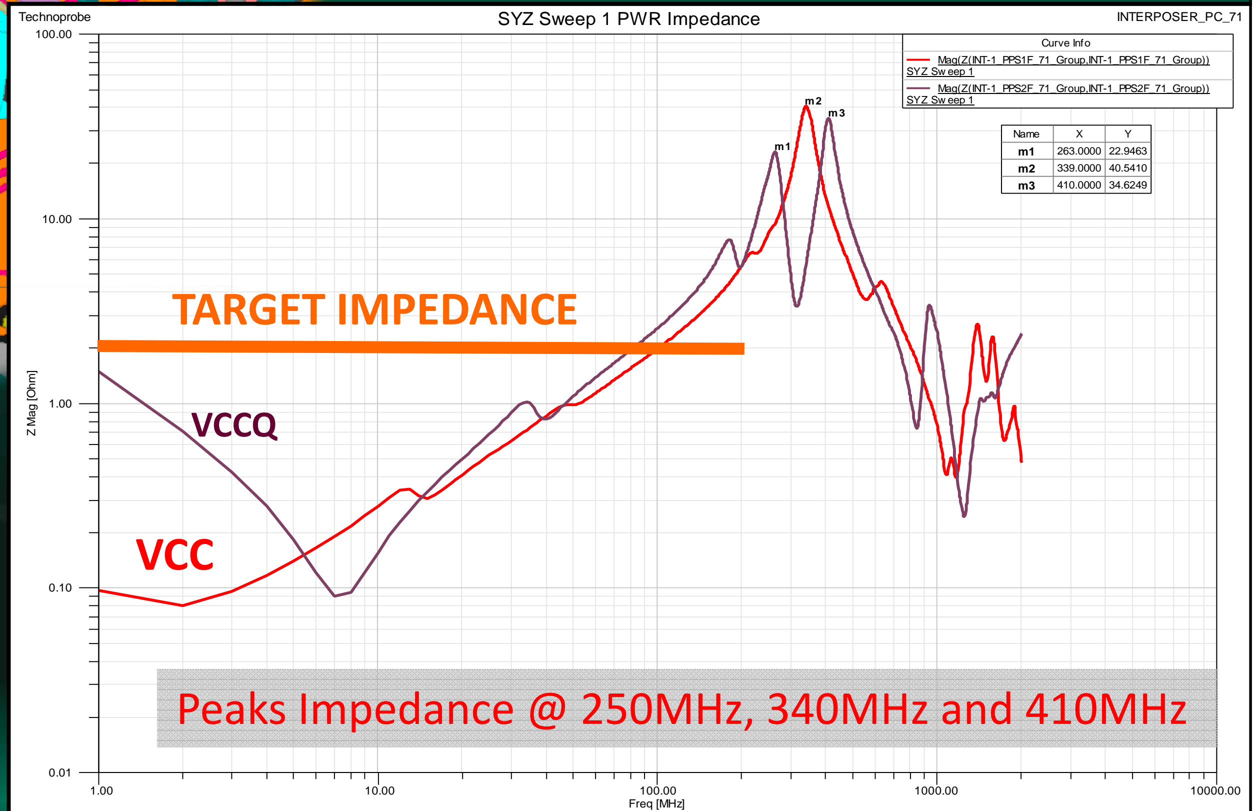
AC Power Delivery System Simulation

Impedance vs Frequency Analysis

$$V_N = Z \cdot I \qquad V_N = L \cdot \frac{di}{dt}$$



Compute Power Plane Self Impedance Z(f)



AC Power Delivery System Simulation

Resonance Modes Analysis

+9.999E-01V
+8.571E-01V
+7.142E-01V
+5.714E-01V
+4.285E-01V
+2.857E-01V
+1.428E-01V
+0.000E+00V
-1.428E-01V
-2.857E-01V
-4.285E-01V
-5.714E-01V
-7.142E-01V
-8.571E-01V
-9.999E-01V

PWR plane bouncing below DUT
High Impedance hot spot area

Decaps are mounted in this area:
too far away from DUT

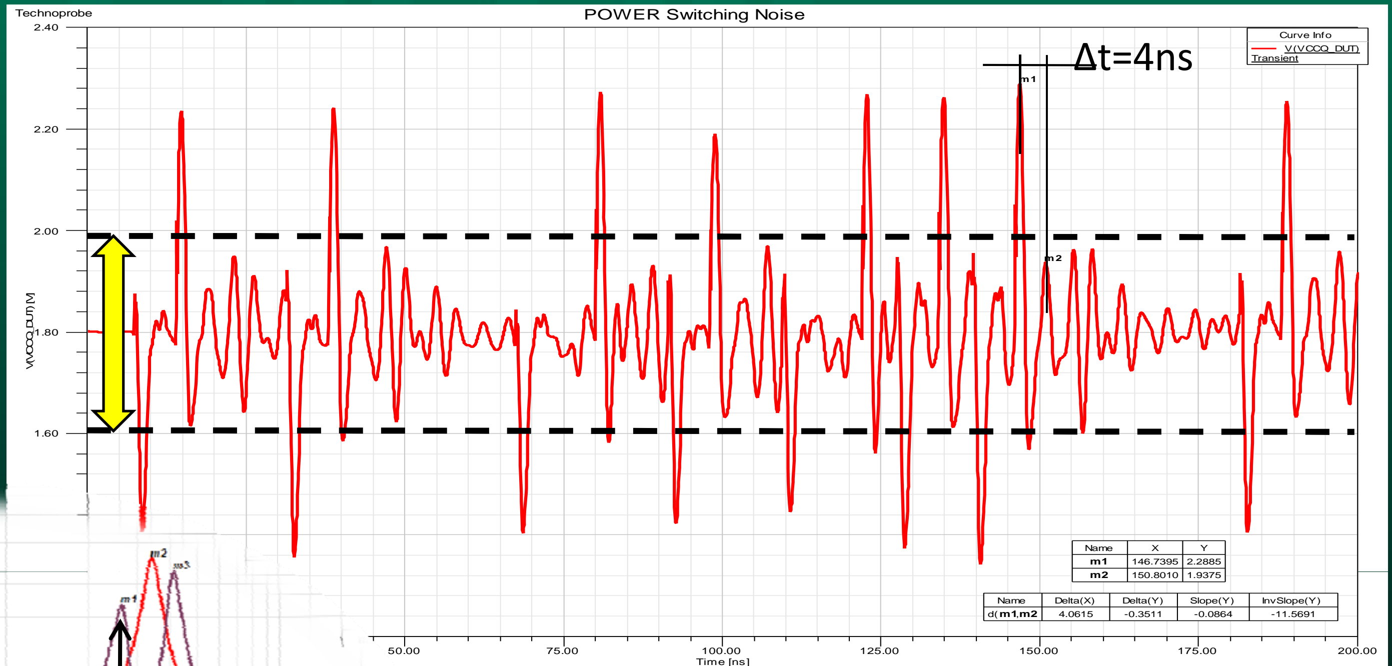
VCCQ Resonant Mode @ 250MHz

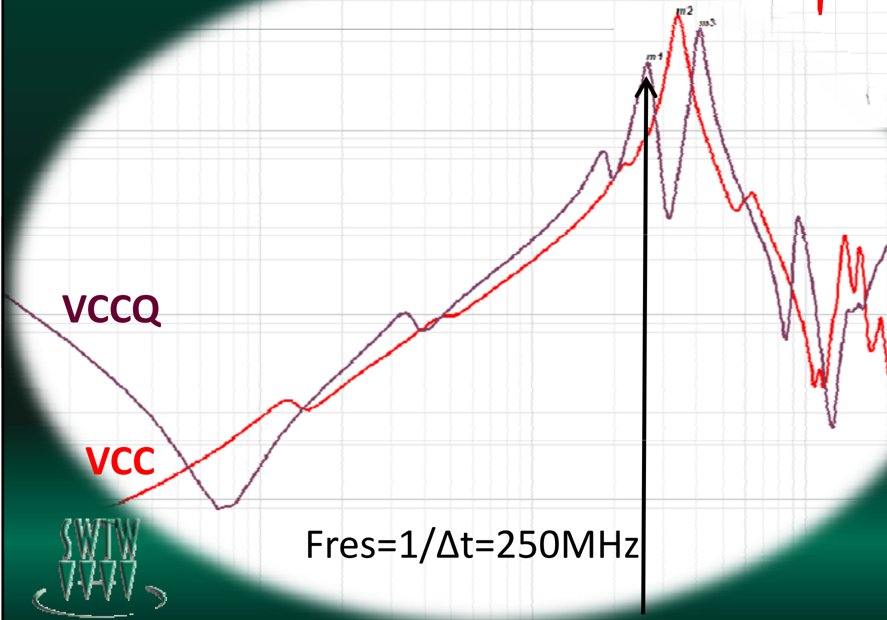
AC Power Delivery System Simulation

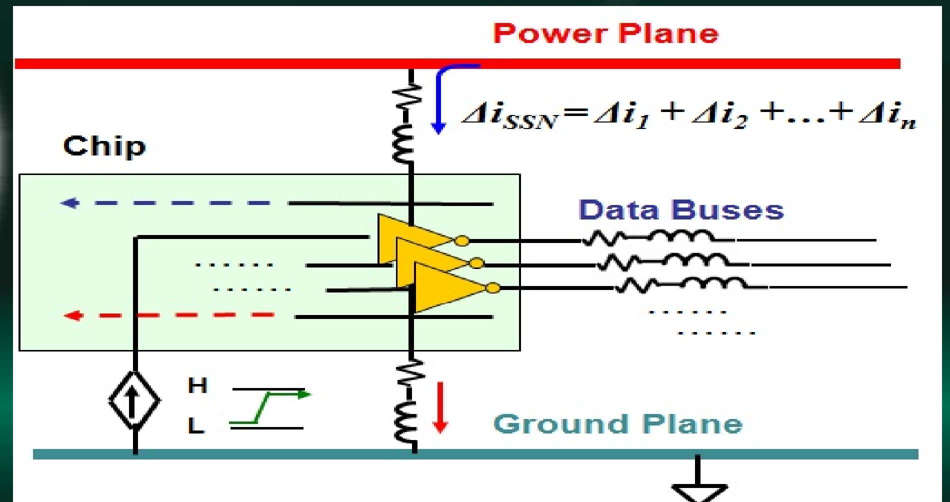
Simultaneous Switching Noise (SSN)

Wide DQ BUS causes SSN/SSO (power and ground bounce, AC drop)

Allowed AC ripple noise

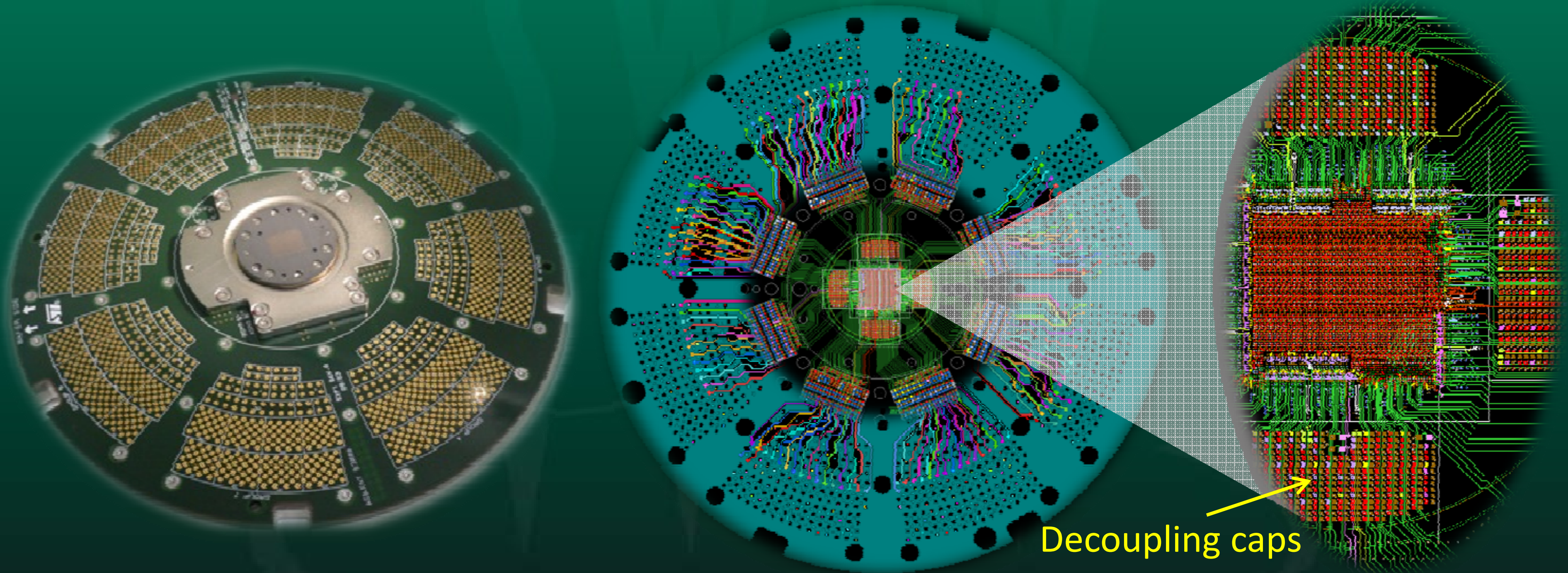






Power Integrity: STEP #3

Optimize Decoupling Capacitors

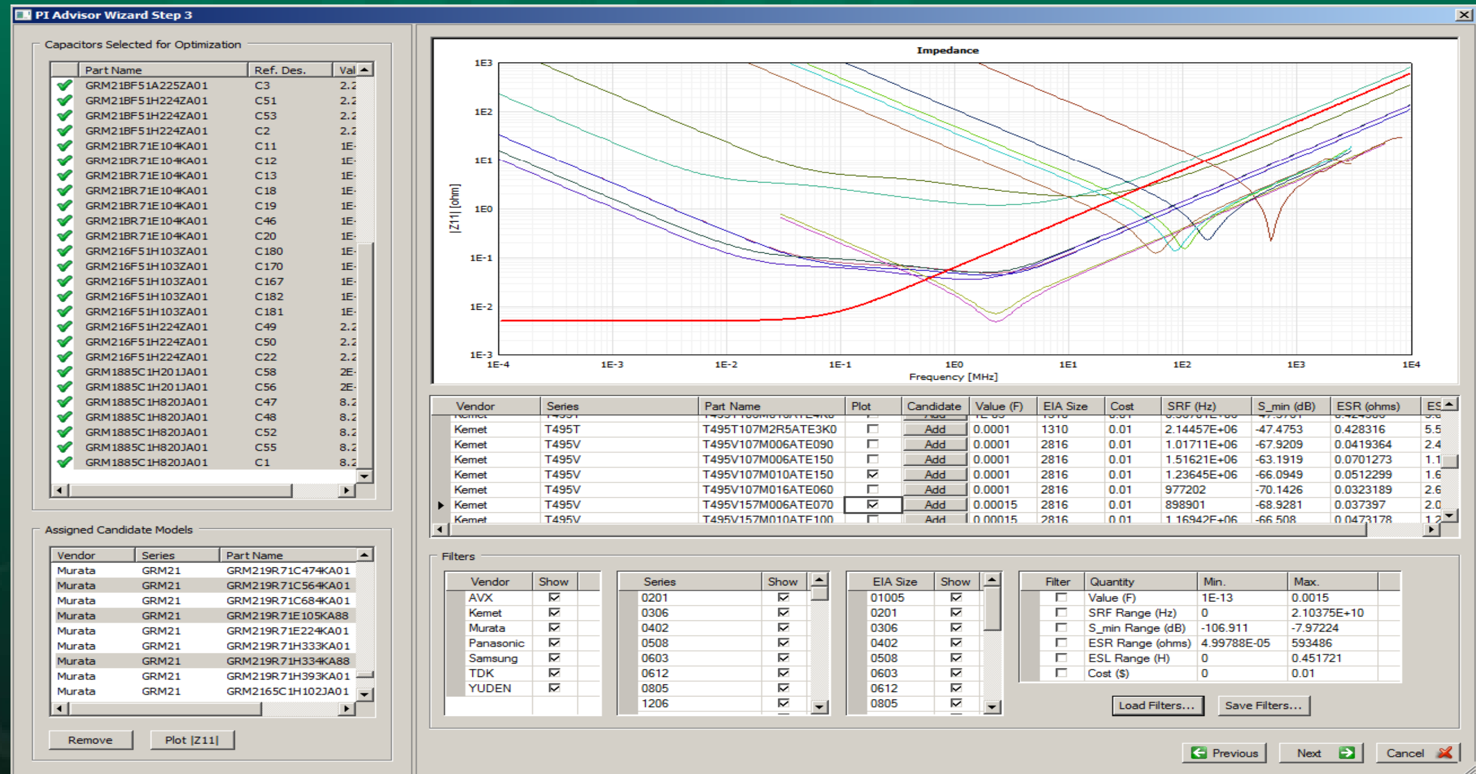


- **Why optimize array decoupling capacitor?**
  - Chose the right number of decoupling capacitors to meet Ztarget
    - *Save space for signals routing, reduce design constrains and effort*
  - Chose the right package size, value and mounting footprint
    - *Minimize mounting inductance, improve PWR impedance profile vs frequency*

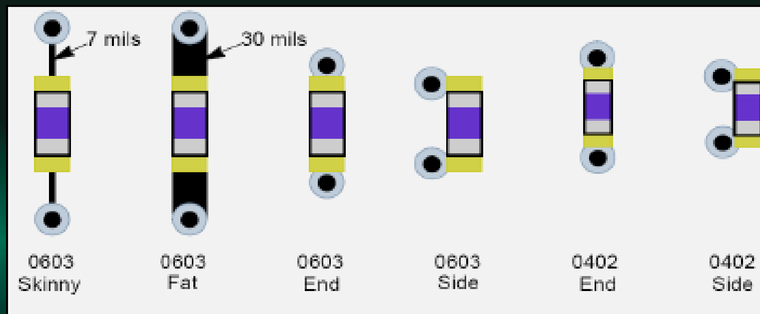
Decoupling Capacitor Selection

Why use only classic 10nF, 100nF?

Select the right capacitor values and package from Cap Vendor's library to obtain the best PWR Impedance profile vs Frequency



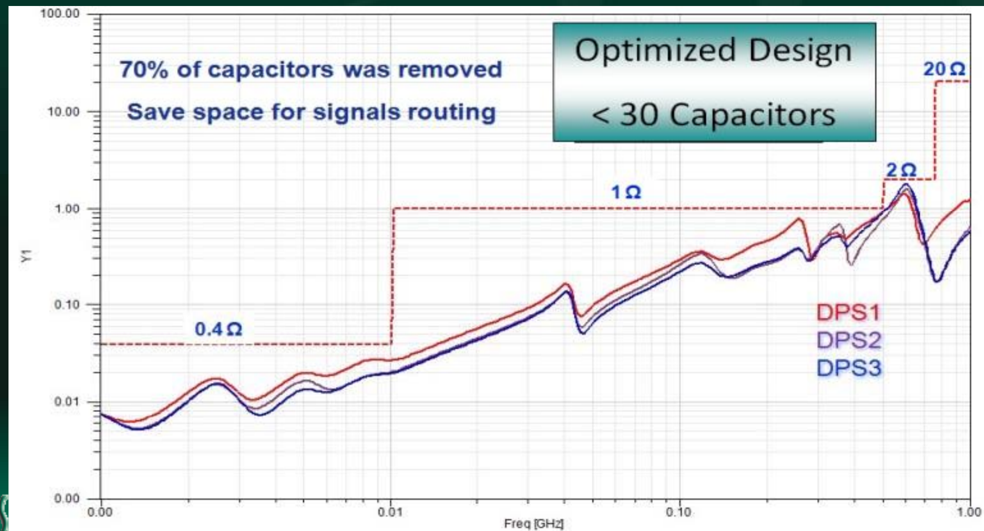
MOUNTING DESIGN

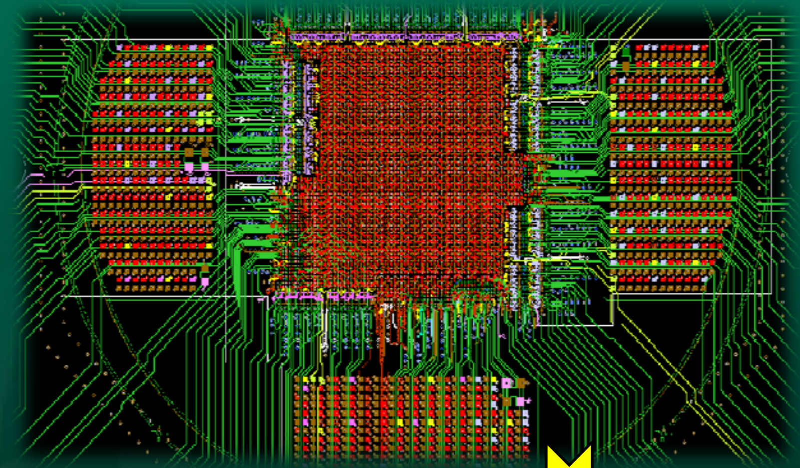


PACKAGE SIZE

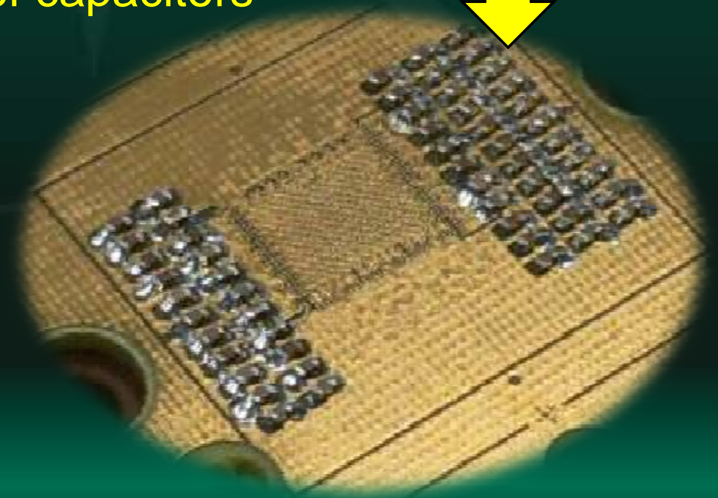
Decaps Reduction

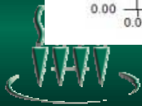
Same Impedance Performance





Reduced number of capacitors



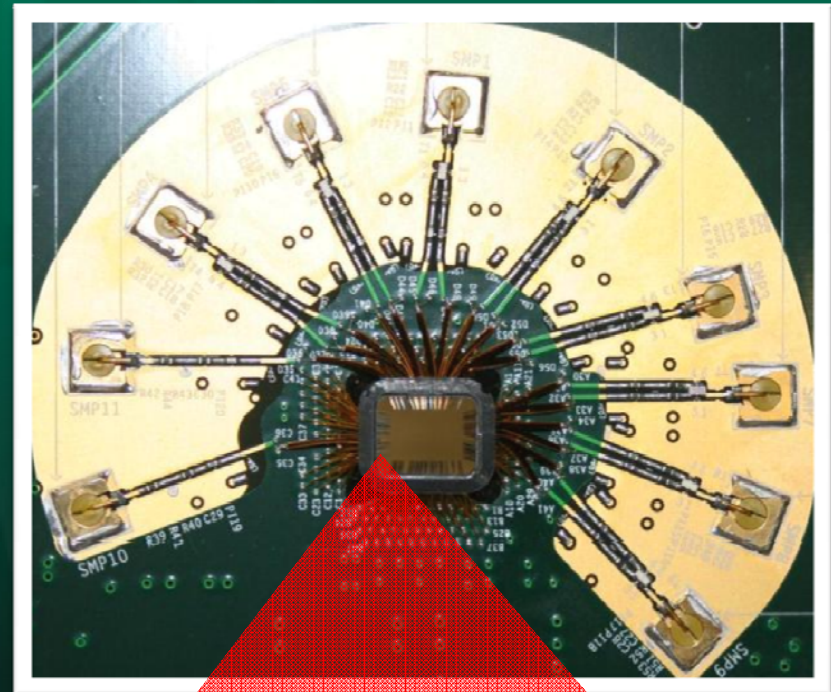


Agenda

- Probe Card Design Flow for high speed performance
- Step by step Signal Integrity Analysis and simulation examples on Probe Card system
- Step by step Power Integrity Analysis and simulation examples on Probe Card system
- **High Frequency Probe Card example**

HF Cantilever Probe Card for RF Wafer Sort

- **Suitable for wireless RF front end wafer sort solution:**
  - Bluetooth (2.4 GHz)
  - 802.11b/g/n (2.4GHz)
  - 802.11y (3.7GHz)
  - 802.11ac (<6GHz)
  - WiMAX (2.3 GHz, 2.5 GHz, 3.5 GHz)
  - Etc.



VNA Measurement

FIRST PASS SYSTEM SUCCESS

m1
freq=5.500GHz
dB(S(2,1))=-1.630

m2
freq=5.500GHz
dB(S(2,2))=-8.244

m3
freq=5.500GHz
dB(S(1,1))=-7.980

dB(S(2,2))
dB(S(2,1))
dB(S(1,2))
dB(S(1,1))

freq, GHz

GOOD Performance up to 6GHz

SUMMARY

- **Many high frequency standards are present in the market today, this require new methodology for Probe Card Design**
- **Usage of complete simulation environment allow Engineers to accurate check both *Signal* and *Power Integrity***
- **A step-by-step approach has been shown**
- **The speed up and accuracy of Electromagnetic Simulator, combined with Circuit Environment, allow to control ENTIRE EWS SYSTEM and Probe Card performance prior to manufacture → FIRST PASS SYSTEM SUCCESS**

Acknowledgment

- Thanks to Massimo Capodiferro (Ansoft Italy) for his support during recent years on simulation setup/check
- Thanks to Flavio Maggioni (Technoprobe Italy) for his valuable contribute on high frequency PCB design

Future Works

- Continuous R&D simulation effort for improving high frequency PC performance and extend production of HF and KGD PC

Questions and Answers