Challenges of CIS high parallelism test

Larry Levy
FormFactor Inc.
Agenda

• CIS Market
• High parallelism
• CIS sort test challenges
• Summary
CIS vs CCD Units

Global forecast of unit shipment market share for area image sensors (CMOS vs. CCD)

. Source: iSuppli, October 2010
CIS vs CCD Revenue

CMOS versus CCD Image Sensor Dollar Volumes

2005-2015 CMOS Sales = 8.1% CAGR
2005-2015 CCD Sales = 2.0% CAGR

Billions of Dollars

Year
05 06 07 08 09 10 11 12 13 14 15

Source: IC Insights
Growing CMOS Image Sensor Market

CMOS image sensor sales will grow 13 percent to a record high $5.1 billion in 2011, as more CMOS sensors are used in camera phones, digital cameras, automotive systems, and embedded webcams in laptops and tablet computers, according to researcher IC Insights.

Source: IC Insights
Automotive applications

**Multi-Function Interior Camera System**
- Occupant Classification
- Driver Recognition
- Drowsy Driver
- Crash Recorder

**Multi-Function Rear Seat Camera**
- Passenger Viewing
- Occupant Classification

**Multi-Function Forward Camera System**
- Urban Cruise Control
- Headlamp Control
- Pre-Crash
- Sign Recognition
- Crash Recorder
- Night Vision

**Multi-Camera Viewing and Processing System**
- “Birds Eye” Surround View System
- Automatic Parking System
- Lane Change Assist

Source: Micron Automotive Segment Marketing
CMOS image sensors Revenues - 2009 Market Shares

(Based on estimated business value of ‘first-level-packaged’ CIS sensors)

Yole Developpement © January 2010

- Sony has grown fast, mainly thanks to the success of the introduction of its BSI CMOS sensor in the camcorders and DSC / SLR camera’s space along with its high-end mobile camera module activity
- Samsung is also growing, both in the low-end and high-end CMOS image sensor space
- Canon pioneered in the introduction of CMOS sensor technology in its high-end DSC / SLR and video camcorder cameras product line

* Others include Cypress, Kodak, Pixel, SiliconFax, PixelPlus, GalaxyCore, Maitere, Himax Imaging, Panasonic, NIT, CMOSIS, Forza, Sumei, a2v, Awaisn, Super-Pix, Canesta, ViT, Foveon, KunShan RuiXin Micro, Crysysview, Anarocus, Atasens, Novatek, Pixim and Daise
Common CIS Device Layout

- Active-Pixel Array
- Row-Select Logic
- Analog Signal Processors
- ADC
- Column Select
- Digital Output

CMOS pixel arrays are fabricated with standard silicon processes, enabling peripheral electronics to be included on the chip.

Light Sensitive Area
Can have 3 sort steps
Light test
Dark test
Logic test

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Common CIS Testers

- Magnum IPC
- Yokogawa
- Advantest T2000

IEEE SW Test Workshop
### CIS Attributes

<table>
<thead>
<tr>
<th></th>
<th>DRAM</th>
<th>Flash</th>
<th>SOC</th>
<th>CIS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Test time increasing with density</td>
<td>Yes</td>
<td>Yes</td>
<td>?</td>
<td>Yes Pixels</td>
</tr>
<tr>
<td>Move to higher //</td>
<td>2 to 6 TD</td>
<td>1TD</td>
<td>slowly</td>
<td>&gt;30TD</td>
</tr>
<tr>
<td>Majority market suppliers</td>
<td>4</td>
<td>5</td>
<td>Many</td>
<td>7</td>
</tr>
<tr>
<td>High speed</td>
<td>Yes</td>
<td>No</td>
<td>Some</td>
<td>Yes</td>
</tr>
<tr>
<td>Power supply levels</td>
<td>Few</td>
<td>Few</td>
<td>Many</td>
<td>Many*</td>
</tr>
<tr>
<td>Major products</td>
<td>Computing</td>
<td>Consumer</td>
<td>Consumer</td>
<td>Consumer</td>
</tr>
<tr>
<td>Average pixel count</td>
<td>N/A</td>
<td>N/A</td>
<td>N/A</td>
<td>Increasing</td>
</tr>
<tr>
<td>Average pixel size</td>
<td>N/A</td>
<td>N/A</td>
<td>N/A</td>
<td>Decreasing</td>
</tr>
</tbody>
</table>

*CIS devices seem to be more noise sensitive*
X-Sectional Image of FormFactor CIS Probe Card

160mm x 150mm light source now available

- Back-plate
- Leaf spring
- Probe head
- Micro-springs
- Planarization screw
- PCB

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Why is CIS Moving to Higher Parallelism?

<table>
<thead>
<tr>
<th></th>
<th># of testers</th>
<th># of probe cards</th>
<th>Cost/good die</th>
<th>Capital reduction*</th>
</tr>
</thead>
<tbody>
<tr>
<td>x8</td>
<td>66</td>
<td>69</td>
<td>$0.0393</td>
<td>Base</td>
</tr>
<tr>
<td>x16</td>
<td>43</td>
<td>45</td>
<td>$0.0320</td>
<td>$9M</td>
</tr>
<tr>
<td>x16 Matrix Array</td>
<td>31</td>
<td>32</td>
<td>$0.0257</td>
<td>$23M</td>
</tr>
<tr>
<td>x32 Matrix array</td>
<td>13</td>
<td>14</td>
<td>$0.0154</td>
<td>$37M</td>
</tr>
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</table>

Sematech model

Cost of Ownership Model Assumptions

- 30K 200mm wafers/Month
- 1,000 DPW
- 1% Yield increase due to MEMs probe card fidelity
- 30% test time reduction for x32 tester

* Capital is calculated as if adding all new testers and probers
### Parallelism vs Touch Downs

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**Diagram:**

- **X 16 Arrays**
  - 2 sided die only
  - [Diagram showing 2-sided die layout]

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## Touch Down Efficiency - 5 to 6mm Square Die

<table>
<thead>
<tr>
<th>//</th>
<th>Array (Skip R &amp; C)</th>
<th>TD</th>
<th>TD reduction %</th>
</tr>
</thead>
<tbody>
<tr>
<td>32</td>
<td>8x4</td>
<td>32</td>
<td>70%</td>
</tr>
<tr>
<td>32</td>
<td>4x8</td>
<td>32</td>
<td>70%</td>
</tr>
<tr>
<td>30</td>
<td>6x5</td>
<td>35</td>
<td>67%</td>
</tr>
<tr>
<td>30</td>
<td>5x6</td>
<td>36</td>
<td>66%</td>
</tr>
<tr>
<td>25</td>
<td>5x5</td>
<td>36</td>
<td>66%</td>
</tr>
<tr>
<td>28</td>
<td>4x7</td>
<td>38</td>
<td>64%</td>
</tr>
<tr>
<td>28</td>
<td>7x4</td>
<td>38</td>
<td>64%</td>
</tr>
<tr>
<td>24</td>
<td>4x6</td>
<td>40</td>
<td>63%</td>
</tr>
<tr>
<td>24</td>
<td>6x4</td>
<td>42</td>
<td>61%</td>
</tr>
<tr>
<td>16</td>
<td>4x4</td>
<td>56</td>
<td>48%</td>
</tr>
<tr>
<td>8</td>
<td>4x2</td>
<td>105</td>
<td>2%</td>
</tr>
<tr>
<td>8</td>
<td>2x4</td>
<td>106</td>
<td>1%</td>
</tr>
<tr>
<td>8</td>
<td>8x1</td>
<td>107</td>
<td>Base</td>
</tr>
<tr>
<td>8</td>
<td>8x1 Solid Diagonal</td>
<td>107</td>
<td>Base</td>
</tr>
</tbody>
</table>
CIS Sort Testing Trend

Springs on 2 sides
Skip row

Springs on 3 sides
Skip row and column
CIS Sort Test Challenges

• Three sided devices have unbalanced force
  – X 16 1.6Kg unopposed force (with low force 5 grams/spring x 20 springs/DUT)
  – X 32 3.2Kg unopposed force

• Impacts scrub mark

Many customers increase OT to try to get larger scrub marks
CIS Sort Test Challenges

- Complex design from inner DUTs

X 32 Matrix array
Light Fixed-Pattern Noise (PRNU)

Origin: non-uniformities on pixel response, threshold variations, gain and offset differences.

Countermeasure:
- look-up tables
- technology dependent
- layout/design dependent
- offset cancellation
CIS Sort Test Challenges

• Light fixed pattern noise sensitivity

  – Many power supply levels
  
  – Noise both within a DUT and across DUTs can cause longer test times and require more frame captures
  
  – Customer data shows MEMs cards reduce noise by ~ 40% within a DUT and >5 time lower across all DUTs

Noise within a DUT

Noise across all DUTs

Source: FormFactor Inc
CIS Sort Test Challenges

Dark Fixed-Pattern Noise

**Origin:** non-uniformities on dark current generation, threshold variations, gain and offset differences.

**Countermeasure:**
- Low temperature
- Technology dependent
- Lay-out/design dependent
- Offset cancellation

Albert Theuwissen ISE 2011
CIS Sort Test Challenges

- FormFactor
- Cantilever

* Capture Image (1frame capture, Dark 7lsb)

noisy

Source: FormFactor Inc

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CIS Sort Challenges

- **Noise sensitivity**
- **Decoupling capacitors provide low Power Delivery System impedance over range of frequencies**
  - Smaller capacitors used for high frequency (high $F_{res}$)

This part shows 19 caps/DUT on the ceramic
Decoupling Capacitors Near the DUT

- Capacitors mounted on boards add loop inductance to Equivalent Series Inductance (ESL)
  - Greater distance from DUT increases loop inductance
  - Decreases effective Fres of capacitor
  - Causes resonant peak to be sharper, reducing effectiveness of capacitor to reduce PDS impedance

- Reducing capacitance to move back Fres to offset effect of loop inductance is less effective because of the increase in sharpness of resonant peak
  
  Always best to keep loop inductance low!

Low loop inductance

High loop inductance

Compensating high loop inductance with smaller capacitance
CIS Sort Test Challenges

- **Uniform light intensity**
  - Design for largest possible window opening
    - Avoid reflection from side walls
  - All hardware must be non reflective

![Diagram of DUT and Pixel area with springs overhanging the opening.](image-url)
Higher Pixel Counts Drive Smaller Pixel Sizes

Image sensor pixel pitch trend

- Pixel pitch (μm)

Sony Tsurumu Haruta ISE 2011
CIS Sort Test Challenges

• Particle sensitivity
  – Smaller Pixels are more prone to particle defects
  – Requires low particle generation sort solution

Greatly enlarged pixels on an image sensor.

Shadows caused by particles cause pixels to fail.
CIS Sort Test Challenges

In-Stat, has projected that by 2016, up to 70 percent of image sensor interfaces in the electronics industry would use the high-speed camera serial interface (CSI) developed by the Mobile Industry Processor Interface (MIPI) Alliance.

- **MIPI requirements**
  - Currently running at >800 mbps
  - Clock and 2 lines (serial interface)

- **Projections for the number of LVDS per DUT increasing over time**
  - Number of pads to be probed remains fairly constant

- **Industry roadmap extends beyond 1.2 gbps need**
  - Device rise time can limit frequency
CIS Sort Test Challenges

Wafer sales and WLCSP are driving more test at sort.

WLCamera Module Assembly Steps:

1) Wafer lenses molding
2) Wafer level packaging with Glass wafer cap
3) Stacking WLOptics module
4) WLCSP image sensor die / wafer
5) Optics to Sensors Assembly
6) Final Housing & Testing
CIS Sort Test Challenges

Wafer sales and WLCSP are driving more test at sort

Lens Module and Diffuser options becoming more common
Installation of lens or diffuser must be at prescribed distance to the device

Lens must fit inside of where probes are attached
CIS Sort Test Challenges

• **X 64 development**
  - TD’s reduced by half from x32
  - Requires larger light source
  - Increased design difficulty
    • In ceramic and PCB
  - MIPI targeted at 1.2 gbps

Touchdown study for development device

~130mm Dia

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Summary

• CIS sort test has some unique requirements
• Increased parallelism offers lower cost of test
• Choice of probe card/ spring type technology can make a difference
• Road blocks exist to increased parallelism
  – Light source area may be a limitation in the future
  – Probe card design is more difficult due to openings in the card
  • Will likely limit frequency
• Future innovation will be required to extend parallelism capability for CIS
Thank You