

Approaches for Reducing the Cost of High Pin Count Probe Card Test



John Strom

Jeff Greenberg

Rudolph Technologies



IEEE SW Test Workshop
Semiconductor Wafer Test Workshop

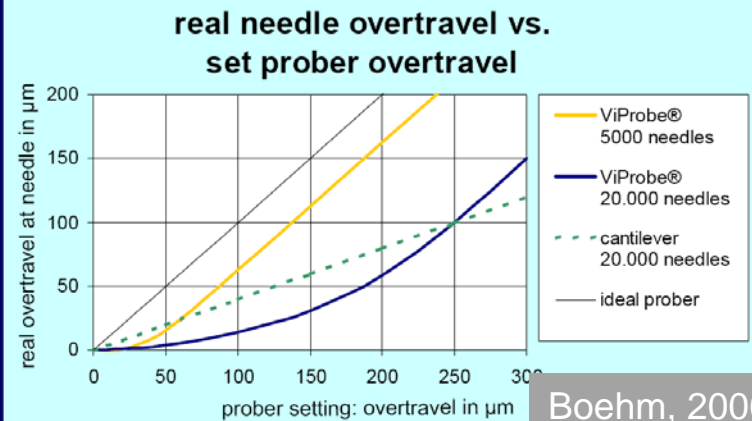
June 10 - 13, 2012 | San Diego, California

Introduction

- **High load probe cards in the test cell typically require**
 - Prober that can apply a large force (up to 450kg)
 - Prober that is structurally stiff (\$\$\$)
 - Tester Interface that is structurally stiff (\$\$\$)
- **Testing the probe card on the Probe Card Analyzer (PCA) – historically we tried to emulate Test Cell**
 - PCA needs to apply a large force (\$\$\$)
 - PCA needs to be structurally stiff (\$\$\$)
 - Probe Card Interface (PCI) that emulates (\$\$\$)
- **Is there a PCA test strategy that is more cost effective?**

Challenges of High Load Probe Cards – Probe Card Vendors

Influence of Prober Deflection to Overtravel Settings



Boehm, 2006
Feinmetall

SWTW June 2006

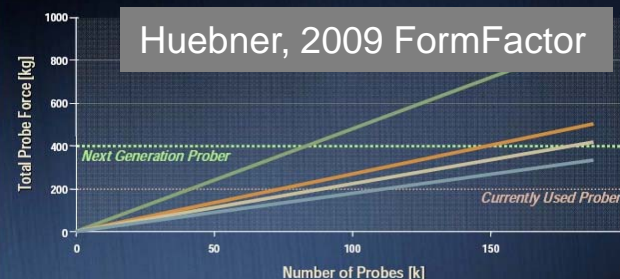
FEINMETALL GmbH, MIC Division, G. Boehm

System Deflection

Huebner, 2008 FormFactor

- System deflection is the biggest concern from the user
- High probe count probe cards create a significant force which leads to deflection in the whole test cell
 - Deflection of the probe card itself
 - Deflection of the chuck
 - Deflection of the head plate
 - Coupling between wafer motherboard and probe card
- System deflection is define as AOT/POT
 - Actual Over Travel / Programmed Over Travel
- How much of the programmed over travel each probe?

Probe Count and Total Probe Force



Huebner, 2009 FormFactor

- For 1 TD or 1500 to 2000 DUT parallel test 75 to 140k probes are needed (depending on probes/DUT)
- Next generation probers are needed to support 2000 DUT
- Majority of installed probers can support ~70k probes
June 7 to 10, 2009
IEEE SW Test Workshop

Interface design impact

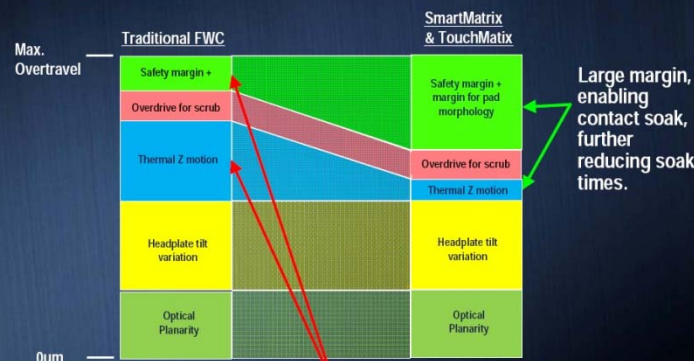
- Larger stiffener span on older test interfaces greatly impacts resulting probecard deformation
 - Next Generation Testers and interfaces with reduced span, provide better structural support for probecard deformation
 - 1 TD Test will require more than just resource sharing
 - Need lower force probes and/or better interface support
 - Higher load probers
 - Balance between thermal performance and structural support



Losey, 2010 Touchdown Technologies

Z Performance & Benefits

- Minimizing 3 things: Translation, Bow and Planarity results in:
 - More uniform scrub marks, minimized pad damage
 - Faster soak time using closer proximity soak and/or contact soak.



Breinlinger, 2010
FormFactor

Insufficient margin for contact soak

SWTW PAGE 14

Challenges of High Load Probe Cards – *IDMs*

Introduction

Caldwell, 2008
Micron Technology

- Challenge
 - High parallelism (1TD 300mm)
 - Thermal deflection
 - High probe count
 - Shrinking bond pads
- Can we maintain the same probe card planarity specification as 32x to 64x parallelism five years ago??
 - Yes!
- Micron has employed techniques for analyzing optical and electrical planarity data; resulting in...
 - Improved test cell performance
 - Better understanding of high parallelism probe card planarity characteristics
 - Correlation between metrology and test cell tools

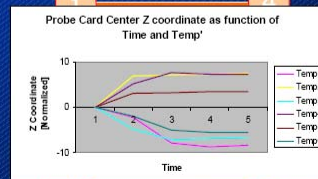
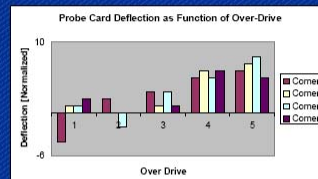
June 8 to 11, 2008

IEEE SW Test Workshop

2

XL Multi-DUT Probing Challenges

- Very large effective probing area :
 - Requirement for a large area contact uniformity through control of Alignment , Planarity and Test-Head deflections.
- High thermal sensitivity:
 - Probe-Cards have to be operational within the required Temp' Range of test.



Dabit, Nguyen, 2005 Intel

Pg 6

June 10 - 13, 2012



IEEE Workshop

4

Challenges of High Pin Count Cards – PCA Vendors

Motivation

- Ever increasing need to test more devices simultaneously
- Probe card pin counts and loads increasing
 - Advanced Technology Cards with > 10,000 probes
- Test Time
 - Need to keep test times acceptable
 - Minutes, not hours
- Accuracy
 - Increased loads cause structural deflection and degrade accuracy
 - Tighter probe pitch and smaller pads require higher accuracy

Greenberg, Kraft, 2003 API

Applied Precision
Enabling the world's core technologies

HIGH PROBE FORCE

• IS IT POSSIBLE TO CHARACTERIZE THE SYSTEM DEFLECTIONS?

- PROVIDING THE METROLOGY TOOL IS REPLICATING THE TESTER INTERFACE IT MAY BE POSSIBLE
- BUT ITS UNLIKELY - EACH TEST PLATFORM, PROBE COUNT, PROBE CARD, STIFFENER, WAFER PROBER, ... WOULD NEED TO ADDRESSED

Schwartz, McLaren 2007 ITC

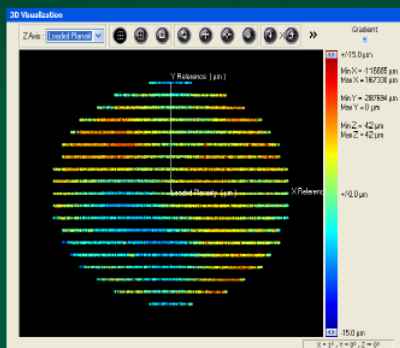
ITC's Design Guidelines

- Emulate Tester Mechanical Conditions
 - Same Forces on Probe Card
 - Same Connector Control Methods
- Emulate Wafer Prober Card Holding Conditions
 - Same Forces on Probe Card
 - Maintain Same Reference Surface
- Requires detailed information from test system manufacturer and custom hardware

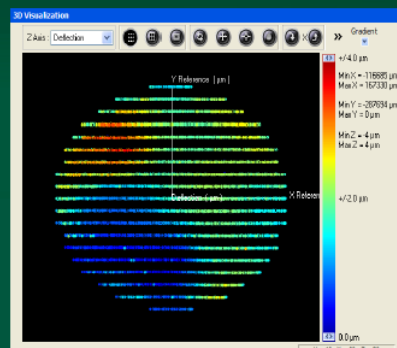
McLaren, 2010 ITC

Probe Card 1: Planarity

Loaded Planarity



Deflection



- Deflection of probe card from no overtravel until all probes are touching ~ 4 microns
- Low probes showing no deflection
- High probes drift up as the probe card is overtraveled

Doe, 2008, Rudolph

The Probe Card Analyzer M5

• Manager 5

Beijert, 2011

The facts of the M5

- Z-force 600 kilo pressure
- Accuracy in Z 0.1 micron
- Alignment 0.1 micron
- Cres 10 Milli-ohm
- Leakage 0.1 Nano-Amp
- Motherboard size max. 1.2 meter
- Total max. probe pressure 600 kilogram force
- Channel count > 100K



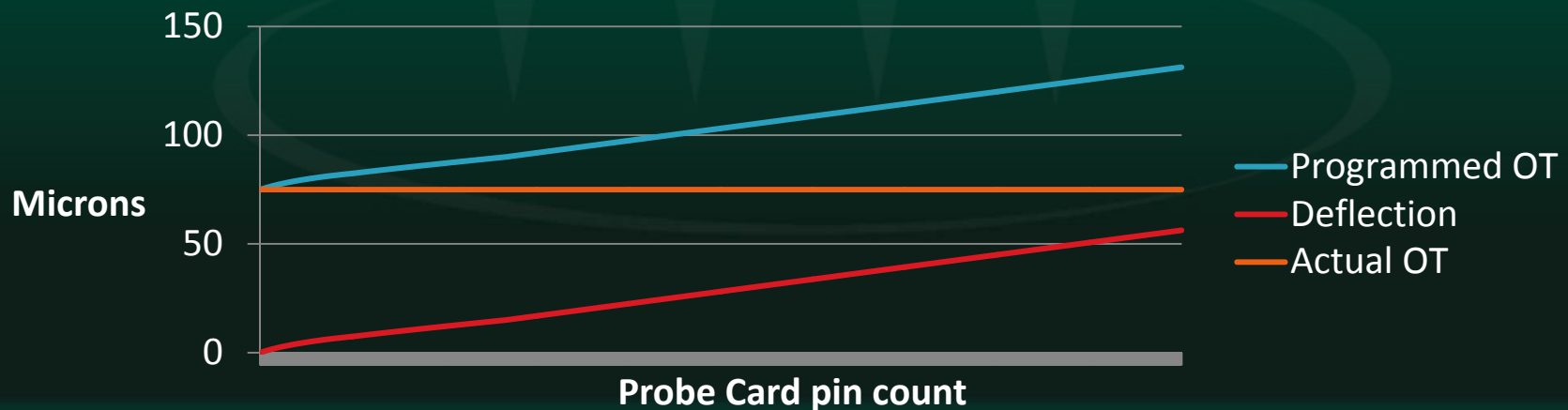
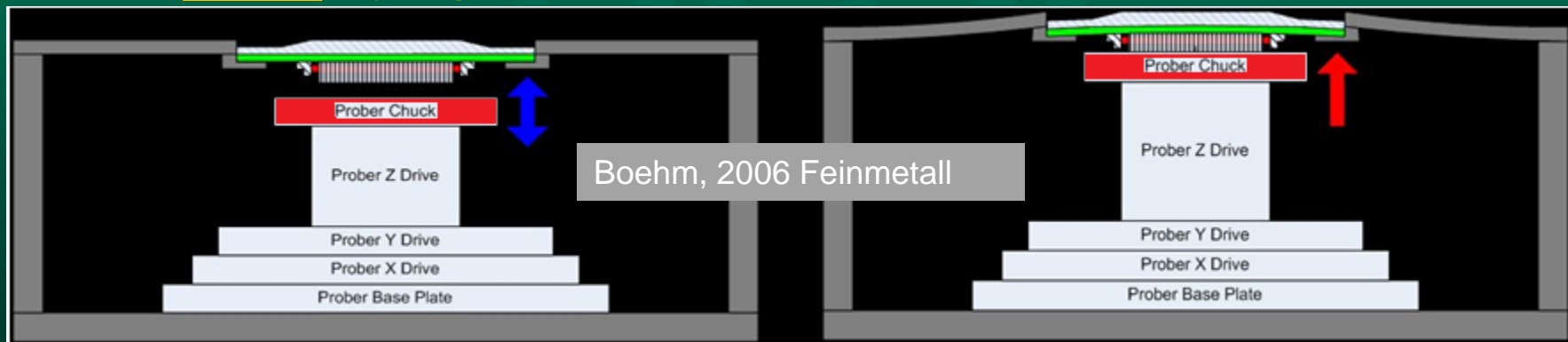
Challenges of High Load Probe Cards

Cost of Probe Card Test

- **The past**
 - Low probe card pin counts and low channel counts
 - Simple PCIs with costs of \$10's of thousands of \$\$
 - P&A measurement non-impacted by probe card load
 - Probe Card Analyzer costs contained
- **Today (for high pin count cards)**
 - High probe card pin counts with corresponding high forces
 - Complex PCIs which cost \$100's of thousands of \$\$
 - PCA costs driven by requirement for high system stiffness
 - Customers are suffering from high cost of probe card test
 - PCI costs may prevent probe card vendors from entering some markets
- **How do we reduce the cost of probe card test?**

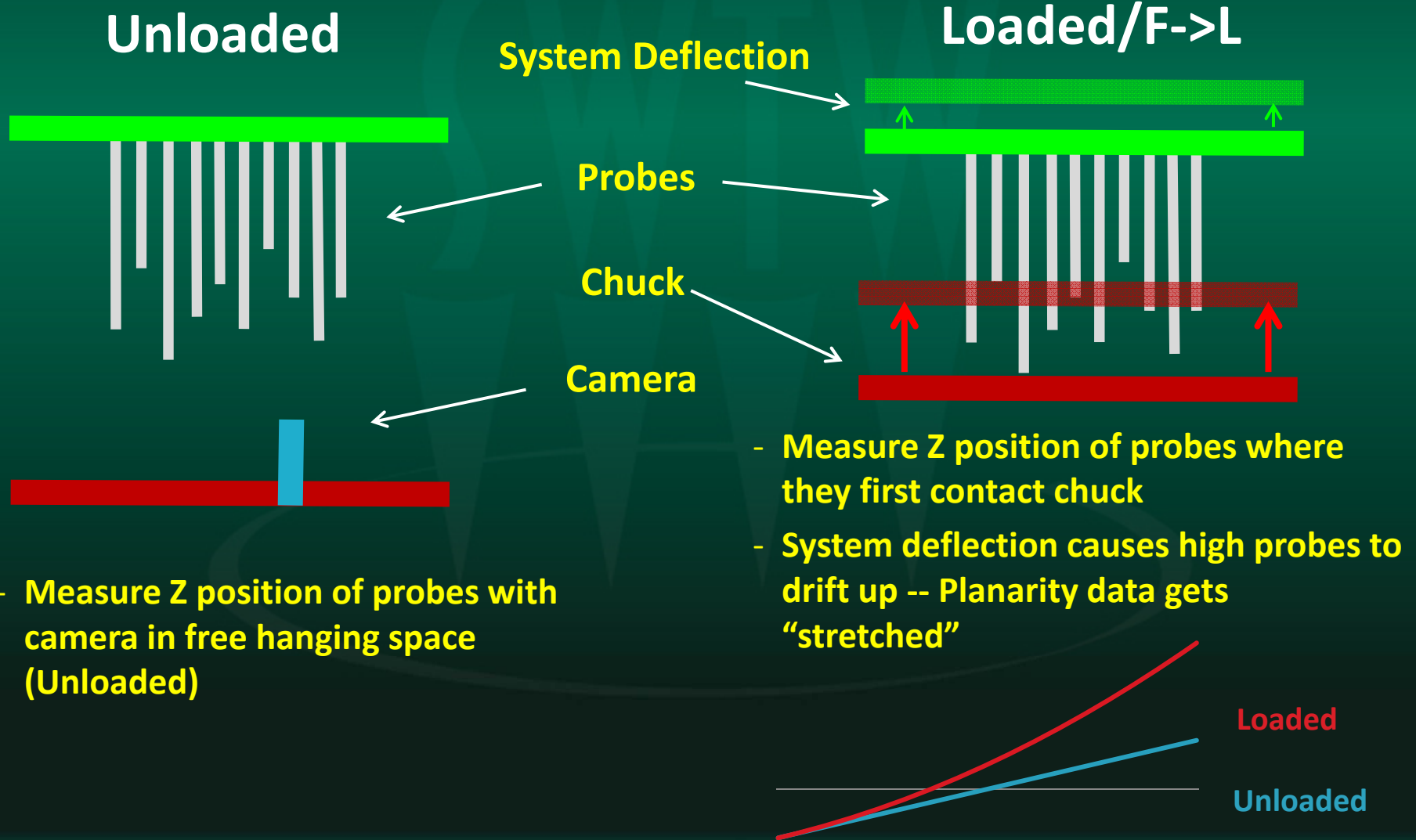
Impact of Probe Card Load on Test Cell

- System deflection cause the actual overtravel to be less than what is programmed
- Need to increase prober's programmed OT to achieve probe card designed OT
- Programmed OT (POT) vs. Actual OT (AOT) is a function of probe card total spring rate and "system" spring rate (stiffness)



Prober Planarity Measurement Methods

System deflection can be seen in the “First to Last” Planarity data



Probe Card Performance on a Prober

Loaded Planarity vs Unloaded Planarity

- **Loaded Planarity range is a function of probe card total spring rate, system stiffness and unloaded planarity range**

10K probes at 0.1gm/um

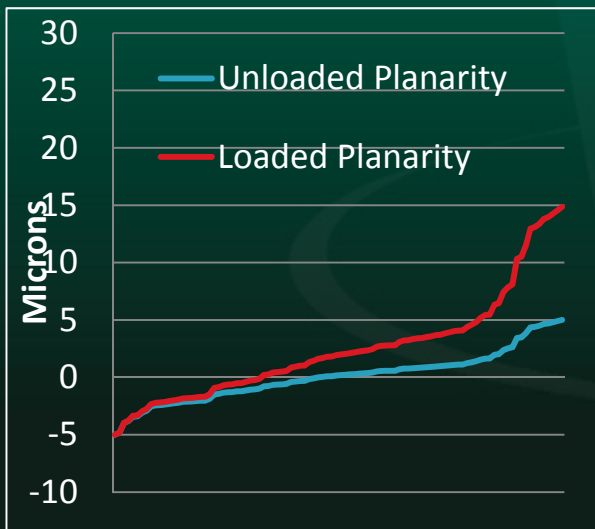
Probe Card Load = 1kg/micron
System Stiffness = 0.5kg/micron
Unloaded Planarity range = 10um
Loaded Planarity range = 20um

10K probes at 0.1gm/um

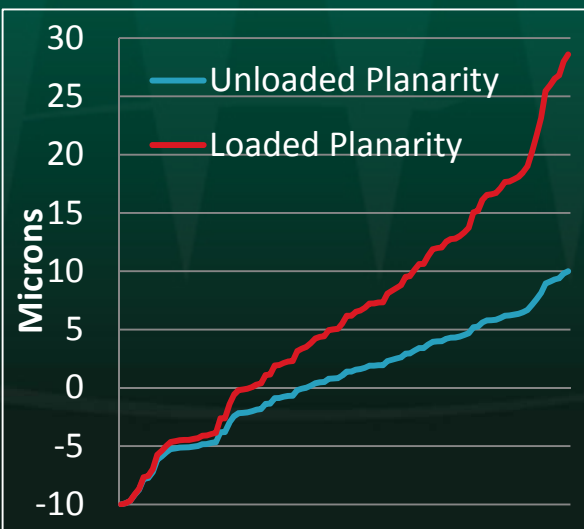
Probe Card Load = 1kg/micron
System Stiffness = 0.5kg/micron
Unloaded Planarity range = 20um
Loaded Planarity range = 40um

40K probes at 0.1gm/um

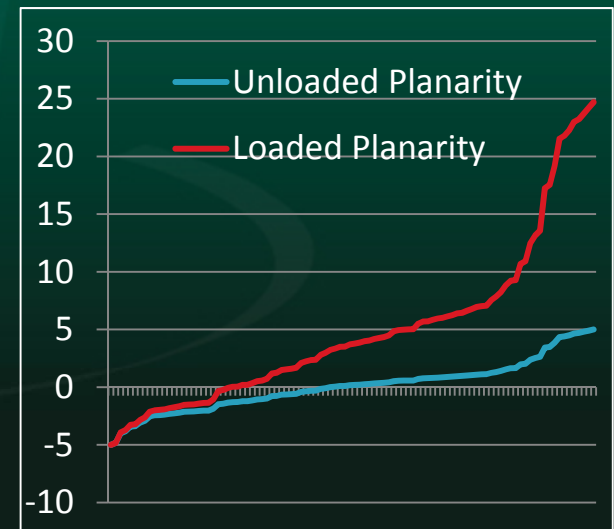
Probe Card Load = 4kg/micron
System Stiffness = 1kg/micron
Unloaded Planarity range = 10um
Loaded Planarity range = 30um



Lowest probe → Highest probe



Lowest probe → Highest probe



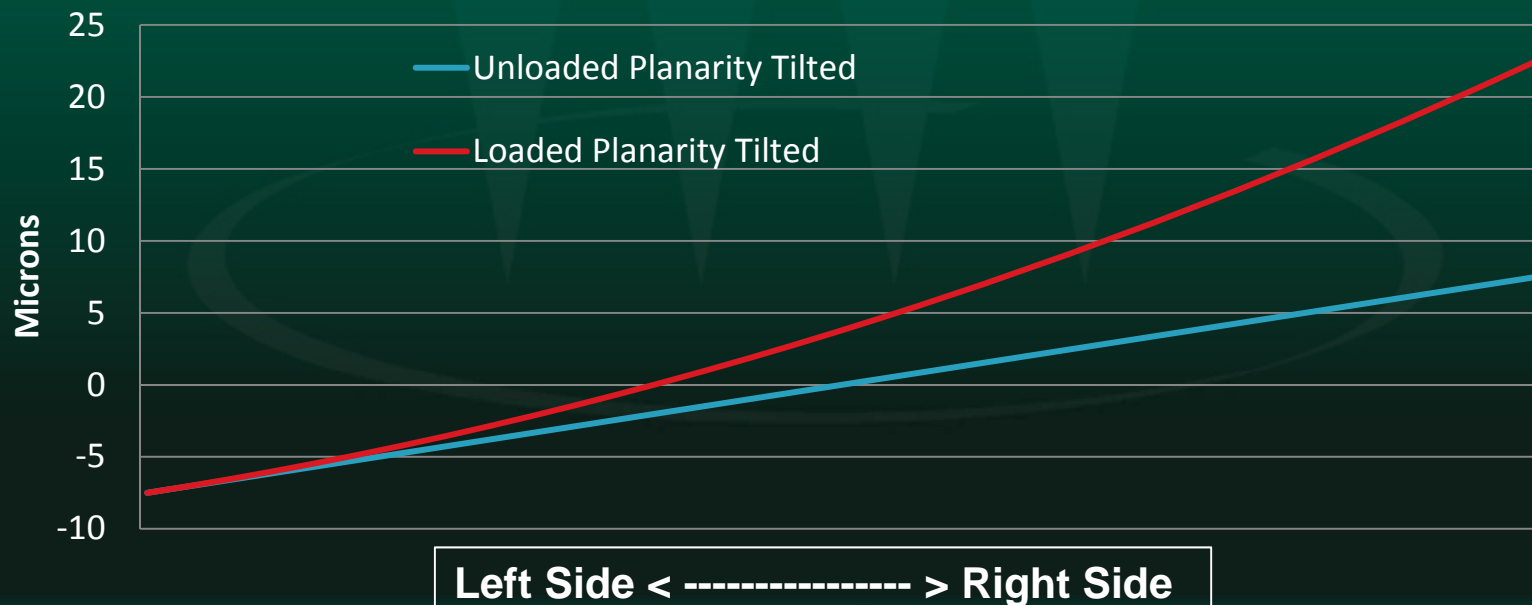
Lowest probe → Highest probe

Probe Card Performance on a Prober

Planarity: Unloaded Pitch/Roll vs. Loaded Pitch/Roll

Probe Card probes:	10K at 0.1gm/um
Probe Card Load :	1kg/micron
System Stiffness:	0.5kg/micron
Unloaded Planarity range:	0um
Unloaded Card Pitch/Roll Error:	15um
Loaded Card Pitch/Roll Error:	30um

Loaded Planarity method can exaggerate probe card tilt



Probe Card Performance on a Prober

- What happens to the actual scrubs produced on the wafer?
- Does linear system deflection affect the uniformity of the scrubs?

EXAMPLE:

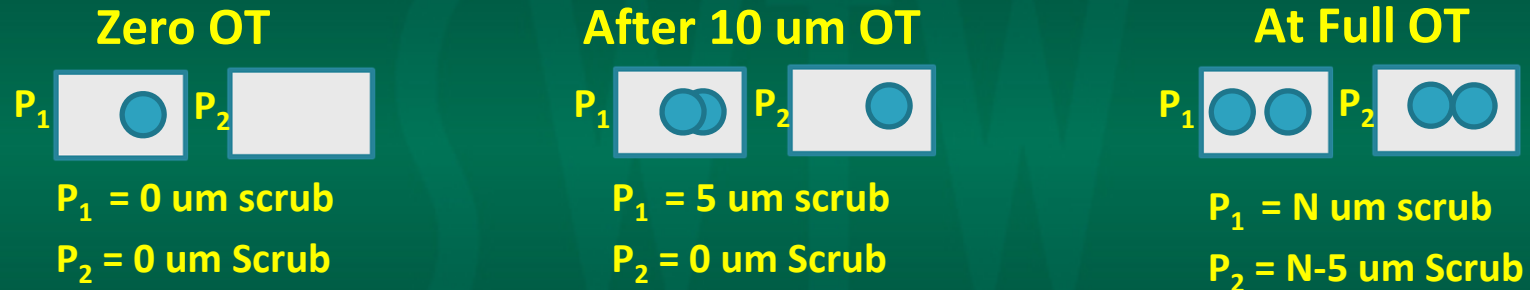
- Probe card Scrub ratio = 0.5 : (i.e. 50u actual OT produces 25um scrub)
- 15um Programmed \rightarrow 10um Actual OT
- Probe card has 10k probes, analyze 2 particular probes
 - Unloaded planarity difference = 10um, implies 5um scrub length differential
 - Loaded planarity difference = 15um, , implies 7.5um scrub length differential



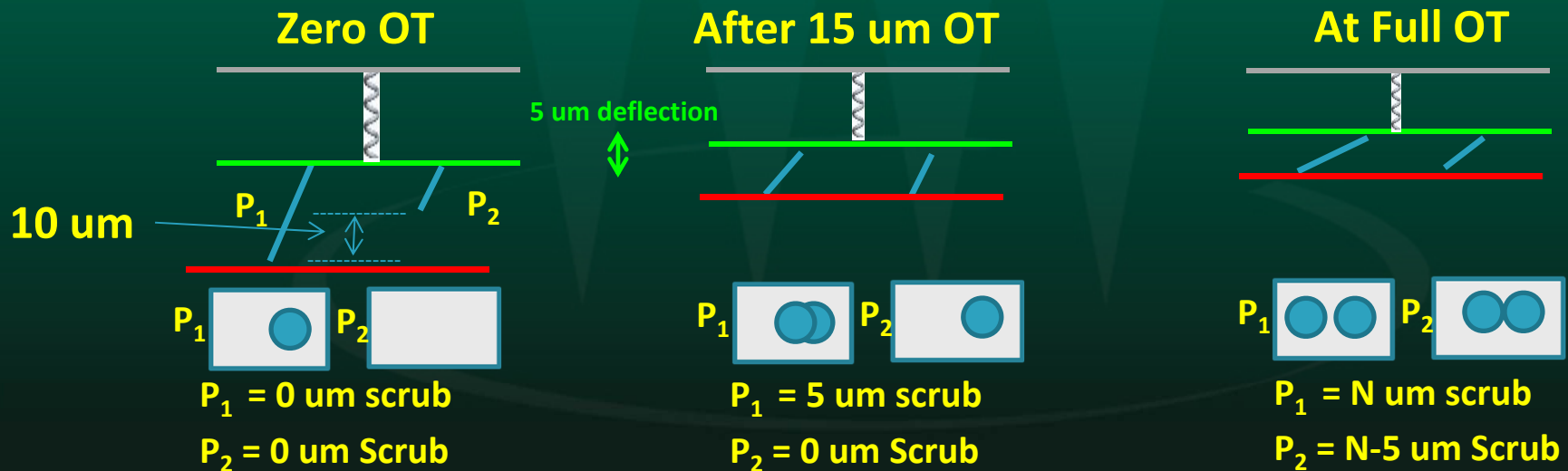
- How will these scrub marks change with system deflection?

Probe Card Performance on a Prober

- Scrub marks on bond pad with perfect “zero” deflection system



- What happens to the actual scrubs produced on the wafer with system deflection?



- Unloaded planarity correlates to scrub uniformity
- Unloaded planarity also correlates to probe force uniformity

PCA Test Strategies

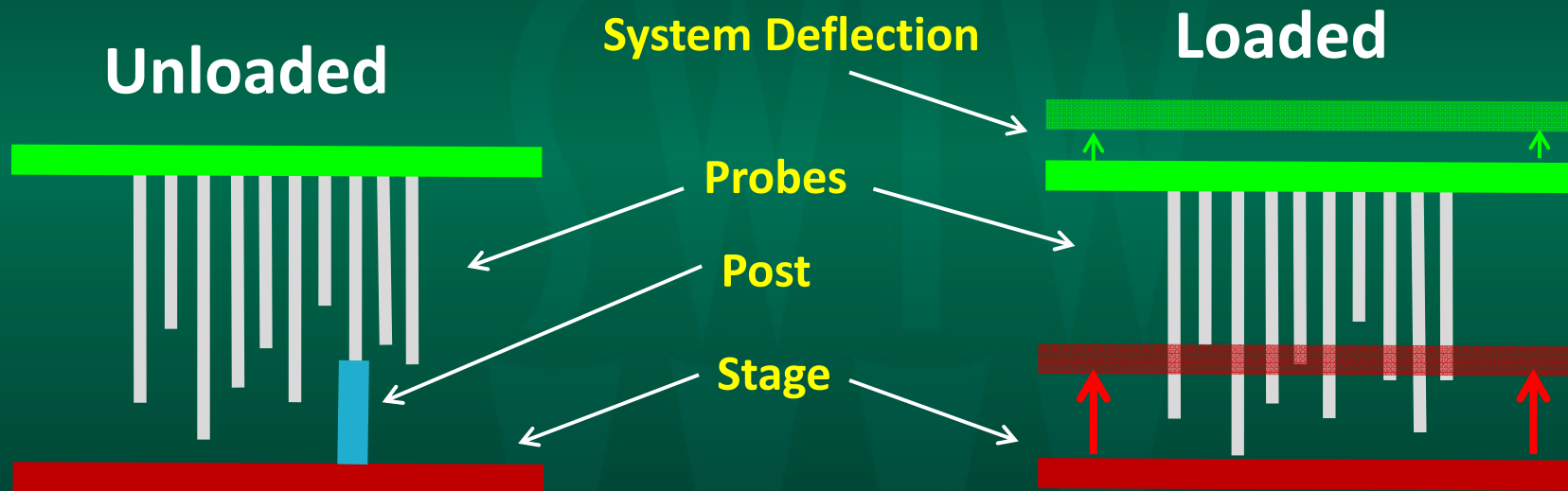
- **Understanding how the card behaves in the test cell...**
 - Unloaded planarity correlates with the uniformity of scrubs
 - Programmed OT \neq Actual OT for high load probe cards
- **What is a *cost effective* test strategy for high load probe cards on a Probe Card Analyzer?**
 - Planarity measurement method
 - Alignment measurement method
 - Probe Card Interface (PCI) design

Test Strategies -- Planarity

- **Purpose of Good Probe Card Planarity**

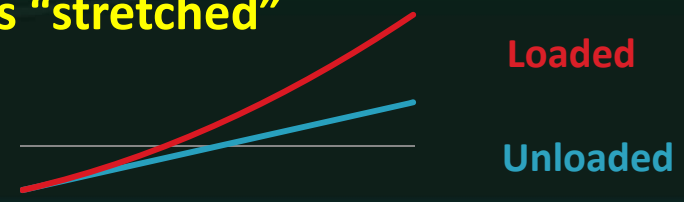
- Produces consistent contact
- Helps produce uniform scrub marks on bond pads
- Helps produce uniform probe force
 - Avoids punch through
- Even probe wear for the life of the probe card

Planarity Measurement Methods – Unloaded / Loaded



- Measure Z position of probes in free hanging space
- No System Deflection
- Z Measurement Techniques
 - Optically via 3D-OCM (PWX)
 - Electrical conductive post (PWX, VX4)
 - Optically via best focus position (WWX)

- Measure Z position of probes where they first contact chuck
- System deflection causes high probes to drift up -- Planarity data gets "stretched"



Planarity Test Methods -- Loaded and Unloaded

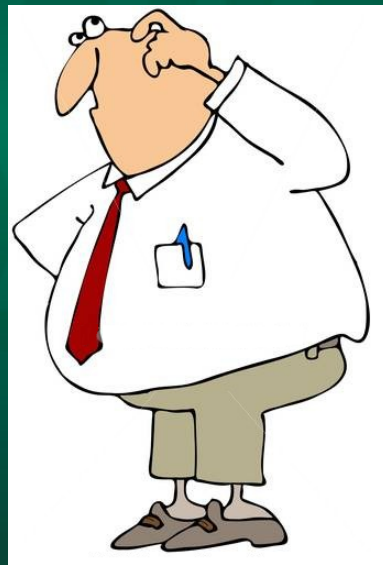
Loaded Planarity

- Exaggerates planarity signature
 - Makes life more difficult for Probe Card manufacturer to meet planarity spec
- Planarity values are dependent on PCI/system stiffness
 - Potential correlation issues due to system deflection differences
- **Does not scale with pin count/ load**
 - PCA upgrades needed over time as probe card loads increase
- **High cost of probe card test**
 - Requires expensive PCA to provide system stiffness
 - Requires expensive PCI to (try to) emulate test environment

Unloaded Planarity

- Measures true planarity of probe card
 - Correlates to the uniformity of scrub marks and probe force on wafer
- Planarity is independent of PCI/system stiffness
 - Better correlation between different unloaded measurement systems
- **Scales with pin count/load**
 - No PCA changes needed for Unloaded Planarity as probe card load increases
- **Reduced cost of probe card test**
 - PCI cost to measure unloaded planarity can be much lower
 - PCA cost to measure unloaded planarity could be much lower

Which Planarity method should I use?

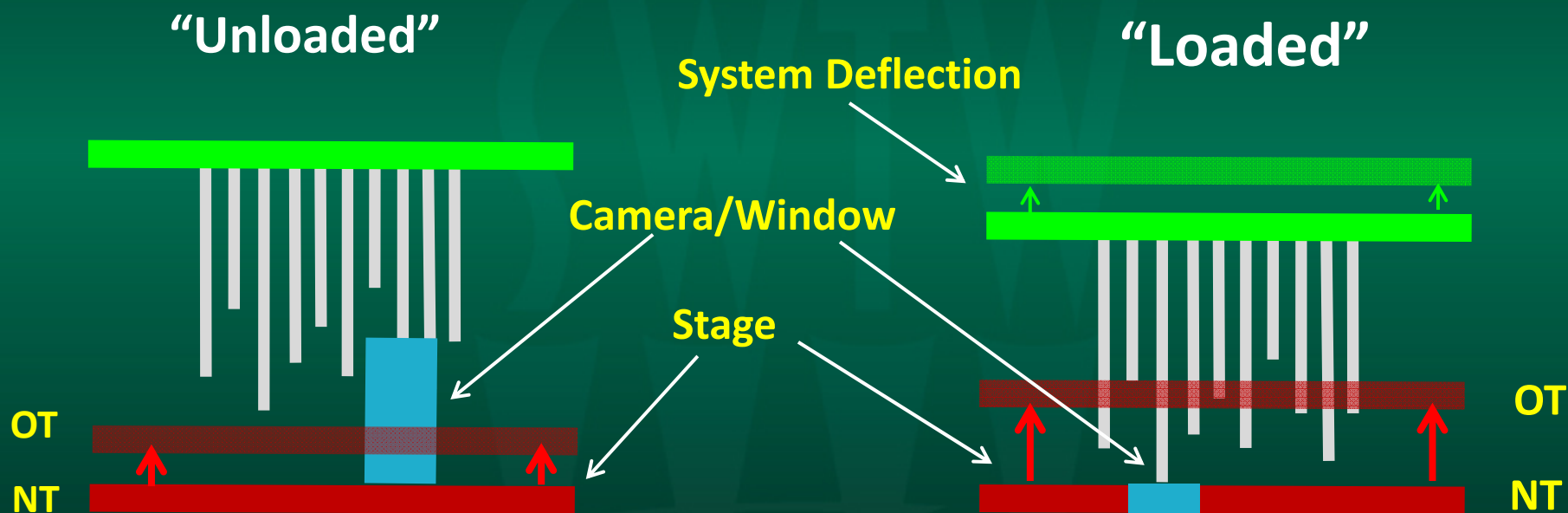


- **Unloaded Planarity will provide the most information at the lowest cost of test**

Test Strategies -- Alignment

- **Purpose of Good Probe Card Alignment**
 - Ensure probe is positioned correctly to for initial contact with the pad/bump
 - Ensure that the probe moves to the correct position on bond pad at designed/actual overtravel
 - Helps minimize bond pad damage
 - Helps ensure that probe does not scrub off bond pad

Alignment Measurement Methods – Unloaded / Loaded



- Measure NT/OT positions with camera/window raised above chuck
- Overtravels only a few probes at a time causing negligible "system" (PCA/PCI/Probe Card) deflection
- Actual OT = Programmed OT

- Measure NT and OT position with camera/window co-planar with chuck
- Probes produce large load at OT position causing "system" (PCA/PCI/Probe Card) deflection
- Actual OT = Programmed OT – "System" Deflection

Alignment Test Methods -- Loaded and Unloaded

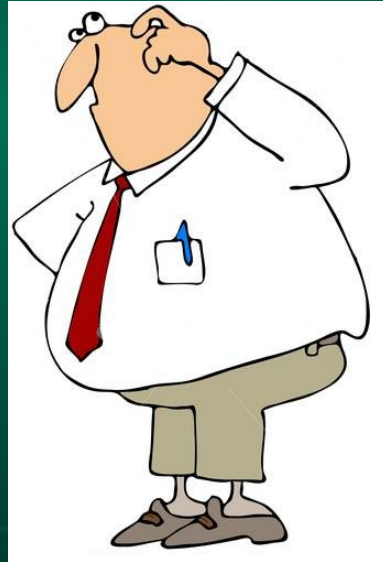
Loaded Alignment

- Accuracy of AOT is unknown
 - AOT = POT - “System” Deflection
 - What POT to test at?
- Alignment measurements are dependent on PCI/system stiffness
 - Difficult to get high accuracy and correlation of measurement
- **Does not scale with pin count/ load**
 - PCA upgrades needed over time as probe card loads increase
- **High cost of probe card test**
 - Requires expensive PCA to provide system stiffness
 - Requires expensive PCI to (try to) emulate test environment

Unloaded Alignment

- Accurate of AOT
 - AOT=POT
- Alignment measurements are independent of PCI/system stiffness
 - Better correlation between different unloaded measurement systems
- **Scales with pin count**
 - No PCA changes needed for Unloaded Alignment as probe card loads increase
- **Reduced cost of probe card test**
 - PCI cost to measure unloaded alignment much lower
 - PCA cost to measure unloaded alignment could be much lower

Which Alignment method should I use?



- **Unloaded Alignment will provide the best information at the lowest cost of test**

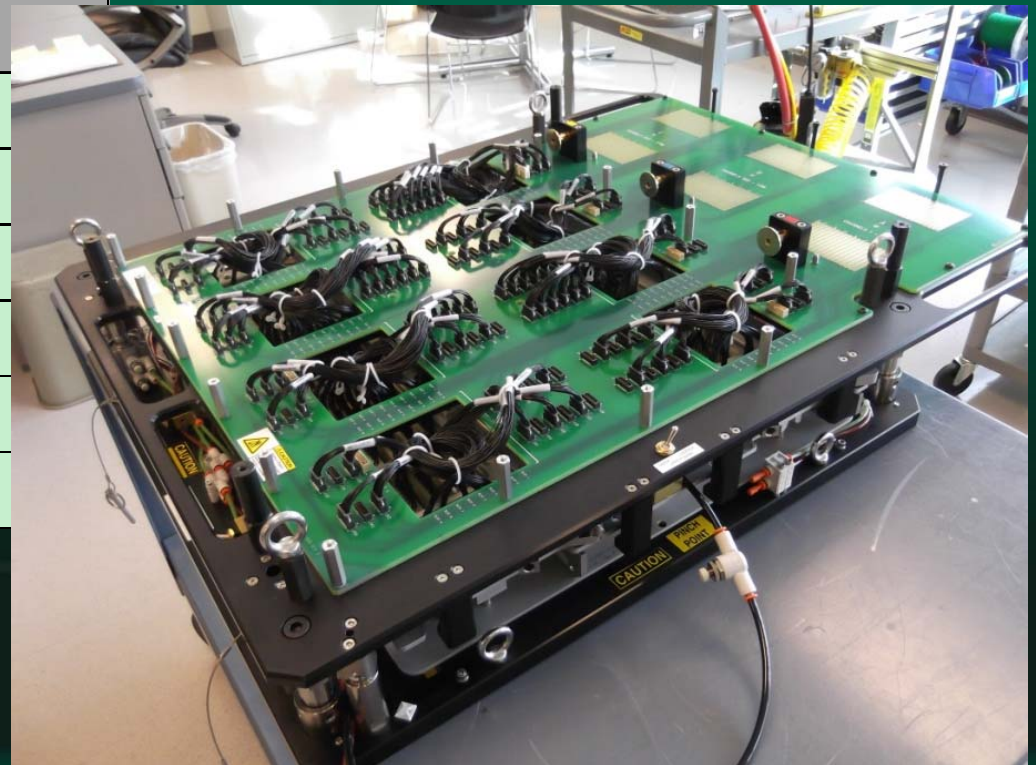
Test Strategies – PCI Design

- **Emulate tester interface mechanically and electrically**
 - Highest cost
 - Industry standard method, but the accuracy of emulation often unknown
- **Simplified tester interface mechanically and/or electrically**
 - Reduced cost is enabled by unloaded Planarity and Alignment measurement
 - Does not attempt to emulate the test environment stiffness
 - Requirements for parallelism of probe card during test can be loosened
 - Can further reduce costs with electrical simplification – low channel count PCA and heavily bussed PCI

Test Cost vs Test Coverage

- **Emulate tester interface mechanically and electrically**
 - Highest cost

Test Coverage	"Emulating" PCI Fully routed
Planarity	YES
Alignment	YES
Full leakage	YES
CRES	YES
Wirechecker	YES
Probe Force	YES

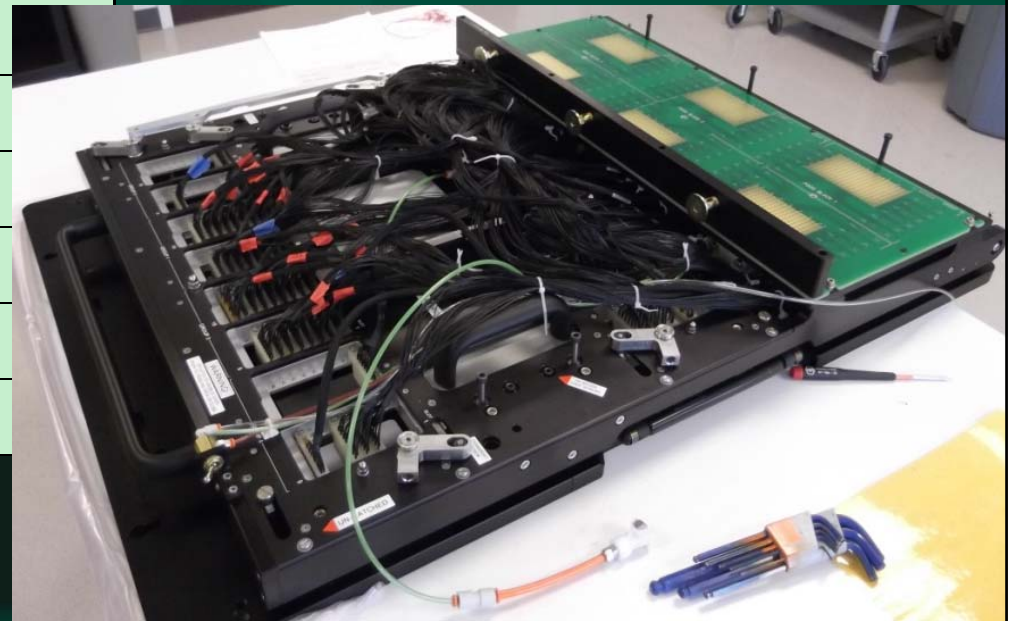


Test Strategies – PCI Design

- **Use simplified PCI mechanics**

- Unloaded Planarity and Alignment enables low cost PCI by eliminating need for system stiffness

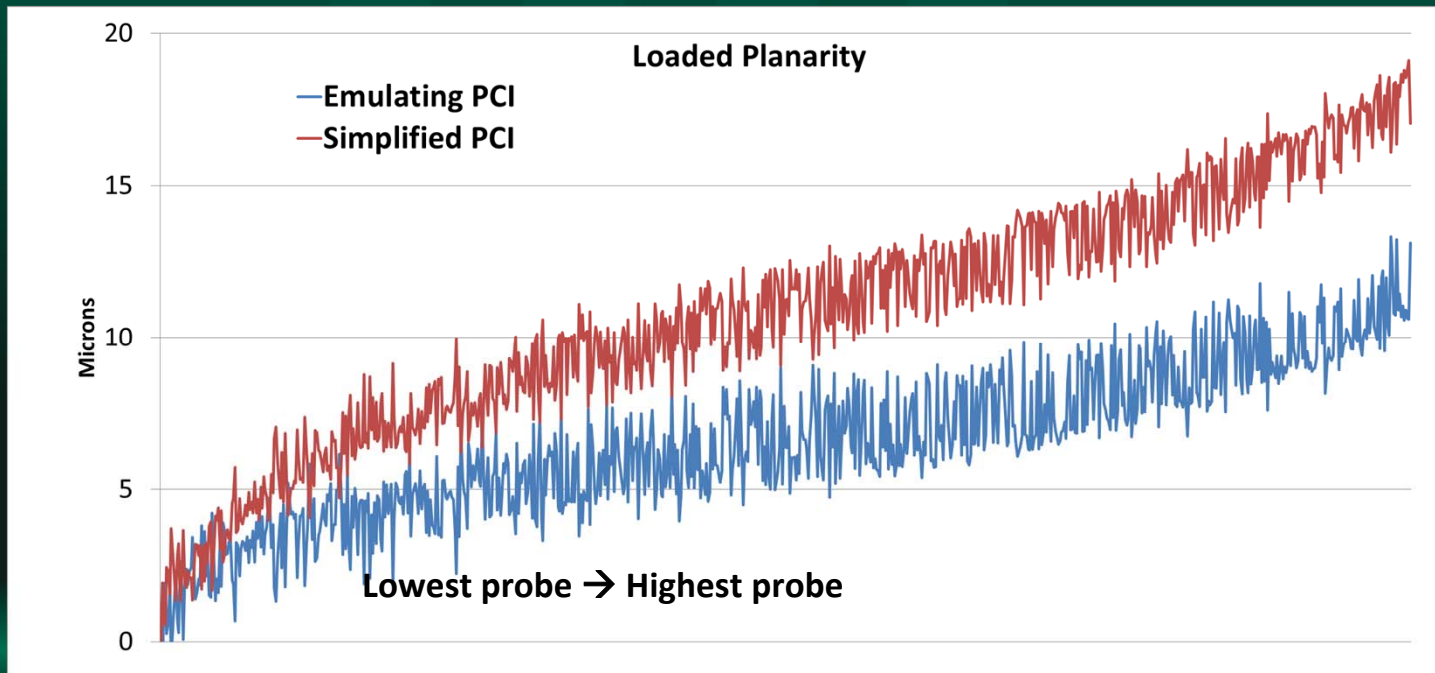
Test Coverage	Simplified PCI Fully Routed
Unloaded Planarity	YES
Unloaded Alignment	YES
Full leakage	YES
Unloaded CRES	YES
Wirechecker	YES
Probe Force	YES



Case Study: Emulating PCI vs Simplified PCI

Loaded Planarity

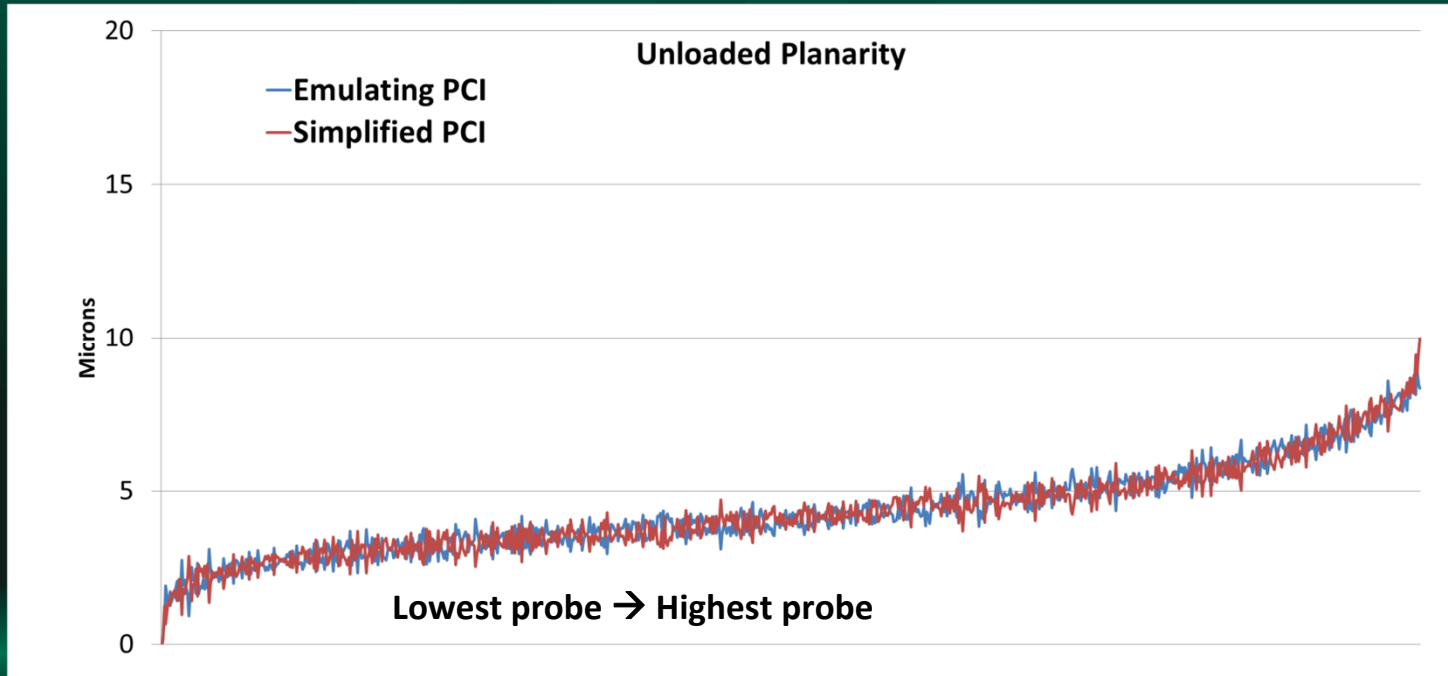
- Emulating PCI = Very stiff, Simplified PCI = Less stiff
- Direct Dock Probe Card –~5000 probes, moderate load
- Loaded Planarity ranges 12um -18um due to PCI stiffness differences
 - Differences will increase as probe card loads increase!
- Results are dependent of probe card load and system stiffness



Case Study: Emulating PCI vs Simplified PCI

Unloaded Planarity

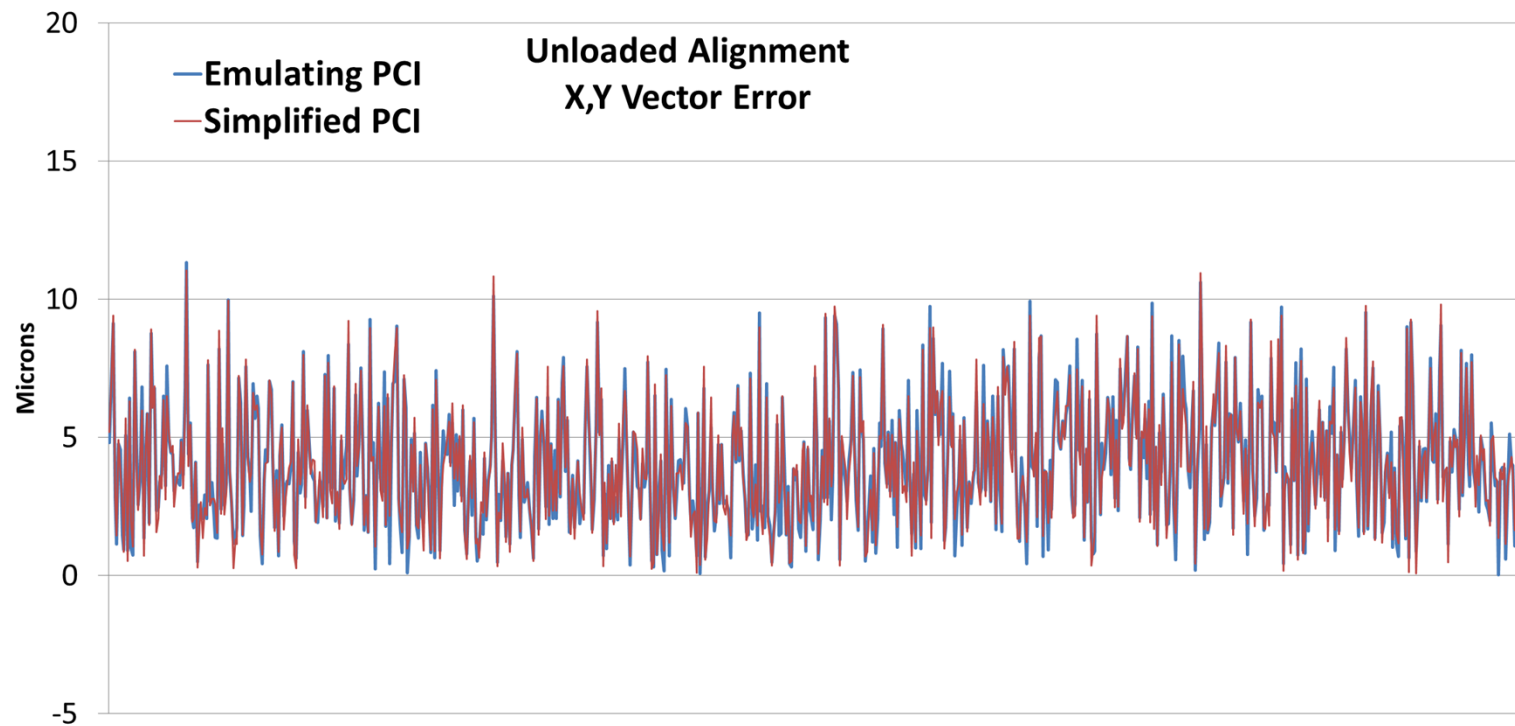
- Emulating PCI = Very stiff, Simplified PCI = Less stiff
- Direct Dock Probe Card – Moderate load ~5000 probes
- Unloaded Planarity range is only 8um and is the same for both PCIs
- Results are independent of probe card load and system stiffness!



Case Study: Emulating PCI vs Simplified PCI

Unloaded Alignment

- Emulating PCI = Very stiff, Simplified PCI = Less stiff
- Direct Dock Probe Card – Moderate load ~5000 probes
- Unloaded Alignment is the same for both PCIs
- Results are independent of probe card load and system stiffness!



Summary

- Customers are demanding reduced cost of probe card test
- Probe card test costs can be significantly reduced by taking advantage of unloaded measurements with appropriately simplified PCI designs for these measurement techniques
- Unloaded measurements can provide more meaningful information than loaded measurements about probe card performance in a test cell
- Unloaded measurements scale with probe card pin count and don't require PCA system changes as probe card loads increase

Acknowledgements

- **Bill Favier, Rudolph Technologies**
- **Ryan Shan, Rudolph Technologies**